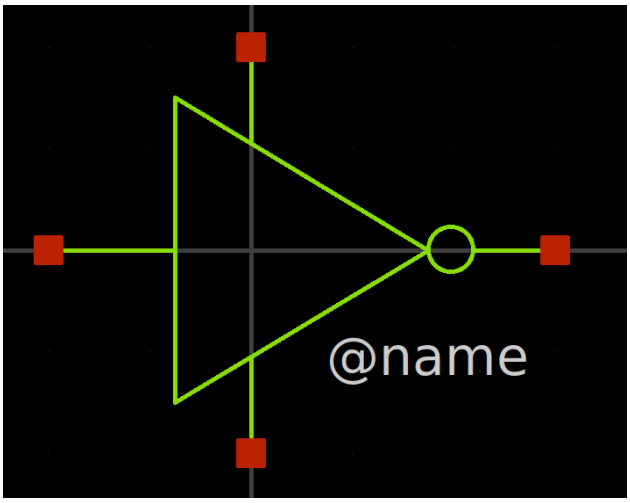
Mixed Analog-Digital VLSI Mini-project 1: 2-Input AND Gate

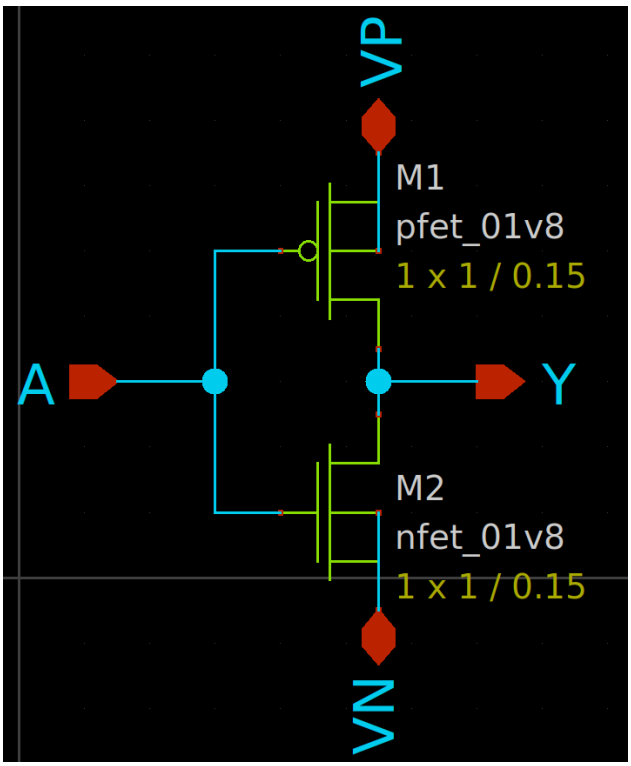
Qingmu Deng

February 11, 2021

1 Schematic Capture and Simulation



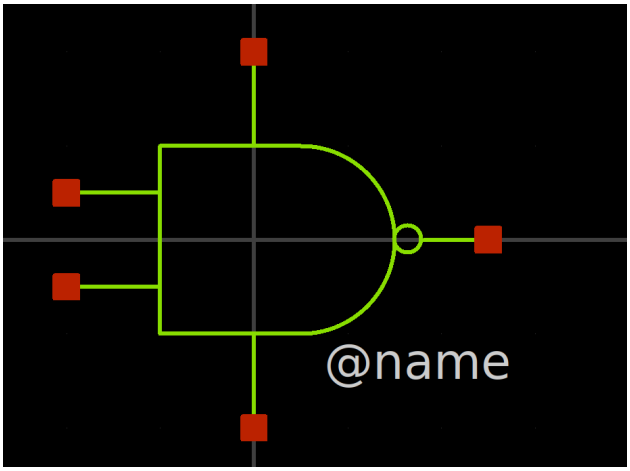
(a) Inverter symbol created in Xschem.



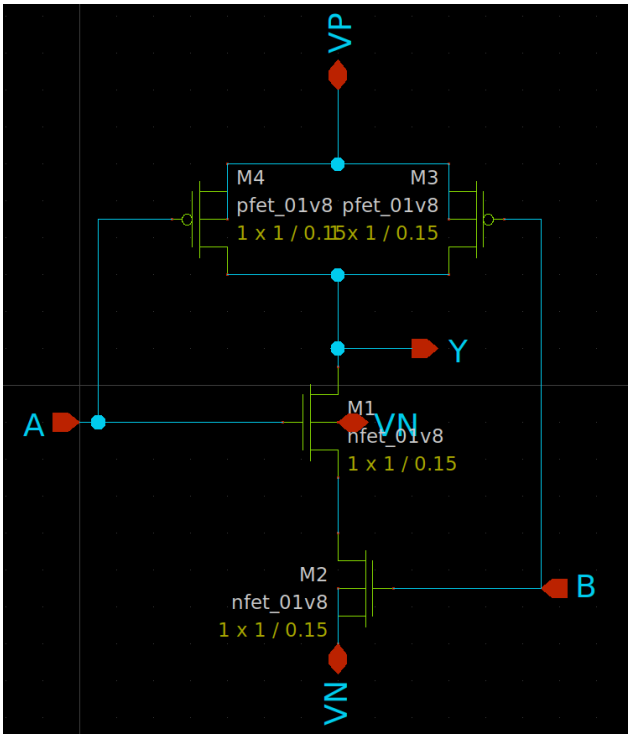
(b) Inverter schematic created in Xschem.

Figure 1: Inverter design in Xschem.

To begin with, I implemented an inverter design shown in Figure 1 as introduced by Professor Minch in his tutorial video. Similarly, I independently created a hierarchy schematic for NAND2 as shown in Figure 2.



(a) NAND2 symbol created in Xschem.



(b) NAND2 schematic created in Xschem.

Figure 2: NAND2 design in Xschem.

I created an AND2 gate by inverting the output of NAND2 with the inverter. You can see the test harness of the AND2 gate in Figure 3. V_{DD} is set to be 1.8 V, and the square waves at NAND2 inputs switches between 0 V and 1.8 V. To capture all four possible inputs, {00, 01, 10, 11}, to be presented to this two-input gate, the square wave at the input node V_B is set to have twice the period of V_A. The output node V_{out} is loaded with a 200 fF capacitor as specified.

As you can see for the simulation results in Figure 4, the only time where V_{out} outputs high is when both V_A and V_B outputs high. This follows out expectation of how an AND2 gate should behave.

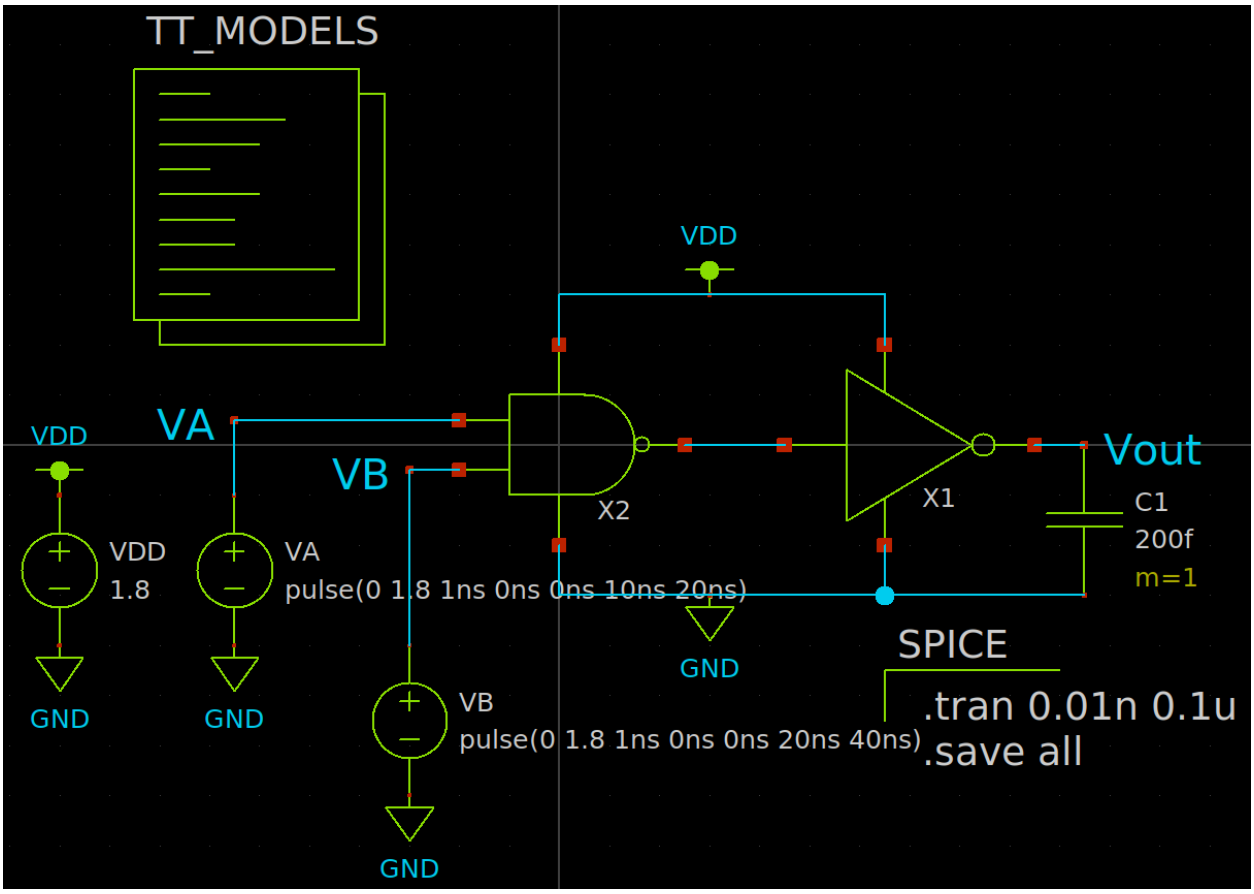


Figure 3: The simulation setup of a AND2 gate made of a NAND2 and an inverter.

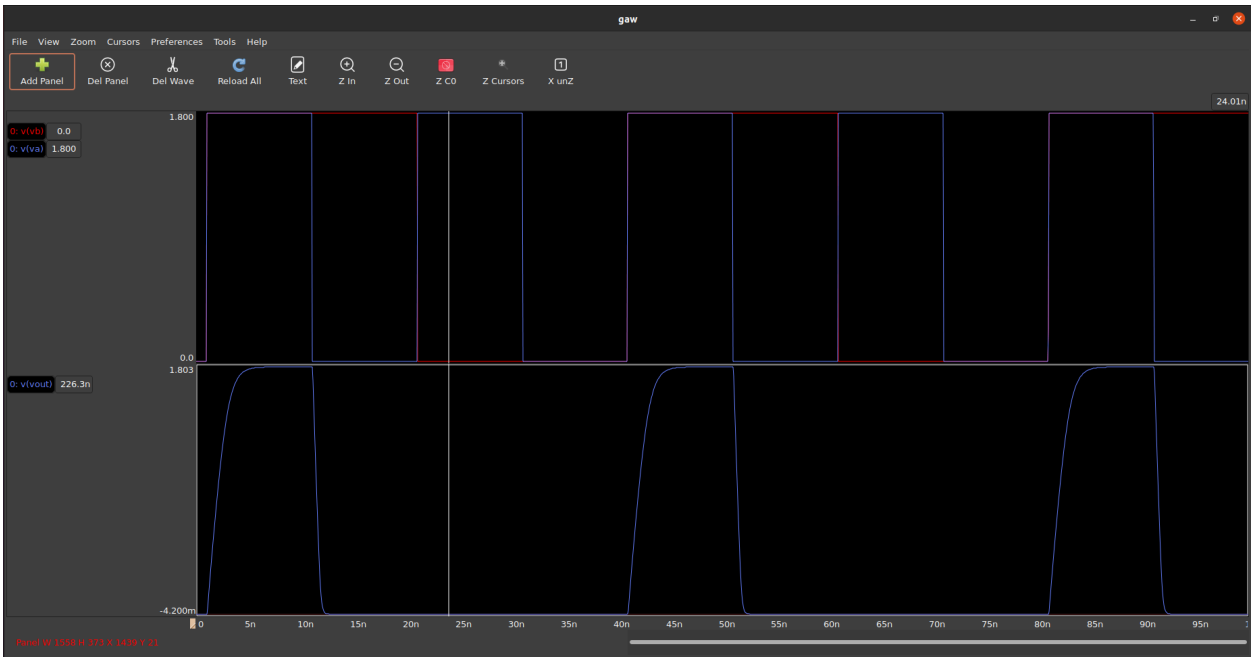


Figure 4: The simulation AND2 gate behavior view in *gaw*.

2 Layout Design

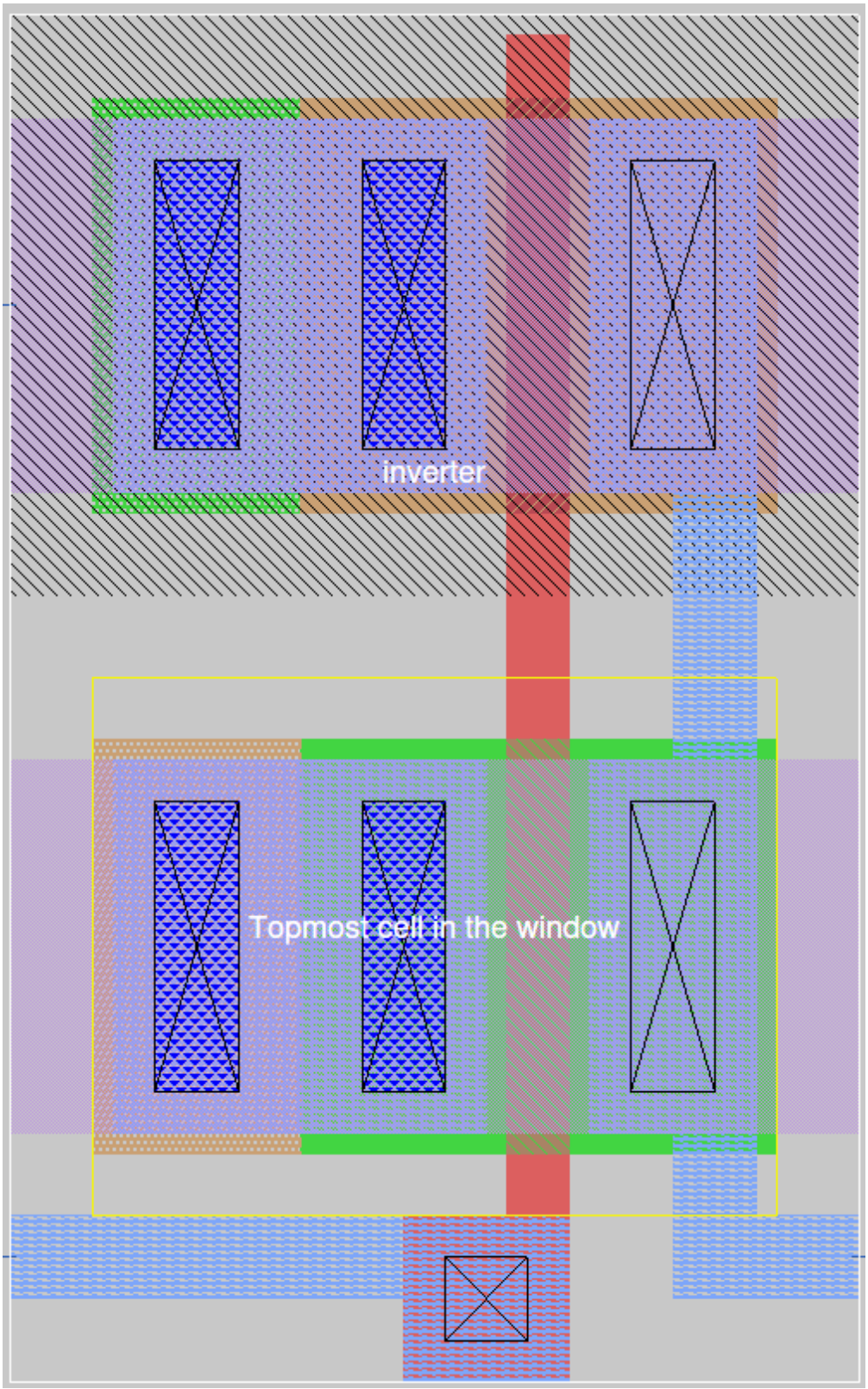


Figure 5: *Magic* layout of the inverter.

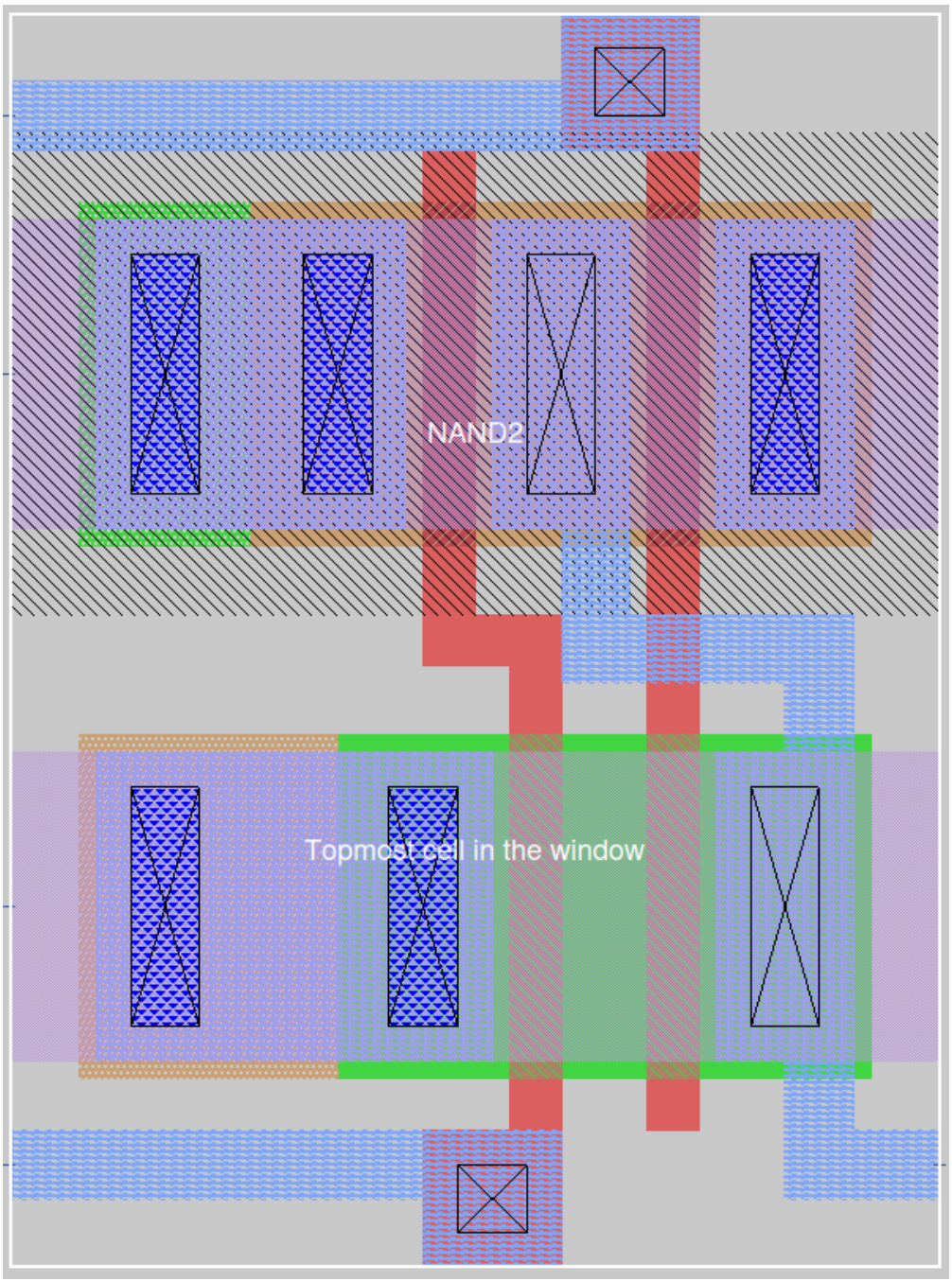


Figure 6: *Magic* layout of the NAND2.

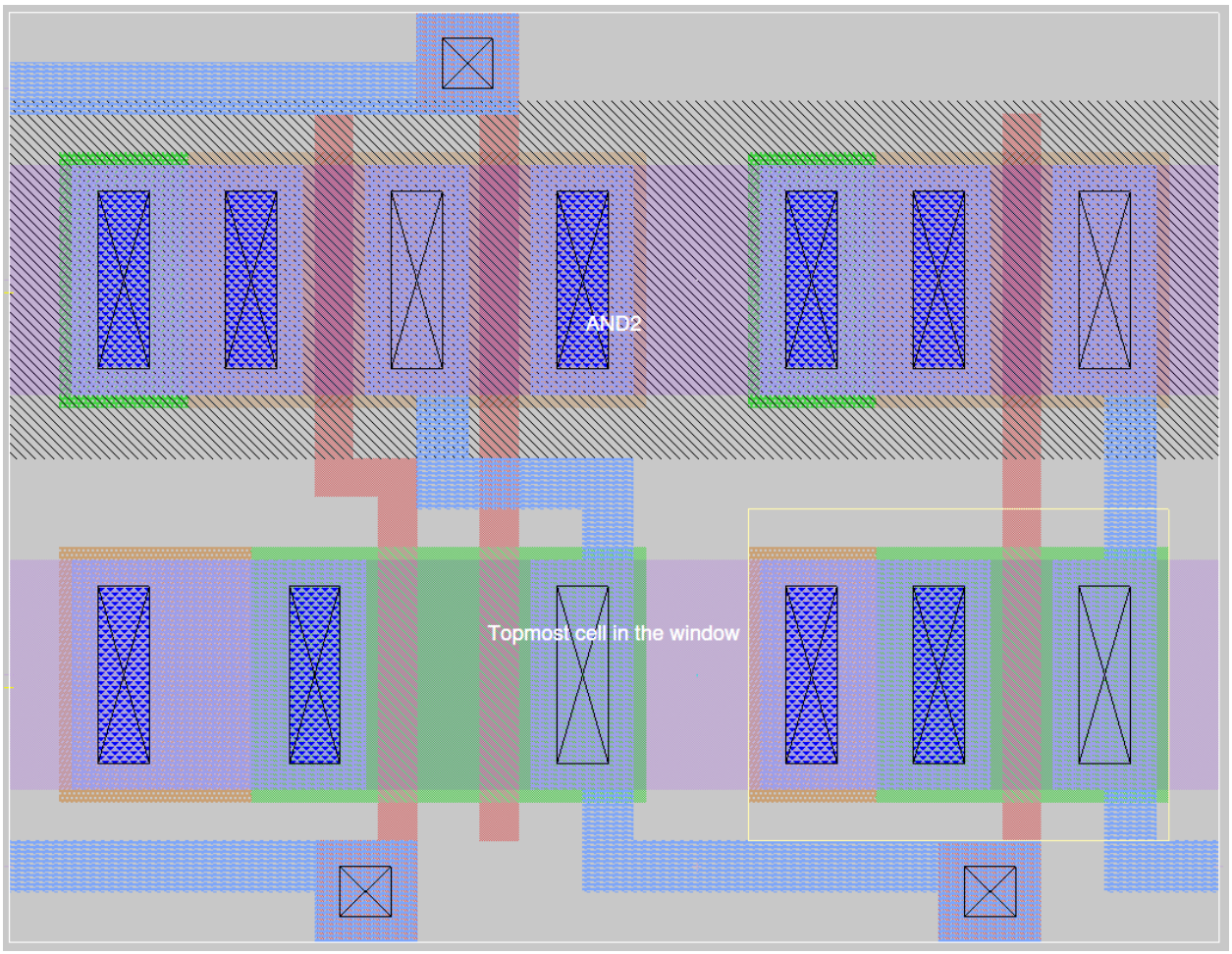


Figure 7: *Magic* layout of the AND2 by combining NAND2 and inverter layouts.

3 Layout versus Schematic