Mixed Analog-Digital VLSI Mini-Project I: 2-Input AND Gate

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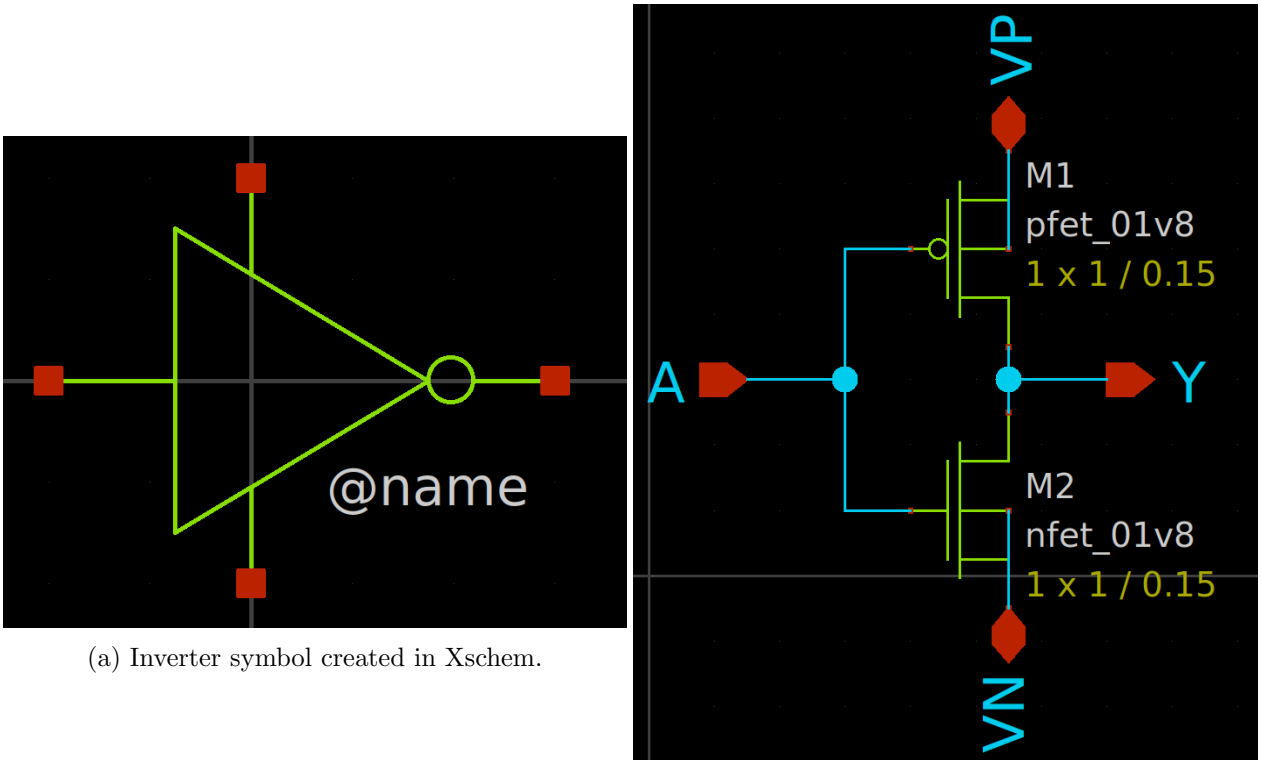
Project Github: https://github.com/QingmuDeng/MADVLSI/tree/main/mini1 project Zip: https://github.com/QingmuDeng/MADVLSI/tree/main/mini1/Deng-mini1.zip

1 Schematic Capture and Simulation

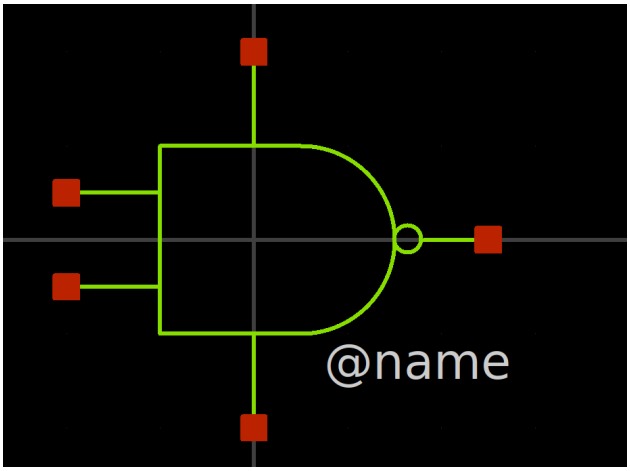


(a) Inverter symbol created in Xschem.

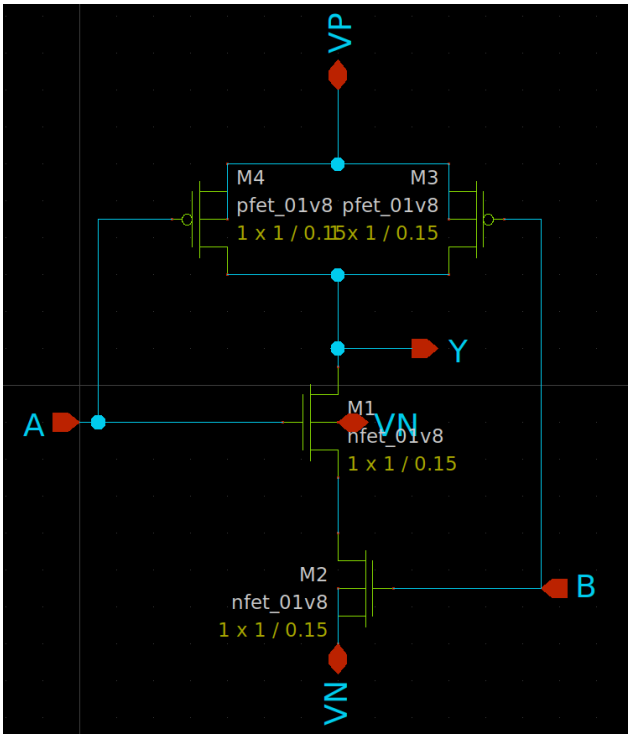
(b) Inverter schematic created in Xschem.

Figure 1: Inverter design in Xschem.

To begin with, I implemented an inverter design shown in Figure 1 as introduced by Professor Minch in his tutorial video. Similarly, I independently created a hierarchy schematic for NAND2 as shown in Figure 2.



(a) NAND2 symbol created in Xschem.



(b) NAND2 schematic created in Xschem.

Figure 2: NAND2 design in Xschem.

I created an AND2 gate by inverting the output of NAND2 with the inverter. You can see the test harness of the AND2 gate in Figure 3. V_{DD} is set to be 1.8 V, and the square waves at NAND2 inputs switches between 0 V and 1.8 V. To capture all four possible inputs, {00, 01, 10, 11}, to be presented to this two-input gate, the square wave at the input node V_B is set to have twice the period of V_A. The output node V_{out} is loaded with a 200 fF capacitor as specified.

As you can see for the simulation results in Figure 4, the only time where V_{out} outputs high is when both V_A and V_B outputs high. This follows out expectation of how an AND2 gate should behave.

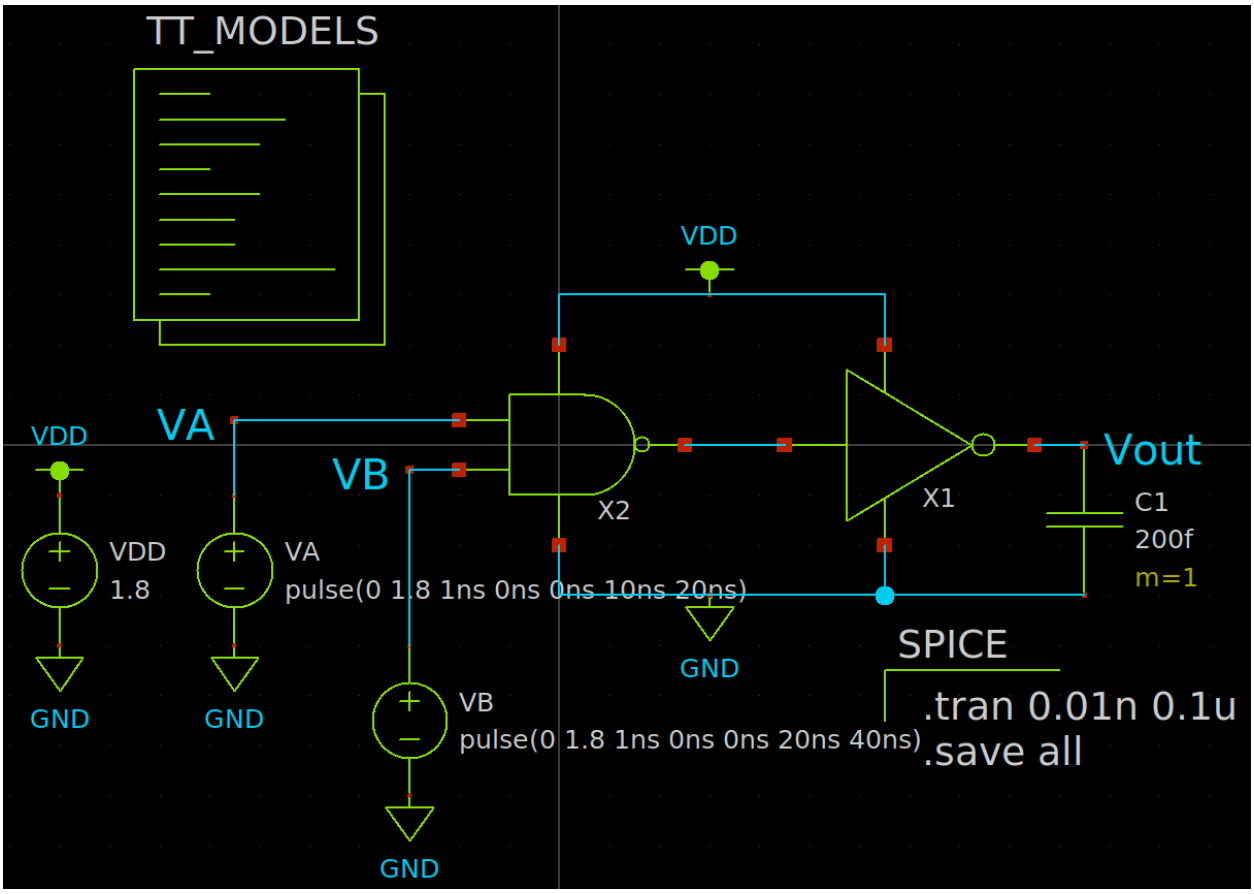


Figure 3: The simulation setup of a AND2 gate made of a NAND2 and an inverter.

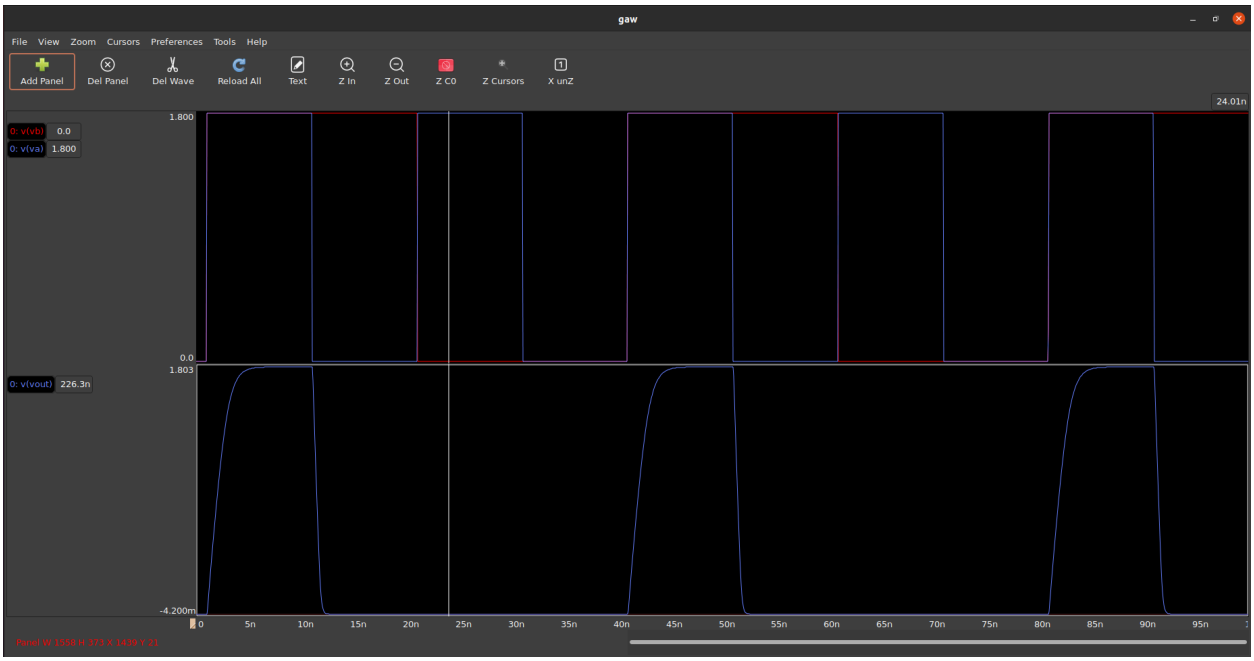


Figure 4: The simulation AND2 gate behavior viewed in *gaw*.

2 Layout Design

Similarly, the inverter and NAND2 were separately laid out in *Magic* as shown in Figure 5 and 6. The output of the NAND2 was designed to align with the input of the inverter such that they can fit together nicely to form AND2 as shown in Figure 7, all the while sharing and extending the same power rails.

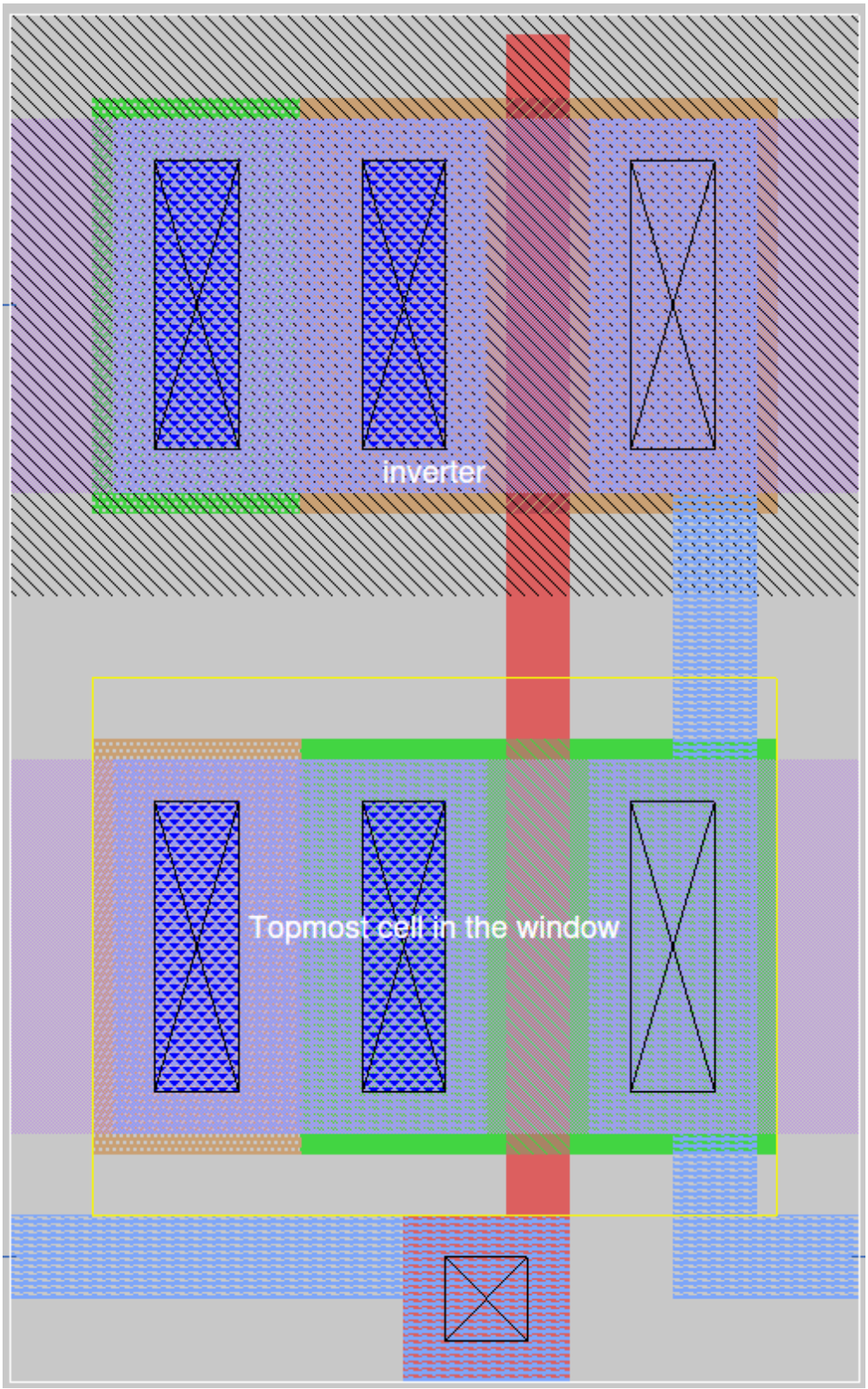


Figure 5: *Magic* layout of the inverter.

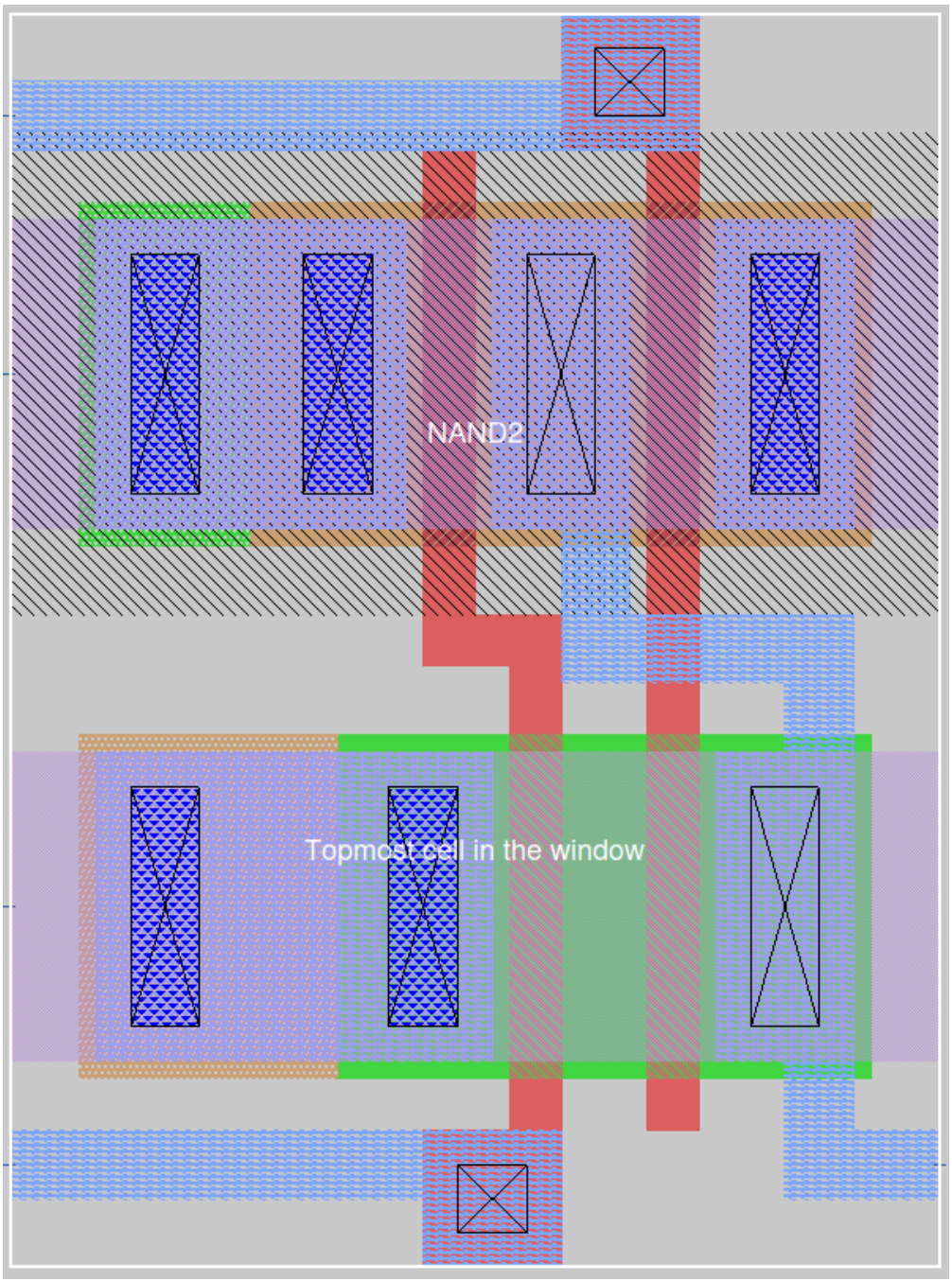


Figure 6: *Magic* layout of the NAND2.

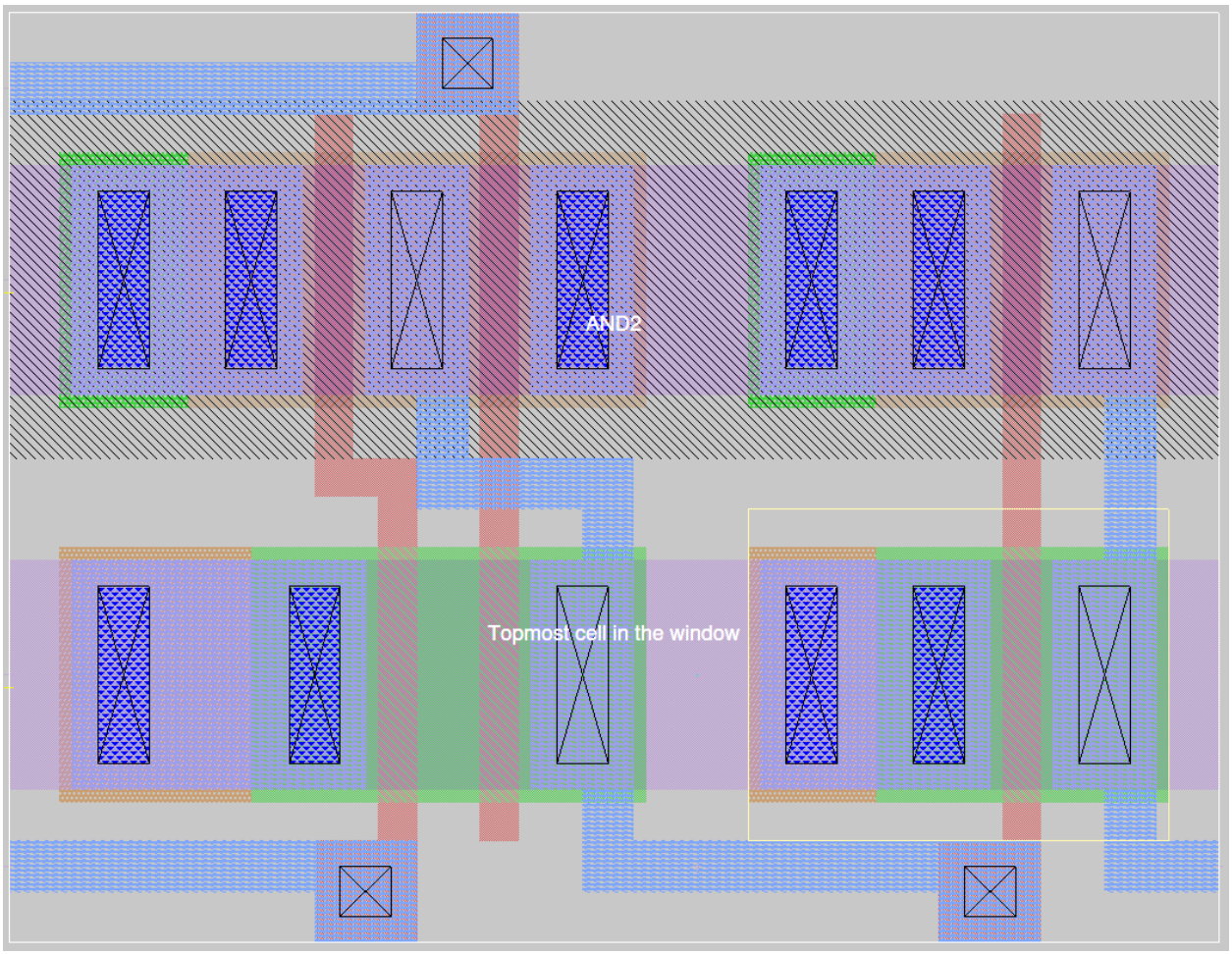


Figure 7: *Magic* layout of the AND2 by combining NAND2 and inverter layouts.

3 Layout versus Schematic

Finally, I compared the two netlists generated through schematic capture and physical layout. The output of the LVS can be found below. The netlists of the two designs were found to be uniquely matching. Although there are two mismatches highlighted, they are spurious as they are simply a permutation of the input pins. As suggested by the LVS output at the end of the block where the two mismatches were reported, the two NAND gate netlists were equivalent.

Listing 1: Netgen comparison between Xschem and Magic AND2

```
Equate elements:  no current cell.
Equate elements:  no current cell.

Subcircuit summary:
Circuit 1: inverter                        |Circuit 2: inverter
-------------------------------------------|-------------------------------------------
sky130_fd_pr__pfet_01v8 (1)                |sky130_fd_pr__pfet_01v8 (1)
sky130_fd_pr__nfet_01v8 (1)                |sky130_fd_pr__nfet_01v8 (1)
Number of devices: 2                       |Number of devices: 2
Number of nets: 4                          |Number of nets: 4
-------------------------------------------|-------------------------------------------
Circuits match uniquely.
Netlists match uniquely.

Subcircuit pins:
Circuit 1: inverter                        |Circuit 2: inverter
-------------------------------------------|-------------------------------------------
Y                                          |Y
A                                          |A
VN                                         |VN
VP                                         |VP
-------------------------------------------|-------------------------------------------
Cell pin lists are equivalent.
Device classes inverter and inverter are equivalent.

Subcircuit summary:
Circuit 1: NAND2                           |Circuit 2: NAND2
-------------------------------------------|-------------------------------------------
sky130_fd_pr__nfet_01v8 (2)                |sky130_fd_pr__nfet_01v8 (2)
sky130_fd_pr__pfet_01v8 (2)                |sky130_fd_pr__pfet_01v8 (2)
Number of devices: 4                       |Number of devices: 4
Number of nets: 6                          |Number of nets: 6
-------------------------------------------|-------------------------------------------
Circuits match uniquely.
Netlists match uniquely.

Subcircuit pins:
Circuit 1: NAND2                           |Circuit 2: NAND2
-------------------------------------------|-------------------------------------------
```

VP	VP
B	A **Mismatch**
A	B **Mismatch**
VN	VN
Y	Y

Cell pin lists are equivalent.
Device classes NAND2 and NAND2 are equivalent.

Subcircuit summary:

Circuit 1: AND_no_C.spice	Circuit 2: layout/AND2.spice
inverter (1)	inverter (1)
NAND2 (1)	NAND2 (1)
Number of devices: 2	Number of devices: 2
Number of nets: 6	Number of nets: 6

Circuits **match** uniquely.
Netlists **match** uniquely.
Cells have no pins; pin matching not needed.
Device classes AND_no_C.spice and layout/AND2.spice are equivalent.
Circuits **match** uniquely.