

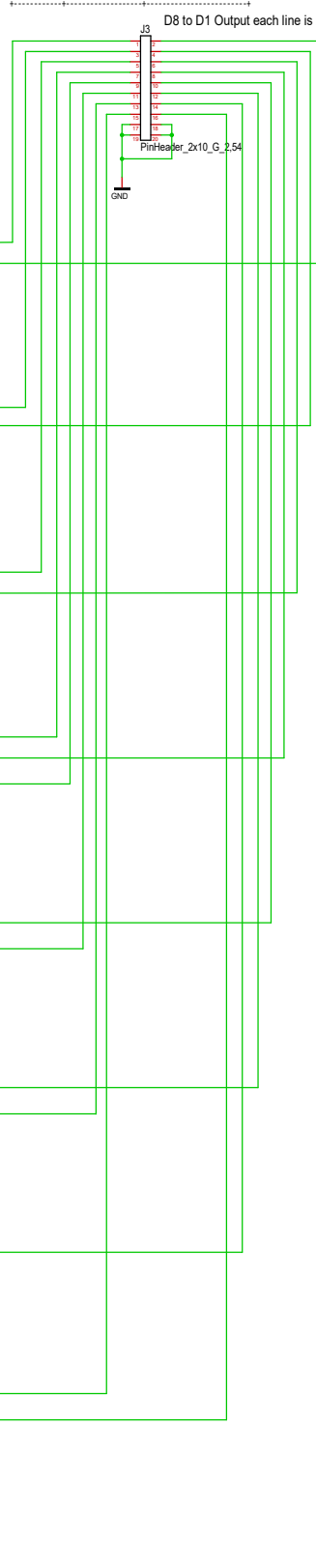
**CS\_Module**

**CS & DAC BUS TO NUCLEO**

DAC_Header_1x12	Description	74HC595 Pin	MCP4822	Nucleo Pin
Pin 1	GND	-	-	GND
Pin 2	GND	-	-	TBD
Pin 3	GND	-	-	TBD
Pin 4	D5	D5	-	P82
Pin 5	SCKP	SCKP	-	P80
Pin 6	STCP	STCP	-	P81
Pin 7	GND	-	-	GND
Pin 8	SPI_Data_In (Single)	-	S01	P812
Pin 9	Clock	-	SCK	P810
Pin 10	Vcc	-	VDD	VDD (3.3V)
Pin 11	GND	-	-	GND
Pin 12	GND	-	-	GND

The diagram illustrates the hardware setup for interfacing a CS Module with eight DAC modules (MCP4822-E/P). The CS Module uses a 74HC595 shift register to manage the bus signals. The DAC modules are connected to the bus through individual headers (D1-D8), each equipped with a 100nF decoupling capacitor. The connections for each DAC module include VDD, \*CS, SCK, SDI, VOUTA, AVSS, VOUTB, and \*LDAC.

D8 to D1 Output each line is 2 output, bottom 2 rows are ground.



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