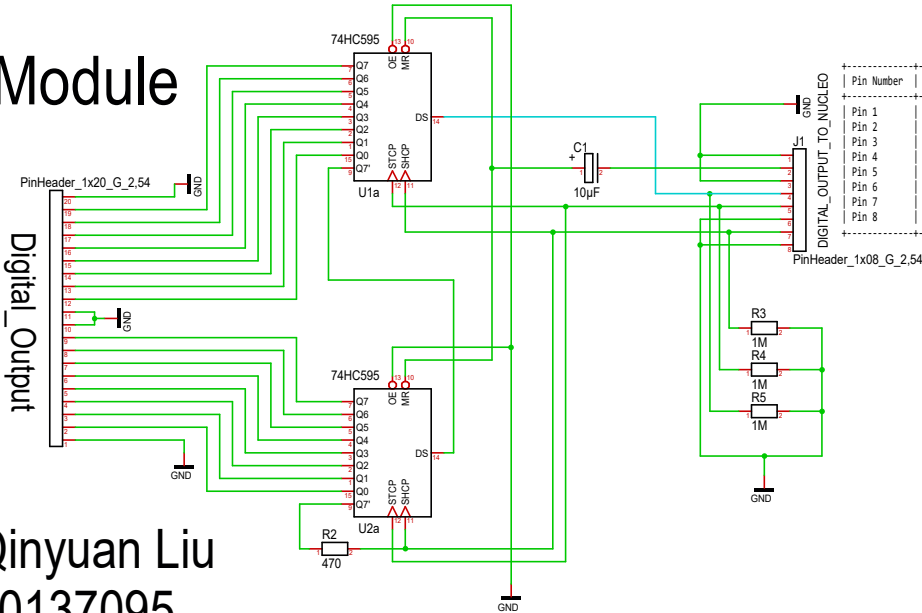


Digital_Output_Module

Header Pin	Description	74HC595 Connection
Pin 1	GND	-
Pin 2	Digital_OUT_1	U1_Q0
Pin 3	Digital_OUT_2	U1_Q1
Pin 4	Digital_OUT_3	U1_Q2
Pin 5	Digital_OUT_4	U1_Q3
Pin 6	Digital_OUT_5	U1_Q4
Pin 7	Digital_OUT_6	U1_Q5
Pin 8	Digital_OUT_7	U1_Q6
Pin 9	Digital_OUT_8	U1_Q7
Pin 10	GND	-
Pin 11	GND	-
Pin 12	Digital_OUT_9	U2_Q0
Pin 13	Digital_OUT_10	U2_Q1
Pin 14	Digital_OUT_11	U2_Q2
Pin 15	Digital_OUT_12	U2_Q3
Pin 16	Digital_OUT_13	U2_Q4
Pin 17	Digital_OUT_14	U2_Q5
Pin 18	Digital_OUT_15	U2_Q6
Pin 19	Digital_OUT_16	U2_Q7
Pin 20	GND	-



Pin Number	Description	74HC595 U1	74HC595 U2	Nucleo Pin	Pin Configuration
Pin 1	GND	-	-	GND	Ground
Pin 2	VDD	VDD	VDD	VDD	Power
Pin 3	GND	-	-	GND	Ground
Pin 4	LATCH	LATCH	LATCH	PA9	GPIO Output (Latch)
Pin 5	DATA	DATA	Q7'	PA2	GPIO Output (Data Set)
Pin 6	GND	-	-	GND	Ground
Pin 7	CLK	CLK	CLK	PA8	Clock
Pin 8	GND	-	-	GND	Ground

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20137095
FYP

Maßstab	66.67%	Firma	Zeichner	Blatt
Änderung	26.10.2024 16:52		Titel	
Ausgabe	27.10.2024 18:55			
Datei	STM32_FYP_Digital_Out_Module.T	Projekt		