A High Precision EEG Acquisition System Based on the CompactPCI Platform

Jingyang Chen, Xiaoqiong Li*, Xue Mi, Shaowu Pan
School of Life Science
Beijing Institute of Technology
Beijing, China

Abstract—**Electroencephalography (EEG) is the recording of electrical activities generated by nerve cells in the cerebral cortex. As the only non-invasive method for measuring brain activities from human scalp, it has been widely used in the area of medical diagnosis, neuroscience research, commercial application, etc. Most of the existing EEG acquisition systems, which are usually comprised of analog switches, operational amplifiers, analog-digital converters and specific instruments, have the weakness of high expenses, limited accuracy and difficult to update. Aiming at the need of cognitive science research and brain computer interface (BCI) design, a high precision EEG acquisition system based on the compact peripheral component interconnect (CompactPCI) platform was designed in this paper. A commercial EEG hat with adjustable electrodes was used to collect interested EEG signals. And ADS1299, a high resolution analogy front end IC proposed by Texas Instruments, was adopted in the system to acquire and convert EEG signals. To facilitate hardware expansion, system integration and data processing, the device was designed in the form of a 3U CompactPCI card and connected to an embedded computer. A graphical user interface (GUI) software was provided to control the data acquiring, storing and processing. In addition, the least mean squares (LMS) adaptive filter was realized to optimize the signals. The compact and highly integrated analogy circuit in this design significantly avoided the contamination of signals by environmental noises and reduced device-to-device connection complexity. Meanwhile, the system structure based on the CompactPCI platform made it easier to adjust signal channels and evaluate novel algorithms. The accuracy tests and alpha wave detection experiments showed that our EEG acquisition system had high accuracy and was applicable to various EEG-related experiments. The research in this paper may have reference value for the development of portable EEG acquisition system and BCI device.**

Keywords-electroencephalography; acquisition system; multi-lead; ADS1299; CompactPCI

I. INTRODUCTION

Electroencephalography (EEG) is the recording of electrical activities which are generated by nerve cells in the cerebral cortex. As the only non-invasive method for measuring brain activities from human scalp, it has been widely used in the area of medical diagnosis, psychological evaluation, neuroscience research, commercial application, etc. [1-4] As EEG signals are weak signals whose amplitude commonly ranges from 0 to 100μV, the acquired EEG data are easy to be contaminated by cardiac artifacts, eye-induced artifacts, muscle activation and external noises [5]. To amplify signals, suppress noises and extract interested data, most of the existing EEG acquisition systems contain complex and large scale analogy front end circuits which are usually comprised of a large number of analogy devices or modules such as operational amplifiers, analog switches, analog-digital converters, notch filters, etc. [6] As a result, these systems have the weakness of large weight, high cost, limited accuracy and difficult to update or adjust. More importantly, it is hard and time-consuming to evaluate online algorithms and process acquired data on these systems in real time, which may be an obstacle to relative researches. In recent years, portable and adjustable EEG systems have become a great trend [7-9]. Manufacturers such as ANT Neuro and Compumedics have introduced a number of portable or mobile EEG acquisition instruments and recording platforms which are equipped with flexible and extensible software [10-11].

Aiming at the need of cognitive science research and brain computer interface (BCI) design, a high precision EEG acquisition system based on the compact peripheral component interconnect (CompactPCI) platform was designed in this paper. To reduce the coupling way of external noises and make the system structure concise, a commercial EEG hat with adjustable electrodes was used to collect EEG signals in specified regions of the scalp. And ADS1299, a high resolution analogy front end IC proposed by Texas Instruments for biopotential measurements was adopted in the system to acquire and convert EEG signals. To facilitate hardware expansion, system integration and data processing, the device was designed in the form of a 3U CompactPCI card and connected to an embedded computer through the PCI interface. A graphical user interface (GUI) software was provided to control the data acquiring, storing and processing. And a least mean square (LMS) adaptive filter was realized to optimize the signal by software. The compact and highly integrated analogy circuit in this design significantly avoided contamination of signals by external noises. And the modular system structure based on the CompactPCI platform made it easier to adjust and expand signal channels. Moreover, the Microsoft Windows-based software platform offered wide room to develop, deploy and evaluate novel algorithms.

The rest of this paper is organized as follows. An overview on the function and structure of our EEG acquisition system

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will be introduced in Section II. The hardware design based on ADS1299 and FPGA will be described in Section III. The software design will be mentioned in Section IV. The results of accuracy test and evaluation experiments will be provided in Section V. Section VI will be conclusion and follow-up relevant research work.

II. Overview of the EEG Acquisition System

A. General Design

As shown in Fig. 1, both hardware and software of the EEG acquisition system were integrated into a 4 slot CompactPCI chassis provided by ADLINK Technology. Up to 4 EEG acquisition devices were optional to install, each of which was designed in the form of a standard 3U CompactPCI card and provided 16 sampling channels. And the software system, including the GUI, programming interfaces, digital filters and device drivers were built on the embedded computer to realize system control and data processing.

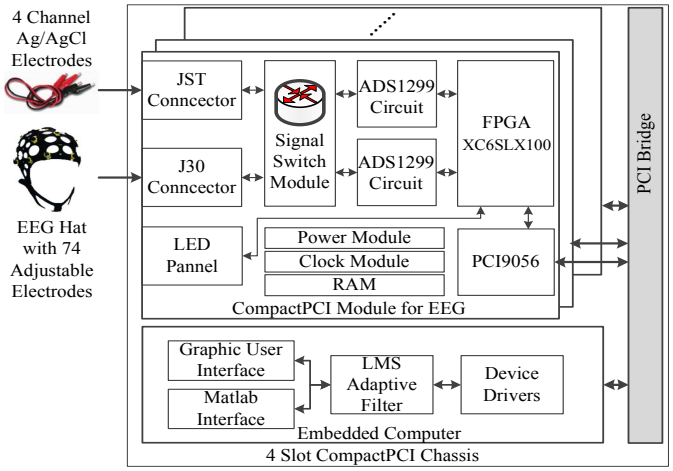


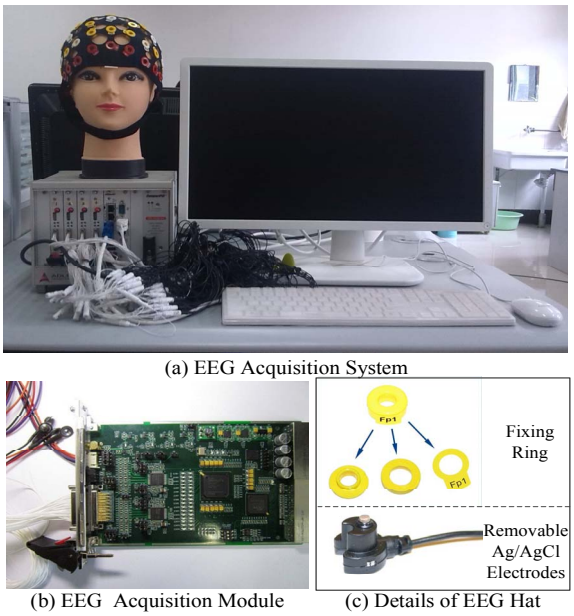
Figure 1. Diagram of EEG Acquisition System

The design of the hardware was based on FPGA and followed the standard of CompactPCI. Beside the baffle of a CompactPCI EEG acquisition device, a JST connector (S4B-PH-K-S) and a J30 connector (J30J-37TJW) were installed to optionally connect to 4 channel Ag/AgCl electrodes and EEG hat with 74 adjustable electrodes. Input signals were routed to the analogy front end circuits via a signal switch module consisted of jumpers and switches. Two ADS1299, a kind of high precision IC for biopotential measurements, were adopted to build analogy front end circuits. The working processes of signal sampling, data converting, PCI communication and device configuration were entirely under the control of a FPGA (XC6SLX100). In addition, a LED panel was designed to display working status of the device in real time.

As to the software of the system, the device drivers and application programs were built on the Microsoft Windows operating system (OS) of the embedded computer. The device drivers were developed based on the framework of WinDriver and controlled devices through the PCI bridge. An LMS adaptive filter was realized on top of drivers by C++ to optimize captured data. GUI applications were designed to provide various functions of data recording, data playback, frequency spectrum analysis, etc. Moreover, programming and data interfaces to MATLAB were offered, which made it more convenient and efficient to design, employ and evaluate novel algorithms.

B. Modular Design and Adjustable EEG hat

The major purpose of the system is to provide a common platform to evaluate novel algorithms and provide references for the design of a portable EEG system. Therefore, a greater emphasis has been placed on modular and reconfigurable design:



(a) EEG Acquisition System

(b) EEG Acquisition Module (c) Details of EEG Hat

Figure 2. Photo of EEG Acquisition System

- As shown in Fig. 2(a) and Fig. 2(b), to facilitate system update and expansion, the CompactPCI platform was selected to integrate EEG acquisition devices. On the one hand, each of our 3U CompactPCI cards for EEG acquisition provided 16 sampling channels and can adjust or route input signal flexibly. On the other hand, other commercial data acquisition devices with CompactPCI interfaces were also supported in this system, which were able to meet special application requirements.
- A commercial EEG hat provided by Medical Computer Systems Corporation was used in this system as the major tool to collect EEG signals. As shown in Fig. 2(c), a removable Ag/AgCl electrode can be mounted to any one of the 74 fixing ring on the EEG hat [12]. So the number and installation position of electrodes can be adjusted flexibly, which made experiments of EEG acquisition more specific and efficient.
- A reconfigurable FPGA was adopted in CompactPCI modules to realize hardware control and data

communication. Meanwhile, a general software platform was provided in the embedded computer of the CompactPCI system for software development. Consequently, it can be fast and convenient to redesign or redeploy algorithms in both software and hardware.

III. HARDWARE DESIGN BASED ON ADS1299 AND FPGA

A. Analogy Front End Circuit Design

The ADS1299 is a 24-bit, low-noise, multichannel analog-to-digital converter (ADC). It is a specific device for biopotential measurements with features of high input impedance, high common mode rejection ratio and low-noise amplification. The built-in programmable gain amplifier (PGA) significantly simplified the analog front end design [13]. Each PGA supports differential inputs and its negative input can be switched between the negative input pin and the bias input pin via the configuration registers. Besides, each channel of ADS1299 has a flexible input multiplexer which can select the input signals independently for various applications.

To further improve the signal quality, there were several methods utilized:

- The analog front end (AFE) of the ADS1299 already has strong abilities of signal filtering and amplification. In order to reduce external noise further, a resistor-capacitor (RC) high-pass filter was placed in front of the sampling circuit to filter the baseline drift.
- The inputs of the ADS1299 were designed to be differential which can reduce the common mode noise caused by the sampling circuit.
- To reduce noise cause by the printed circuit board (PCB), the filter capacitors were placed close to the VREF pins to reduce the distance between the VREF pin to GND plane.
- The separation of planes is also considered in this mixed signal circuit when designing the PCB. The analogy and digital sections were separated strictly and no jagged staggered area was allowed.

B. FPGA Design

The FPGA, which acted as processing core of the system, controlled the working processes of other ICs and the PCI communication. Configured by FPGA, ADS1299 sampled EEG signals and converted them to the digital signals. And PCI9056, the PCI bus master, transmitted the access commands and controlled data flow between FPGA and the computer.

The firmware of the FPGA, as shown in Fig. 3, consisted of the clock module, state control module, inner random access memory (RAM) read/write module, ADS1299 control module, data sampling module and PCI communication module.

As the maximum sample rate of ADS1299 was 16 KHz, while the clock of PCI bus was 33MHz. The inner RAM of FPGA was necessary to assist data transmission between these two asynchronous clock domains. It was used as a ping-pong buffer which consisted of two dual-ported RAM, when one was being written, the other was being read. Moreover, considering the width of the data bus of PCI is 32 bits, while ADS1299 is a 24 bits ADC. The excess 8 bits were used as the index of channels from 1 to 64 and also reserved for future expansion.

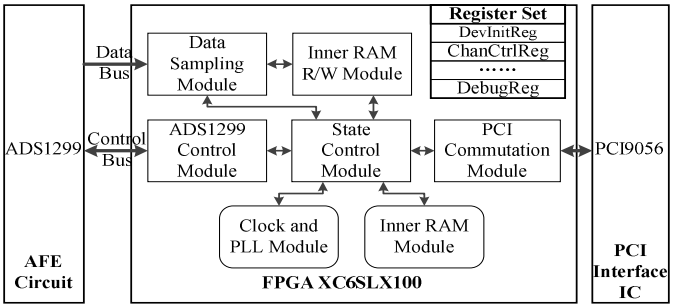


Figure 3. FPGA Modular Design

As shown in the Fig. 4, the working flow of the FPGA was as follows.

- The FPGA initialized the configuration of ADS1299, including the sampling rate, the gain of PGA and the positive and negative inputs.
- The FPGA started to sample the outputs of the ADS1299 through a serial peripheral interface (SPI) and stored the data into the inner RAM continuously.
- When either of the ping-pong RAM was full, the FPGA triggered a PCI interrupt to the PCI9056 which indicated that the data was ready and the computer should set up a PCI direct memory access (DMA) to transfer the data.
- The computer started a PCI DMA to acquire the data. When the DMA operation was finished, the FPGA checked if there were any valid PCI commands for changing the configuration of ADS1299. If there was a command, it re-initialized the ADS1299. Otherwise, it continued to sample data.

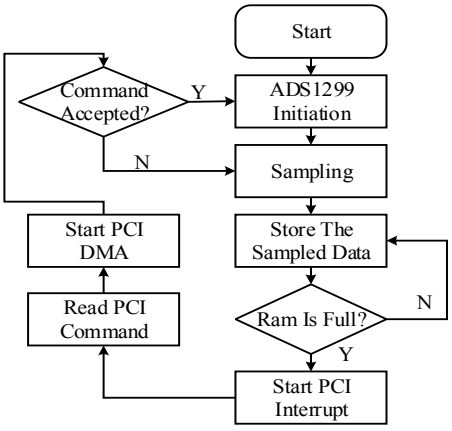


Figure 4. FPGA Flow Diagram

IV. SOFTWARE DESIGN AND FILTERING ALGORITHM

A. Architecture of Software

Figure 5 shows the architecture of software in this design. The software of the system, which mainly included device drivers, the LMS filter and the GUI software, was developed upon Microsoft Windows by C++ and WinDriver. The GUI software was capable of acquiring, storing and processing data on the basis of the OS. Additionally, it was supported to play back the historical data files, convert data to the mat files and call MATLAB programs or toolboxes for advanced analysis. Besides, an LMS adaptive filtering algorithm was employed to suppress the power-line interference and baseline drift.

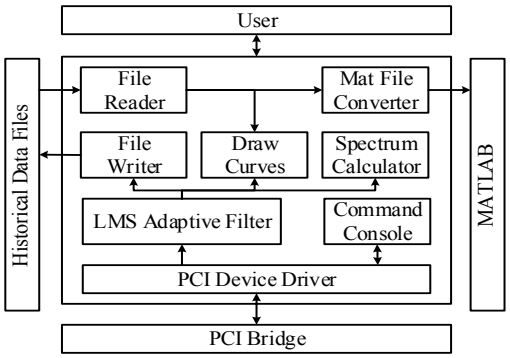


Figure 5. Diagram of Software Architecture

B. Software flow Diagram

The data transfer between the GUI software and the PCI device was completed by the device driver. The working flow of the software is as shown in Fig. 6. Firstly, the software tried to find and open the specific PCI device. Secondly, it allocated some memory as the data buffer, set the parameters for DMA and enabled the PCI interrupt. Thirdly, when an interrupt came, it called interrupt service routine and started acquiring and filtering data. Fourthly, it notified three sleeping threads to do different work including drawing curves, saving data to files and calculating the frequency spectrum before it returned to wait for the new interrupt.

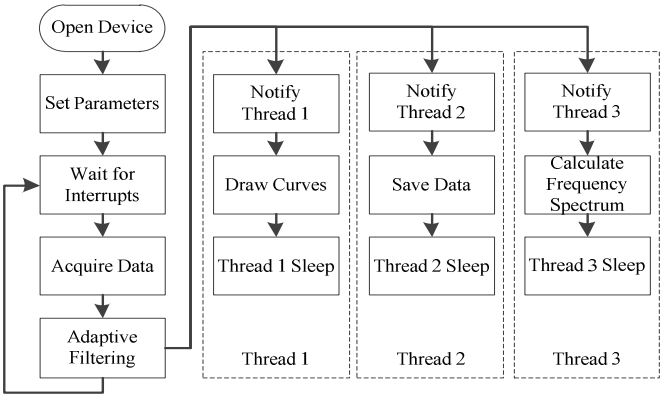


Figure 6. Software Flow Diagram

C. Filtering Algorithm Realization

The EEG signals are extremely weak so that they can easily be contaminated. Therefore it is quite necessary to improve the signal to noise ratio (SNR) by applying signal filtering.

The least mean square (LMS) adaptive filtering algorithm is a simple and efficient filtering method which updates filter weights step by step (starts with zero in most cases). At each step, the weights are calculated by finding the gradient of the mean square error. As shown in Fig. 7, the weights can converge to the optimum filter weights which makes reference signal close to the noise finally. This paper proposes two types of reference signals for the LMS filter to suppress power-line interference and baseline drift.

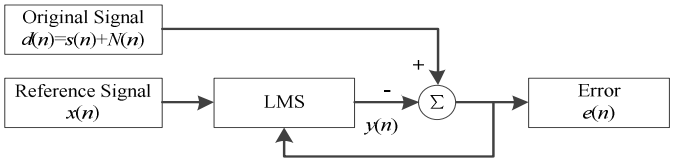


Figure 7. LMS Filter

As shown in (1), in order to suppress the power-line interference, the sine and cosine signals were used as reference signals where f_0 equaled the power-line frequency and f_s equaled the sampling rate.

$$\begin{aligned} x_1 &= C_0 \sin(k\omega_0) \\ x_2 &= C_0 \cos(k\omega_0) \\ \omega_0 &= 2\pi f_0 / f_s \end{aligned} \tag{1}$$

As shown in (2), in order to suppress the baseline drif, the nonzero DC signal was chosen as another reference signal.

$$x_3 = C_{DC} \tag{2}$$

After several iteration steps, the best filter weights will be gotten and the output error *e(n)* will approach to the pure EEG signals.

Moreover, the step size is crucial to the LMS algorithm. If the step size is chosen to be too large, the filter weights would not converge and cause instability. On the other hand, if the step size is too small, the convergence speed would be too slow. Thus, a proper step size should be obtained by experiments and 0.03125 was used in this paper.

V. TEST AND EXPERIMENT

A. Accuracy Test

Table I shows the major performance parameters of our EEG acquisition system. To test the sampling accuracy, the working parameters of ADS1299 were set as Table II and a channel input was shorted externally. Then the input noise of the system can be gotten by sampling. And the average peak-to-peak noise was 0.77μV when the sampling time was 60 seconds. The test result was close to accuracy data provided by Texas Instruments and the accuracy of our system was sufficient for EEG-related researches.

TABLE I. TECHNICAL SPECIFICATIONS

Item	Parameters
Channels	64 (16×4 modules)
A/D Resolution	24 Bit
Sampling Rate	250 Hz to 16 kHz
Input Signal Range	0 ~ 5 V/-2.5 ~ +2.5V
Input Noise	1.0 μV (70 Hz BW)
Input Impedance	>1 GΩ
CMRR	110dB

TABLE II. TEST CONDITIONS

Item	Parameters
Input Mode	differential
Gain of the PGA	24
Sampling Rate	250 Hz
VREF	Internal
Power Suply	±2.5 V

B. *Evaluation Experiment*

There were three healthy male subjects, whose ages ranged from 22 to 23 years old, participating in the evaluation experiment of alpha wave detection. Firstly, the subjects sit about 1 meter away from the computer in a quiet experiment room and rest for at least 20 minutes. Secondly, 64 electrodes were connected to subjects' scalp and adjusted properly to avoid invalid connection according to the real-time EEG signals. The sampling rate of the system was set to 250 Hz. Thirdly, each subject was told to keep his eyes open for 1 minutes and remain closed for another 1 minutes.

The acquired data was processed on the MATLAB and the frequency spectrum of the Alpha Band (8-12 Hz) was calculated by the fast Fourier transform (FFT) method.

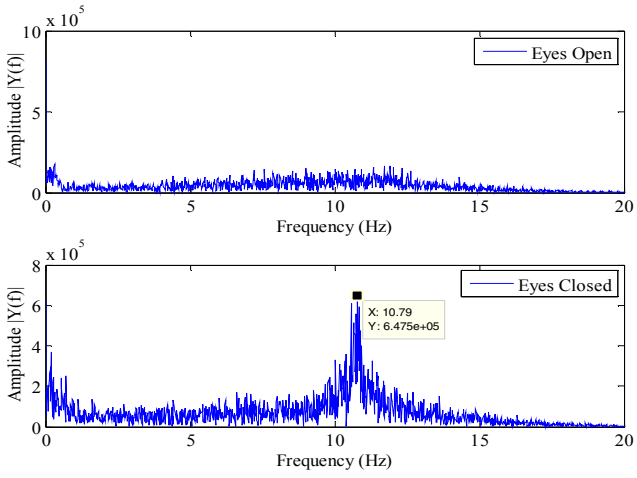


Figure 8. Alpha Wave Detection Experiment Result

As shown in Fig. 8, there was an obvious aptitude increase in Alpha Band when the subjects closed their eyes. And the frequency of the peak point was 10.79 Hz. So the system can detect alpha wave successfully.

VI. CONCLUSION AND FUTURE WORK

This paper proposed a high precision EEG acquisition system for cognitive science research and brain computer interface (BCI) design. ADS1299, a high performance IC for biopotential measurements, was used to acquire and convert EEG signals. And the CompactPCI platform was adopted to integrate the system, which provided sufficient room for hardware expansion and a general software platform. The highly integrated analogy circuit significantly improved the precision of acquired data and reduced device-to-device connection complexity. With the adjustable and reconfigurable design in electrodes and signal switches, the system was able to meet the need of various kinds of EEG experiments. The performance tests and alpha wave detection experiments showed that our EEG acquisition system was highly precise and applicable to EEG-related experiments.

With the development of modern integrated electronics, it has become a trend to develop portable or mobile EEG systems. The design in this paper only provided an evaluation platform for the minimization of EEG systems. Our future work will focus on the design of portable and low power EEG acquisition instruments for long term monitor.

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