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EEG data acquisition circuit system Based on ADS1299EEG FE

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Abstract— **The EEG analog front end evaluation module based on ADS1299 is presented in this paper. ADS1299EEG-FE is a recently introduced product by Texas Instruments enabling more efficient evaluation and prototyping of the EEG signals than most of the devices being used today. It is an eight-channel, 24 bit, low power, low noise, simultaneous sampling analog front end device for EEG signal acquisition and evaluation. This module uses MMBO Modular EVM motherboard that connects to the ADS1299EEG FE evaluation board using jumpers. This device provides a compact, cost effective mode of EEG signal evaluation with enhanced acquisition features enabling high levels of accuracy and portability.**

Keywords— **EEG data acquisition, ADS1299, analog front end evaluation module, MMBO, ADS1299EEG FE**

I. INTRODUCTION

Electroencephalography is one of the chief methods of detecting epileptic seizures, psychogenic non-epileptic seizures, migraine, encephalopathy and depression. EEG signals record the spontaneous electrical activity of the brain along the scalp over a period of time. Thus reliable EEG data acquisition is one of the chief aspects to analyse the EEG signals. ADS1299EEG FE is intended for evaluating and prototyping EEG FE signal using a simulator. Currently this model is used for development purposes and not for end equipment application.

The core is ADS1299 analog front end device for biopotential measurements and ADS1299EEG FE gives the EEG specific data acquisition module of the device. It is an eight-channel, 24-bit, simultaneous sampling device with low power and low noise features. It expedites the evaluation process and enables system development while keeping the device compact vis-à-vis size and providing a real-time simulator for signal evaluation.

II. EXISTING EEG AFE MODELS

One of the existing models as suggested by *Wenhui Quin et al. [1]* in 2014 is a CMOS based bio-potential acquisition system. This device includes a capacitively coupled chopper instrumentation amplifier, spike filter and a variable gain amplifier. The device uses 0.35µm CMOS technology. Noise is 0.85µVrms (0.5-100HZ) and has an external 80 kHz clock.

Another compressed sensing AFE biosensor suggested by *Daibashish Gangopadhyay, et al. [2]* is based on 0.13µm CMOS with alias-free sub-Nyquist acquisition through compressed sensing.

Shang-Lin Wu et al. [3] proposed a fully integrated 16 channel AFE circuitry comprising of differential difference amplifiers and DC offset rejection components. It has a noise efficiency factor 2.78 and total input referred noise of 0.826µVrms. Also, it works in the target frequency range of 0.1Hz-1.0 kHz.

*Seunghyun Lim et al. [4]*suggested the use of AC coupled stabilised instrumentation amplifier for low noise and a capacitive impedance boosting loop for high input impedance. This method leads to an input impedance of 3.5GΩ and a CMRR of 139.1dB. This AFE was fabricated using a 0.18µm CMOS process. The input noise was measured to be 0.205µVrms in the bandwidth of 0.5Hz-100Hz.

A biopotential acquisition AFE suggested by *Seunghyun Im et al. [5]*provides effective DC offset and ripple rejection. This uses a capacitively coupled chopper instrumentation amplifier to achieve low noise. Input noise is 1.6 µVrms in a bandwidth from 1Hz to 100Hz. Ripple artifacts are reduced using a continuous time AC coupled ripple reduction loop and DC servo loop.

FPGA is used for devising the wireless healthcare monitor system as proposed by *Kuen-Chih Lin and Wai-Chi Fang [6]*. This highly integrated hardware design includes a biomedical front end device to acquire and digitize EEG or ECG data. This also includes a control interface to control front end circuits. Wireless Bluetooth is used to transmit the signal between processor and display platform.

Pavan Bhargava et al [7] designed a 262nW AFE for batteryless EEG acquisition. This 'deploy and forget' EEG system is capable of batteryless wireless transmission of neural data. It uses digital feedback loop to cancel electrode offset and noise pre-amplification. A dual-slope charge

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sampling acquisition neural system is proposed by *Seung Bae Lee et al [8]*. This AFE uses the charge sampling technique for conditioning the acquired data-amplifying, filtering and sampling the data simultaneously. The PWM output is input into a circular shift register to produce a pseudo-digital output for wireless transmission. This system is 8-channel, fabricated on 0.35µm CMOS consuming 255µW. The input referred noise is 6.50µVrms in the 288-10k frequency range.

III. SYSTEM STRUCTURE AND SCHEME OF ADS1299EEG FE

ADS1299 (for EEG application) hardware consists of the MMBO Modular EVM motherboard (as the digital control interface) connected to the ADS 1299EEG FE evaluation board. A universal AC to DC wall adapter is present to provide the +6V DC supply.

TABLE 1

Some of the features supported include-

HARDWARE FEATURES	SOFTWARE FEATURES
>Configurable - -bipolar/unipolar supply operation -internal/external clock -DC coupled inputs -reference electrode -bias electrode >External bias electrode drive >External shield drive amplifier	>virtual oscilloscope, FFT, histogram for analysis >enable data exporting for data post processing

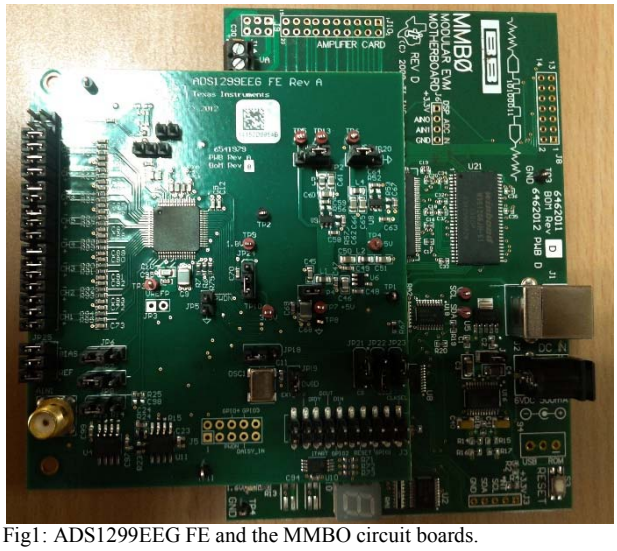


Fig1: ADS1299EEG FE and the MMBO circuit boards.

Figure 1 gives the ADS1299EEG FE circuit board along with the MMBO control board. This evaluation module (EVM) is further connected to the computer using a USB port for analysis of the data.Figure 2 gives the schematic diagram for the ADS circuit board.

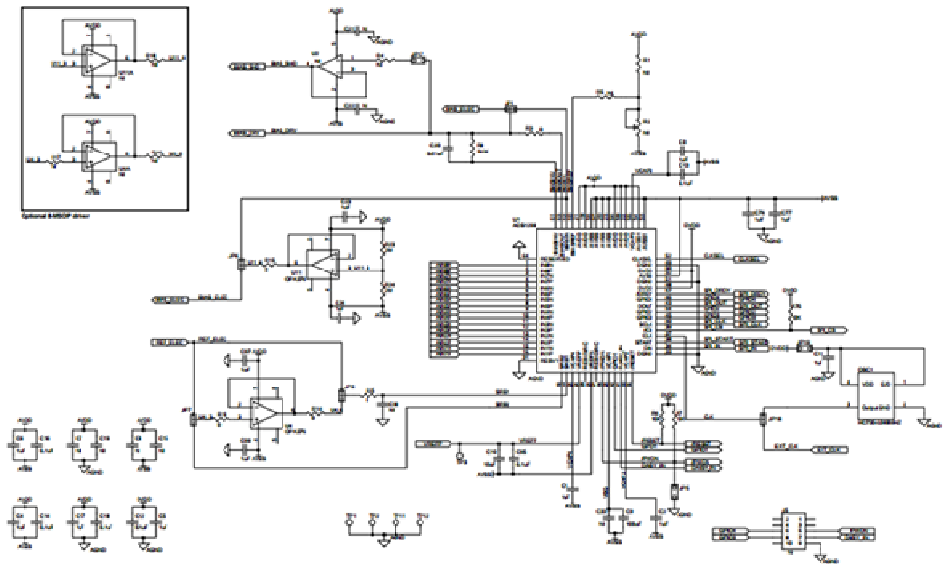


Fig2:ADS1299EEG FE schematic

IV. HARDWARE DESIGN AND COMPONENTS

The ADS1299EEG FE board is configured (Fig.3) to be used with MMBO data converter.

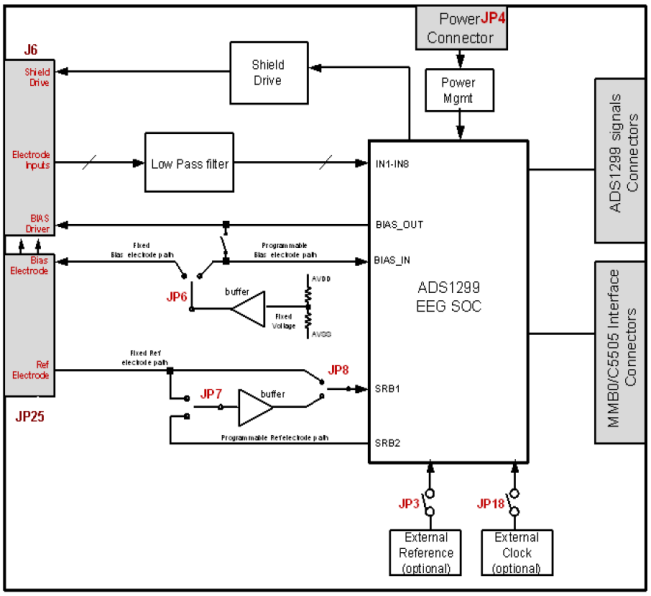


Fig3: ADS 1299 EEG functional block diagram [8]

External support circuitry provided for testing includes external references, clocks, lead-off resistors and shield drive amplifiers. Some of the hardware components are-

- *Power Supply*: The main power supplies for the front-end board are supplied by MMBO through jumper J4. ADS1299EEG FE is set for a default unipolar analog supply of +5V and +1.8V or +3V digital supply.
- *Clock*: ADS1299 has an on-chip oscillator circuit with a frequency of 2.048 ± 5% MHz powered by +1.8V or +3V digital supply. The provision of attaching an external clock is also present for higher accuracy needs.
- *Reference*: There is an on-chip reference circuit which provides reference voltages. External reference can be provided using U3 generator and driver buffer.
- *Analog inputs*: The device board is designed for 8 channel input. It works on 2 modes-

1) Differential Input Mode
2) Single Ended Inputs

Apart from these hardware features, some of the other system on chip features are-

- On-chip bias amplifier and oscillator
- Programmable MUX to enable setting of reference and bias electrode.
- DC/AC lead off detection
- Low channel noise (1µVpp for 65Hz bandwidth)
- Eight integrated INAs and eight 24-bit ADCs
- Data rates of 250 to 16,000 samples per second

V. SOFTWARE PACKAGE GUI AND CHANNEL REGISTERS

The ADS1299EEG FE evaluation module GUI has the following features:

- ADC register: This tab includes all the control registers (channel registers, LOFF and BIAS, GPIO and other registers, register map) in a series of tabs
- Analysis: This tab provides different ways to interpret the acquired data in a series of related tabs (Scope, FFT, Histogram)
- Apart from these, there is an 'About tab' and 'Save tab' for providing information about the EVM and saving the data respectively.

Registers: The following are the ADC registers and their functions (as present in ADS1299EEG FE)-

- *Global channel Register*:

This allows the user to manipulate the device configuration such as MRB/Daisy-chain mode, clock connection, data rate, internal test source amplitude and frequency, reference voltage, bias drive and the lead-off registers.

- *Channel Control Registers*:

This enables the user to configure the front end MUX globally or individually.

- *GPIO and Other Registers*:

This controls the four general purpose I/O pins, SRB1 control, pulse mode control and lead off comparators.

- *Lead-Off and BIAS Registers*:

This includes controls for lead-off detection, lead-off status register, bias voltage and internal bias drive amplifier.

- *Register Map*:

This allows the user to view the state of all the internal registers.

Analysis: This measures the exact amplitude of the input signals from each channel. Also, noise, sampling rate, PGA gain can also be evaluated.

- *Waveform examination tool*: This helps zoom in the waveform for selective analysis.
- *Histogram tool*: This gives the bin separation of different amplitudes of the EEG waveform harmonics in the form of histograms.

FFT tool: This allows the user to examine the channel specific spectrum and also evaluate SNR, THD, CMRR, etc.

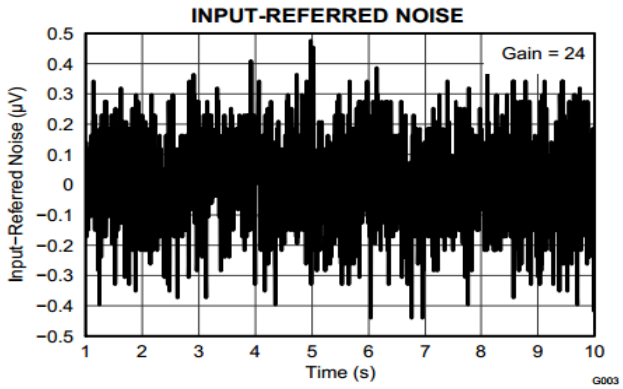
VI. SYSTEM CHARACTERISTICS

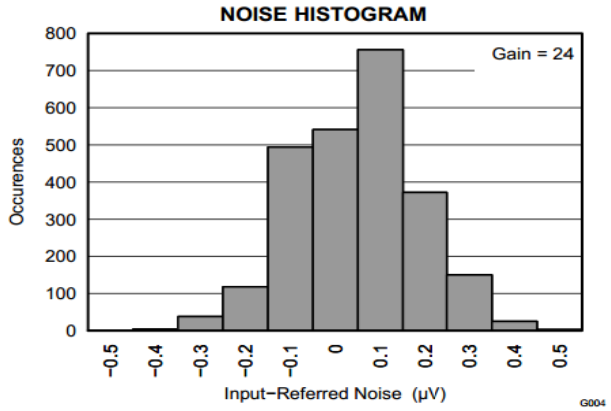
Following are some of the electrical characteristics of the ADS1299 that makes it superior to some of its counterparts.

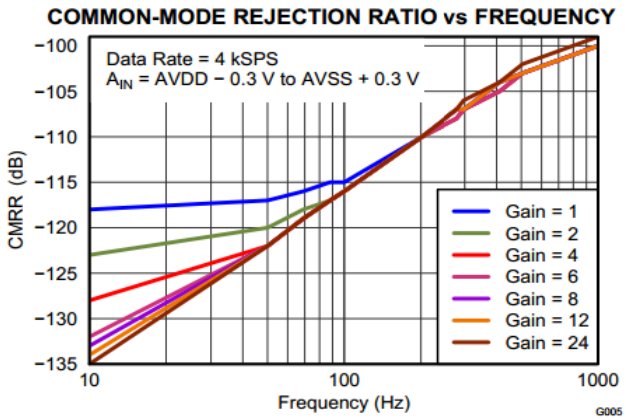
- Input referred noise- 1µVpp for a frequency range of 0.01-70Hz
- Offset error- 60µV
- Gain error- 0.1% of full scale

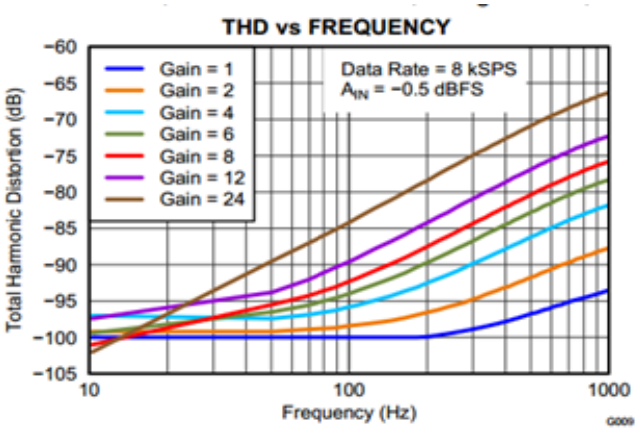
- Common mode rejection ratio- (-)120dB [f_{CM}=50Hz and 60Hz]
- Total Harmonic Distortion- (-)99dB [V_{IN}=-0.5dBFs, f_{IN}=10Hz]

Some of the characteristic plots of the electrical characteristics of ADS1299 [10]









VII. EVM TEST OPTIONS

(a) On-Chip Input Short

This test gives the channel noise present and the offset. To conduct this test, the input is internally shorted by setting the input MUX of each channel to 001. Control registers are set such that gain is 24, SRB2 is open, channel input shorted and power-down is normal.

(b) External Input Short

Here the positive and negative input channels are tied to a common voltage via a 5kΩ resistor. This test is used to determine the input bias current on noise. Here, the bias current appears as a DC offset because of the input 5k impedance.

(c) Common Reference on Negative Inputs

Here all negative inputs are connected to a common reference. Consequently an on-board test using this setting is used to check the noise present. The noise in this test includes the channel noise and that of the two 5kΩ resistors.

(d) Buffered Common Reference Input

The previous test yields leakage current of the order of 3.2nA for a 16 channel system which increases progressively with increase in the number of channels. To avoid this, the common reference is buffered before connecting all negative inputs. Reduced leakage current however has a trade-off with increased noise introduced by an additional op-amp (buffer).

(e) Test Signal and Other MUX inputs

The internally generated test signal is used to check signal integrity while the MUX is used to measure supply voltage, temperature, etc.

(f) Arbitrary Input Signal

Any arbitrary input signal can be fed via J6 and the corresponding results obtained. This can be done by either using the differential input method or the single ended input method.

VIII. CONCLUSION

ADS1299EEG analog front end module provides an overall improvement in the existing technologies. This 8 channel simultaneous sampling device provides low noise, low power

data acquisition. Apart from these, it has a host of hardware programmable features which makes it user friendly. The software provides a host of features for data analysis and evaluation thus giving signal processors an apt simulation platform.

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