CSCI 340
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Topics: Synchronization using hardware support

Test-and-Set (TS)

In a uniprocessor environment, the CS problem could be simply solved if we could disallow interrupts while a shared variable is being modified. This solution is not feasible in a multiprocessor environment. Many machines provide special hardware instructions that allow to test and modify the content of a word, or to swap the content of two words, atomically (without interruption).

TS of a memory location causes the content of the specified memory location to be loaded into the CPU register and the memory to be written with a value of True.

Definition of the Test-and-Set instruction:

```
boolean TS (target:boolean) {

        TS = target;
        target = true;
    }
```

Mutual-Exclusion implementation with TS:

Mutual Exclusion is satisfied: