UNIVERSITI TEKNOLOGI MALAYSIA

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SECR1013 DIGITAL LOGIC

MODULE 7: LATCHES & FLIP-FLOPS

FACULTY OF COMPUTING

Objectives:

- To introduce the various types of latches and flip-flop;
- To explain the characteristic of latches and flip-flop;
- To illustrate the timing diagram asociated with each latches and flip-flop operations.

Topics Outline:

LATCH

- S-R Latch
- Gated S-R Latch
- Gated D Latch

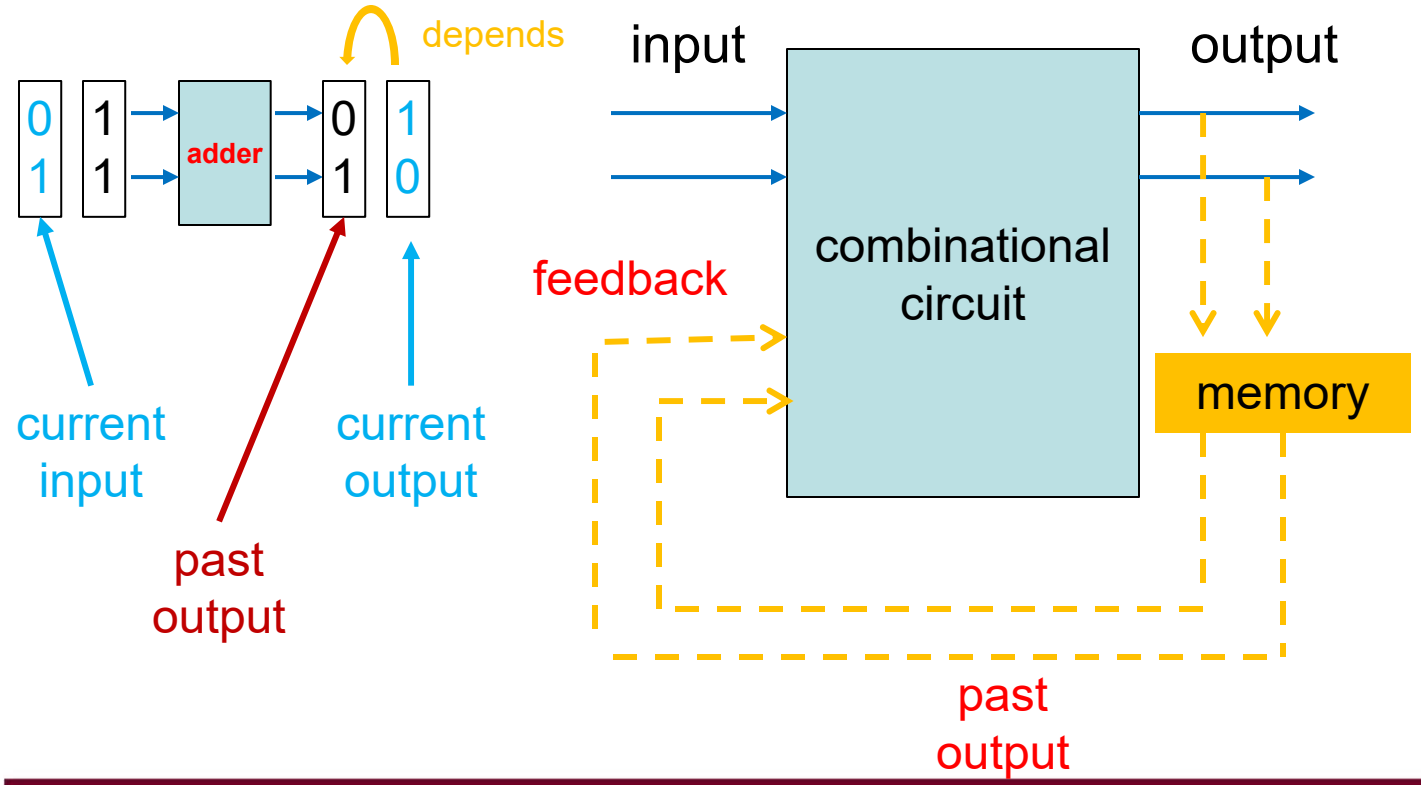
FLIP-FLOPS

- S-R Flip-Flop
- J-K Flip-Flop
- D Flip-Flop
- T Flip-Flop

Introduction to Latch & Flip-Flop

Introduction

- In sequential circuits, the current output depends on the current input as well as past output / outputs



Example of seq. circuits:
a) flip flop
b) counter
c) register

counter 0 to 5

0: 0
1: **0** + 1
2: **1** + 1
3: **2** + 1
4: **3** + 1
5: **4** + 1

Sequential Vs Combinational Logic Circuit

unlock:

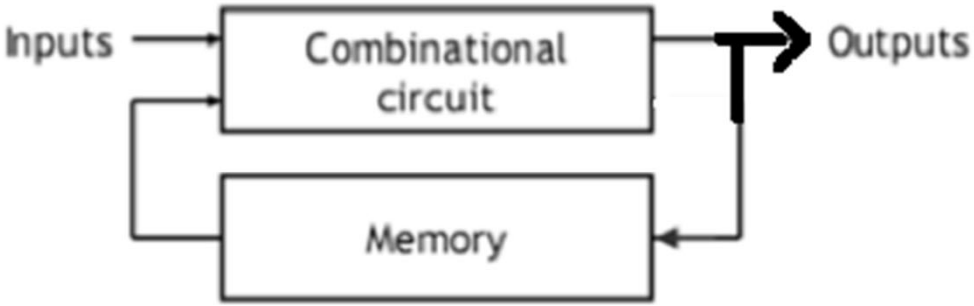
4 5 6 7

Combinational Logic Circuit:

key sequence is NOT matter

- The output depend on the input
- It has no memory element
  - Therefore, it cannot memorize the previous output

Sequential Logic Circuit:



unlock:

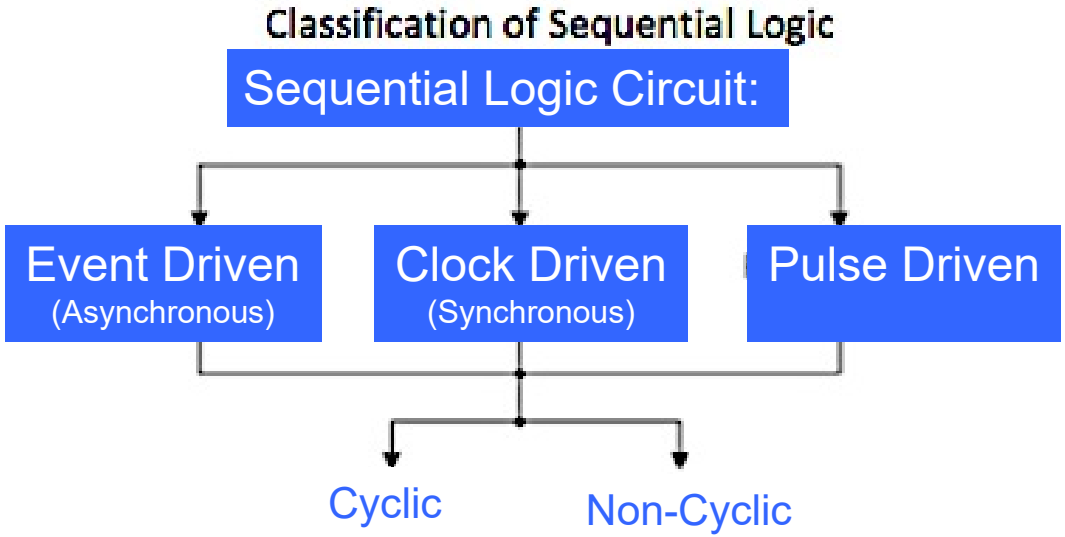
4 → 5 → 6 → 7

To unlock:
key sequence is MATTER

- It has memory element
- The output depend on the input, as well as the previous output from the feedback elements

Sequential Logic circuits can be divided into 3 main categories:

1. Clock Driven - Synchronous Circuits that are synchronized to a specific clock signal.
2. Event Driven - Asynchronous Circuits that react or change state when an external event occurs.
3. Pulse Driven - Which is a Combination of Synchronous and Asynchronous.



Sequential logic circuits that return back to their original state once reset, i.e. circuits with loops or feedback paths are said to be "Cyclic" in nature.

Latches

Latch

- Latch is a type of temporary storage device
- It has two stable states (bi-stable).
- Latch is level sensitive, or level-triggered.
  - are dependent on the voltage level applied (0/1), not on any signal transition.
- Type of Latch :
  - i) S-R
  - ii) Gated S-R
  - iii) Gated D

LOW HIGH

INFO :

A ***bi-stable*** state is one with *two-stable* output states.

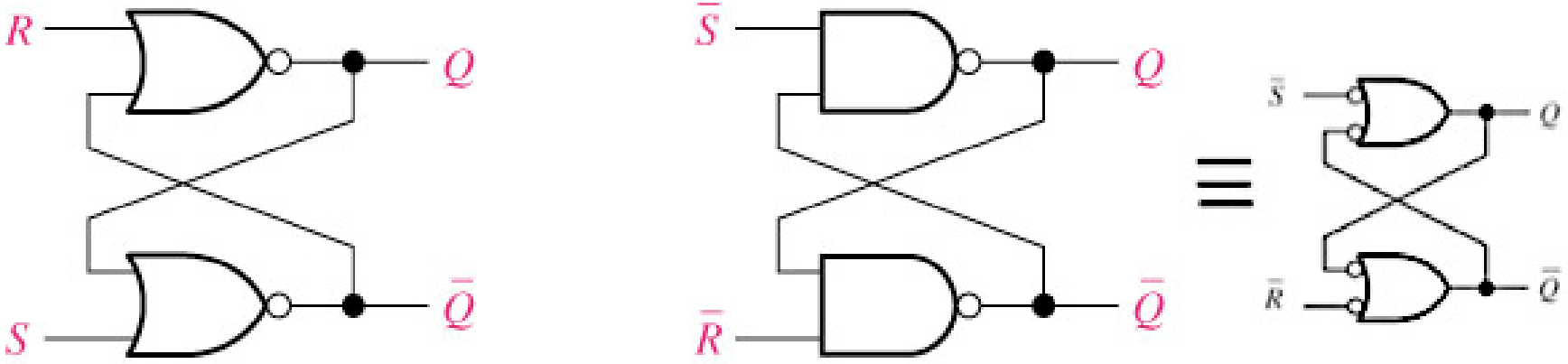
S → Set

R → Reset

D → Data

(i) S-R Latch

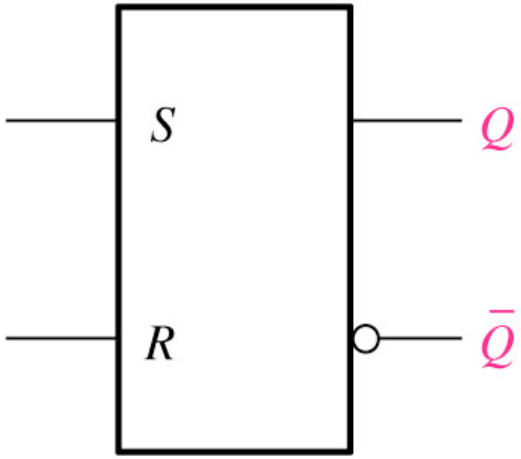
- The output of each gate is connected to an input of the opposite data.
- This produces a regenerative feedback.



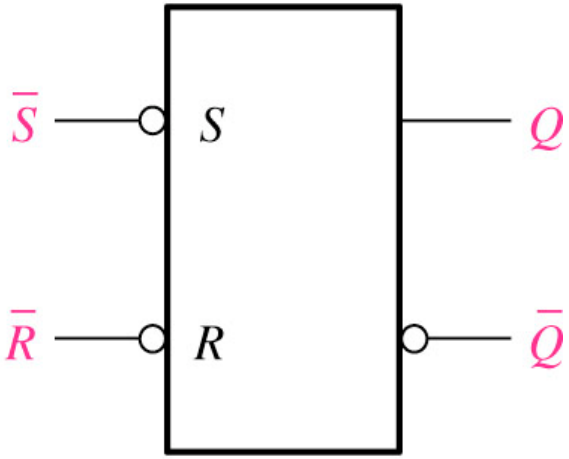
(a) Active-HIGH input S-R latch

(b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

S-R Latch: Logic symbol

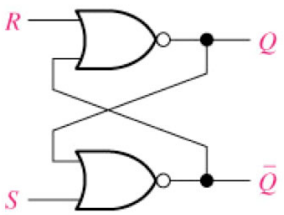


(a) Active-HIGH input S-R latch



(b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

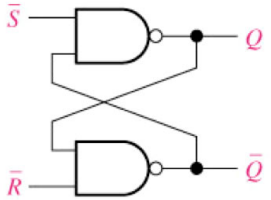
Circuit (a) Active-HIGH input S-R latch :



- use NOR gate
- Input R and S
- Output Q and Q'

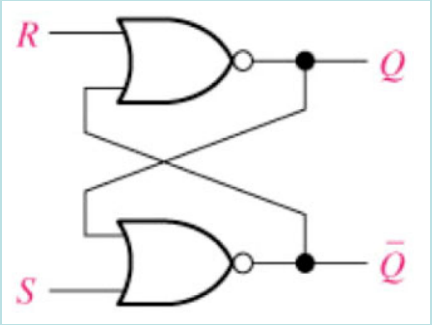
Circuit (b) Active-LOW input S'-R' latch :

- use NAND gate
- Input S' and R'
- Output Q and Q'



Active-HIGH

INPUTS		OUTPUTS		COMMENTS
S	R	Q	$\overline{Q}$	
0	0	NC	NC	No change. Latch remains in present state
0	1	0	1	Latch RESET
1	0	1	0	Latch SET
1	1	0	0	Invalid condition

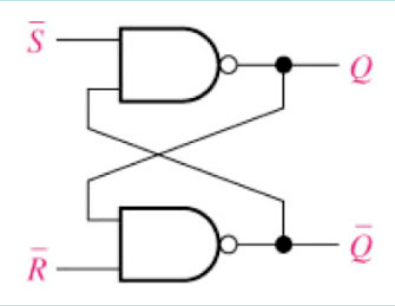


Explanation :

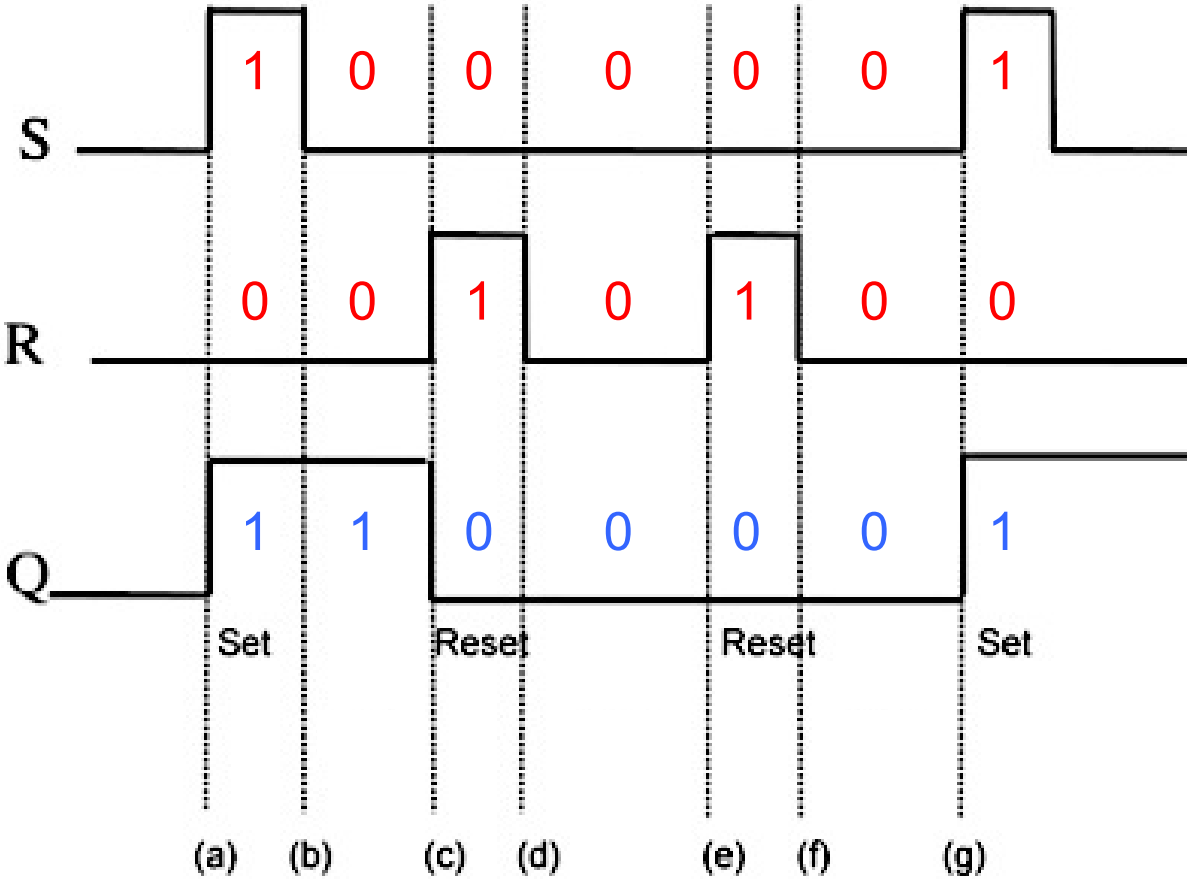
- The Q and Q-bar outputs are supposed to be in opposite states.
- Q=1 and Q-bar=0 is defined as *Set* (by making S=1 and R=0)
- Q=0 and Q-bar=1 is defined as *Reset* (by making S=0 and R=1)
- When S and R are both equal to 0, the latch's outputs *Not Change* in their prior states.
- If Q and Q-bar happen to be forced to the same state (both 0 or both 1), that state is referred to as *invalid*.

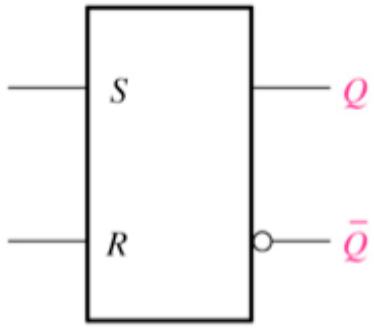
Active-LOW

INPUTS		OUTPUTS		COMMENTS
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	
0	0	1	1	Invalid condition
0	1	1	0	Latch SET
1	0	0	1	Latch RESET
1	1	NC	NC	No change. Latch remains in present state



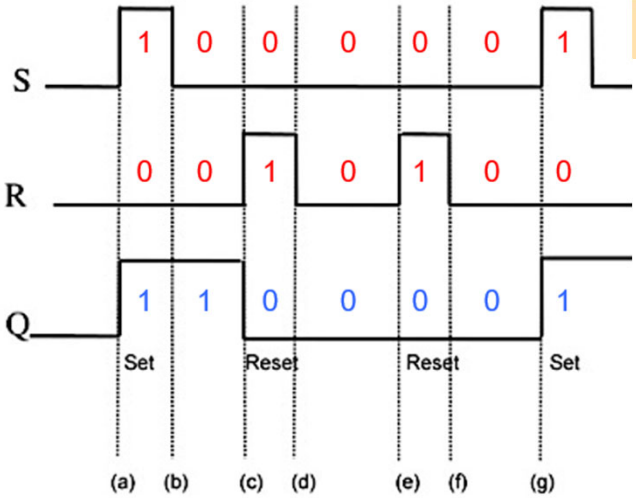
Example: S-R Latch (Active HIGH)

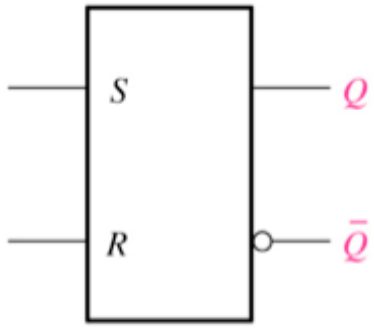




Logic symbol

continue...





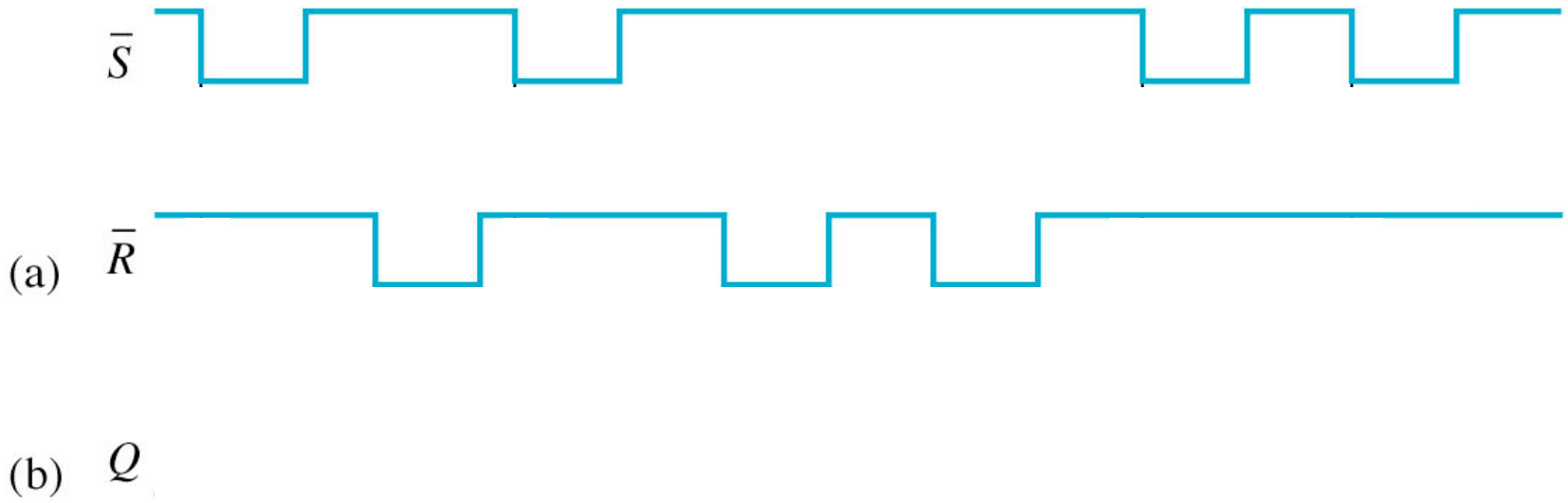
Logic symbol

Explanation:

Location	S	R	Q	State
(a)	1	0	1	SET
(b)	0	0	1	HOLD
(c)	0	1	0	RESET
(d)	0	0	0	HOLD
(e)	0	1	0	RESET
(f)	0	0	0	HOLD
(g)	1	0	1	SET

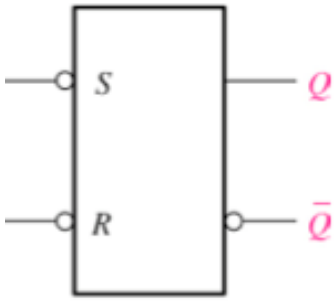
Extra

Exercise 7.1: If the $\overline{S}$ and $\overline{R}$ waveform in (a) are applied to the inputs of latch (active-LOW), determine the waveform that will be observed on the Q output in (b). Assume that Q is initially LOW.



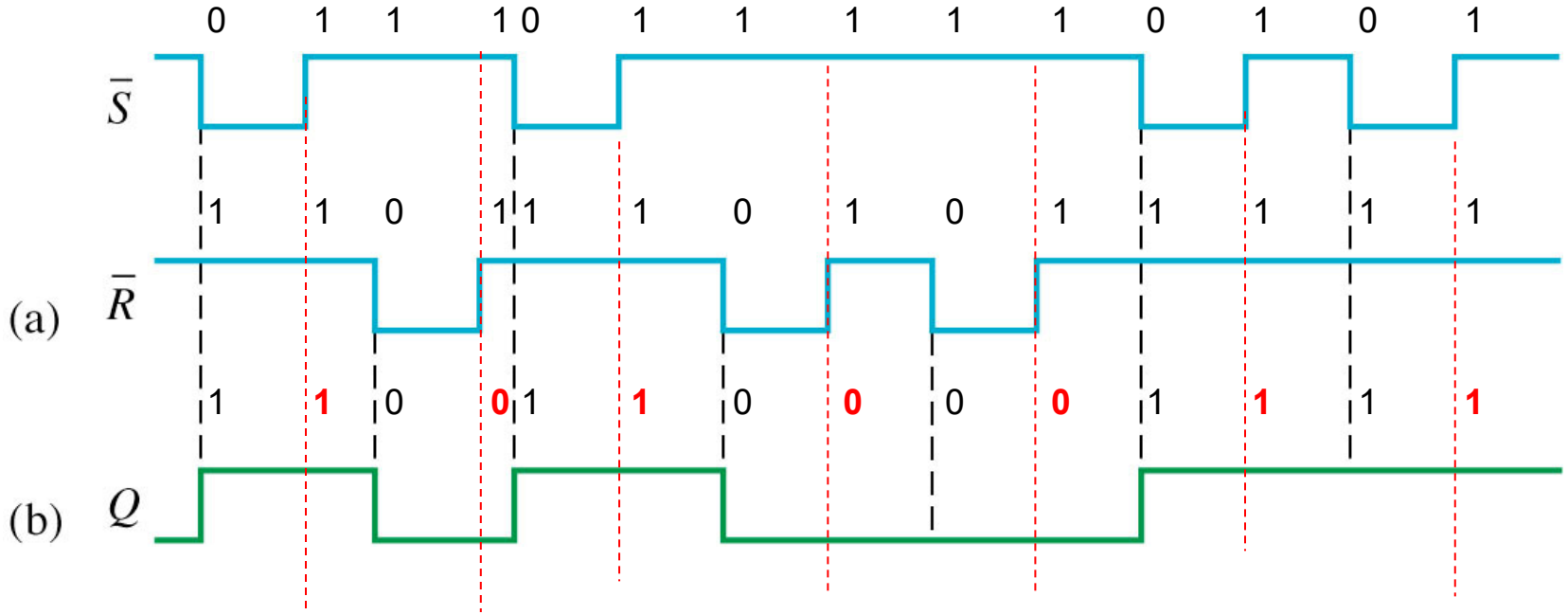
Active-LOW

INPUTS		OUTPUTS		COMMENTS
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	
0	0	1	1	Invalid condition
0	1	1	0	Latch SET
1	0	0	1	Latch RESET
1	1	NC	NC	No change. Latch remains in present state



Logic symbol

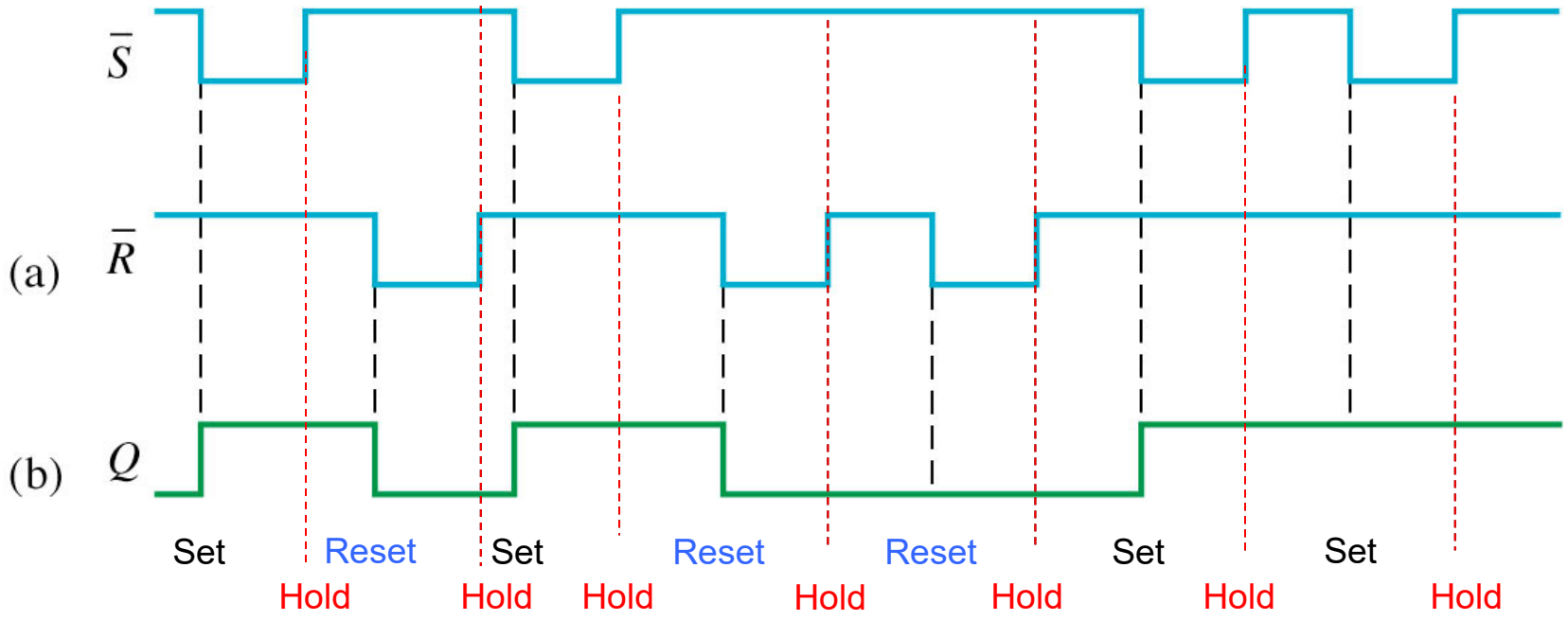
Solution: *(Red 0/1 is no change or hold)*



Extra

Self-Test:

Define when the states are *set, reset, hold* or *invalid* from the output waveform for each of the inputs.

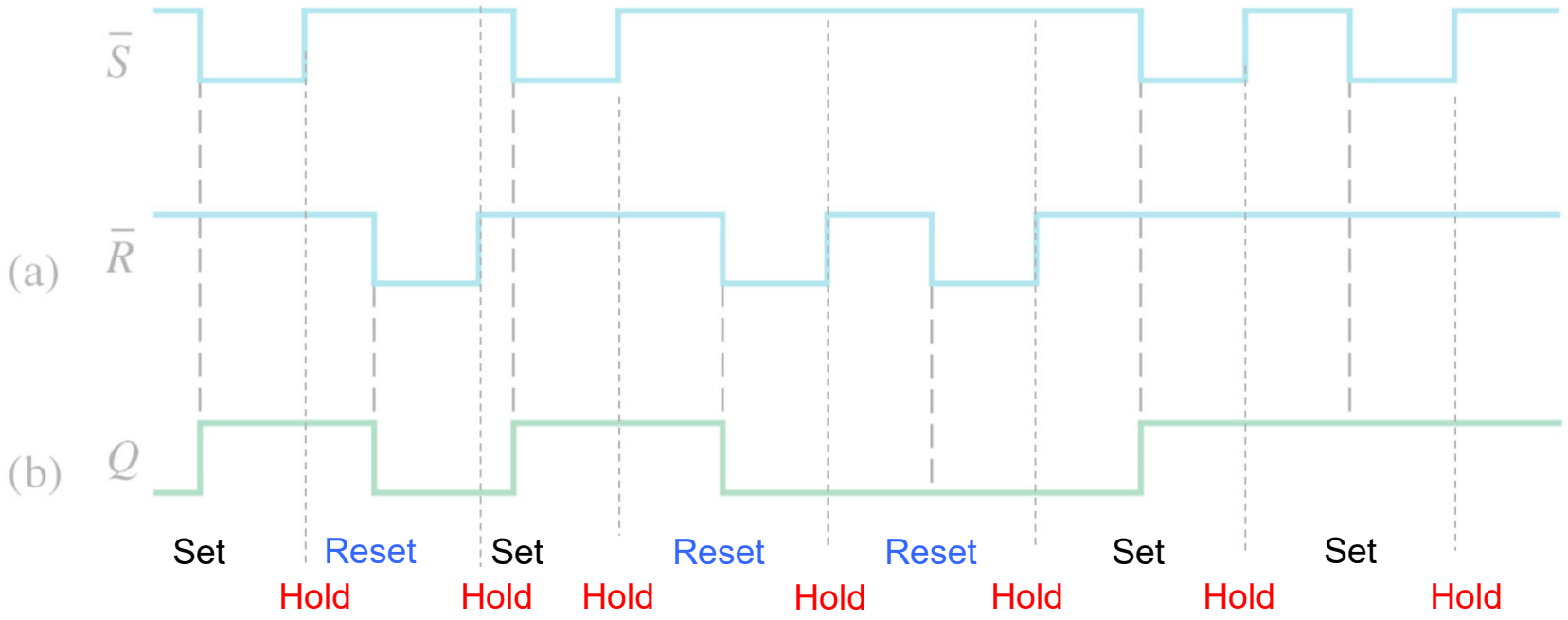


Extra

Self-Test:

Write the sequence of the states (*set, reset, hold* or *invalid*) for the output Q waveform for all inputs from the beginning.

Set → Hold → Reset → Hold → Set → Hold → Reset → Hold → Reset → Hold → Set → Hold → Set → Hold



(ii) Gated S-R Latch

- Is a SR Latch controlled by an enable input (**EN**) switch.
- The S and R inputs control the state to which the latch will function when a HIGH level is applied to the EN input.
- The latch will not change until EN is HIGH, and as long as it remains HIGH, the output is controlled by the state of the S and R input.

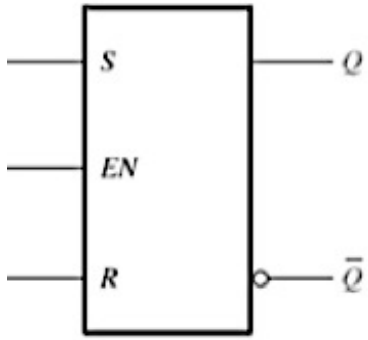
- The invalid state occurs when both S and R are simultaneously HIGH.

INFO :

EN = 1, Latch is On
EN = 0, Latch is Off

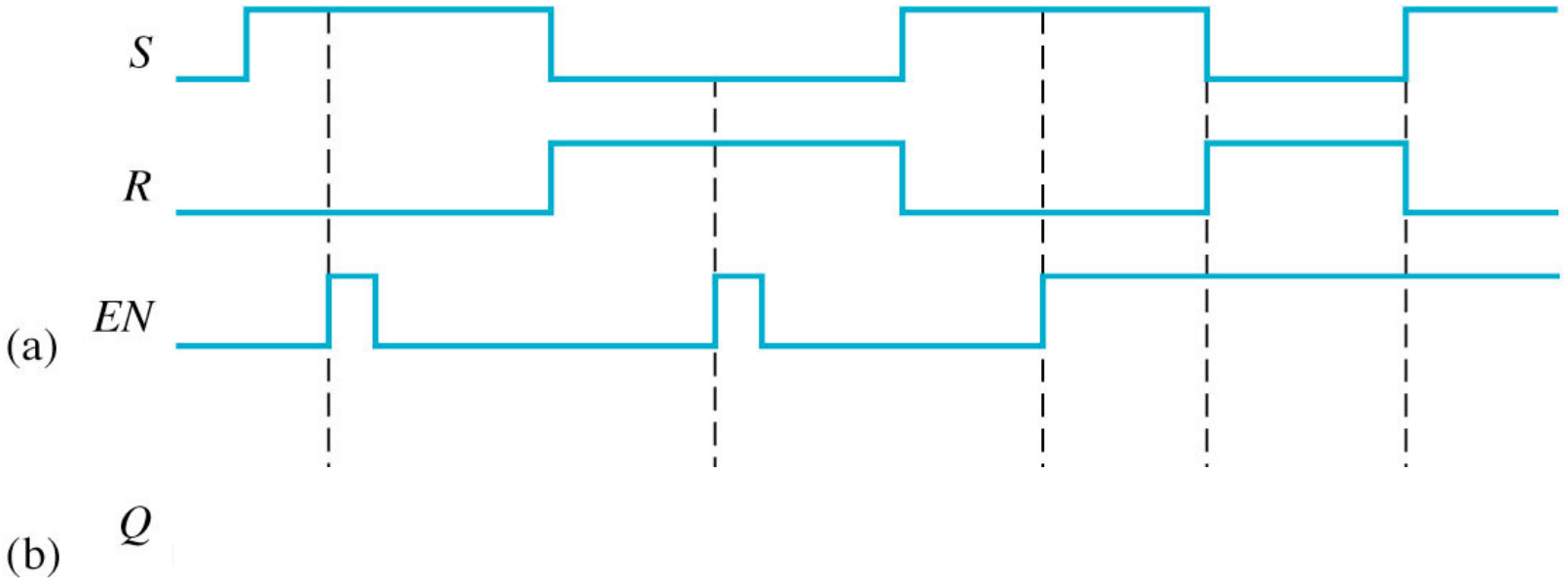
Gated S-R Latch: Truth Table

EN	S	R	Output, Q
0	0/1	0/1	No Change
1	0	0	No Change
1	0	1	Q=0 (Reset)
1	1	0	Q=1 (Set)
1	1	1	Invalid

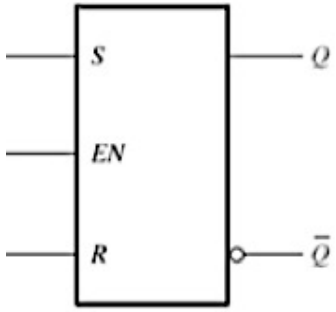


Logic symbol

Example: Gated S-R Latch.
Find the waveform for Q.
Assume that Q is initially LOW.

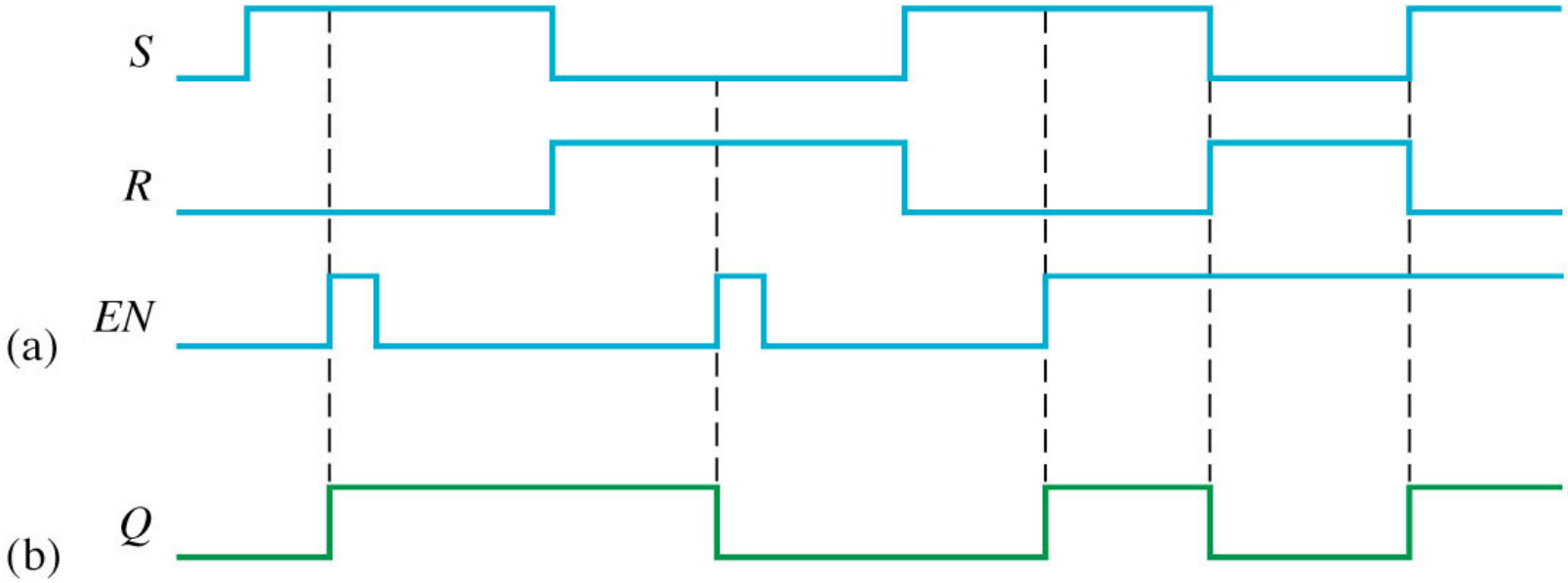


INPUTS		OUTPUTS	
S	R	Q	$\overline{Q}$
0	0	NC	NC
0	1	0	1
1	0	1	0
1	1	0	0



Logic symbol

Solution: Assume that Q is initially LOW.



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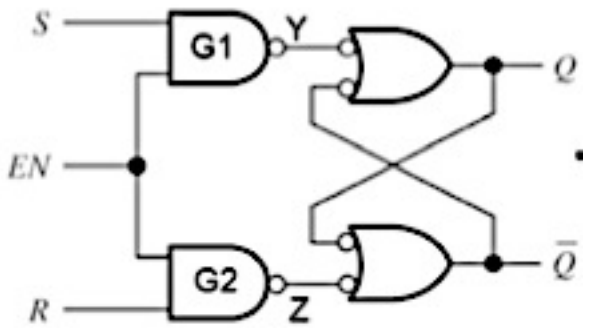
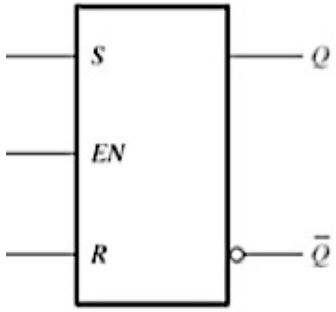
Exercise 7.2:



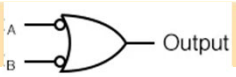


Referring to logic diagram above, fill in the table. Assume initially Q = 0 and Q' = 1

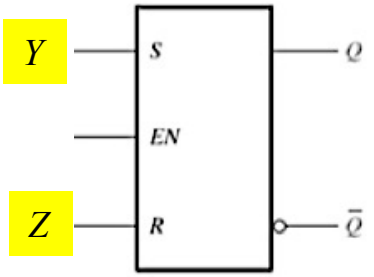
			$\overline{S \cdot EN}$	$\overline{R \cdot EN}$	
EN	S	R	Y	Z	Q
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

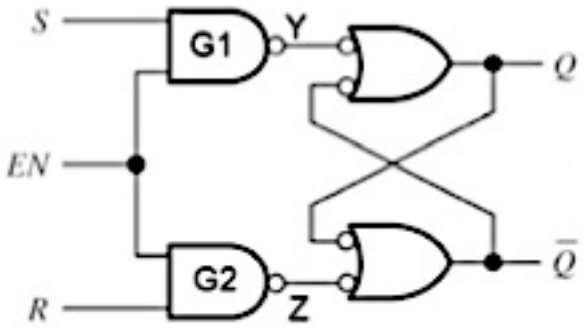
Active-LOW

INPUTS		OUTPUTS		COMMENTS
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	
0	0	1	1	Invalid condition
0	1	1	0	Latch SET
1	0	0	1	Latch RESET
1	1	NC	NC	No change. Latch remains in present state



A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0





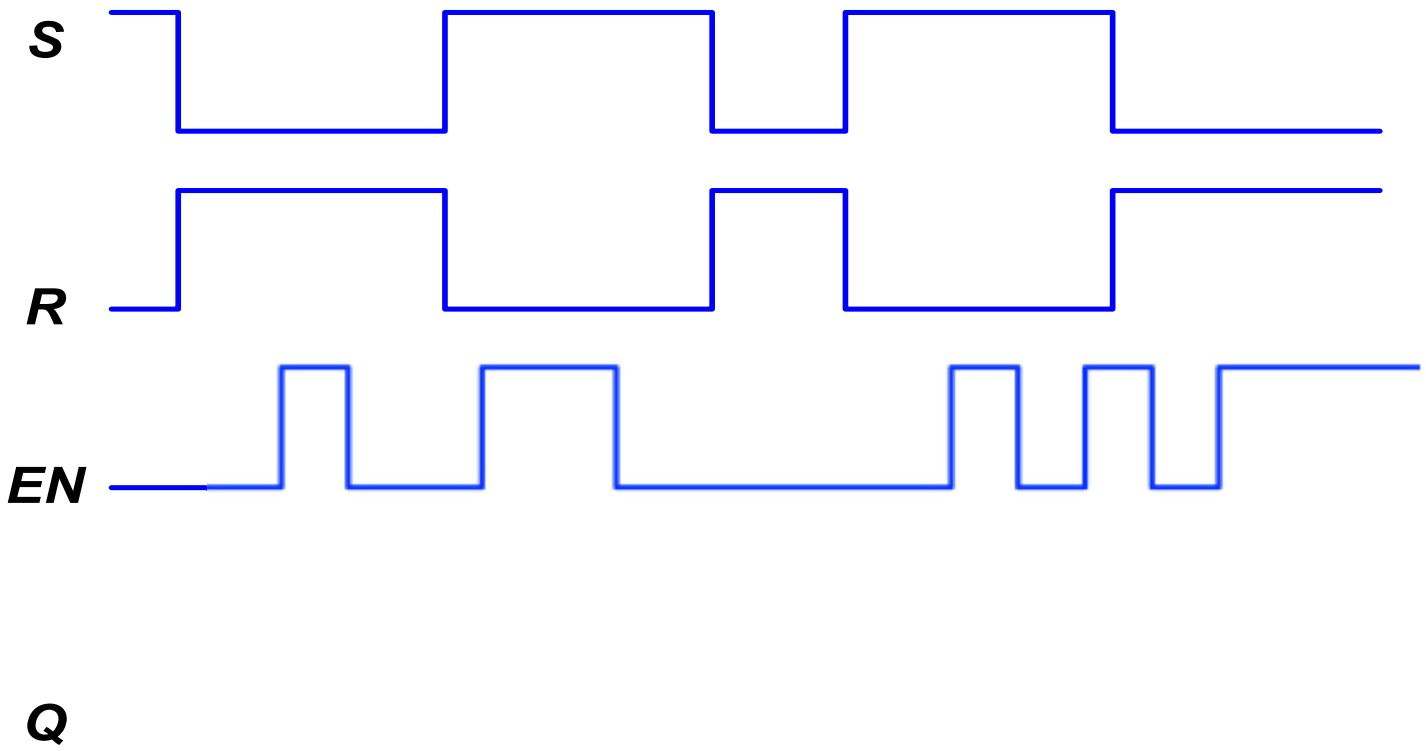
Solution:

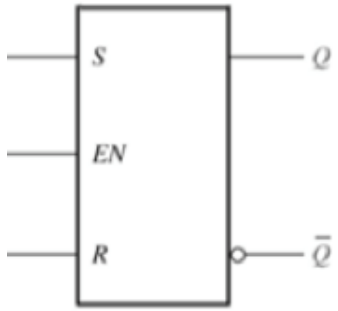
Referring to logic diagram above, fill in the table. Assume initially Q = 0 and Q' = 1

Q → Run as '*Active Low S-R*' latch when EN = 1

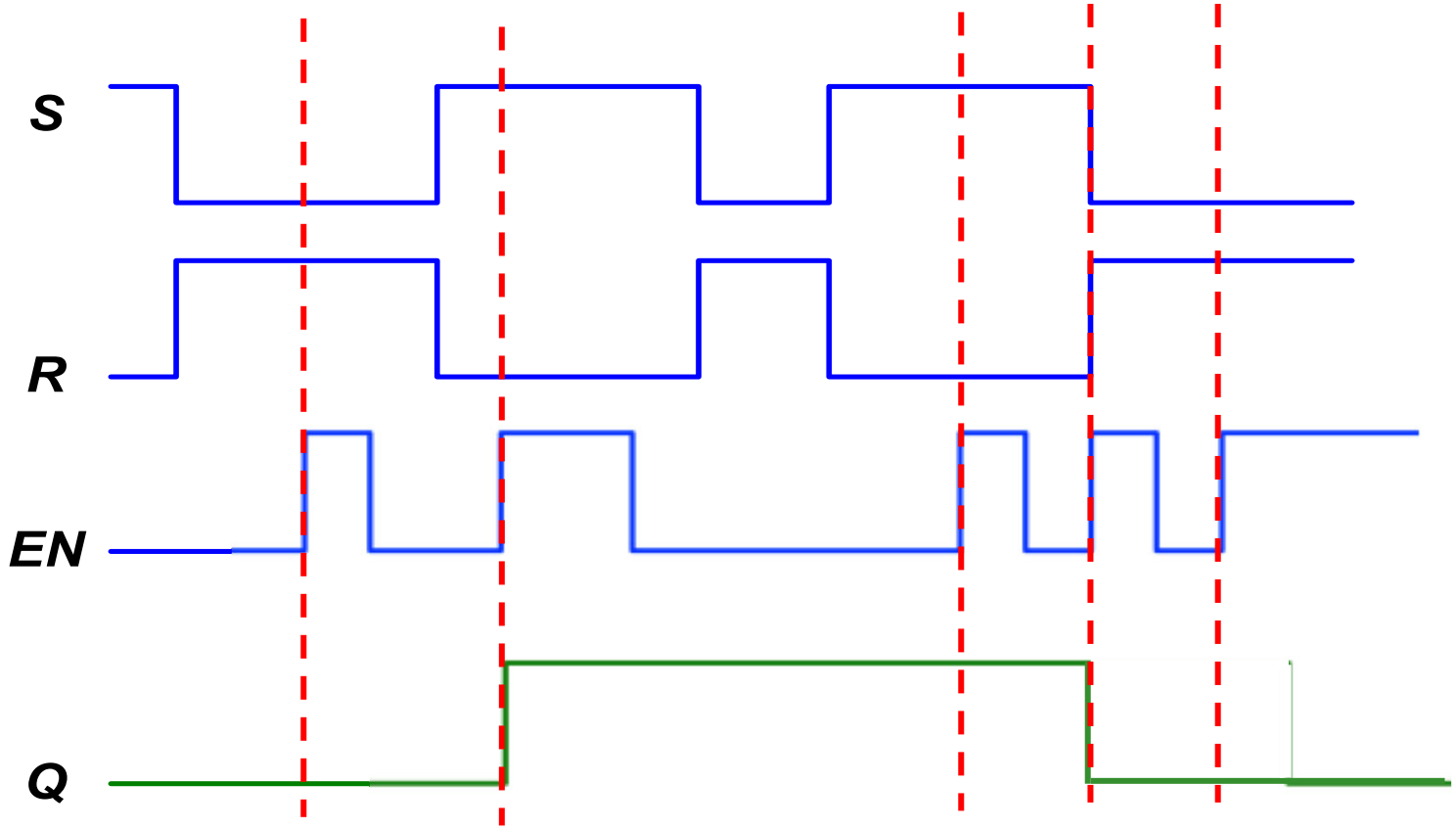
EN	S	R	$\overline{S \cdot EN}$ Y	$\overline{R \cdot EN}$ Z	Q	STATE	
0	0	0	1	1	0	*Hold*	
0	0	1	1	1	0	*Hold*	*EN=0*
0	1	0	1	1	0	*Hold*	
0	1	1	1	1	0	*Hold*	
1	0	0	1	1	0	*Hold*	
1	0	1	1	0	1	*Set*	*EN=1*
1	1	0	0	1	0	*Reset*	
1	1	1	0	0	-	*Invalid*	

Example: Gated S-R Latch.
Find the waveform for Q.
Assume that Q is initially LOW.





Solution: Assume that Q is initially LOW.



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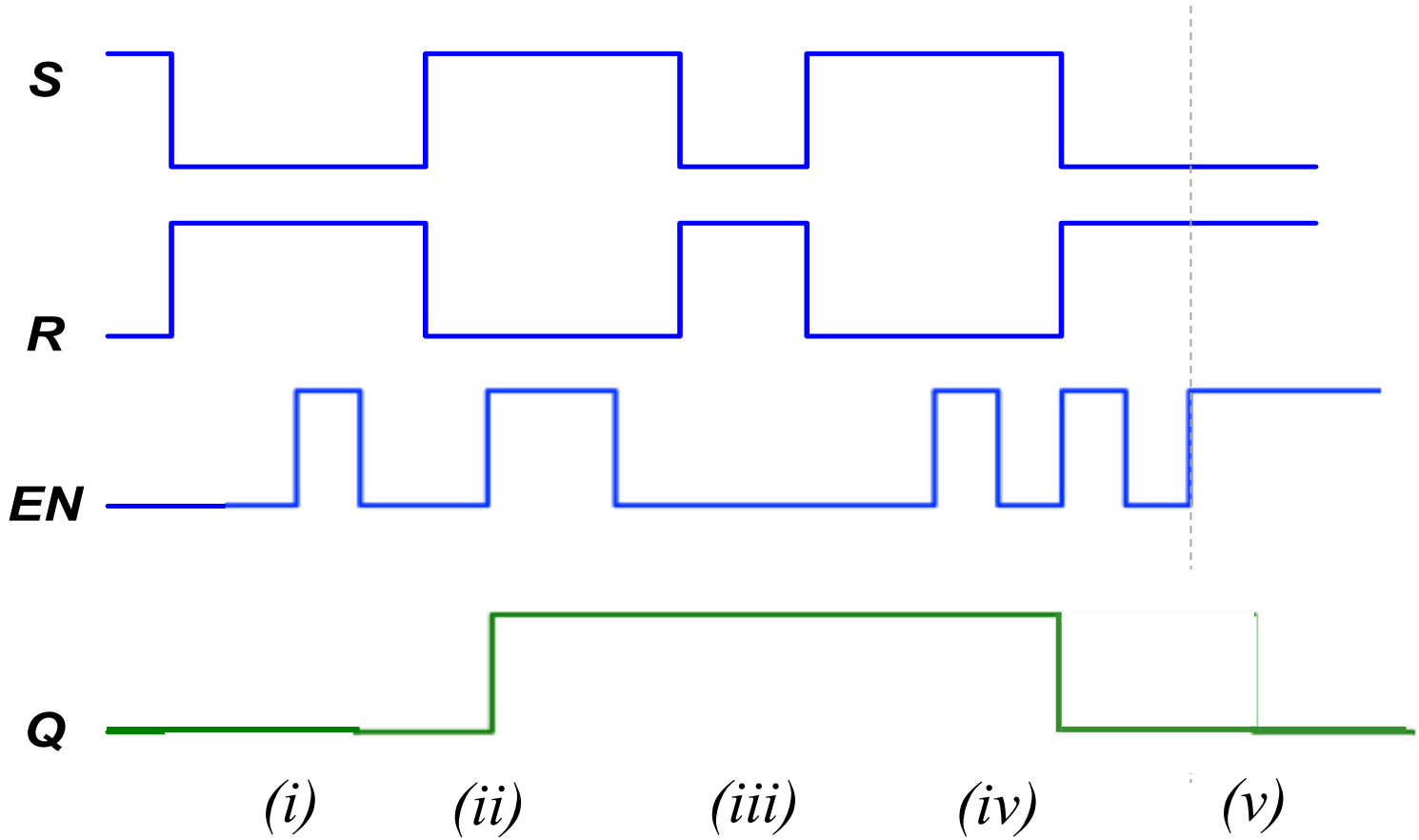
Self-Test:

Define the states (*set, reset, hold* or *invalid*) for all outputs waveform Q that label as i, ii, iii, iv and v.



Solution:

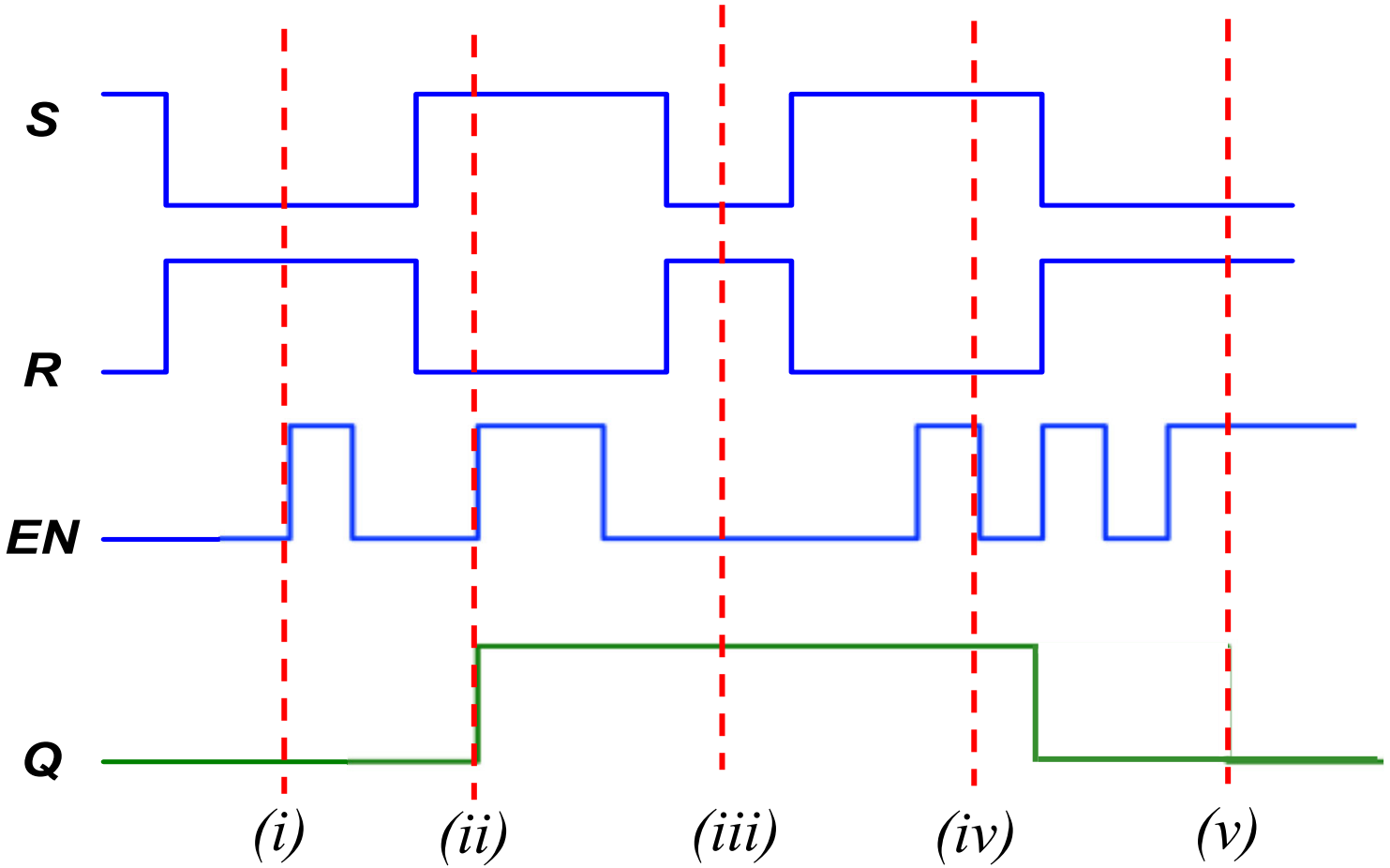
(i) Reset

(ii) Set

(iii) Hold / No change

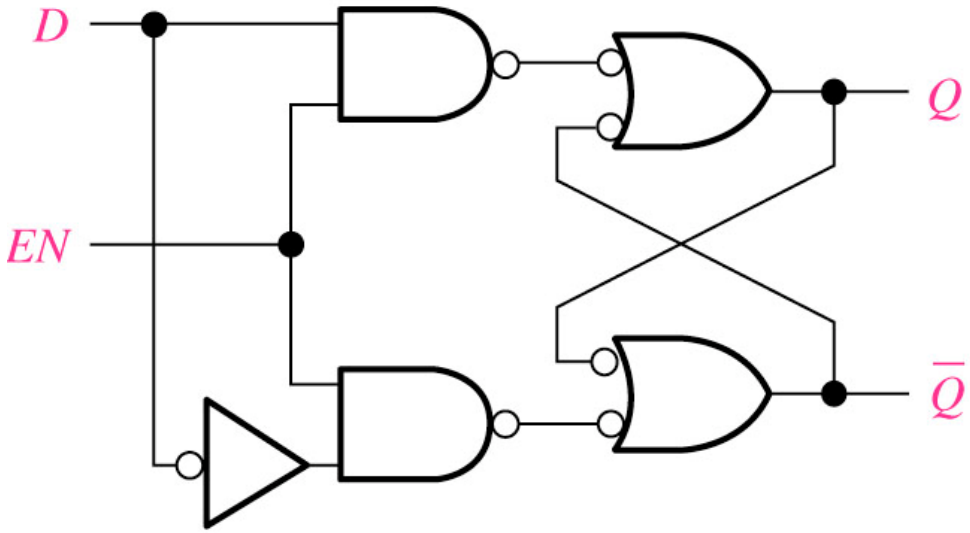
(iv) Hold / No change

(v) Reset

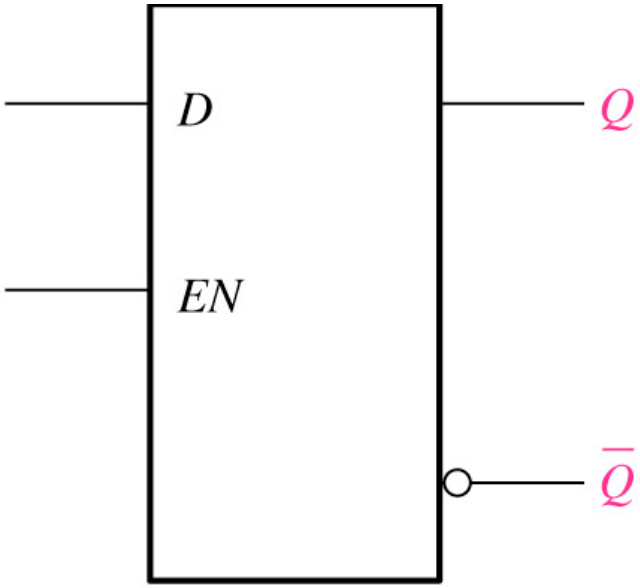


(iii) Gated D Latch:

Logic diagram & logic symbol

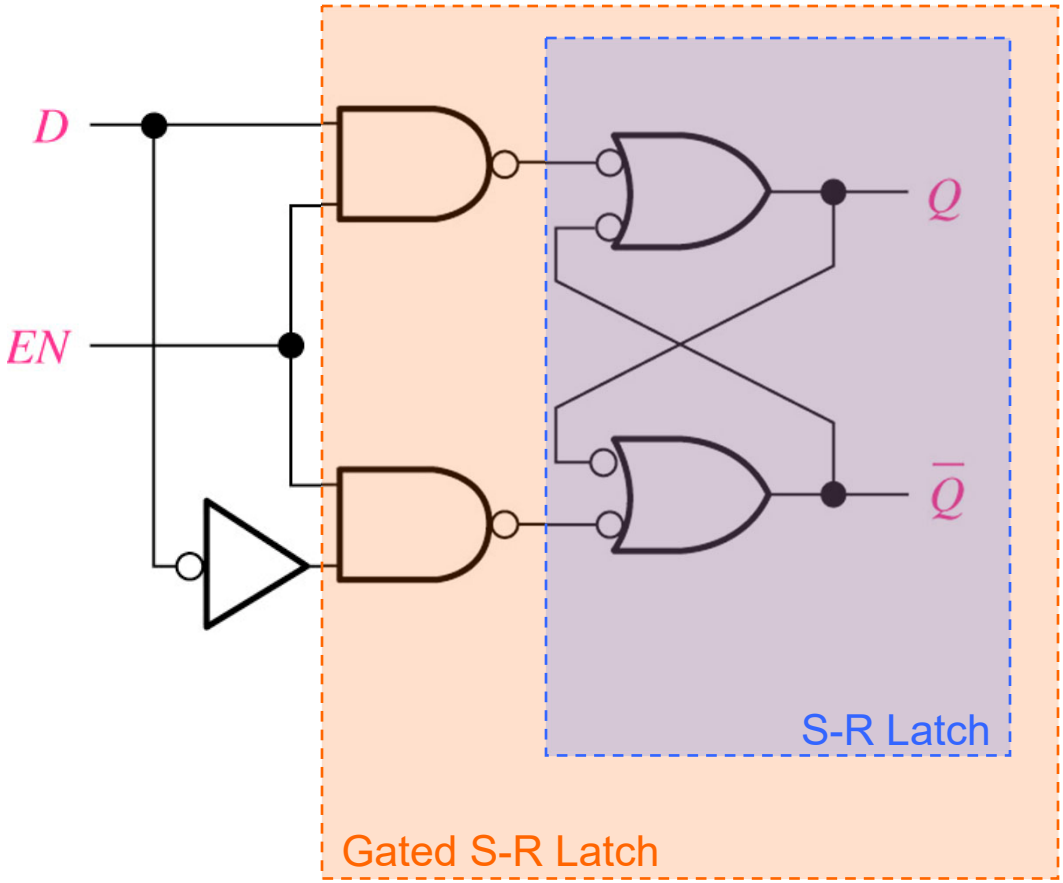


(a) Logic diagram

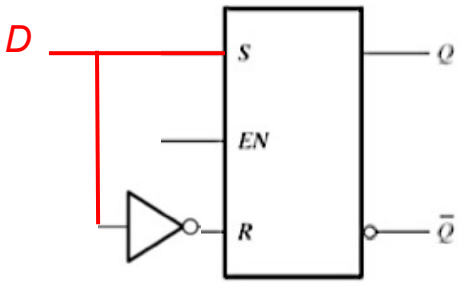


(b) Logic symbol

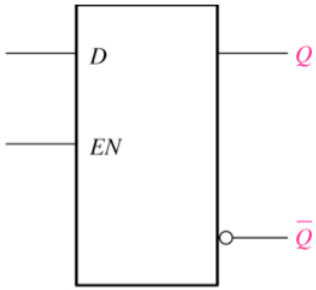
Gated D Latch



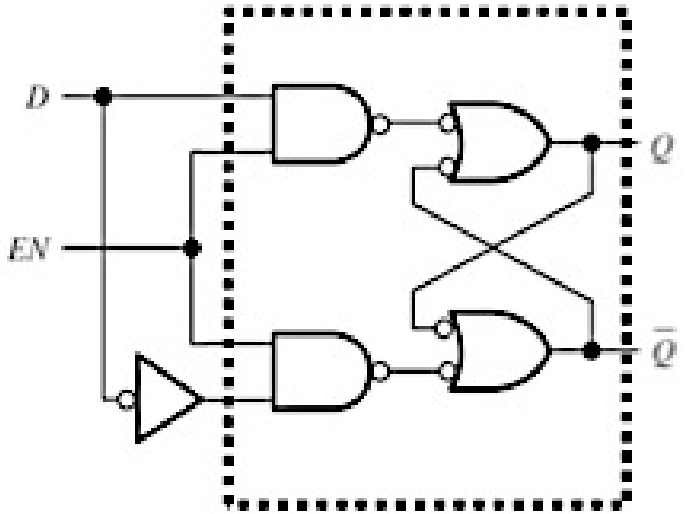
Modified Gated S-R Latch

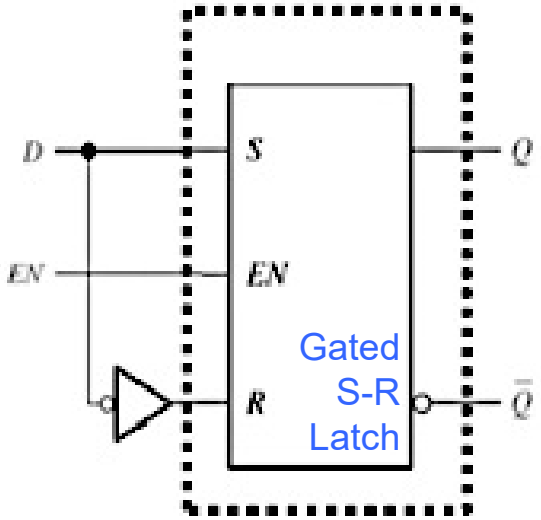


Gated D Latch



Gated D Latch:





The purpose of the inverter is to make sure that R is the complement of S and R will never be the same as S. So that, we have only two condition at the input of SR.

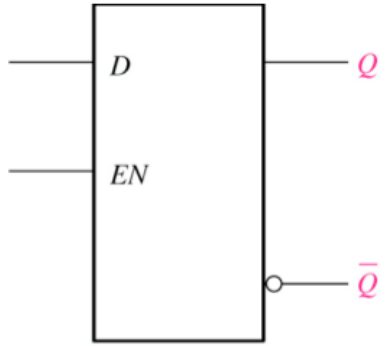
Condition 1: D = 0, therefore S = 0, R = 1 which make Q = 0
Condition 2: D = 1, therefore S = 1, R = 0 which make Q = 1

Just like gated SR, when EN=0, the output does not change. BUT, if EN=1, the output will depend on the value of input D.

So, we can conclude that Q=D when EN=1.

EN=1 → Q=D

Gated D Latch: Truth Table



EN	D	Output, **Q**
0	0	No Change
0	1	No Change
1	0	Q = 0
1	1	Q = 1

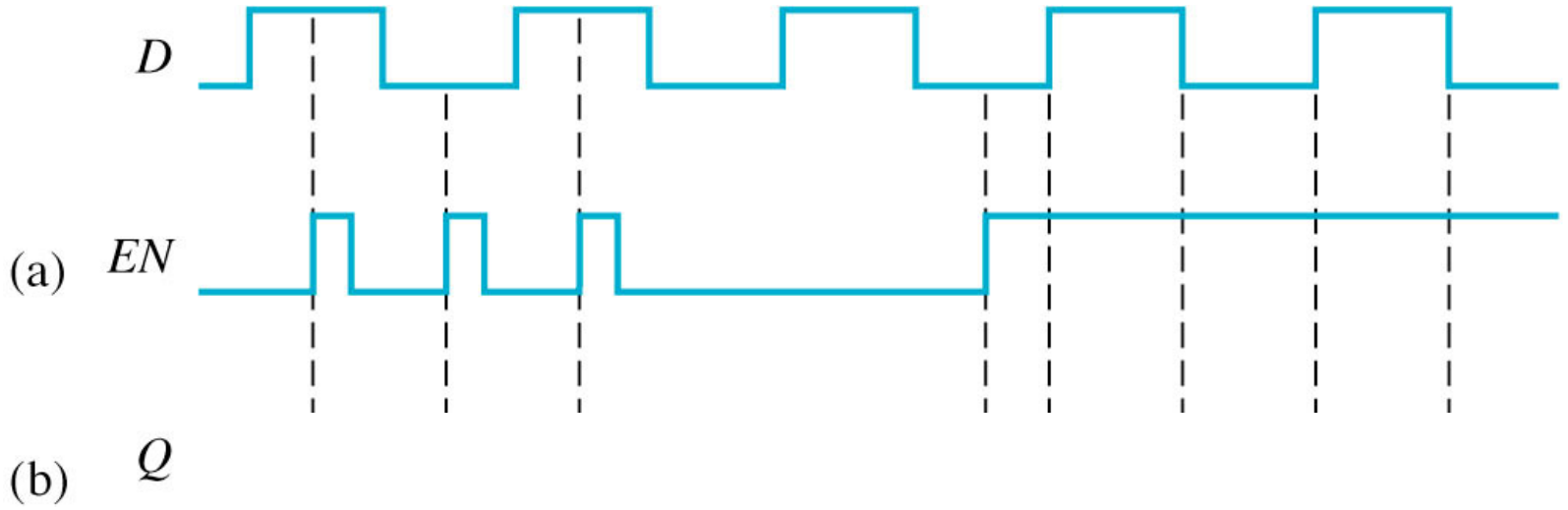
EN = 1, Latch is On
EN = 0, Latch is Off

EN = 1 → Q = D

Example: Gated D Latch.

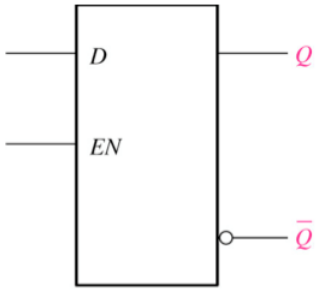
Find the waveform for Q.

Assume that Q is initially LOW.

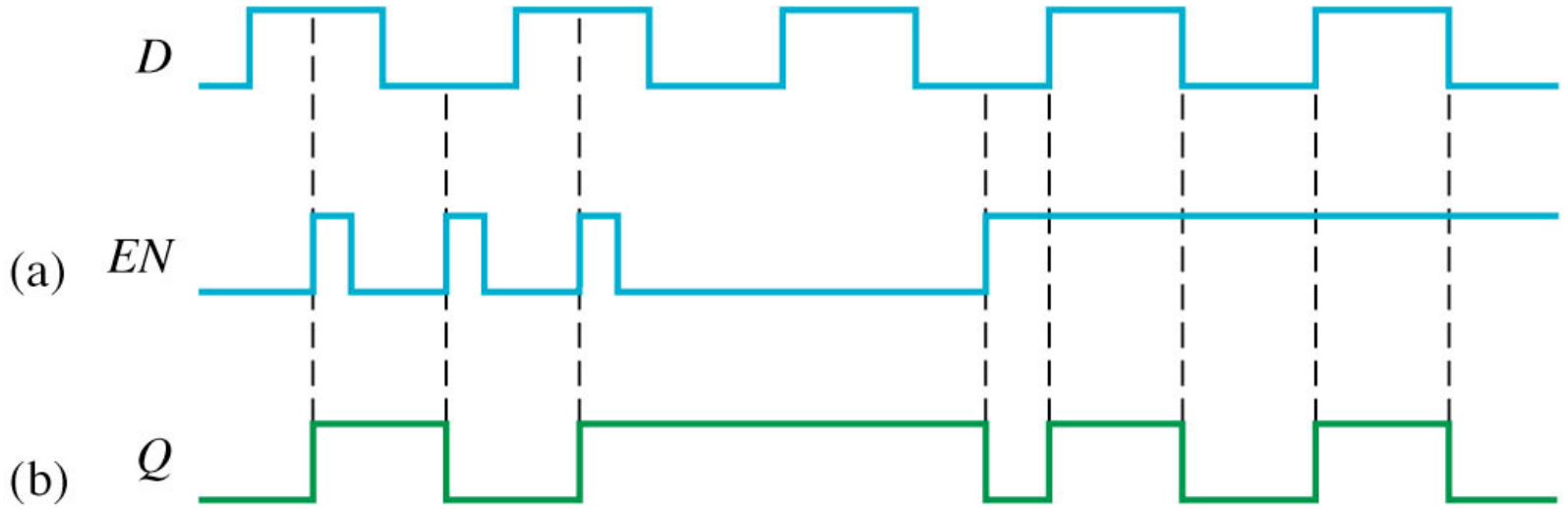


Solution:

EN	D	Output
0	0	No Change
0	1	No Change
1	0	Q = 0
1	1	Q = 1



Logic symbol



Flip-Flops

Flip-Flop

- Flip-flops (FF) are synchronous bi-stable storage devices capable of storing one bit, where the output state only changes at a specified point on a triggering input called the Clock (C).

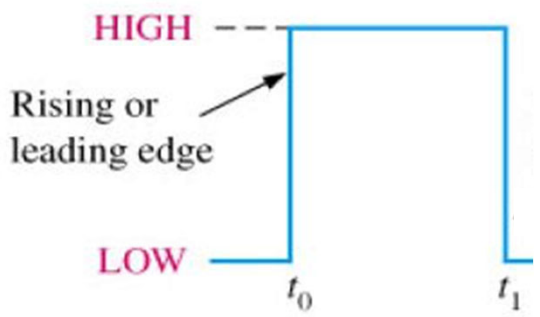
- FFs are edge-triggered, means that the output changes are synchronized with the Clock signal. This may either be
  - a LOW-to-HIGH (rising edge) transition or
  - a HIGH-to-LOW (falling edge) transition

- Type of Flip-Flops:
  - i) S-R
  - ii) D
  - iii) J-K
  - iv) T

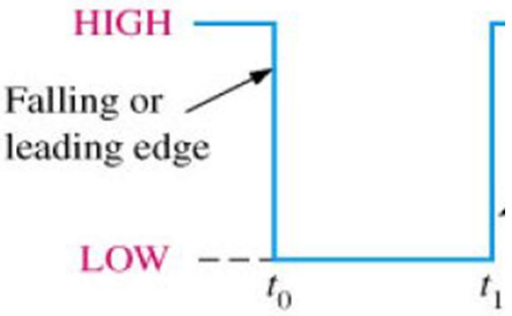
Edge-Triggered FF

KEY TERMS :
Rising edge = positive edge
Falling edge = negative edge

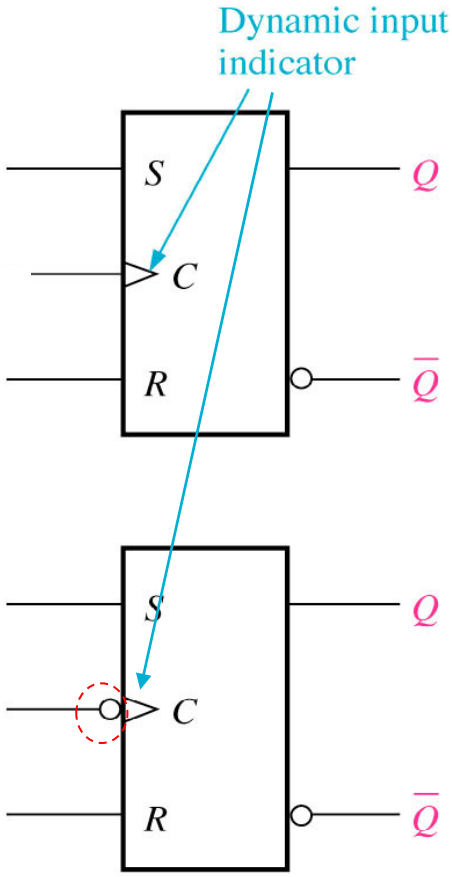
Flip-flop is an important device in a sequential circuit



(a) Positive–going pulse



(b) Negative–going pulse



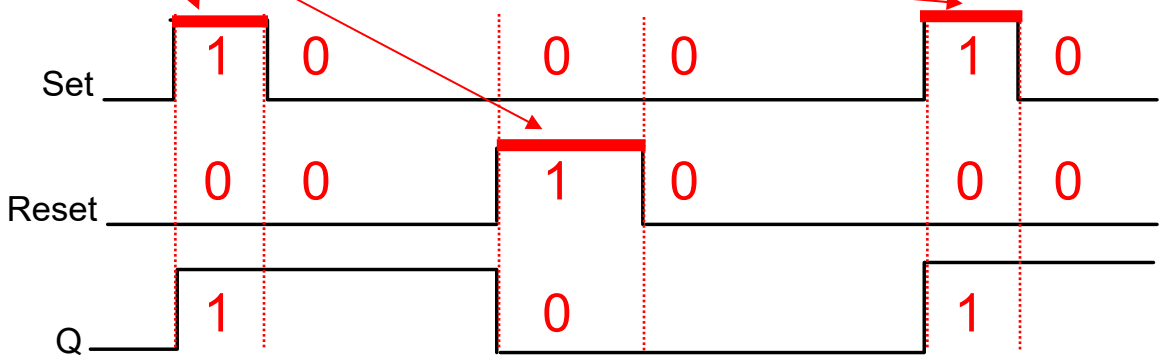
Edge-Triggered FF logic symbol

Difference:

Latch vs Flip-Flop

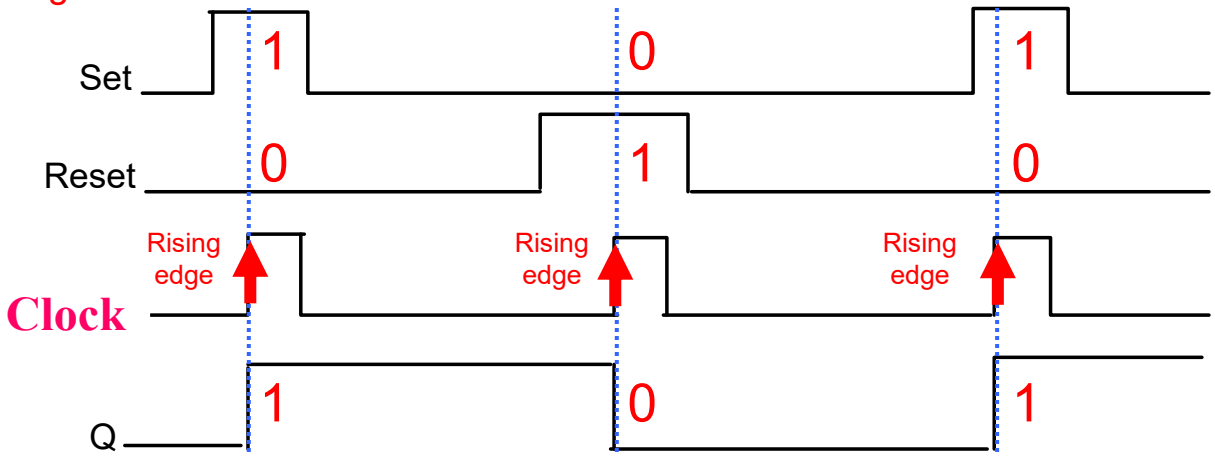
activated by level-triggered, i.e., HIGH or LOW voltages from the input signals

Latch



activated by edge-triggered, i.e., voltage transitions from HIGH to LOW or LOW to HIGH at the clock signals

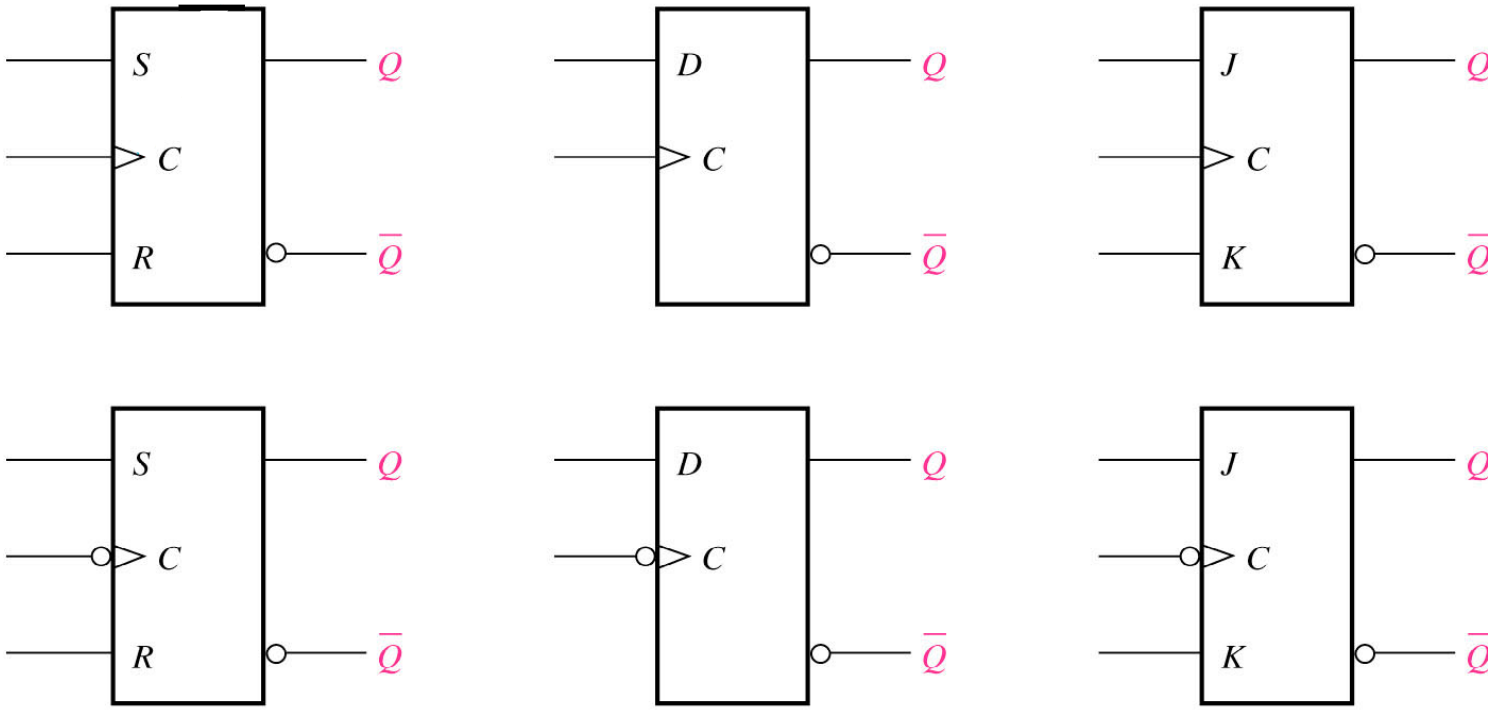
Flip-flop



Type of Flip-Flops

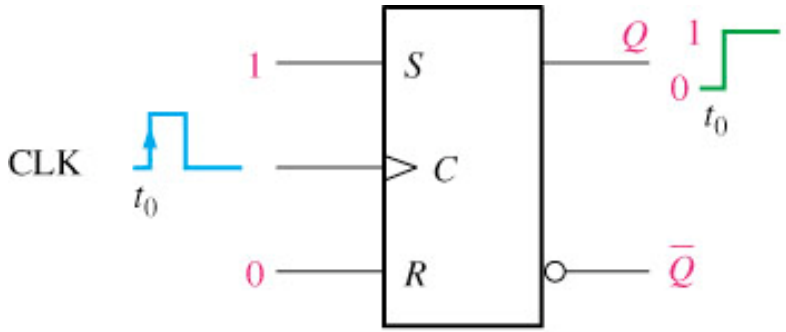
(Positive edge-triggered)

(Negative edge-triggered)

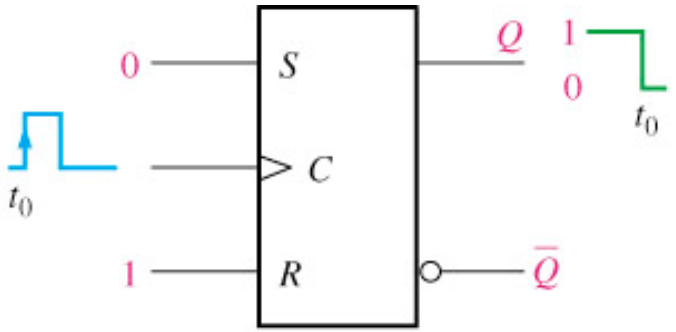


(a) S-R (b) D (c) J-K

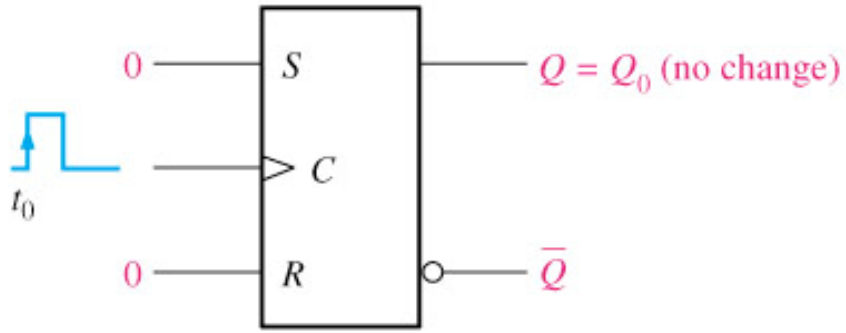
(i) S-R Flip-Flop



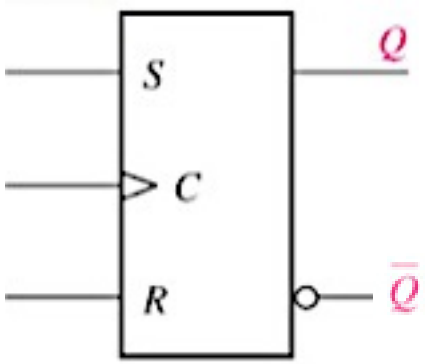
(a) $S = 1, R = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $S = 0, R = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



(c) $S = 0, R = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

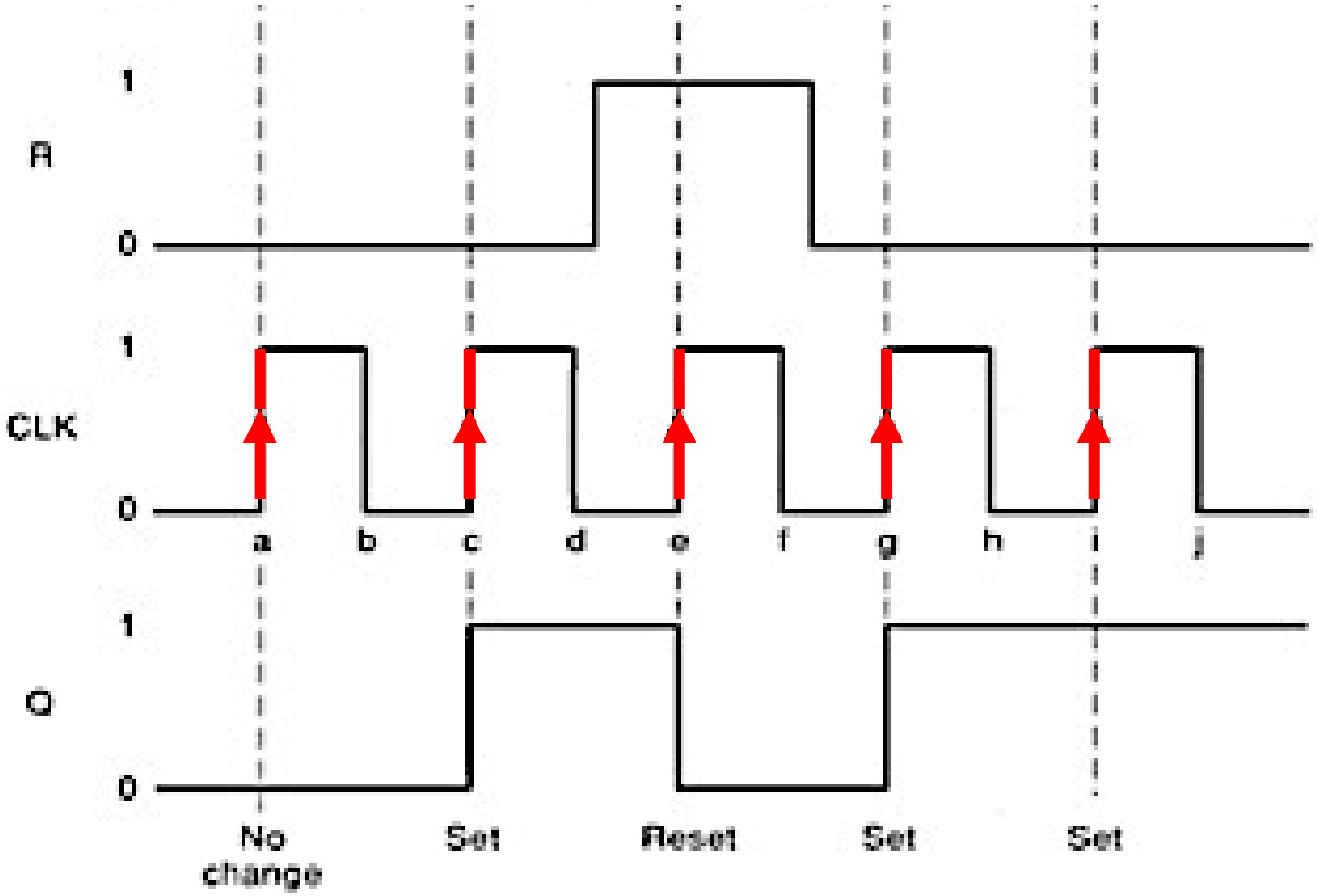


S	R	CLK	Output		Comments
			Q	$\overline{Q}$	
0	0	↑	Q_0	$\overline{Q}_0$	No Change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid

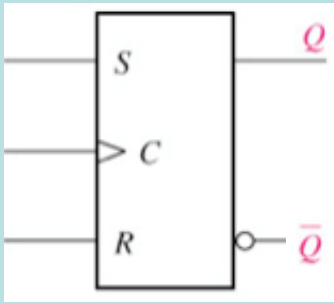
TRUTH TABLE

↑ = clock transition LOW to HIGH

Q_0= output level prior to clock transition



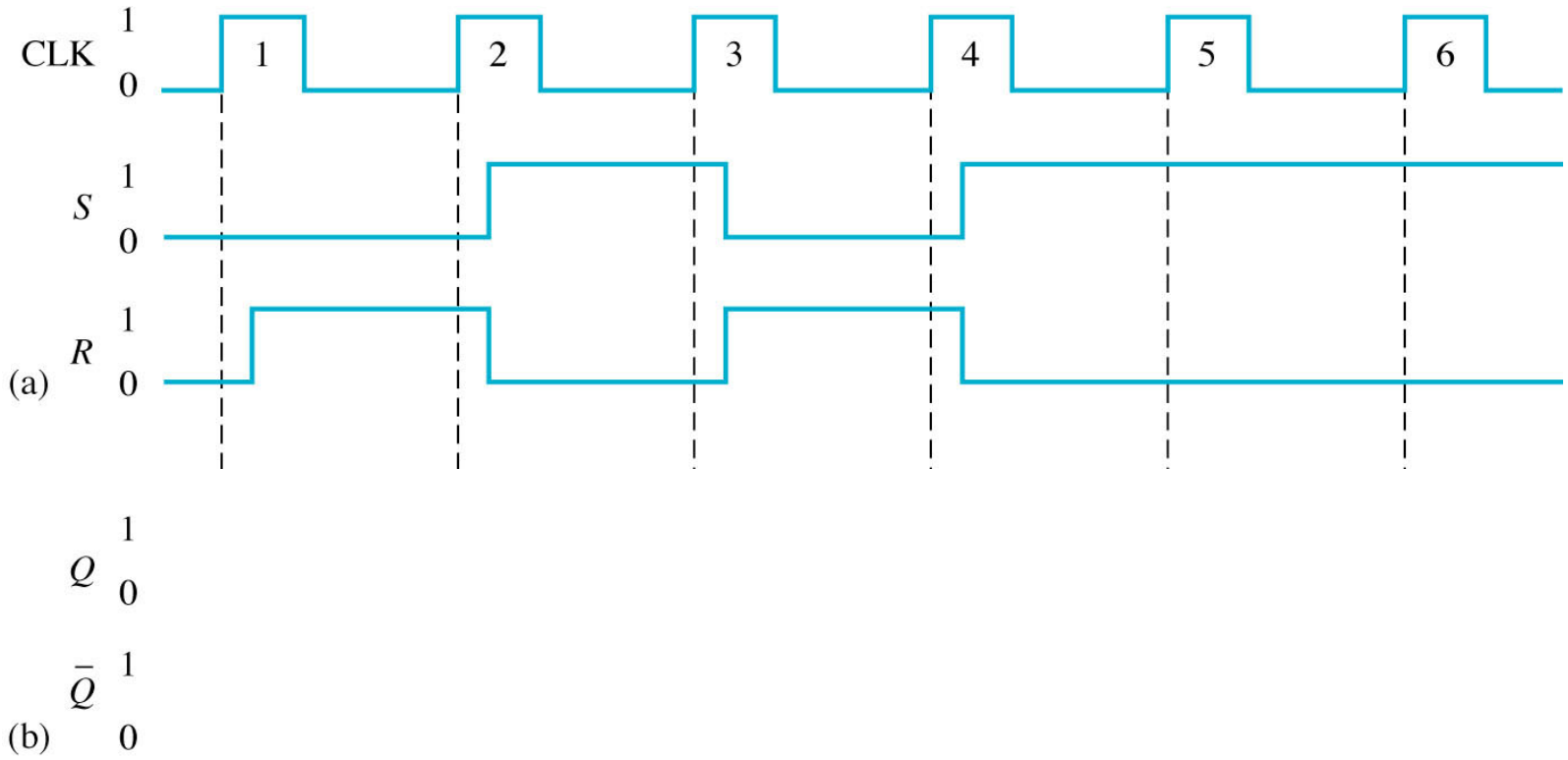
Positive edge-triggered



Example: S-R Flip-Flop.

Find the waveform for Q and $\overline{Q}$.

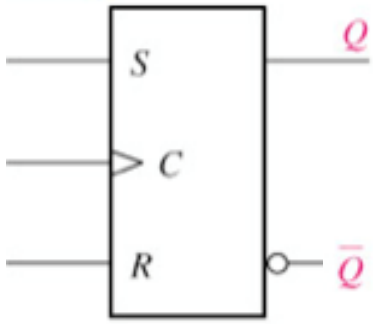
Assume that the positive edge-triggered flip-flop is initially RESET.



S-R Flip-Flop.

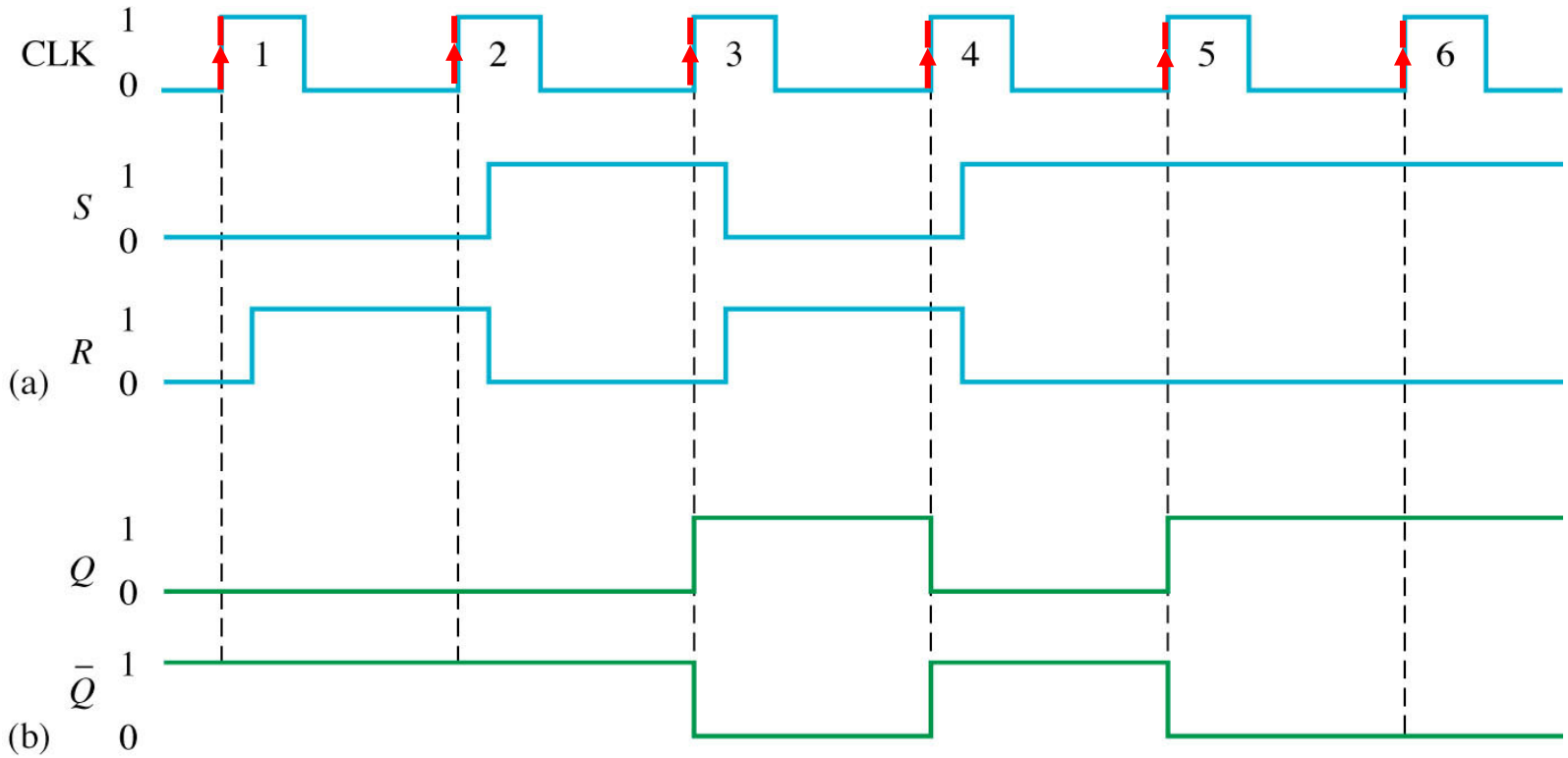
Find the waveform for Q and Q bar.

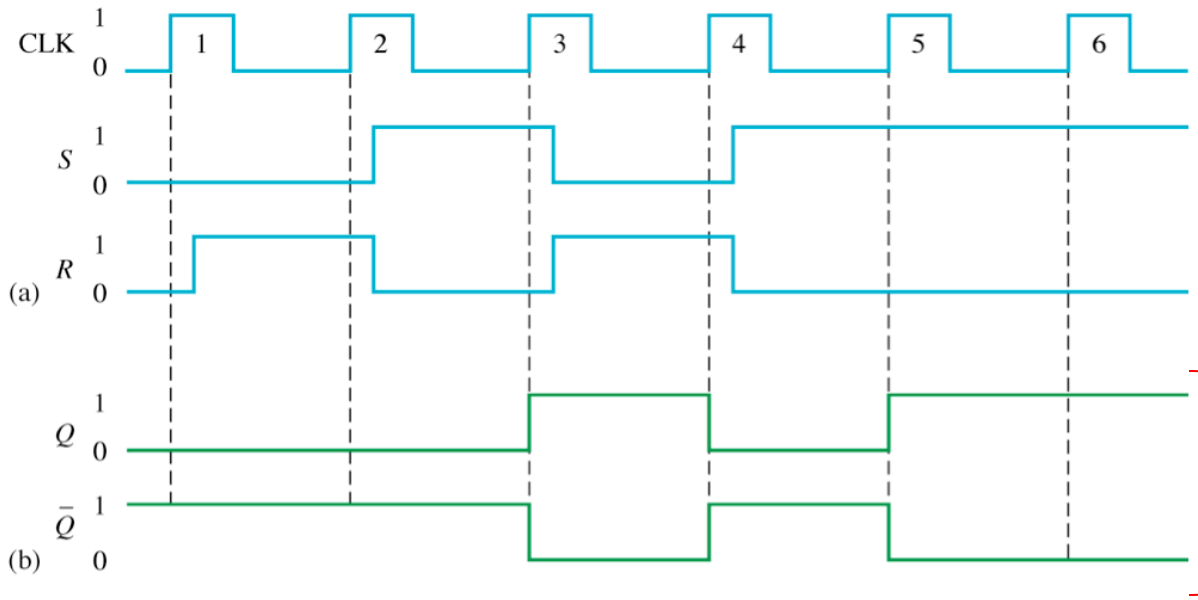
Assume that the positive edge-triggered , flip-flop is initially RESET.



Logic symbol

Solution:



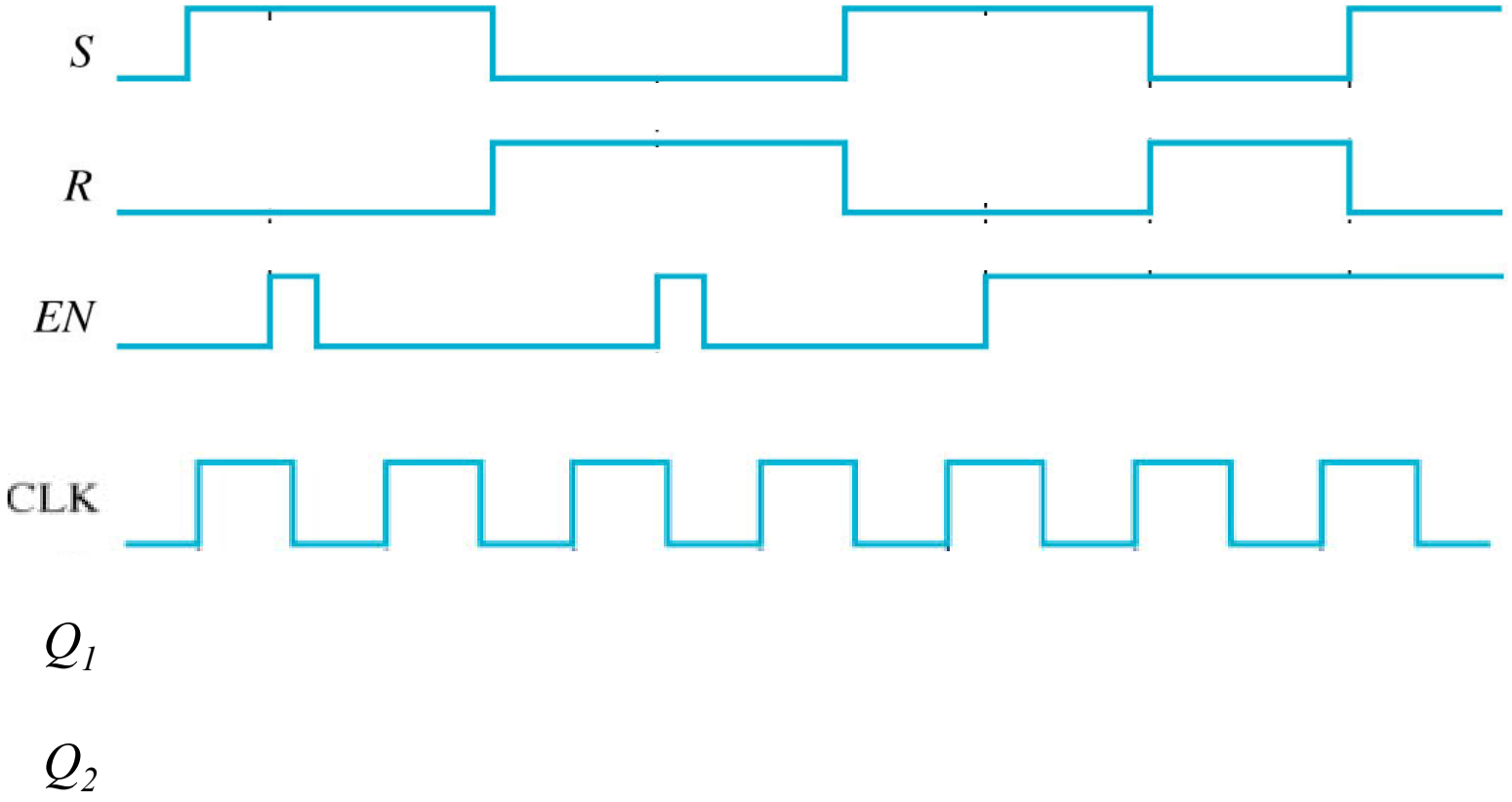


Once Q is determined, $\bar{Q}$ is easily found since it is simply the complement of Q.

Clock Pulse	S	R	Q
1	0	0	Does not change
2	0	1	LOW (RESET)
3	1	0	HIGH (SET)
4	0	1	LOW (RESET)
5	1	0	HIGH (SET)
6	1	0	Stay HIGH

Exercise 7.3:

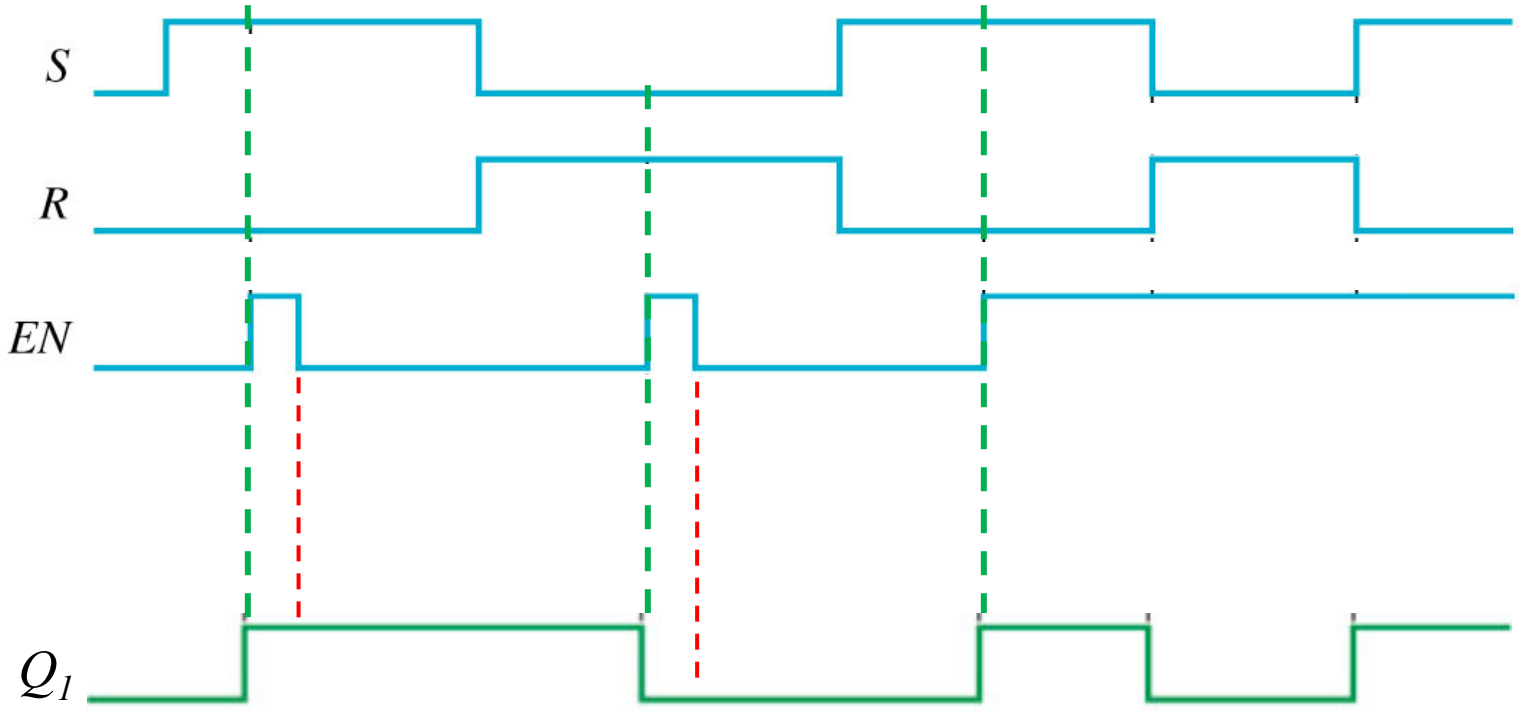
Given the inputs S and R for Gated S-R Latch with the output Q_1, and for flip-flop with output Q_2. Find the waveforms for Q_1 and Q_2. Assume that both outputs are initially LOW and the flip-flop activated at positive edge-triggered.



Solution 7.3:

Gated S-R Latch with the output Q_1

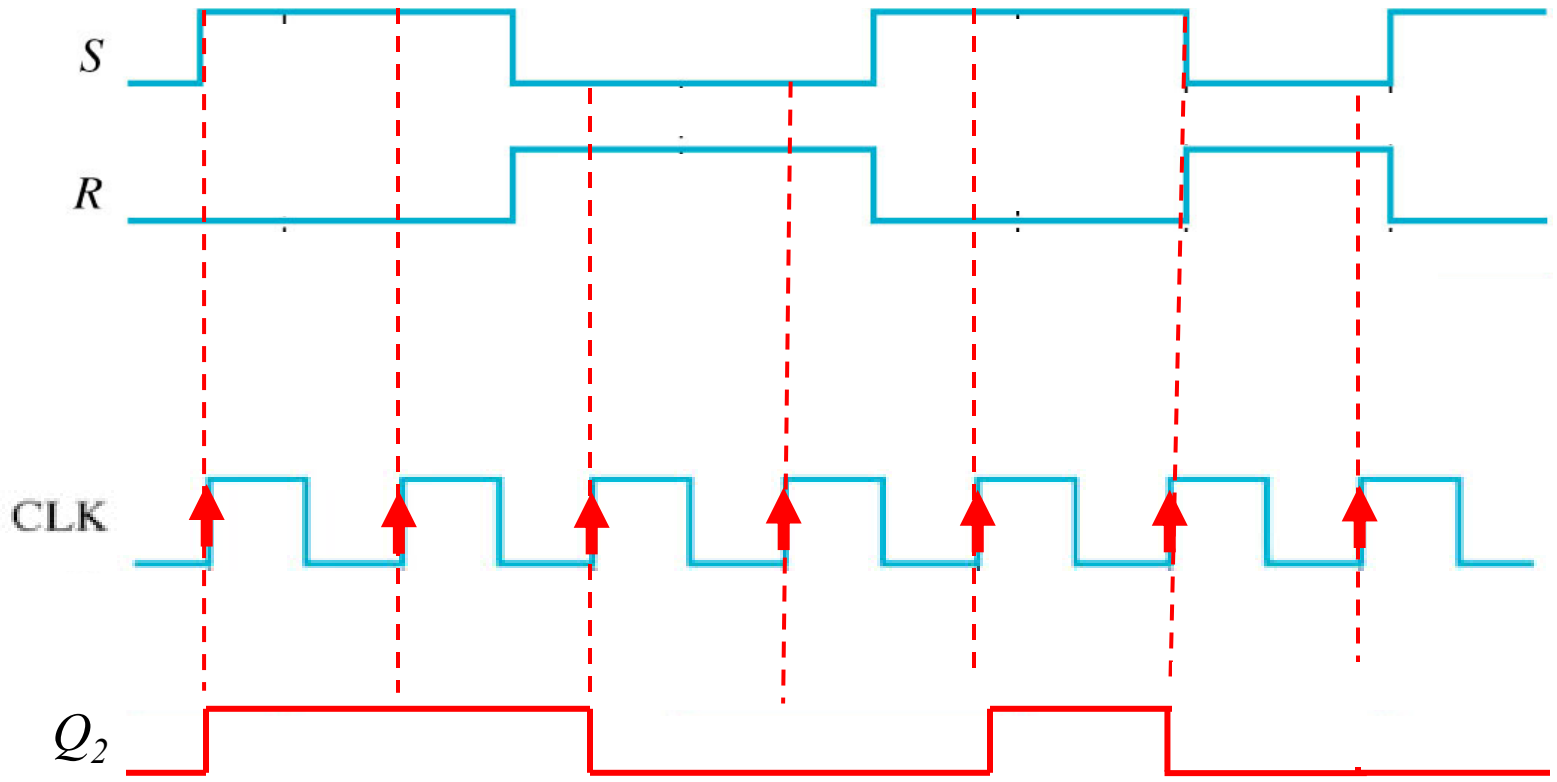
-> waveforms for Q_1 :



Solution 7.3:

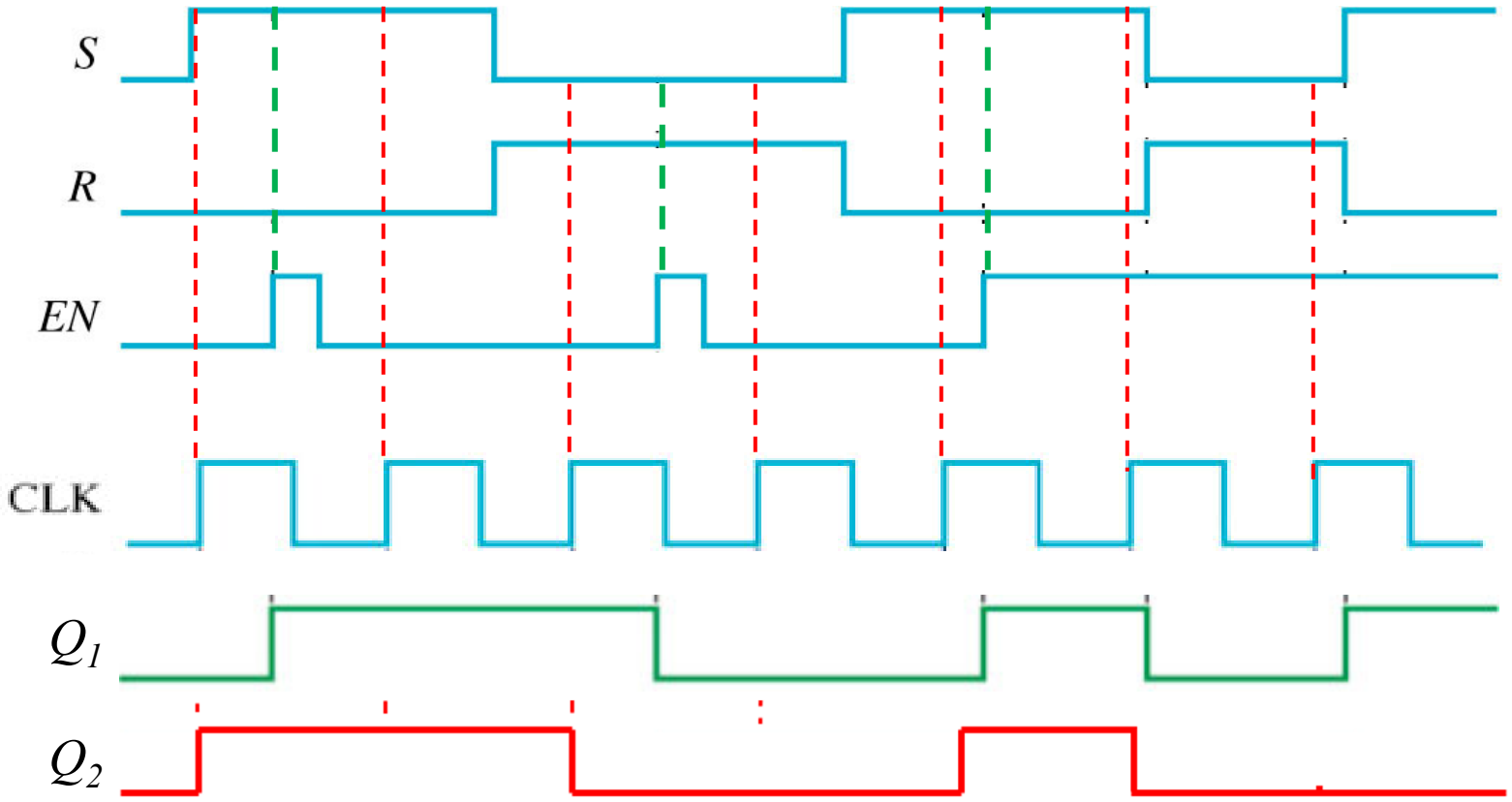
Flip-flop with output Q_2 and activated at positive edge-triggered

-> waveforms for Q_2.:



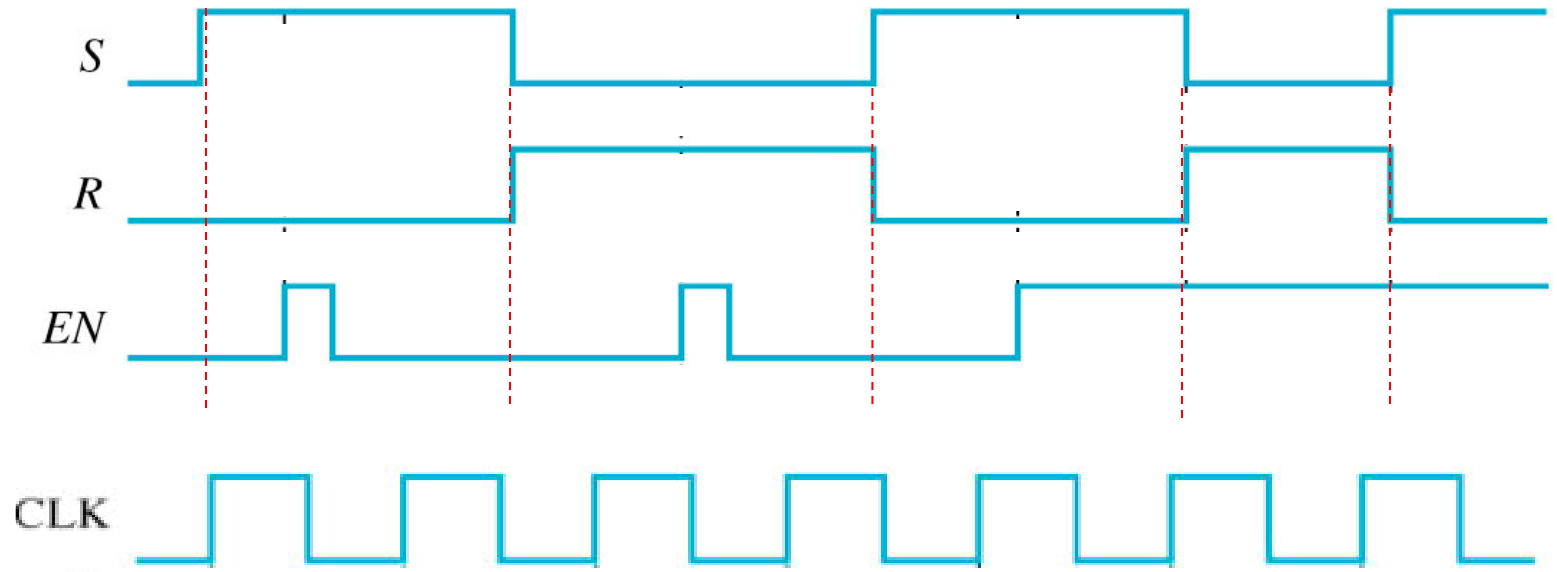
Solution 7.3:

Combined waveforms for Q_1 and Q_2 :



Self-Test:

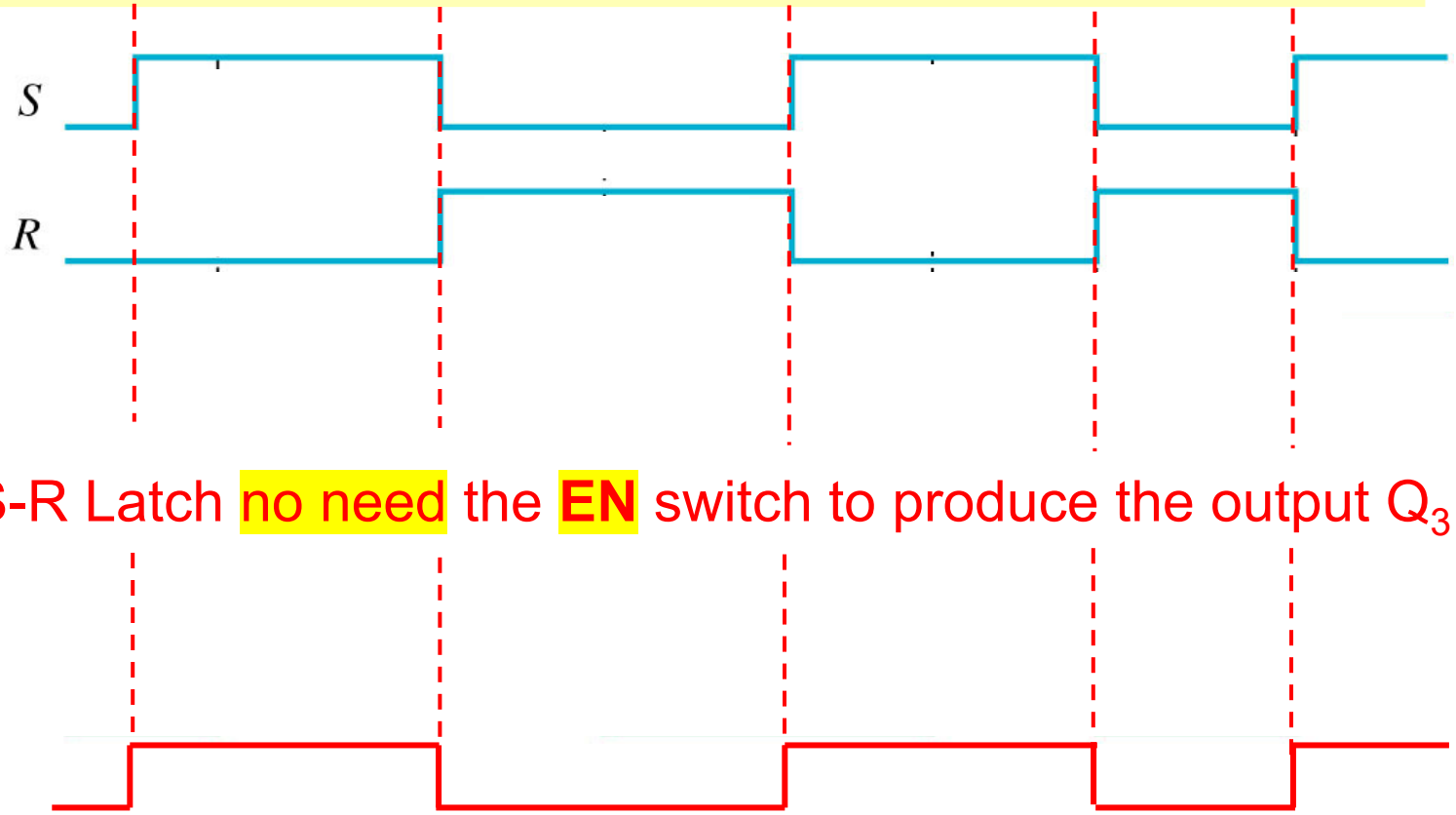
If a S-R Latch is used with output Q_3, find the waveforms for Q_3. Is the waveforms Q_3 similar to the waveform Q_1 in Exercise 7.3. Justify your answer. Assume that the outputs are initially LOW.



Q_3

Self-Test:

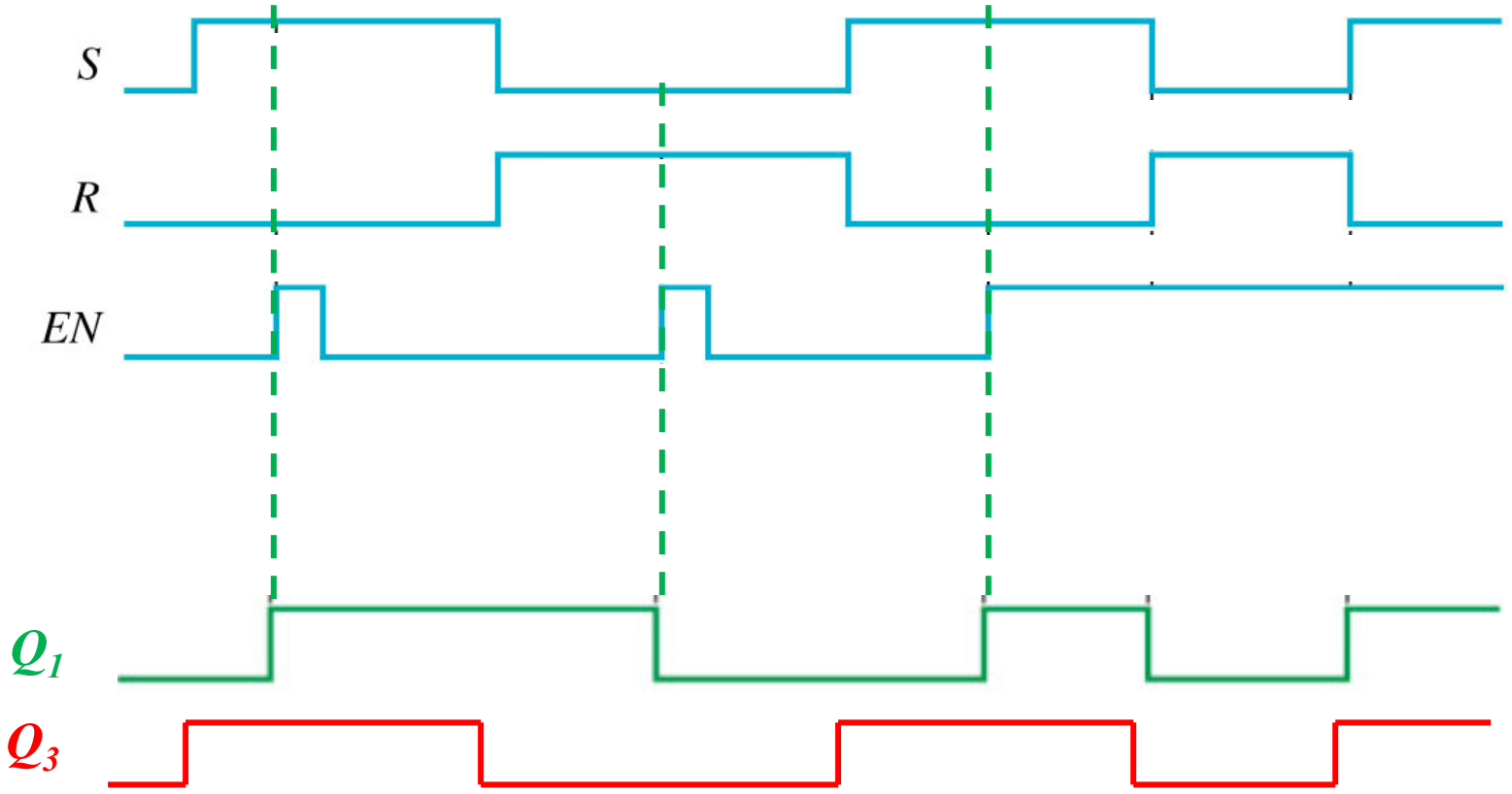
S-R Latch is used with output Q_3, … the waveforms for Q_3.



S-R Latch no need the **EN** switch to produce the output Q_3

Self-Test:

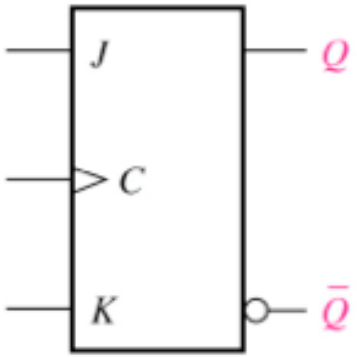
Is the waveforms Q_3 similar to the waveform Q_1 in Exercise 7.3 ? Justify your answer.



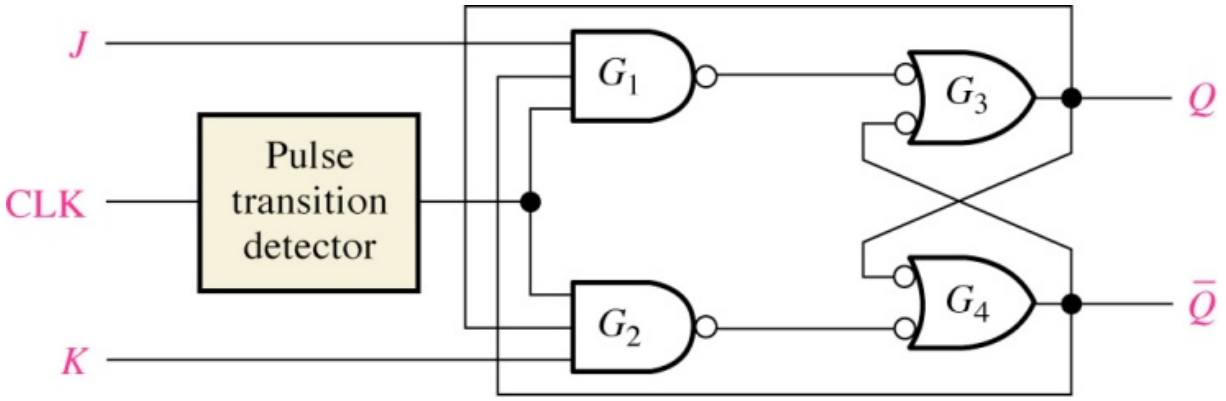
(ii) J-K Flip-Flop

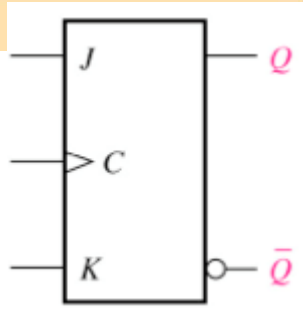
- The JK FF is versatile and is a widely used type of FF.
- The difference between J-K and S-R:

J-K has no invalid state as S-R.



Logic Symbol





Logic symbol

J	K	CLK	Output		Comments
			Q	$\bar{Q}$	
0	0	↑/↓	Q_0	$\bar{Q}_0$	No Change
0	1	↑/↓	0	1	RESET
1	0	↑/↓	1	0	SET
1	1	↑/↓	$\bar{Q}_0$	Q_0	Toggle

TRUTH TABLE

↑ = clock transition LOW to HIGH

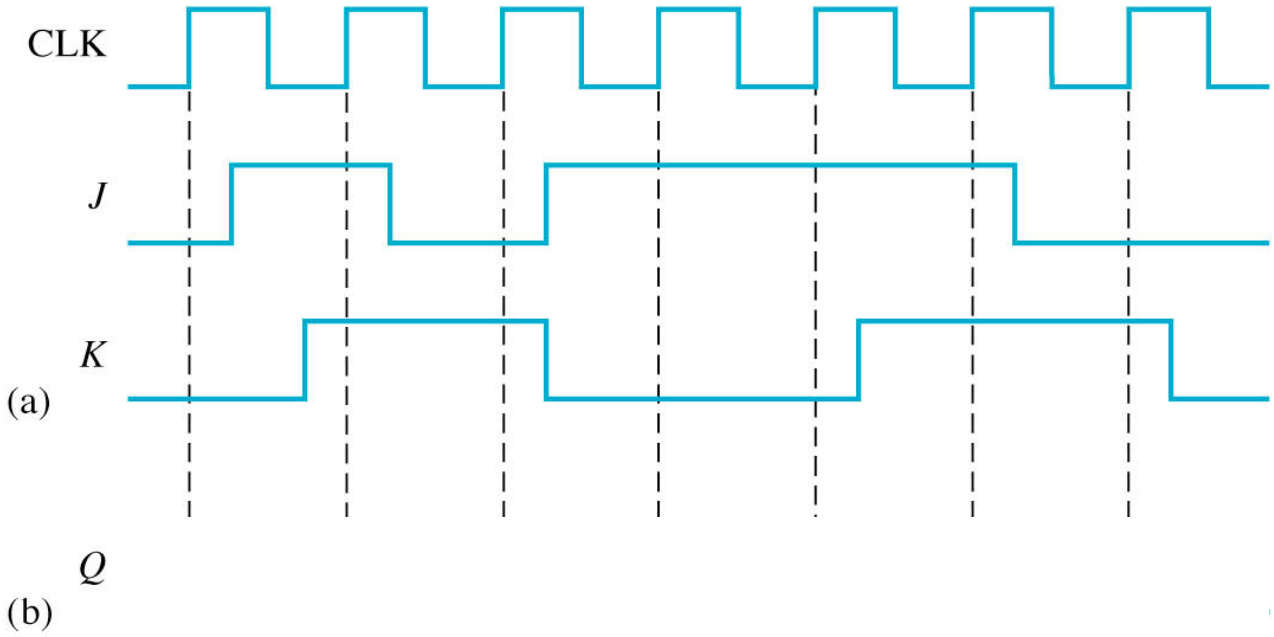
Q_0= output level prior to clock transition

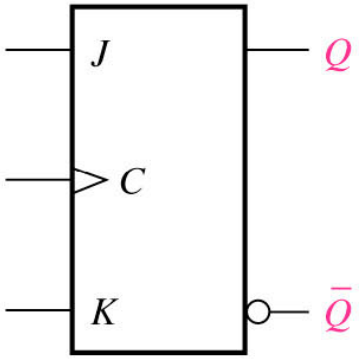
Example: J-K Flip-Flop.
Find the waveform for Q.
Assume that Q is initially LOW.

Positive

or

negative triggered?





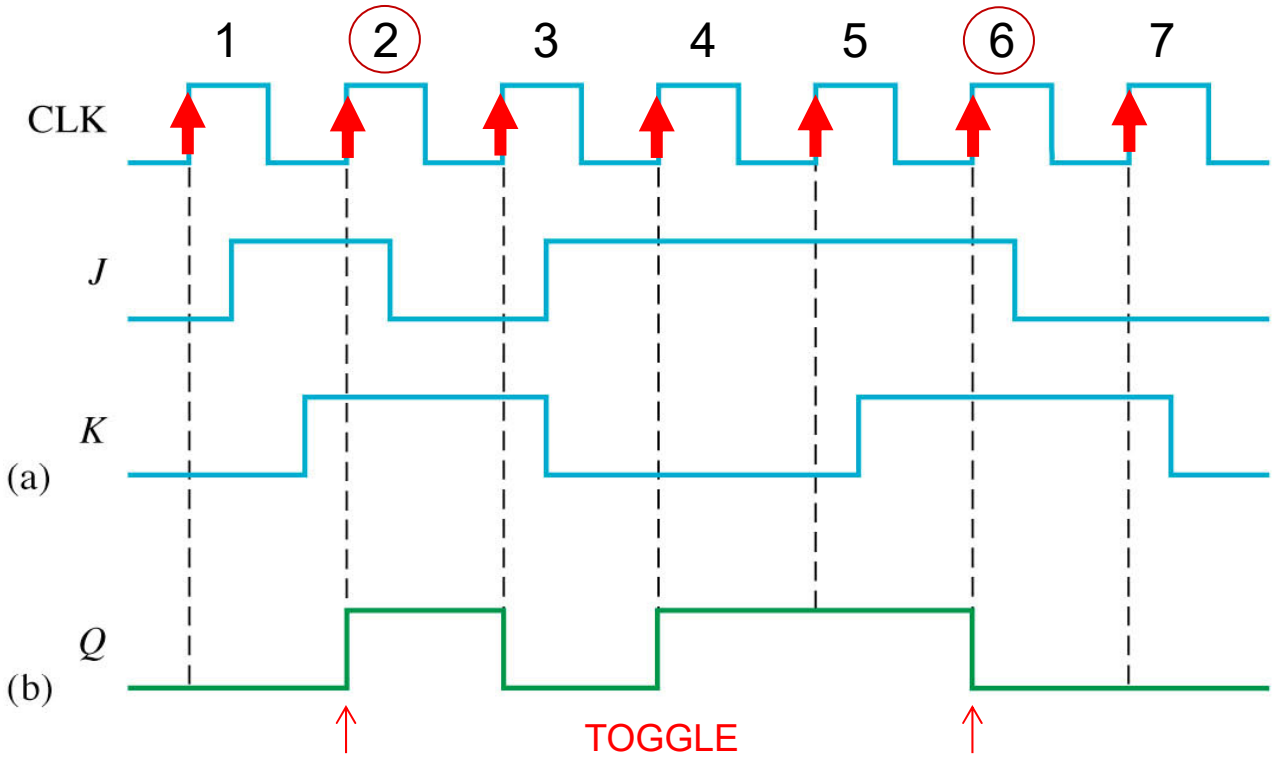
Logic symbol

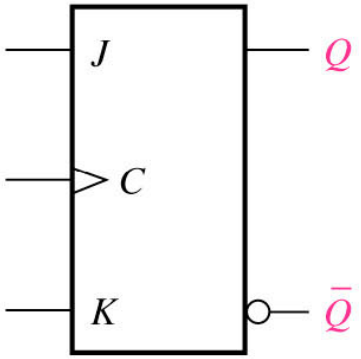
Solution:

J	K	CLK	Output		Comments
			Q	$\overline{Q}$	
0	0	↑/↓	Q_0	$\overline{Q_0}$	No Change
0	1	↑/↓	0	1	RESET
1	0	↑/↓	1	0	SET
1	1	↑/↓	$\overline{Q_0}$	Q_0	Toggle

Positive triggered

When the output **toggled**?





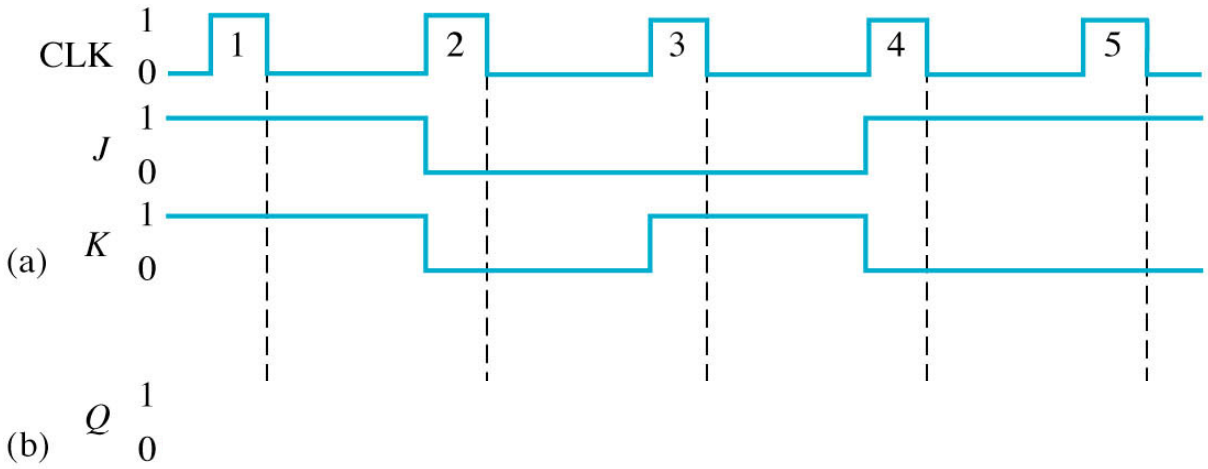
Logic symbol

Example: J-K Flip-Flop.
Find the waveform for Q.
Assume that Q is initially LOW.

Positive

or

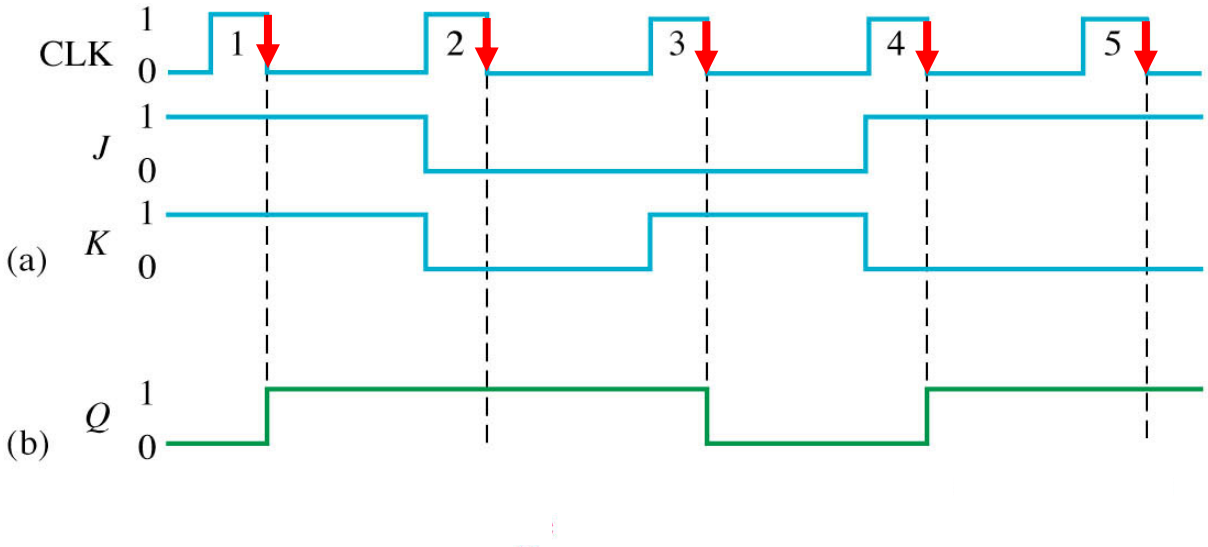
negative triggered?

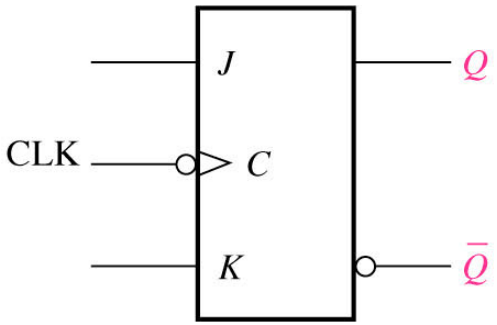


Solution:

J	K	CLK	Output		Comments
			Q	$\overline{Q}$	
0	0	↑/↓	Q_0	$\overline{Q_0}$	No Change
0	1	↑/↓	0	1	RESET
1	0	↑/↓	1	0	SET
1	1	↑/↓	$\overline{Q_0}$	Q_0	Toggle

negative triggered



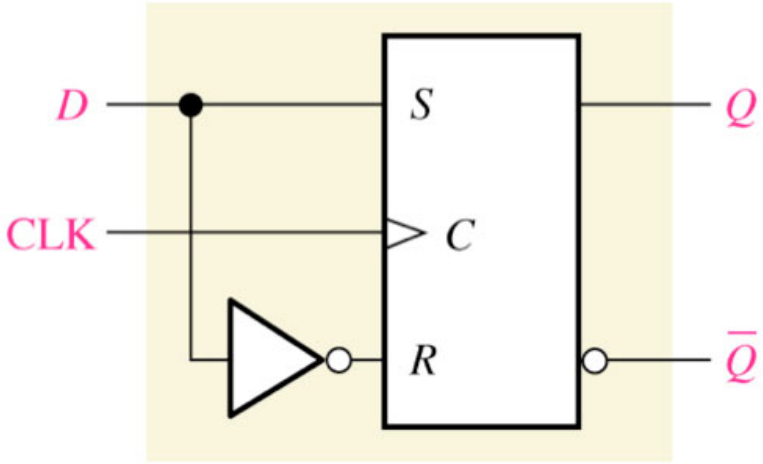


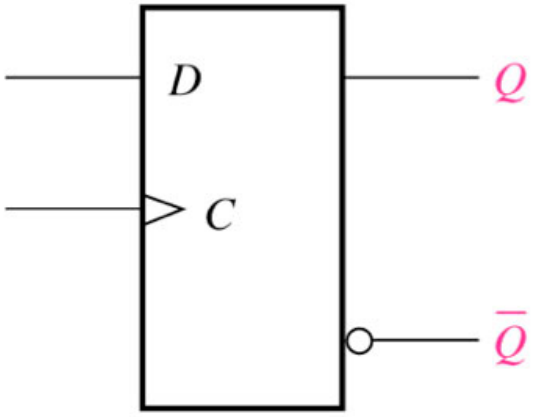
Logic symbol

(iii) D Flip-Flop

D → Data or Delay

- D FF is useful when a single data bit (1 or 0) is to be stored.
- The addition of an inverter to an S-R FF creates basic D FF where a positive edge-triggered type is shown below:



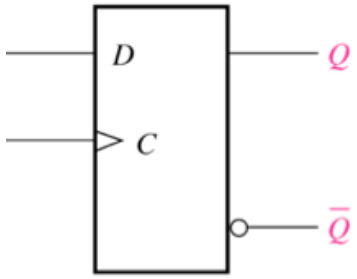


Logic symbol

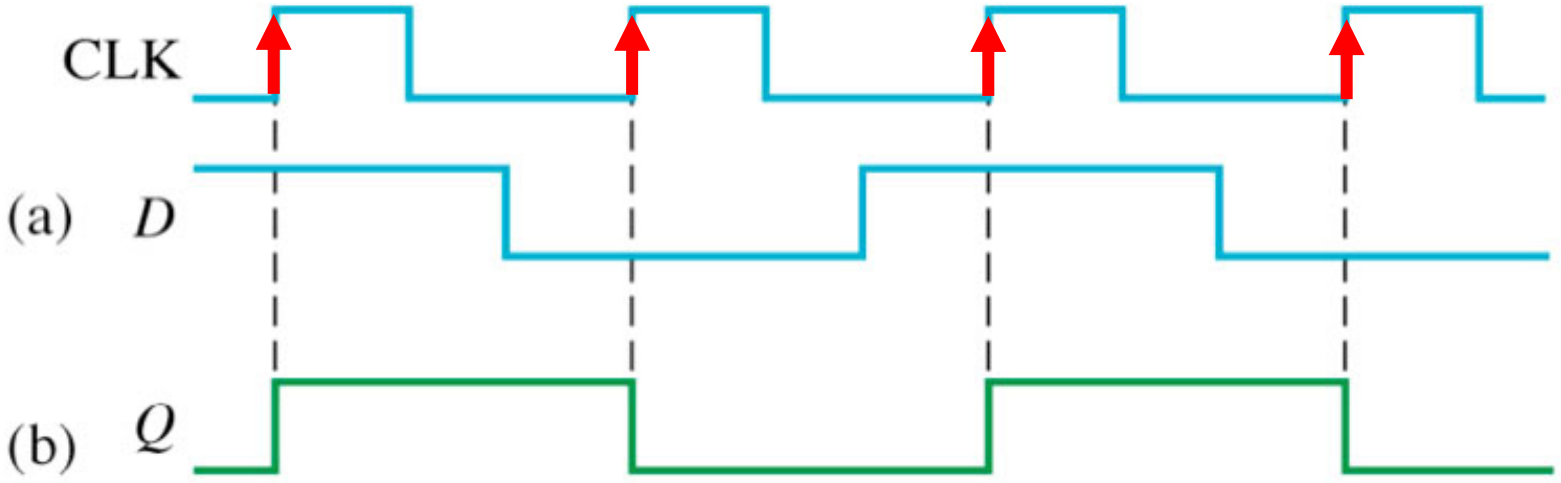
TRUTH TABLE

INPUTS		OUTPUTS		COMMENTS
D	CLK	Q	$\overline{Q}$	
1	↑	1	0	SET (store a 1)
0	↑	0	1	RESET (store 0)

(for positive edge-triggered)



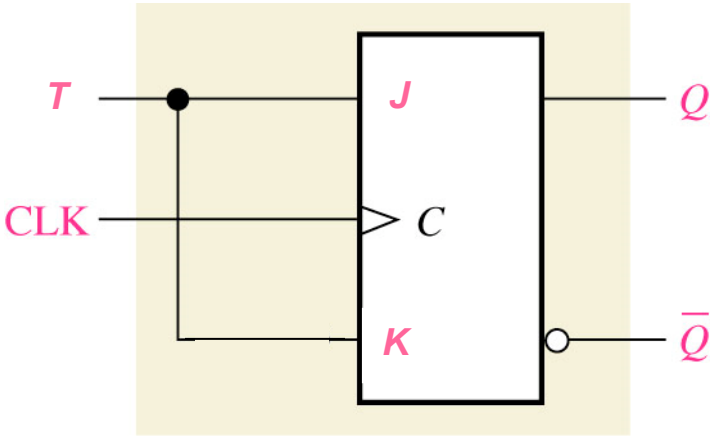
Logic symbol

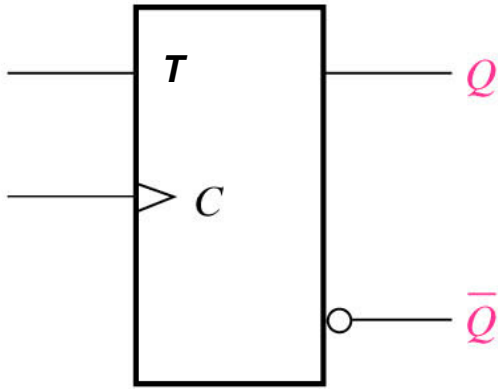


Remember, Q follows D at the active triggering clock edge.

(iv) T Flip-Flop

- Also called as toggle flip-flop.
- Frequently used in building counters.

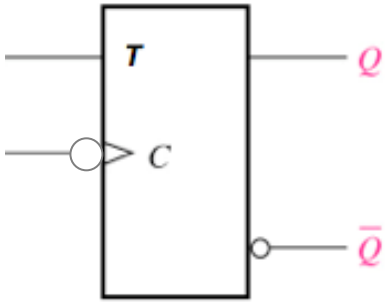




Logic Symbol

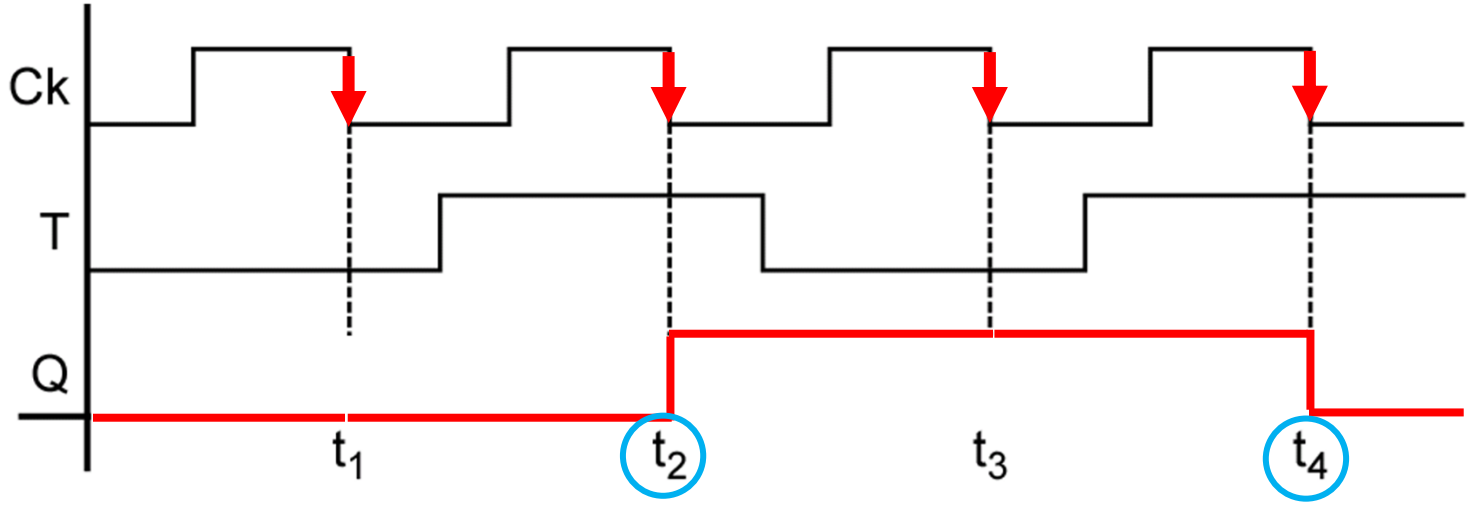
TRUTH TABLE

T	CLK ↑/↓	Output		Comments
		Q	Q_{next}	
0	↑/↓	0	0	HOLD
0	↑/↓	1	1	HOLD
1	↑/↓	0	1	TOGGLE
1	↑/↓	1	0	TOGGLE



Logic symbol

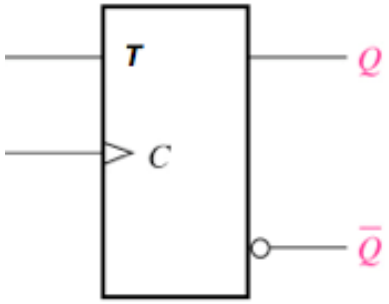
Timing Diagram for T Flip-Flop (Negative-Edge Triggered)



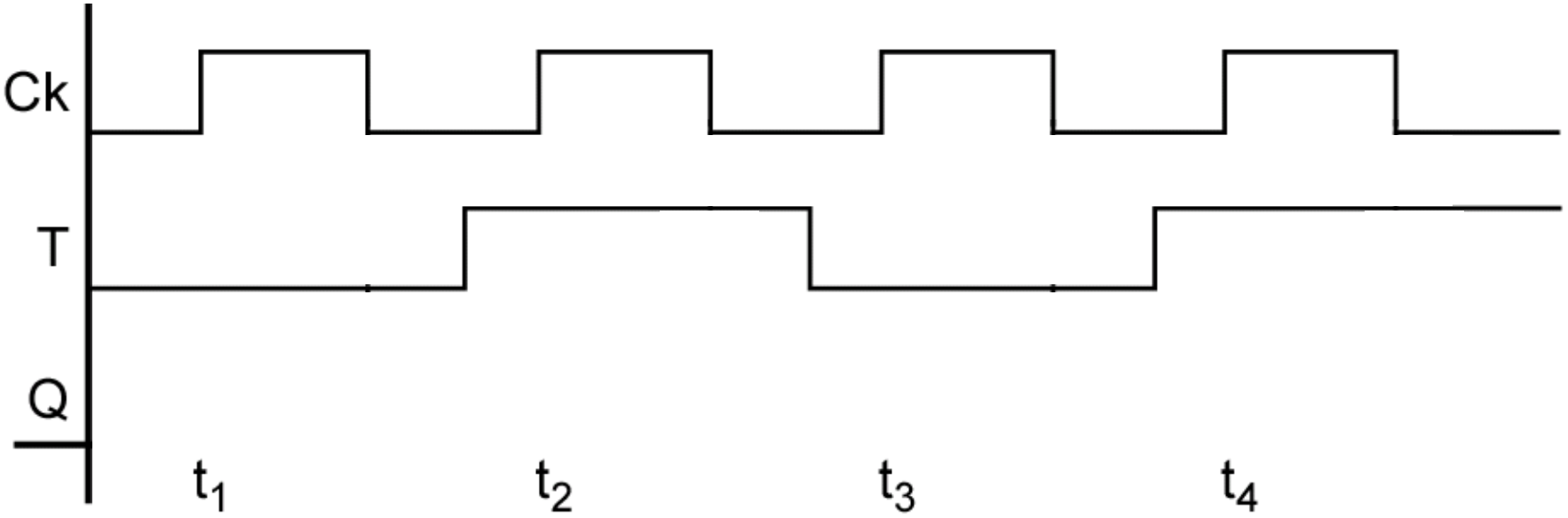
Homework

Try :

Consider a positive-edge trigger for a T-FF. Draw the waveforms for Q. Assume that the output is initially LOW.



Logic symbol



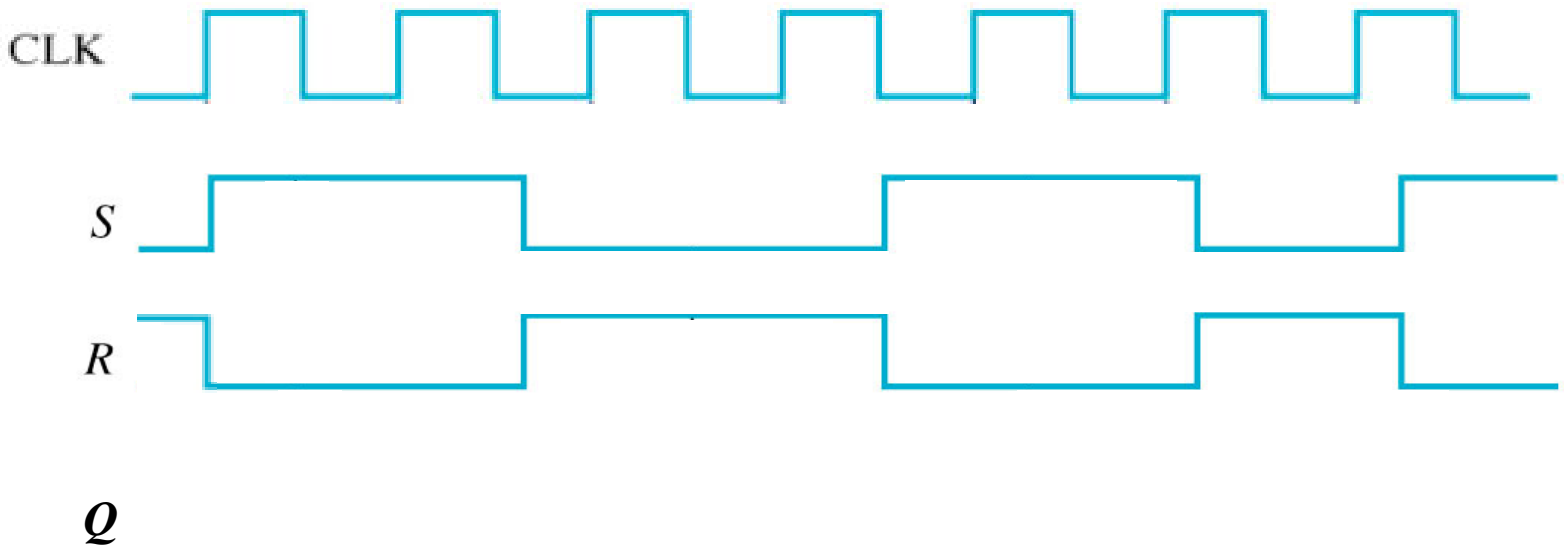
Homework

Exercise 7.4:

Given the inputs S and R for flip-flop with the inputs always complement to each other and activated at negative edge-triggered.

(i) Draw the logic symbol for the flip-flop.

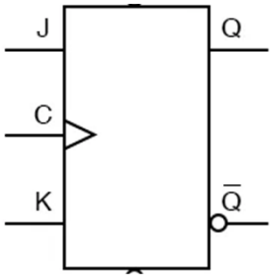
(ii) Find the waveforms Q. Assume that the output is initially LOW.

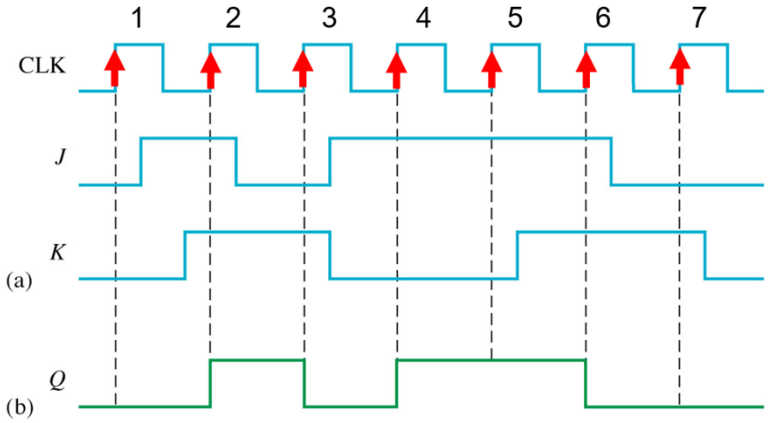


JK Flip Flop with Asynchronous Input

- The J and K inputs are called synchronous inputs since they only influence the state of the flip flop when the clock input is present.

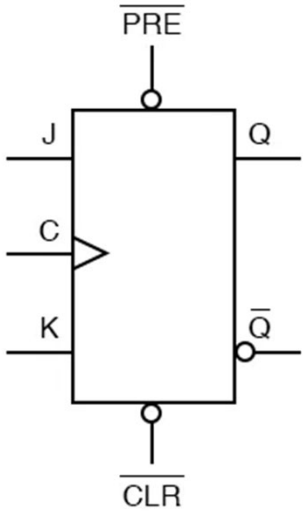
- Synchronous → J and K inputs transferred on the triggering edge of the clock



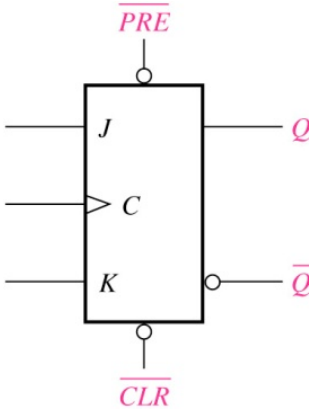


JK Flip Flop with Asynchronous Input

- This flip flop can also have other inputs called Preset and Clear that can be used for *setting* the flip flop to 1 or *resetting* it to 0.
- Asynchronous → These inputs can change the state of the flip flop regardless of the clock signal.
  - Preset ($\overline{\text{PRE}}$) or Direct SET
  - Clear ($\overline{\text{CLR}}$) or Direct RESET



TRUTH TABLE



$\overline{PRE}$	$\overline{CLR}$	FF	MODE
0	1	SET	Asynchronous
1	0	RESET	Asynchronous
1	1	JK	Synchronous
0	0	-	-

FF Response:

$Q = 1$

$Q = 0$

FF Clock Working

Not Used

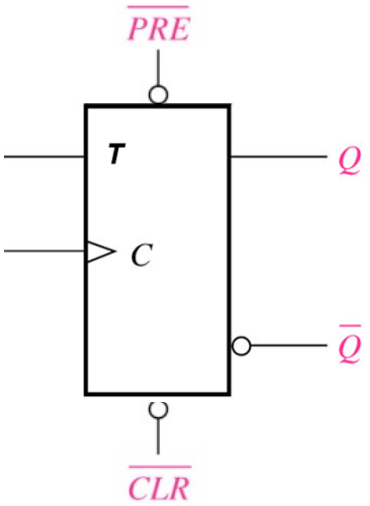
- Flip-flop input priority:

Priority	FF Input
Highest	$\overline{PRE}, \overline{CLR}$ (Asynchronous input)
Medium	Clock
Lowest	J-K, S-R, D, T (Synchronous input)

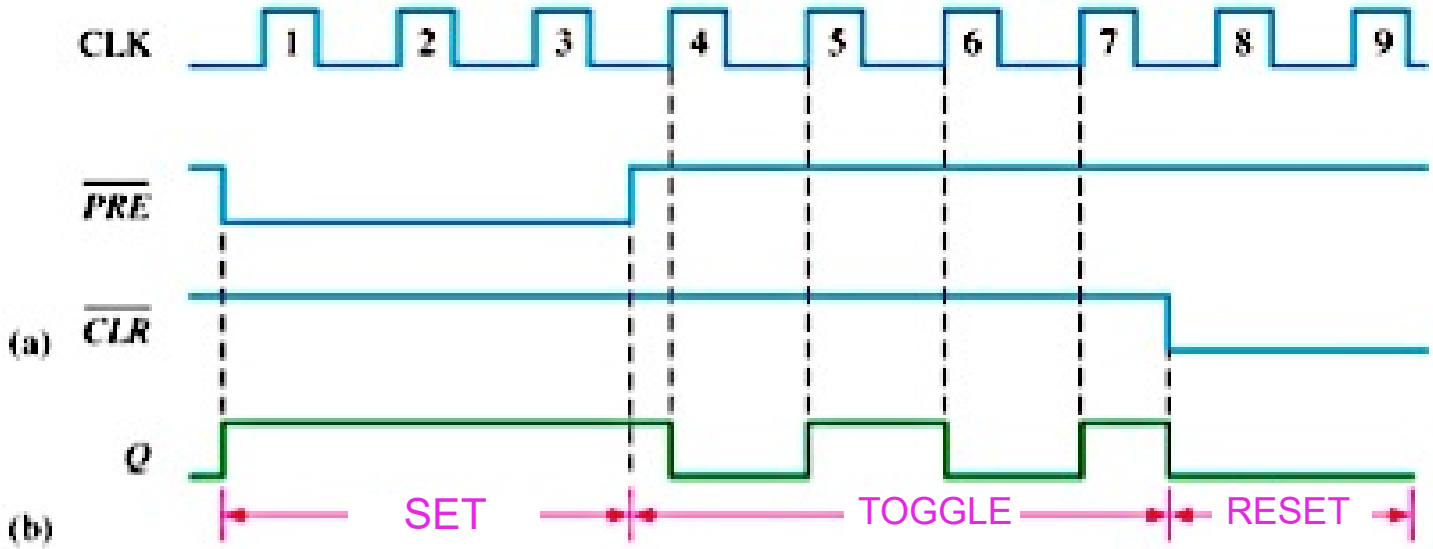
- Flip-flop asynchronous input has the highest priority.
  - Which means that if the asynchronous input active, the output will immediately change regardless the value of synchronous input or clock.

$\overline{PRE}$	$\overline{CLR}$	FF
0	1	SET
1	0	RESET
1	1	JK

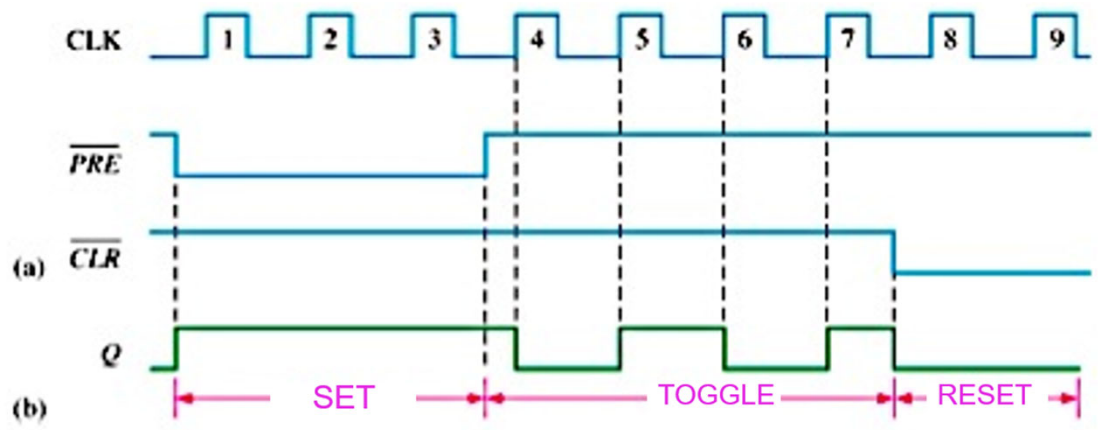
Note:
When J = K = 1,
it works as T flip-flop



Example: J-K Flip-Flop with both inputs are HIGH.
Find the waveform for Q.
Assume that Q is initially LOW.



$\overline{PRE}$	$\overline{CLR}$	FF	MODE
0	1	SET	Asynchronous
1	0	RESET	Asynchronous
1	1	JK	Synchronous



Q

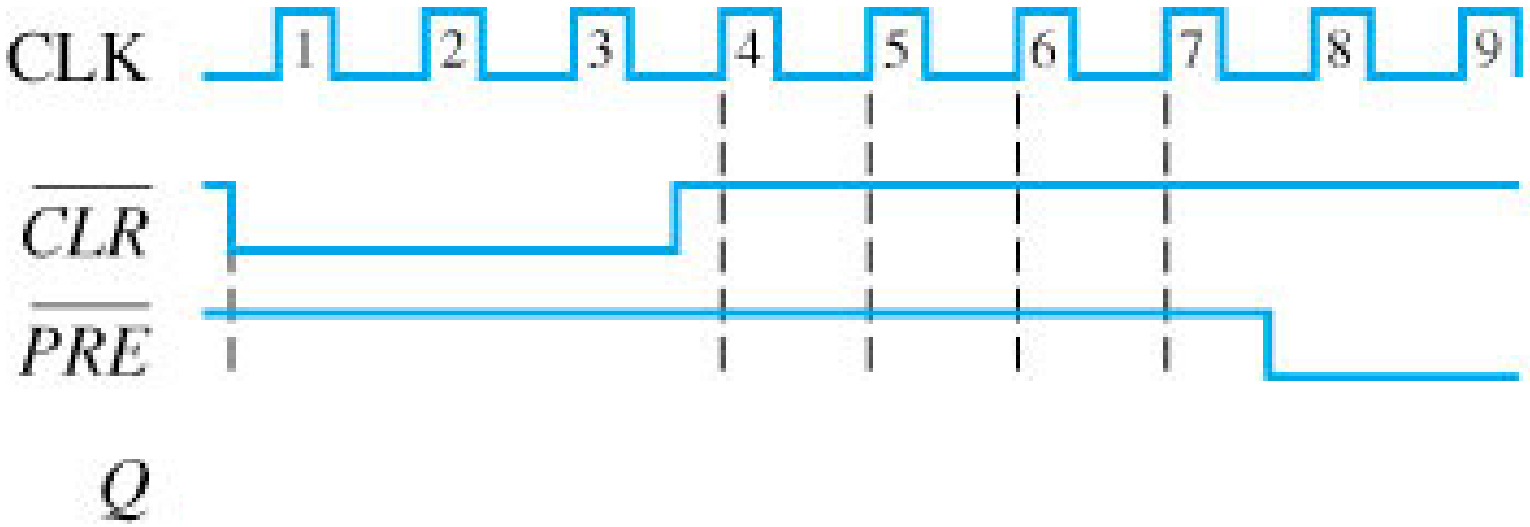
clk pulse	$\overline{PRE}$	$\overline{CLR}$	J	K	FF	Comment
1,2,3	0	**1**	1	1	SET	JK inputs - dont care
4,5,6, 7	1	1	1	1	Toggle	Synchronous mode.
8,9	**1**	0	1	1	RESET	JK inputs - dont care

Homework

Exercise 7.5:

Find the waveform for Q.

Assume that asynchronous J-K FF is used with both inputs are HIGH, and Q is initially LOW.

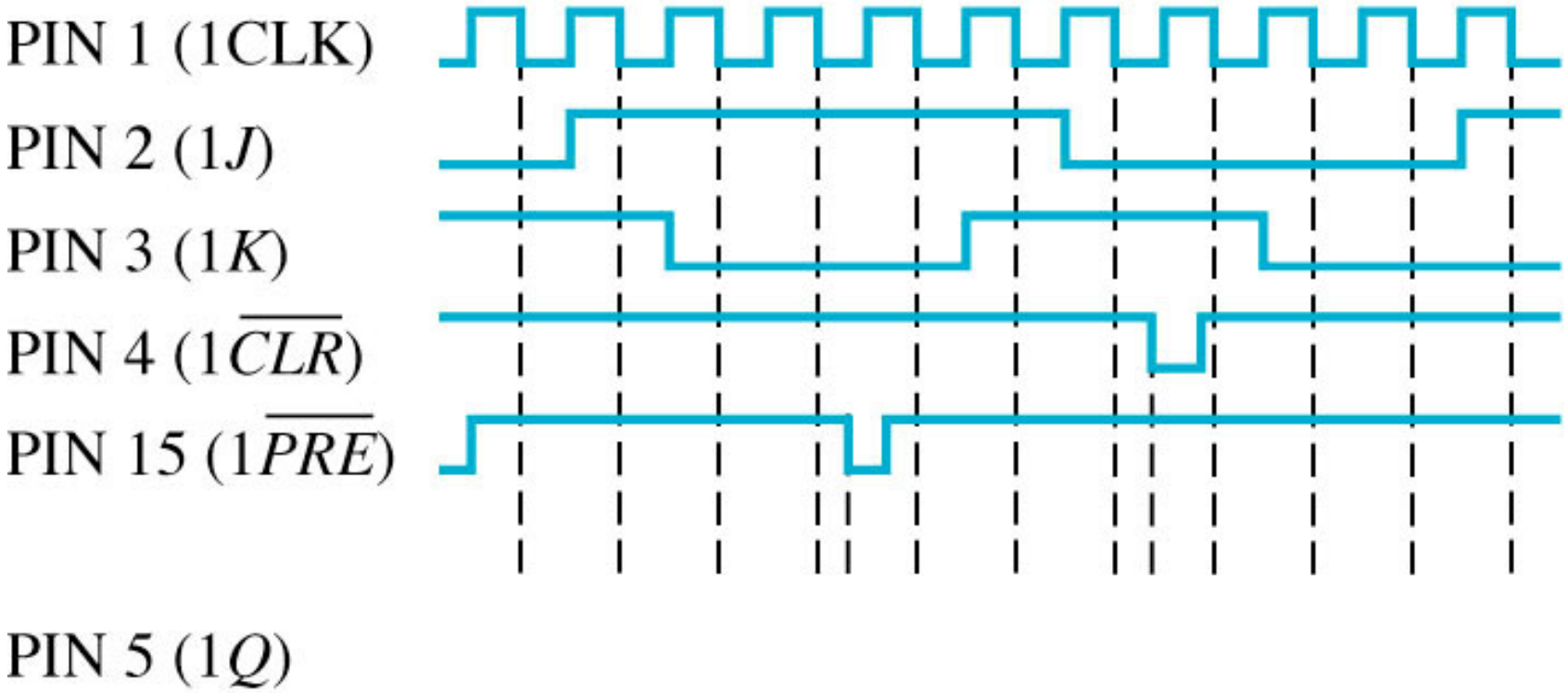


Homework

Exercise 7.6:

Find the waveform for Q for asynchronous J-K FF.

Assume that Q is initially HIGH.



Homework

Exercise 7.7: Complete the table in sequence.

Assume a J-K flip-flop is used with $\overline{PRE}$ and $\overline{CLR}$ inputs, and output Q.

$\overline{PRE}$	$\overline{CLR}$	J	K	Q	Mode	Comment
1	1	1	0			
1	1	1	1			
0	1	0	1			
1	1	0	0			
1	0	1	0			
0	1	1	1			
1	1	0	0			
1	1	1	1			

Mode: (Asynchronous / Synchronous)

Comment: (SET / RESET / HOLD/ TOGGLED / PRESET / CLEAR / INVALID)

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Summary

Latch & Flip-Flop

	Latch	Gated Latch	Flip-Flop
Output Characteristics	Output / next state depends to: • current inputs & • previous outputs / state	Output / next state depends to • enable gate input • current inputs • previous outputs / state	Output / next state depends to: • edge-triggered clock • current inputs • previous outputs / state

S-R Latch/FF

Basic Operation Truth-table

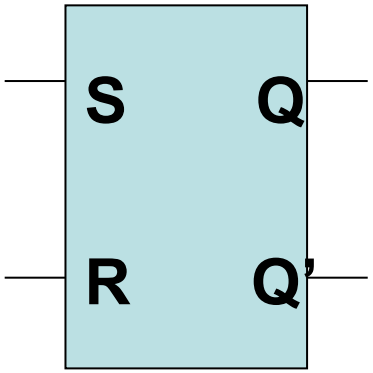
S	R	Q	Q’
0	0	Q	Q’
0	1	0	1
1	0	1	0
1	1	-	-

For:

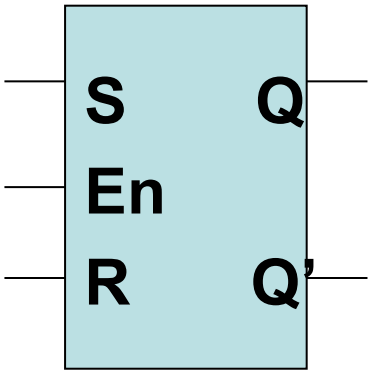
- En = 1 (Gated Latch)
- ↑ & ↓ FF

Block Diagram

Latch

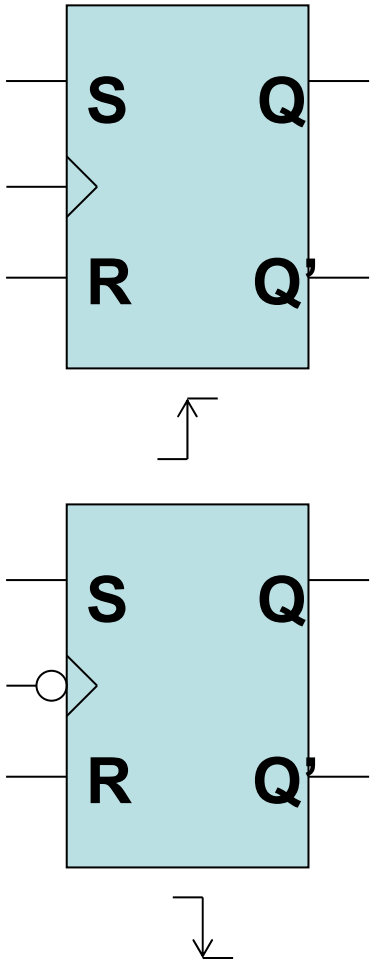


Gated Latch



S	R	En	Q	Q’
0	0	1	Q	Q’
0	1	1	0	1
1	0	1	1	0
1	1	1	-	-
X	X	0	Q	Q’

Flip-Flop



D Latch/FF

Block Diagram

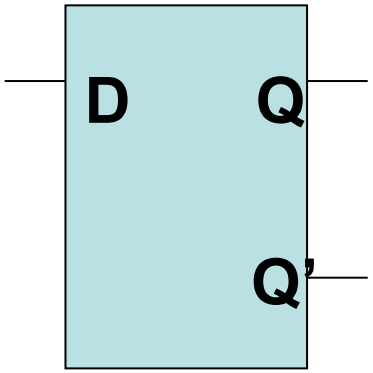
Basic Operation Truth-table

D	Q	Q’
0	0	1
1	1	0

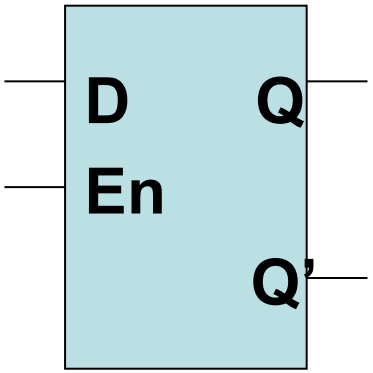
For:

- En = 1 (Gated Latch)
- ↑ & ↓ FF

Latch

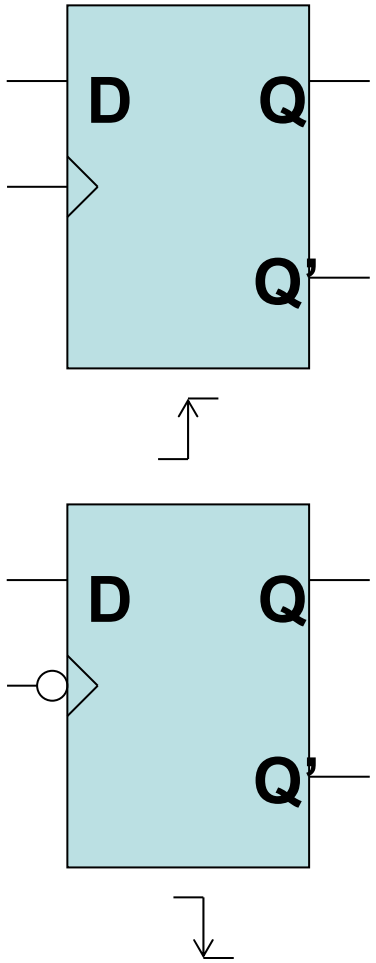


Gated Latch



D	En	Q	Q’
0	1	0	1
1	1	1	0
X	0	Q	Q’

Flip-Flop

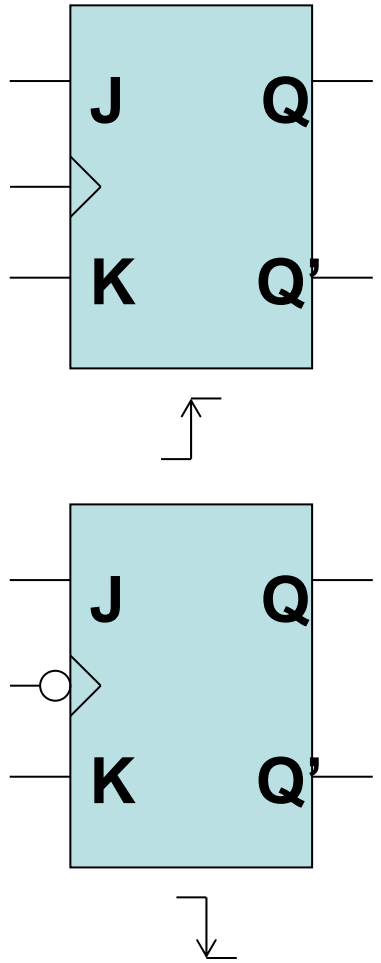


J-K FF	Block Diagram		
Basic Operation Truth-table	Latch	Gated Latch	Flip-Flop

J	K	Q	Q’
0	0	Q	Q’
0	1	0	1
1	0	1	0
1	1	Q’	Q

Nil

Nil



Asyn. J-K FF

Block Diagram

Basic Operation Truth-table	Latch	Gated Latch	Flip-Flop

$\overline{PRE}$	$\overline{CLR}$	FF
0	1	SET
1	0	RESET
1	1	JK

J	K	Q	Q’
0	0	Q	Q’
0	1	0	1
1	0	1	0
1	1	Q’	Q

Nil

Nil