UNIVERSITI TEKNOLOGI MALAYSIA

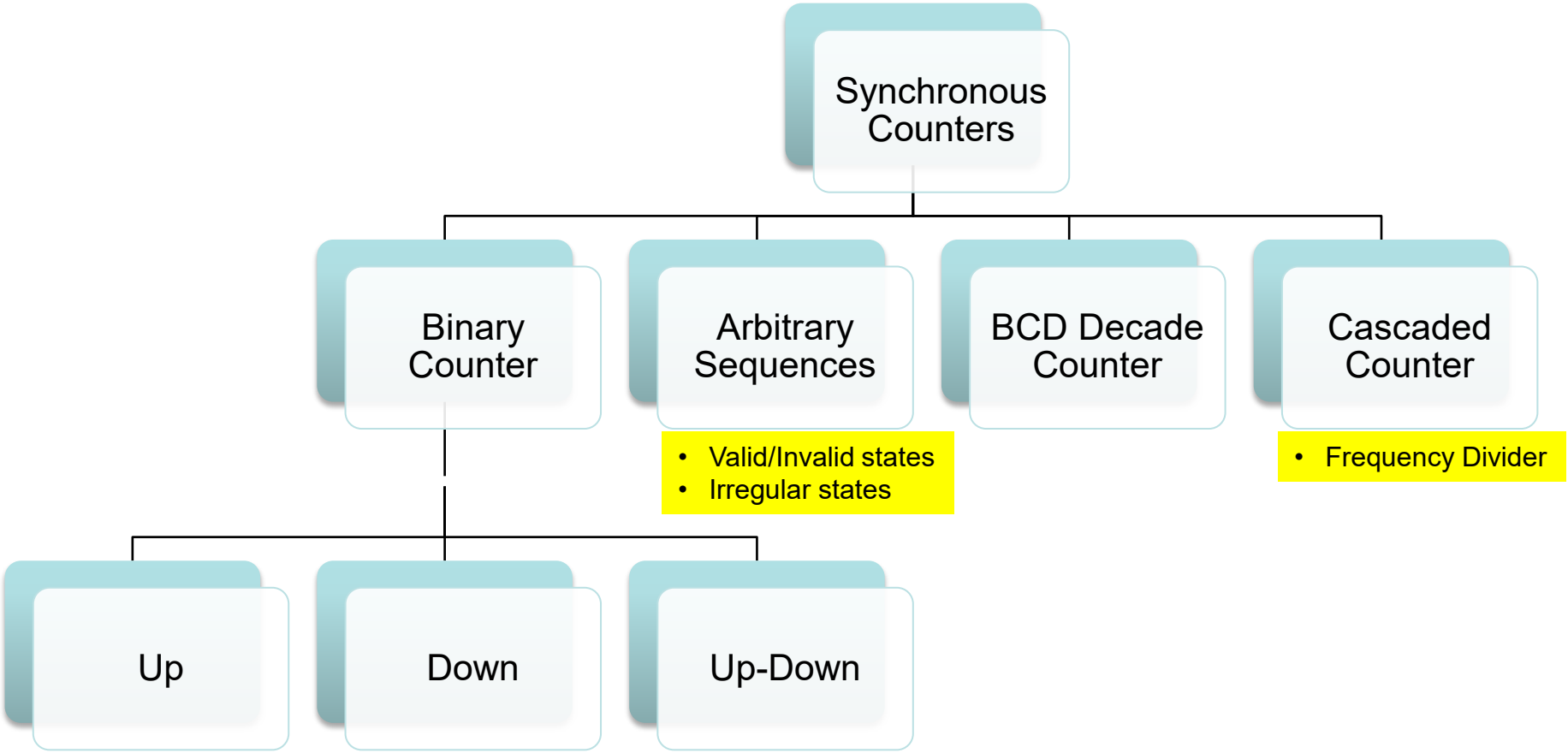
www.utm.my

SECR1013 DIGITAL LOGIC

MODULE 8b: COUNTERS (SYNC)

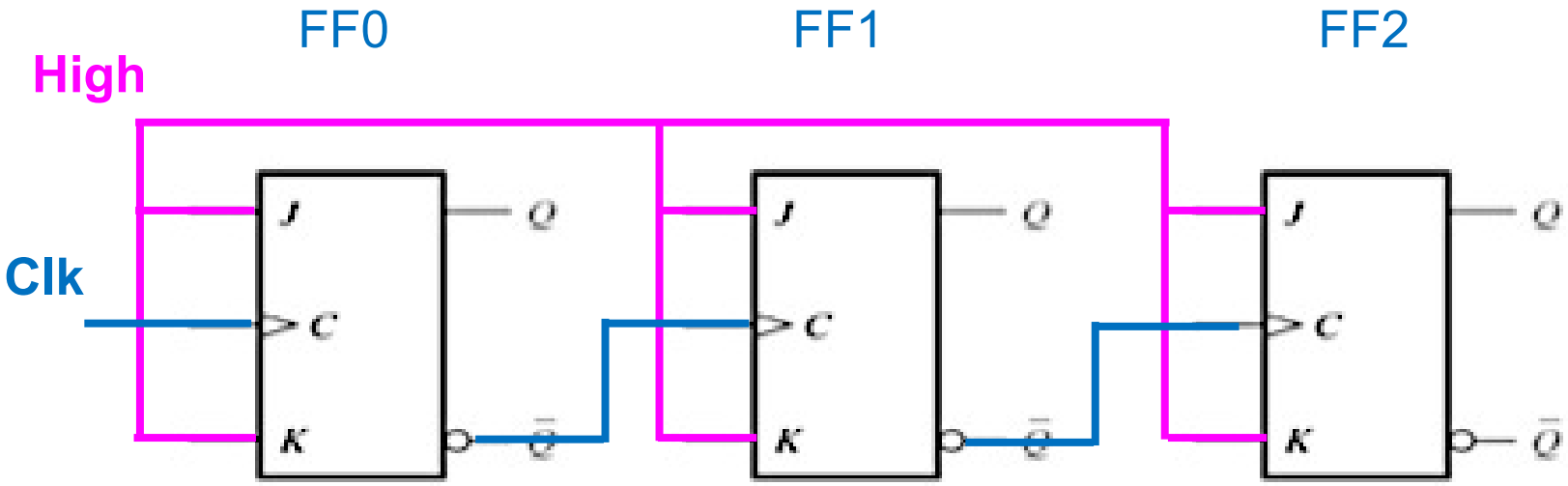
FACULTY OF COMPUTING

Synchronous Counters:


Synchronous Counters
Binary Counter
Arbitrary Sequences
BCD Decade Counter
Cascaded Counter
• Valid/Invalid states
• Irregular states
• Frequency Divider
Up
Down
Up-Down

RECAP

Design 3-bit Count Up Asynchronous Counter using J-K Flip-flop

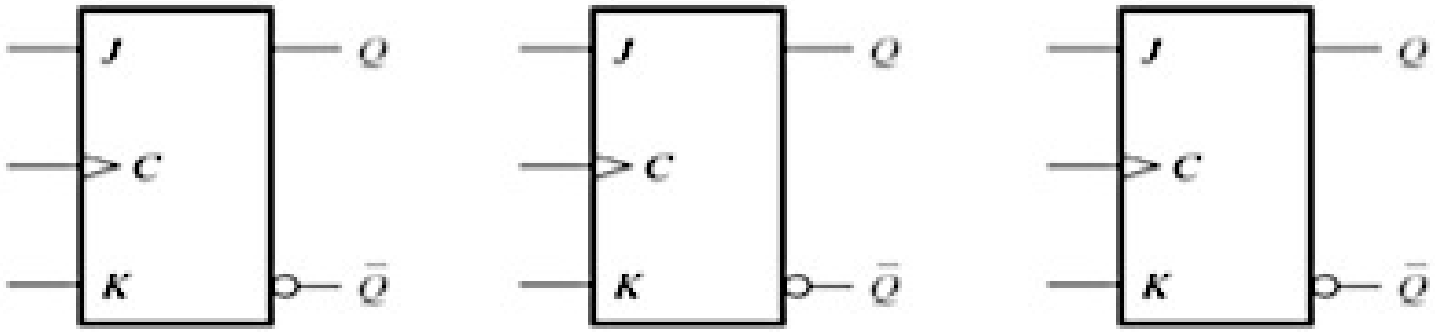


Async counter is easy, straight forward to design

How …

Design 3-bit Count Up Synchronous Counter using J-K Flip-flop

FF0 FF1 FF2



Sync counter is **not** straight forward to design!

Synchronous Counter Design

- Step 1
  Describe a general sequential circuit in terms of its basic parts and its input and outputs.
- Step 2
  Develop state diagram.
- Step 3
  Create next state table.
- Step 4
  Create flip-flop transition table.

Excitation Table

- Step 5
  Use K-maps to derive the logic equations.
- Step 6
  Implement counter implementation.

FF Excitation Table

Truth table for a positive edge-triggered J-K flip-flop.

Inputs			Outputs		
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

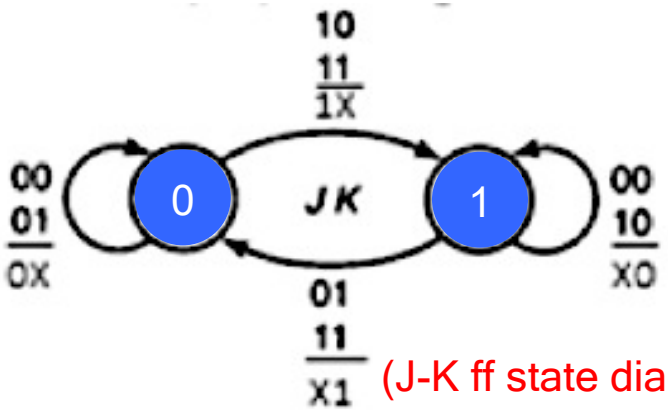
- JK Flip-Flop

Refer to JK FF truth table

	FF State		Present State	Next State
	J	K	Q_n	Q_{n+1}
NO CHANGE	0	0	0	0
	0	0	1	1
RESET	0	1	0	0
	0	1	1	0
SET	1	0	0	1
	1	0	1	1
TOGGLE	1	1	0	1
	1	1	1	0

About creating Transition table

J,K = 0/1 = **X**
**don't care*



(J-K ff state diagram)

FF Excitation Table

Truth table for a positive edge-triggered J-K flip-flop.

Inputs			Outputs		
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

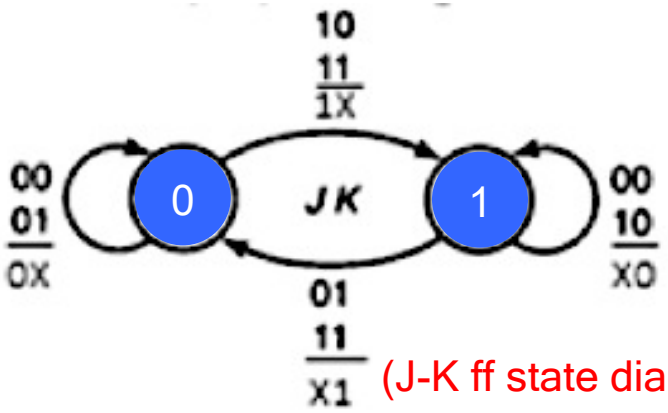
- JK Flip-Flop

Refer to JK FF truth table

	FF State		Present State	Next State
	J	K	Q_n	Q_{n+1}
NO CHANGE	0	0	0	0
	0	0	1	1
RESET	0	1	0	0
	0	1	1	0
SET	1	0	0	1
	1	0	1	1
TOGGLE	1	1	0	1
	1	1	1	0

JK-ff Excitation Table

Present State	Next State	FF State	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



(J-K ff state diagram)

Exercise 8b.1:

Construct the excitation table for **D flip-flop**

(using its state diagram)

Solution:

D flip-flop excitation table

Present State	Next State	FF State
Q_n	Q_{n+1}	D

Exercise 8b.1:

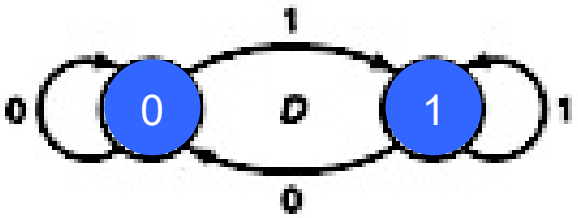
Construct the excitation table for **D flip-flop**

(using its state diagram)

D	Present state Q_n	Next state Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Truth table of D flip flop

D flip flop state diagram



D flip-flop excitation table

Present State	Next State	FF State
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

≡

Q_{n+1}	D
0	0
1	1

Exercise 8b.2:

Construct the excitation table for **T flip-flop**

(using its state diagram)

Solution:

T flip-flop excitation table

Present State	Next State	FF State
Q_n	Q_{n+1}	T

Exercise 8b.2:

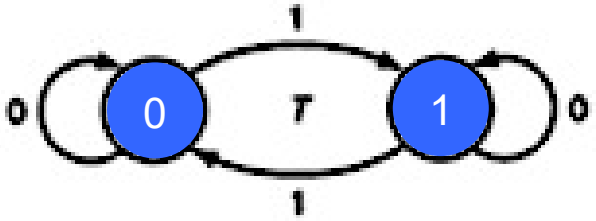
Construct the excitation table for **T flip-flop**

(using its state diagram)

T	Q	Q_{+1}	State
0	0	0	NO CHANGE
0	1	1	
1	0	1	TOGGLES
1	1	0	

Truth Table of T flip flop

T flip flop state diagram



T flip-flop excitation table

Present State	Next State	FF State
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

≡

Q_{n+1}	T
Q_n	0
$\overline{Q}_n$	1

Note:
These **excitation tables** will be used while filling in the flip-flop transition table in STEP 4 of designing synchronous counter.

Summary

Excitation tables of flip-flops:

Q_{n+1}	D
0	0
1	1

D flip-flop

Present State	Next State	FF State	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

NO CHANGE / RESET

SET / TOGGLE

RESET / TOGGLE

NO CHANGE / SET

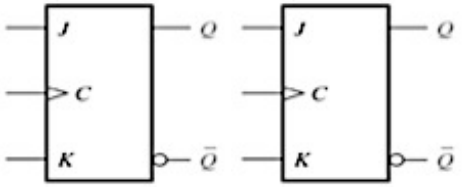
J-K flip-flop

Q_{n+1}	T
Q_n	0
$\overline{Q_n}$	1

T flip-flop

Synchronous Counters:

Up

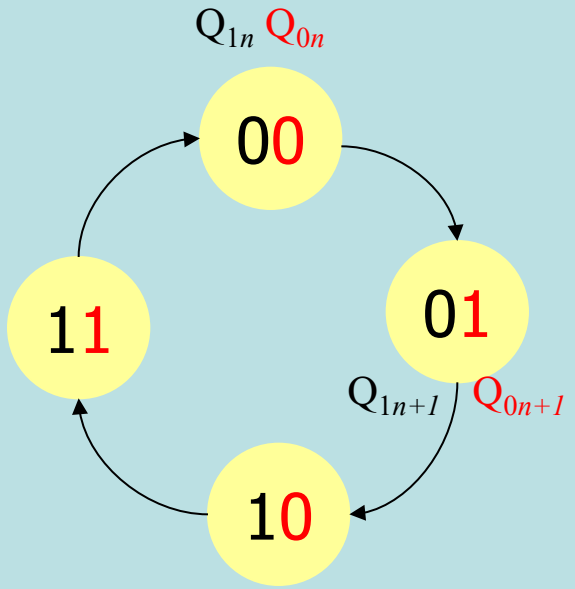


Design 2-bit Up Synchronous Counter:

J-K Flip-flop

- Step 1:
  To design 2-bit up synchronous counter using JK FF.

- Step 2: Draw state diagram



- Step 3: Create next state table

Present State		Next State	
Q_{1n}	Q_{0n}	Q_{1n+1}	Q_{0n+1}
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0

Note:
While filling in the flip-flop transition table, refer to the excitation table.

Present State	Next State	FF State	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

- Step 4:

  Construct the flip-flop transition table

FF1 FF0

Present State		Next State		JK Transition			
Q_{1n}	Q_{0n}	Q_{1n+1}	Q_{0n+1}	J_1	K_1	J_0	K_0
0	0	0	1				
0	1	1	0				
1	0	1	1				
1	1	0	0				

Note:
While filling in the flip-flop transition table, refer to the excitation table.

Present State	Next State	FF State	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

- Step 4:

  Construct the flip-flop transition table

FF1 FF0

Present State		Next State		JK Transition			
Q_{1n}	Q_{0n}	Q_{1n+1}	Q_{0n+1}	J_1	K_1	J_0	K_0
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	1	1	X	0	1	X
1	1	0	0	X	1	X	1

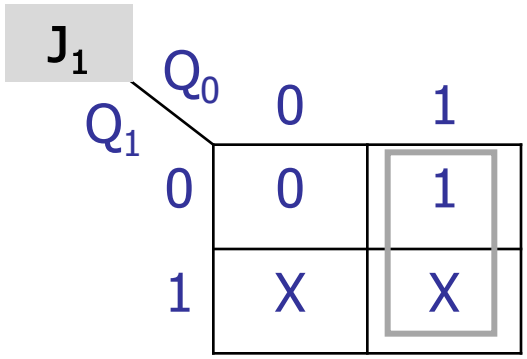
FF1 FF0

Present State		Next State		JK Transition			
Q_{1n}	Q_{0n}	Q_{1n+1}	Q_{0n+1}	J_1	K_1	J_0	K_0
0	0			0	X	1	X
0	1			1	X	X	1
1	0			X	0	1	X
1	1			X	1	X	1

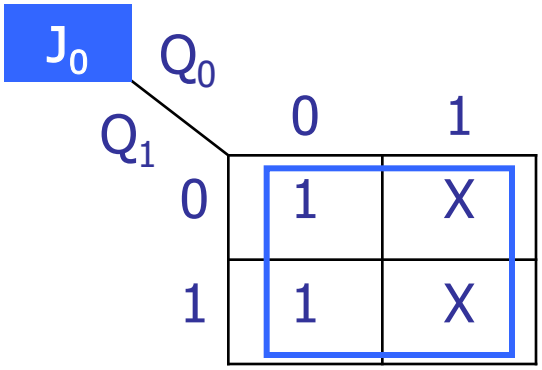
- Step 5:

  Use K-maps to derive the logic equations

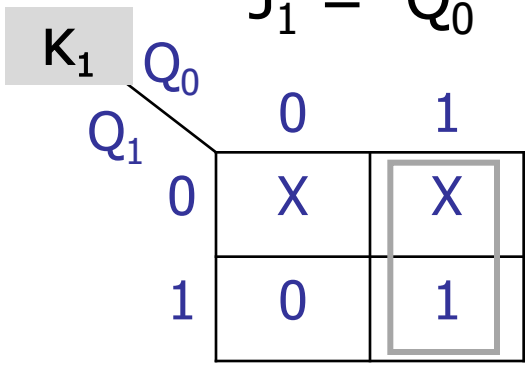
  (*for present state only*).



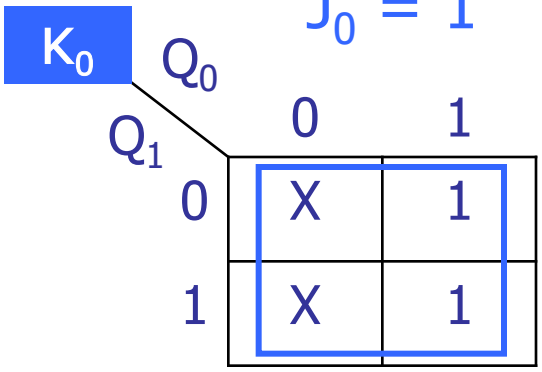
$J_1 = Q_0$



$J_0 = 1$



$K_1 = Q_0$



$K_0 = 1$

- Step 6: Implement counter by drawing the logic symbol connection / counter circuit.

FF0

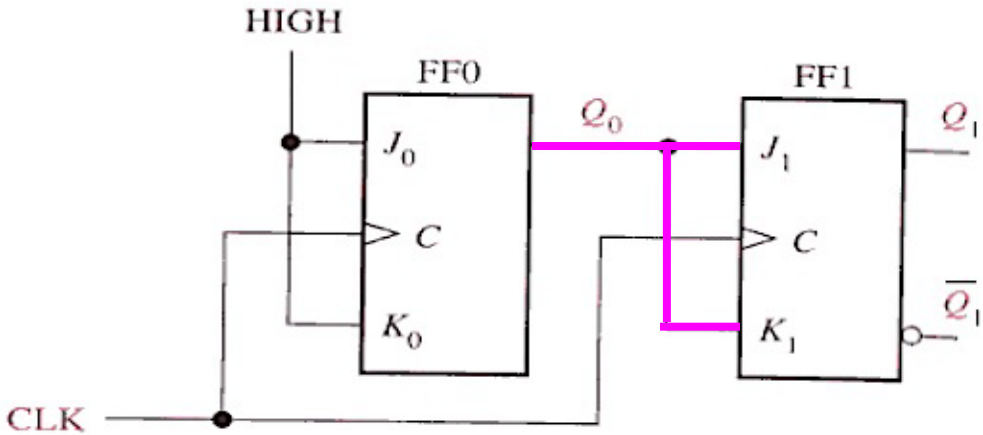
$J_0 = 1$

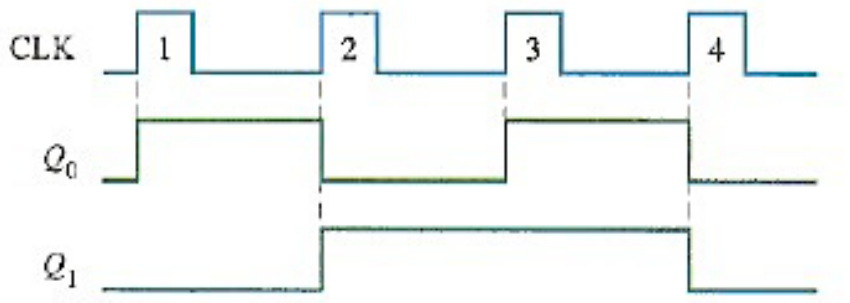
$K_0 = 1$

FF1

$J_1 = Q_0$

$K_1 = Q_0$





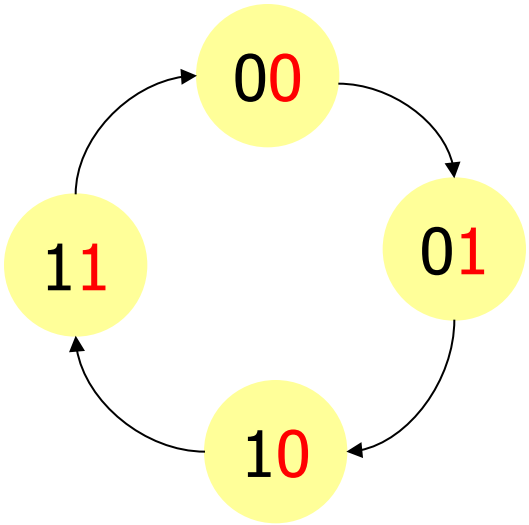
Q_1 toggle when Q_0=1

- Q_0 toggle at positive edge (CLK1, CLK2, CLK3, CLK4)
- Q_1 toggle when Q_0=1 at positive edge (CLK2, CLK4)

Exercise 8b.3: Design 2-bit up synchronous counter that using D flip-flop with positive edge triggered. Show all steps clearly.

Solution 8b.3:

- Step 2: Draw state diagram



- Step 3: Create next state table

Present State		Next State	
Q_1	Q_0	Q_{1+}	Q_{0+}
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0

Note:
While filling in the flip-flop transition table, refer to the excitation table.

Q_{n+1}	D
0	0
1	1

- Step 4:

  Construct flip-flop transition table using D excitation table.

Present State		Next State		D Transition	
Q_1	Q_0	Q_{1+}	Q_{0+}	D_1	D_0
0	0	0	1	0	1
0	1	1	0	1	0
1	0	1	1	1	1
1	1	0	0	0	0

Note:
While filling in the flip-flop transition table, refer to the excitation table.

Q_{n+1}	D
0	0
1	1

- Step 4:
  Construct flip-flop transition table using D excitation table.

(for present state only).

Present State		Next State		D Transition	
Q_1	Q_0	Q_{1+}	Q_{0+}	D_1	D_0
0	0			0	1
0	1			1	0
1	0			1	1
1	1			0	0

- Step 5:
  Use K-maps to derive the logic equations.

D_0

Q_1 \ Q_0	0	1
0	1	0
1	1	0

$$D_0 = \overline{Q}_0$$

D_1

Q_1 \ Q_0	0	1
0	0	1
1	1	0

$$D_1 = Q_0\overline{Q}_1 + \overline{Q}_0 Q_1$$
$$= Q_0 \oplus Q_1$$

(XOR Page: 97, 152)

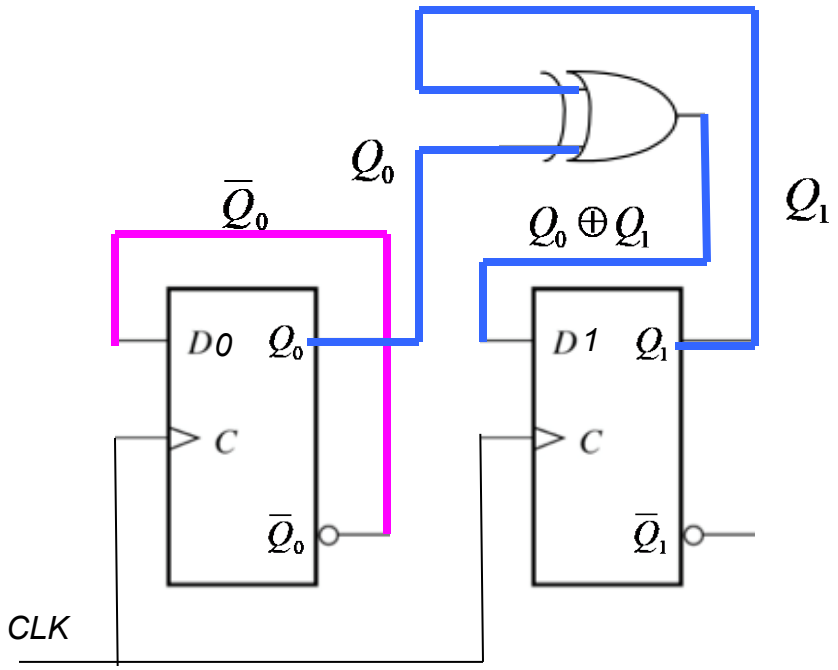
- Step 6: Implement counter implementation by drawing the logic symbol connection / counter circuit.

FF0

$$D_0 = \overline{Q}_0$$

FF1

$$D_1 = Q_0 \oplus Q_1$$

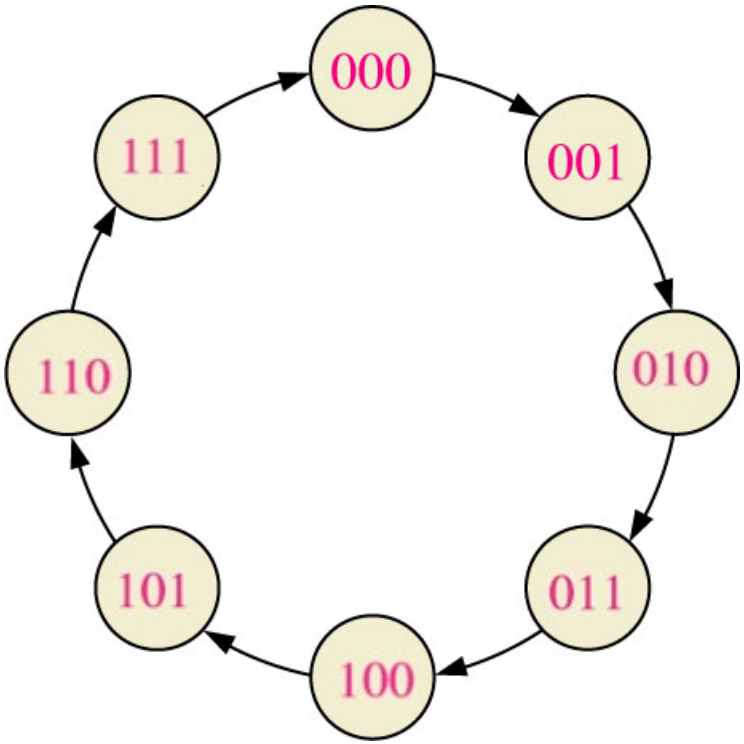


Exercise 8b.4: Design 3-bit up synchronous counter that using T flip-flop with positive edge triggered. Show all steps clearly.

Design 3-bit Up Synchronous Counter:

J-K Flip-flop

- Step 2: State diagram



- Step 3: Next State table

Present State			Next State		
Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

Note:
While filling in the flip-flop transition table, refer to the excitation table.

Present State	Next State	FF State	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

- Step 4:

  FF transition table

FF2 **FF1** **FF0**

Present State			Next State			JK Transition Table					
Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

(Module page: 259)

Present State			Next State			JK Transition Table					
Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0				0	X	0	X	1	X
0	0	1				0	X	1	X	X	1
0	1	0				0	X	X	0	1	X
0	1	1				1	X	X	1	X	1
1	0	0				X	0	0	X	1	X
1	0	1				X	0	1	X	X	1
1	1	0				X	0	X	0	1	X
1	1	1				X	1	X	1	X	1

- Step 5:

Create K-map to determine the Boolean expression

Q_2 \ Q_1Q_0	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$J_2 = Q_1Q_0$

Q_2 \ Q_1Q_0	00	01	11	10
0	0	1	X	X
1	0	1	X	X

$J_1 =$

Q_2 \ Q_1Q_0	00	01	11	10
0	1	X	X	1
1	1	X	X	1

$J_0 =$

Q_2 \ Q_1Q_0	00	01	11	10
0				
1				

$K_2 =$

Q_2 \ Q_1Q_0	00	01	11	10
0				
1				

$K_1 =$

Q_2 \ Q_1Q_0	00	01	11	10
0				
1				

$K_0 =$

(Module page: 259)

Present State			Next State			JK Transition Table					
Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0				0	X	0	X	1	X
0	0	1				0	X	1	X	X	1
0	1	0				0	X	X	0	1	X
0	1	1				1	X	X	1	X	1
1	0	0				X	0	0	X	1	X
1	0	1				X	0	1	X	X	1
1	1	0				X	0	X	0	1	X
1	1	1				X	1	X	1	X	1

- Step 5:

Create K-map to determine the Boolean expression

Q_2 \ Q_1Q_0	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$$J_2 = Q_1Q_0$$

Q_2 \ Q_1Q_0	00	01	11	10
0	0	1	X	X
1	0	1	X	X

$$J_1 = Q_0$$

Q_2 \ Q_1Q_0	00	01	11	10
0	1	X	X	1
1	1	X	X	1

$$J_0 = 1$$

Q_2 \ Q_1Q_0	00	01	11	10
0	X	X	X	X
1	0	0	1	0

$$K_2 = Q_1Q_0$$

Q_2 \ Q_1Q_0	00	01	11	10
0	X	X	1	0
1	X	X	1	0

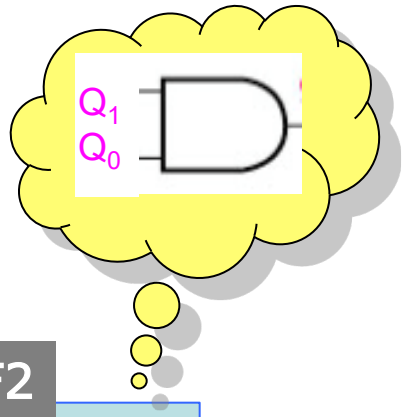
$$K_1 = Q_0$$

Q_2 \ Q_1Q_0	00	01	11	10
0	X	1	1	X
1	X	1	1	X

$$K_0 = 1$$

- Step 6:

  The implementation of 3-bit synchronous counter



FF0

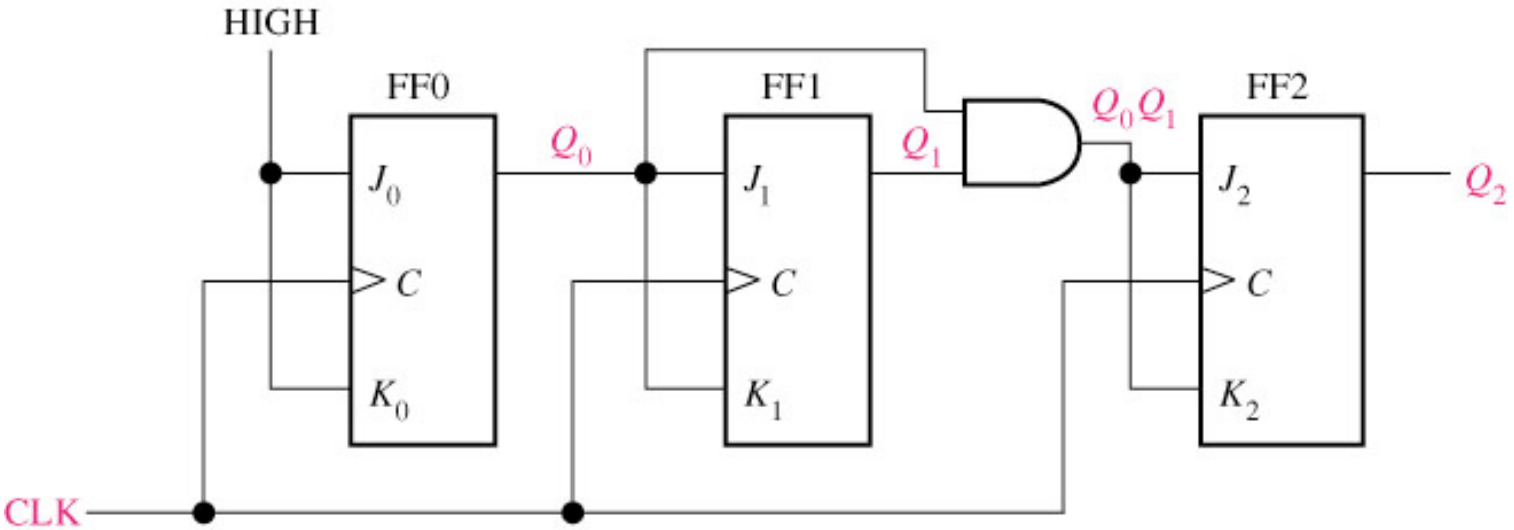
$$J_0 = 1$$
$$K_0 = 1$$

FF1

$$J_1 = Q_0$$
$$K_1 = Q_0$$

FF2

$$J_2 = Q_1 Q_0$$
$$K_2 = Q_1 Q_0$$



Exercise 8b.5: Design 3-bit up synchronous counter that using D flip-flop with positive edge triggered. Show all steps clearly.

Exercise 8b.6: Design 4-bit up synchronous counter that using the following flip-flops with negative edge triggered. Show all steps clearly.

(a) D flip-flop.

(b) T flip-flop.

Synchronous Counters:

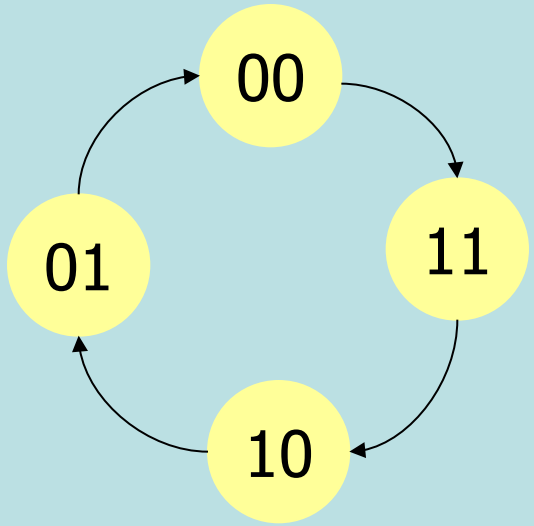
Down

2-bit Down Synchronous Counter:

D Flip-flop

- Step 1:
  To design 2-bit down synchronous counter using D flip-flop.
  There is no input or output element in this design.

- Step 2: Draw state diagram



- Step 3: Create next state table

Present State		Next State	
Q_1	Q_0	Q_{1+}	Q_{0+}
0	0	1	1
0	1	0	0
1	0	0	1
1	1	1	0

Q_{n+1}	D
0	0
1	1

- Step 4:

  Draw flip-flop transition table. For D flip-flop, D input is the same as the next state values.

Present State		Next State		D Transition	
Q_1	Q_0	Q_{1+}	Q_{0+}	D_1	D_0
0	0	1	1	1	1
0	1	0	0	0	0
1	0	0	1	0	1
1	1	1	0	1	0

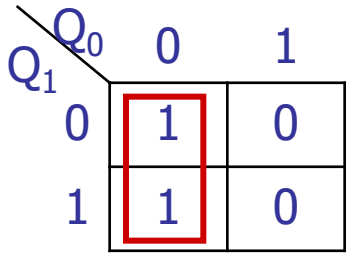
Q_{n+1}	D
0	0
1	1

- Step 4:

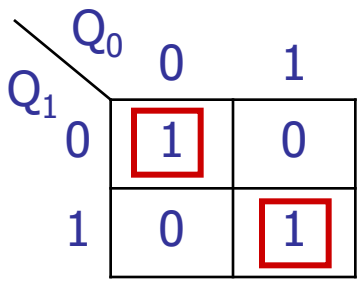
  Draw flip-flop transition table. For D flip-flop, D input is the same as the next state values.

Present State		Next State		D Transition	
Q_1	Q_0	Q_{1+}	Q_{0+}	D_1	D_0
0	0			1	1
0	1			0	0
1	0			0	1
1	1			1	0

- Step 5: K-Map.



$$D_0 = \overline{Q}_0$$



$$D_1 = \overline{Q}_1\overline{Q}_0 + Q_1Q_0$$

$$D_1 = Q_0 \odot Q_1$$

XNOR

Exercise 8b.7: Draw the circuit for of 2-bit down synchronous counter using D flip-flop with $D_1 = Q_0 \odot Q_1$ and $D_0 = \overline{Q}_0$

Exercise 8b.8: Design 3-bit down synchronous counter that using the following flip-flops with negative edge triggered. Show all steps clearly.

(a) J-K flip-flop.

(b) D flip-flop.

(c) T flip-flop.

Exercise 8b.9: Design 4-bit down synchronous counter that using the following flip-flops with positive edge triggered. Show all steps clearly.

(a) D flip-flop.

(b) T flip-flop.

Synchronous Counters:

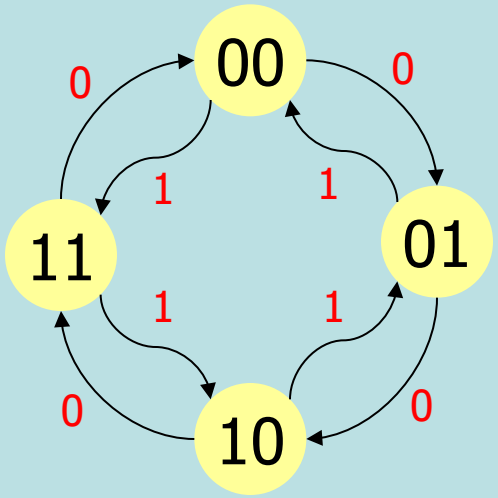
Up-Down

2-bit UP/DOWN Synchronous Counter:

D Flip-flop

- **Step 1:**
  To design 2-bit up-down synchronous counter using D flip-flop based on input X. When **X=0 → Count UP** and **X=1 → Count DOWN**

- **Step 2:**
  Given the state diagram.



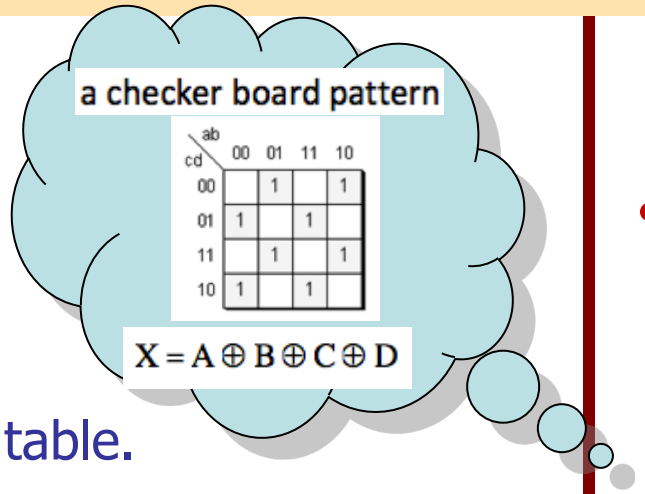
- **Step 3:** Create next state table

	Input, X	Present State		Next State	
		$Q1_n$	$Q0_n$	$Q1_{n+1}$	$Q0_{n+1}$
Count up	0	0	0	0	1
	0	0	1	1	0
	0	1	0	1	1
	0	1	1	0	0
Count down	1	0	0	1	1
	1	0	1	0	0
	1	1	0	0	1
	1	1	1	1	0

- Step 4:

  D flip-flop transition table.

Input, X	Present State		Next State		D FF	
	$Q1_n$	$Q0_n$	$Q1_{n+1}$	$Q0_{n+1}$	D1	D0
0	0	0	0	1	0	1
0	0	1	1	0	1	0
0	1	0	1	1	1	1
0	1	1	0	0	0	0
1	0	0	1	1	1	1
1	0	1	0	0	0	0
1	1	0	0	1	0	1
1	1	1	1	0	1	0



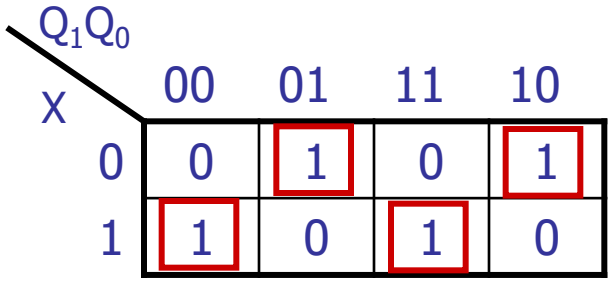
- Step 4:

  D flip-flop transition table.

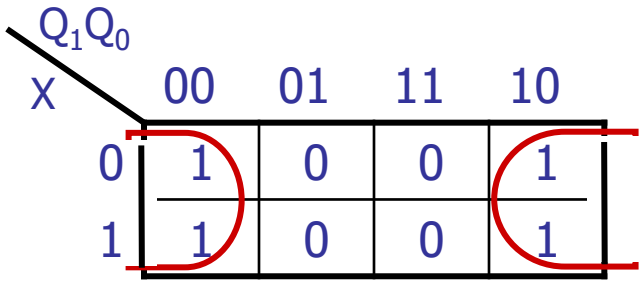
Input, X	Present State		Next State		D FF	
	$Q1_n$	$Q0_n$	$Q1_{n+1}$	$Q0_{n+1}$	D1	D0
0	0	0			0	1
0	0	1			1	0
0	1	0			1	1
0	1	1			0	0
1	0	0			1	1
1	0	1			0	0
1	1	0			0	1
1	1	1			1	0

- Step 5:

  Define logic equation. (create k-maps)



$$D_1 = X \oplus Q_1 \oplus Q_0$$



$$D_0 = \overline{Q}_0$$

Exercise 8b.10: Draw the circuit for of 2-bit up-down synchronous counter using D flip-flop with: $D_1 = X \oplus Q_1 \oplus Q_0$

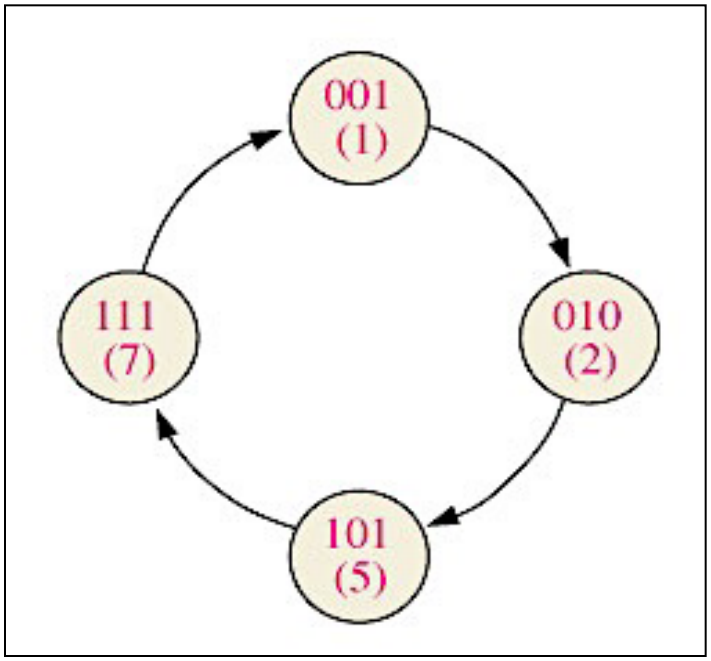
$$D_0 = \overline{Q}_0$$

Synchronous Counters:

Arbitrary Sequences || BCD Decade Counter || Cascaded Counter

Counter for Arbitrary Sequences

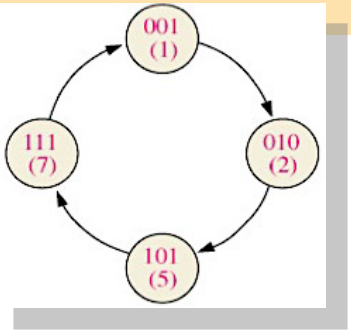
- Design the counter base on the given state diagram using T flip-flop.



- The counter is 3-bit counter
- The total number state = $2^3 = 8$

- Only 4 state (1, 2, 5, 7)
  → **Valid State**

- Other states (0, 3, 4, 6)
  → **Invalid State**
  (never occur /don't care)

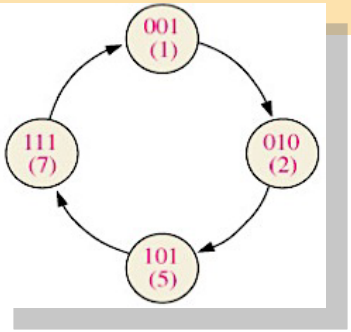


- State table and T flip-flop transition table.

Present State			Next State			T FF		
Q_{2n}	Q_{1n}	Q_{0n}	Q_{2n+1}	Q_{1n+1}	Q_{0n+1}	T_2	T_1	T_0
0	0	0	X	X	X	X	X	X
0	0	1						
0	1	0						
0	1	1	X	X	X	X	X	X
1	0	0	X	X	X	X	X	X
1	0	1						
1	1	0	X	X	X	X	X	X
1	1	1						

**Fill in the next state and T FF transition column

Q_{n+1}	T
Q_n	0
$\overline{Q_n}$	1



- State table and T flip-flop transition table.

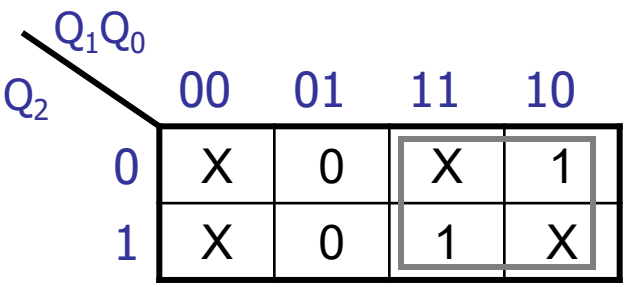
FF2 FF1 FF0

Present State			Next State			T FF		
Q_{2n}	Q_{1n}	Q_{0n}	Q_{2n+1}	Q_{1n+1}	Q_{0n+1}	T_2	T_1	T_0
0	0	0	X	X	X	X	X	X
0	0	1	0	1	0	0	1	1
0	1	0	1	0	1	1	1	1
0	1	1	X	X	X	X	X	X
1	0	0	X	X	X	X	X	X
1	0	1	1	1	1	0	1	0
1	1	0	X	X	X	X	X	X
1	1	1	0	0	1	1	1	0

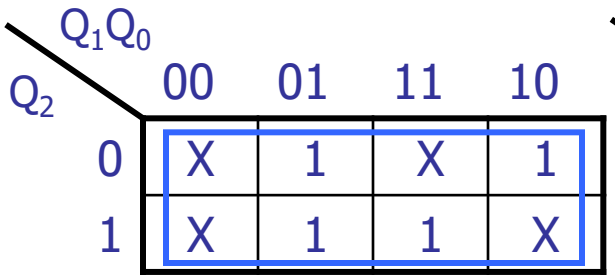
**Fill in the next state and T FF transition column

Present State			Next State			T FF		
Q_{2n}	Q_{1n}	Q_{0n}	Q_{2n+1}	Q_{1n+1}	Q_{0n+1}	T_2	T_1	T_0
0	0	0				X	X	X
0	0	1				0	1	1
0	1	0				1	1	1
0	1	1				X	X	X
1	0	0				X	X	X
1	0	1				0	1	0
1	1	0				X	X	X
1	1	1				1	1	0

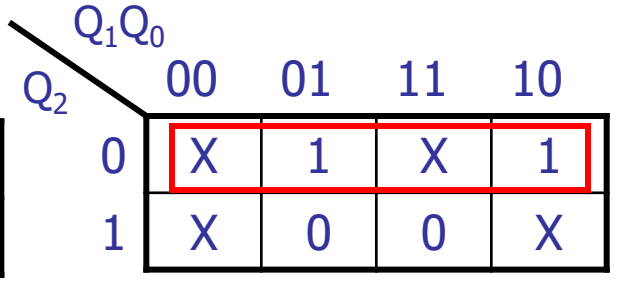
- Step 5: Create K-map to determine the Boolean expression



$$T_2 = Q_1$$

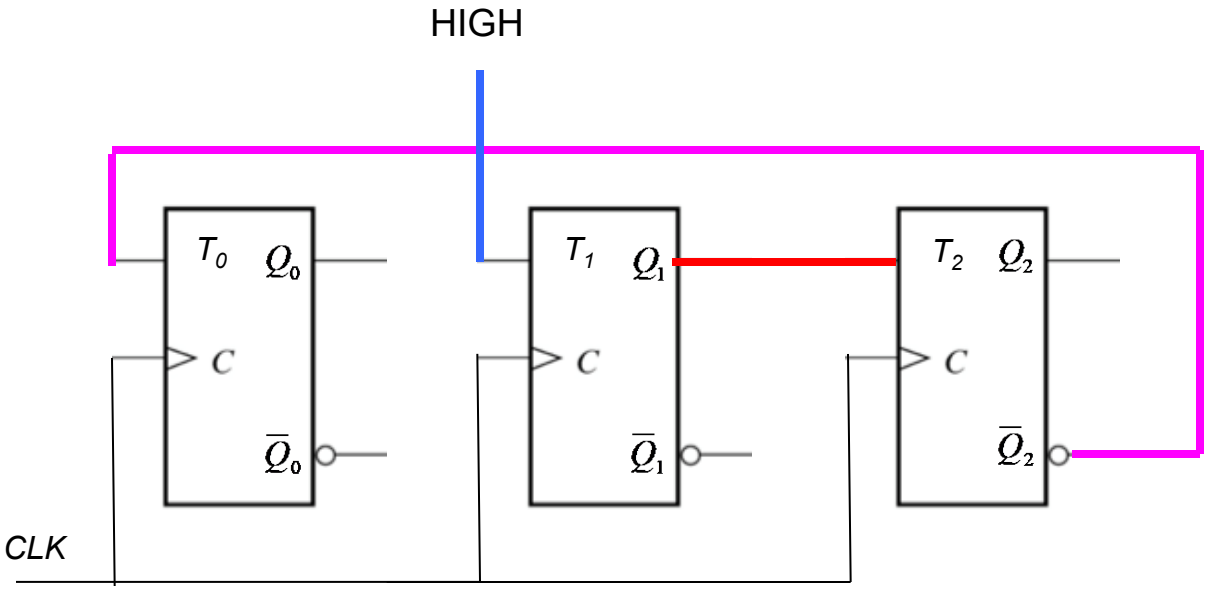


$$T_1 = 1$$



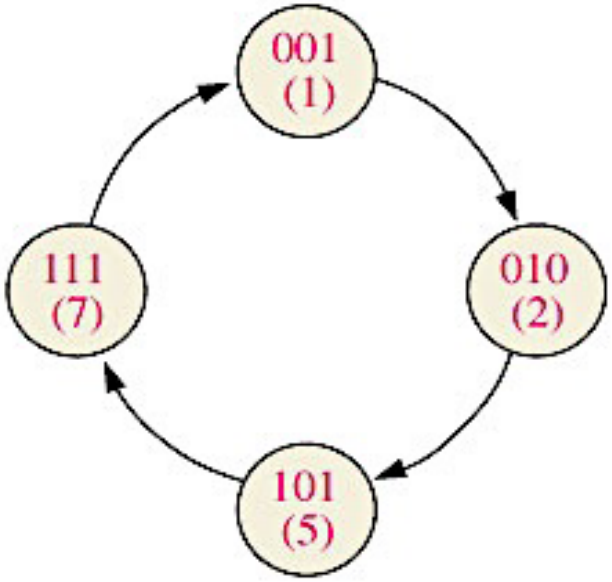
$$T_0 = \overline{Q}_2$$

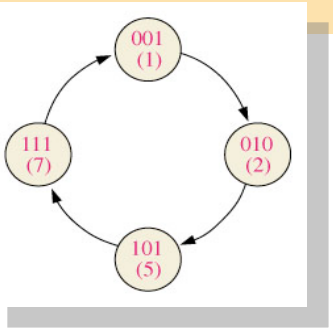
- Step 6: Draw the circuit design.



$$T_0 = \overline{Q}_2 \qquad T_1 = 1 \qquad T_2 = Q_1$$

Exercise 8b.14: Design a counter with the irregular binary count sequence as shown in the state diagram below using J-K flip-flop.





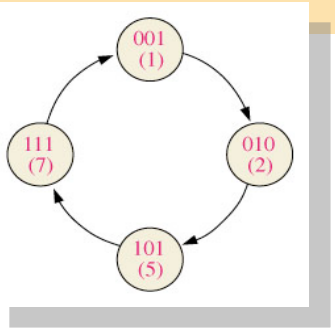
Solution 8b.14:

- Step 3 and 4: Next state table and FF transition table.

**Fill in the next state and T FF transition column

Present State			Next State			JK Transition Table					
Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	X	X	X						
0	0	1	0	1	0						
0	1	0	1	0	1						
0	1	1	X	X	X						
1	0	0	X	X	X						
1	0	1	1	1	1						
1	1	0	X	X	X						
1	1	1	0	0	1						

Present State	Next State	FF State	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



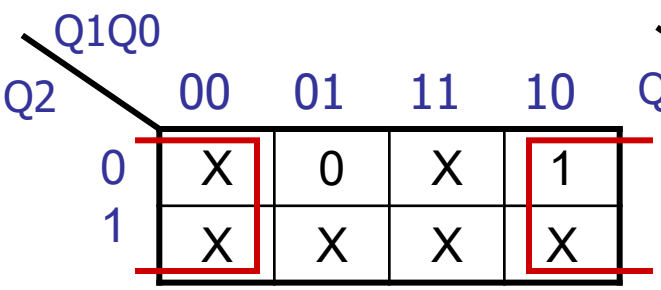
- Step 3 and 4: Next state table and FF transition table.

FF2 FF1 FF0

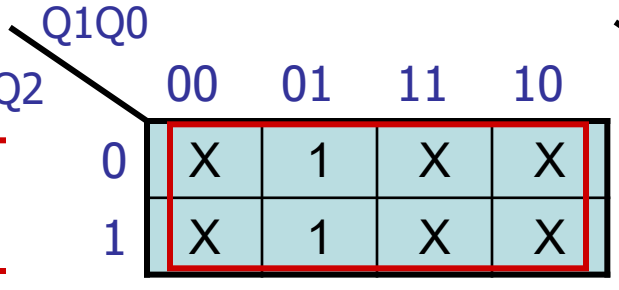
Present State			Next State			JK Transition Table					
Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	X	X	X	X	X	X	X	X	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	1	1	X	X	1	1	X
0	1	1	X	X	X	X	X	X	X	X	X
1	0	0	X	X	X	X	X	X	X	X	X
1	0	1	1	1	1	X	0	1	X	X	0
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	0	0	1	X	1	X	1	X	0

- Step 5:

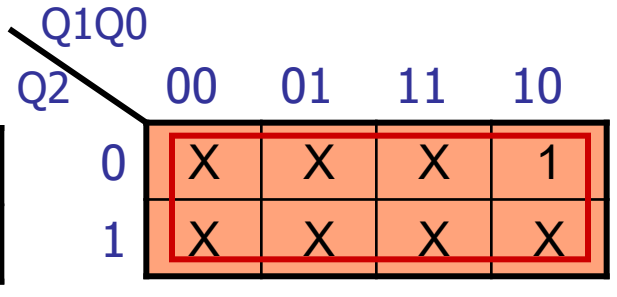
  Create K-map to determine the Boolean expression



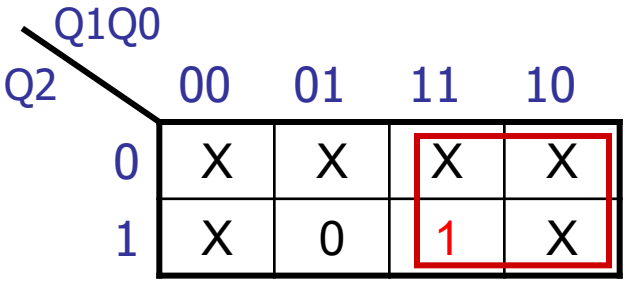
$J_2 = \overline{Q}_0$



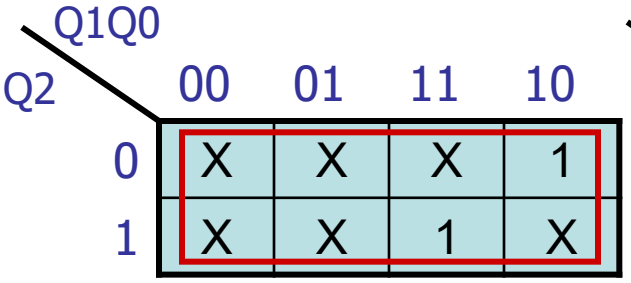
$J_1 = 1$



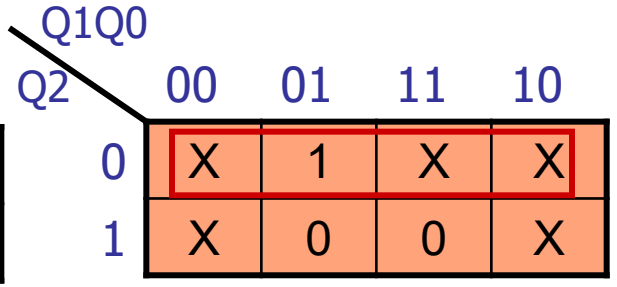
$J_0 = 1$



$K_2 = Q_1$



$K_1 = 1$

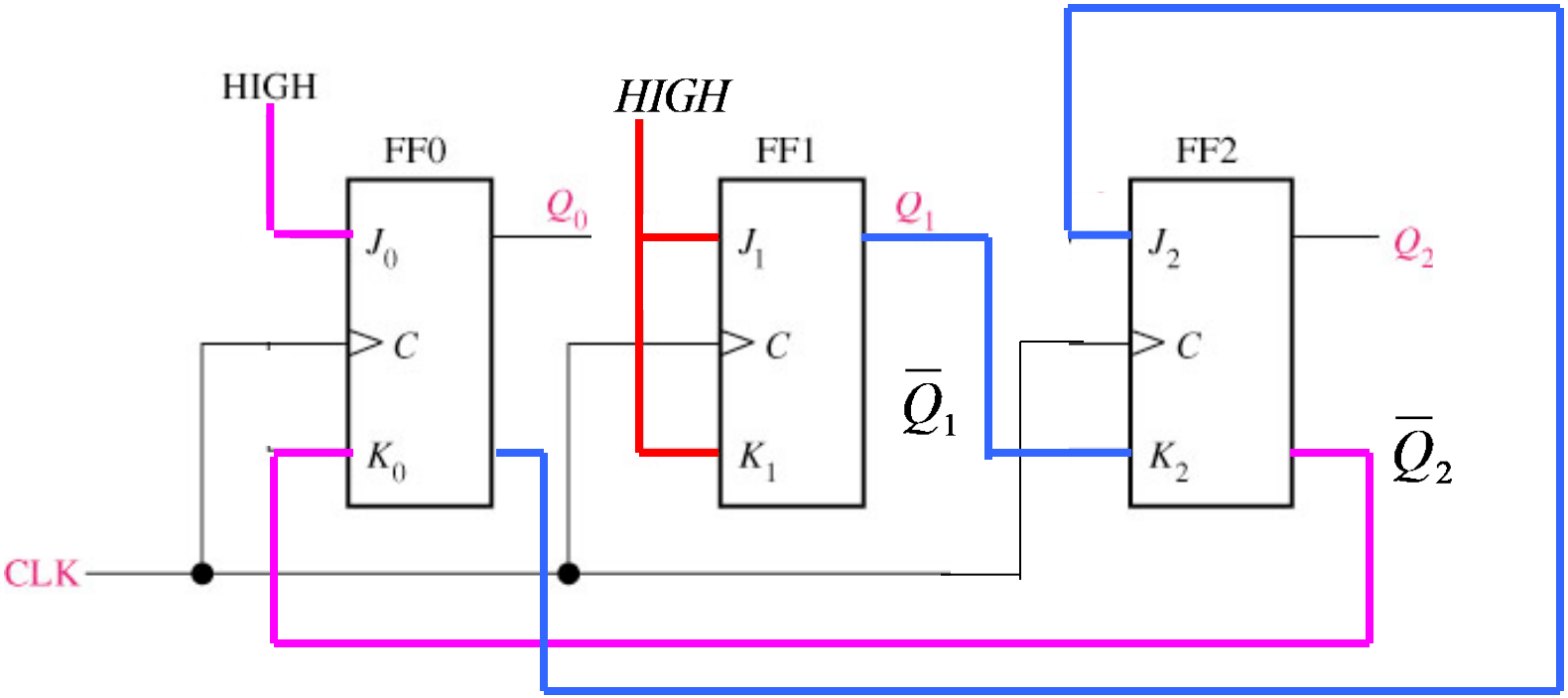


$K_0 = \overline{Q}_2$

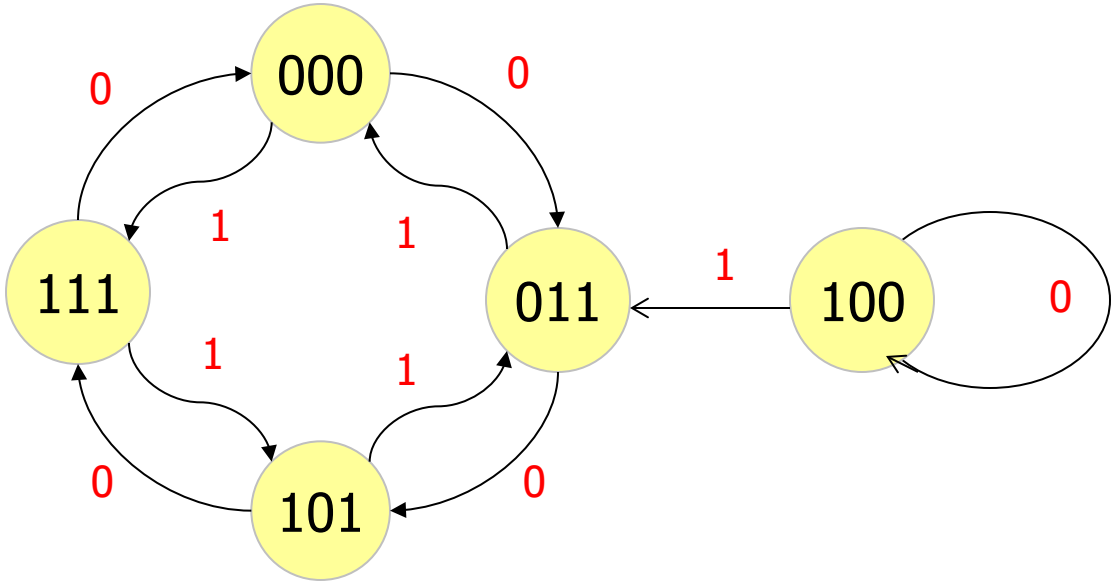
Step 6: Draw the circuit design

$$J_0 = 1 \qquad J_1 = 1 \qquad J_2 = \overline{Q}_0$$

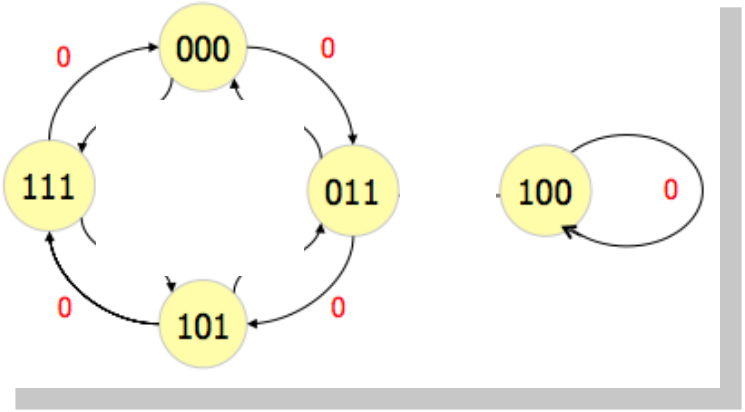
$$K_0 = \overline{Q}_2 \qquad K_1 = 1 \qquad K_2 = Q_1$$



Exercise 8b.16: Design a synchronous counter with the binary count sequence as shown in the state diagram below using J-K flip-flop.



Solutions:

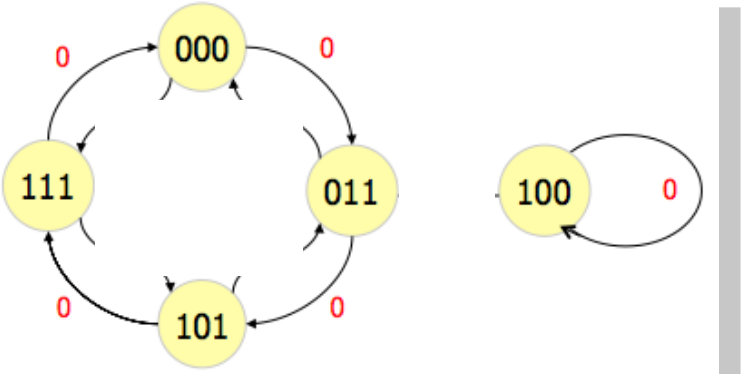


Input, X = 0

Input	Present State			Next State		
X	Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			

Solutions:

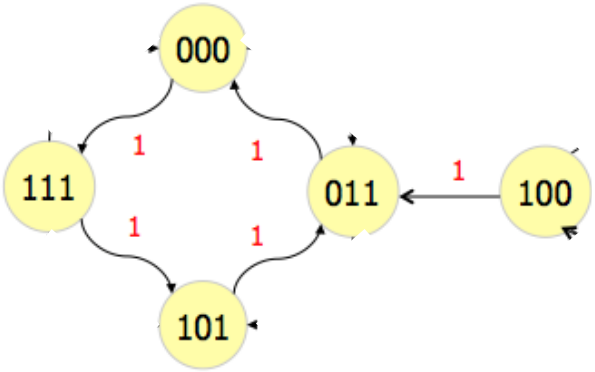
Present State	Next State	FF State	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



Input, X = 0

Input	Present State			Next State		
X	Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}
0	0	0	0	0	1	1
0	0	0	1	X	X	X
0	0	1	0	X	X	X
0	0	1	1	1	0	1
0	1	0	0	1	0	0
0	1	0	1	1	1	1
0	1	1	0	X	X	X
0	1	1	1	0	0	0

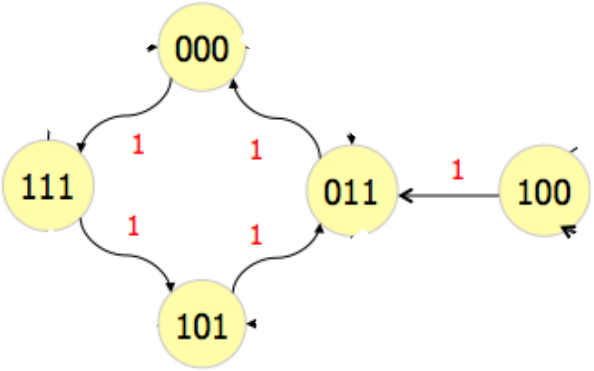
JK Transition Table					
J_2	K_2	J_1	K_1	J_0	K_0
0	X	1	X	1	X
X	X	X	X	X	X
X	X	X	X	X	X
1	X	X	1	X	0
X	0	0	X	0	X
X	0	1	X	X	0
X	X	X	X	X	X
X	1	X	1	X	1



Input, X = 1

Input	Present State			Next State		
X	Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

Present State	Next State	FF State	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



Input, X = 1

Input	Present State			Next State		
X	Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}
1	0	0	0	1	1	1
1	0	0	1	X	X	X
1	0	1	0	X	X	X
1	0	1	1	0	0	0
1	1	0	0	0	1	1
1	1	0	1	0	1	1
1	1	1	0	X	X	X
1	1	1	1	1	0	1

JK Transition Table					
J_2	K_2	J_1	K_1	J_0	K_0
1	X	1	X	1	X
X	X	X	X	X	X
X	X	X	X	X	X
0	X	X	0	X	0
X	1	1	X	1	X
X	1	1	X	X	0
X	X	X	X	X	X
X	0	X	1	X	0

Input, X = 0

Input	Present State		
X	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1

Use K-maps to derive the logic equations for each J and K.

JK Transition Table					
J_2	K_2	J_1	K_1	J_0	K_0
0	X	1	X	1	X
X	X	X	X	X	X
X	X	X	X	X	X
1	X	X	1	X	0
X	0	0	X	0	X
X	0	1	X	X	0
X	X	X	X	X	X
X	1	X	1	X	1

Input, X = 1

Input	Present State		
X	Q_2	Q_1	Q_0
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Use K-maps to derive the logic equations for each J and K.

JK Transition Table					
J_2	K_2	J_1	K_1	J_0	K_0
1	X	1	X	1	X
X	X	X	X	X	X
X	X	X	X	X	X
0	X	X	0	X	0
X	1	1	X	1	X
X	1	1	X	X	0
X	X	X	X	X	X
X	0	X	1	X	0

K-maps:

**Fill in the K-maps

XQ_2 \ Q_1Q_0	00	01	11	10
00	0	X	1	X
01	X	X	X	X
11	X	X	X	X
10	1	X	0	X

$J_2 =$

XQ_2 \ Q_1Q_0	00	01	11	10
00	1	X	X	X
01	0	1	X	X
11	1	1	X	X
10	1	X	X	X

$J_1 =$

XQ_2 \ Q_1Q_0	00	01	11	10
00	1	X	X	X
01	0	X	X	X
11	1	X	X	X
10	1	X	X	X

$J_0 =$

XQ_2 \ Q_1Q_0	00	01	11	10
00	X	X	X	X
01	0	0	1	X
11	1	1	0	X
10	X	X	X	X

$K_2 =$

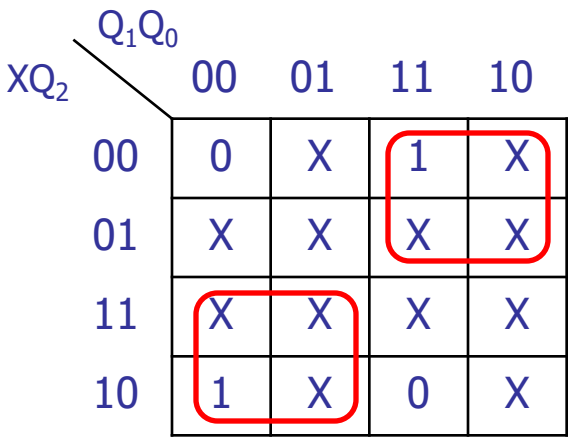
XQ_2 \ Q_1Q_0	00	01	11	10
00	X	X	1	X
01	X	X	1	X
11	X	X	1	X
10	X	X	0	X

$K_1 =$

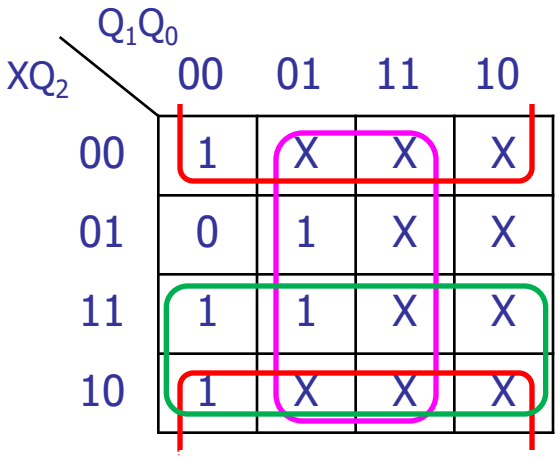
XQ_2 \ Q_1Q_0	00	01	11	10
00	X	X	0	X
01	X	0	1	X
11	X	0	0	X
10	X	X	0	X

$K_0 =$

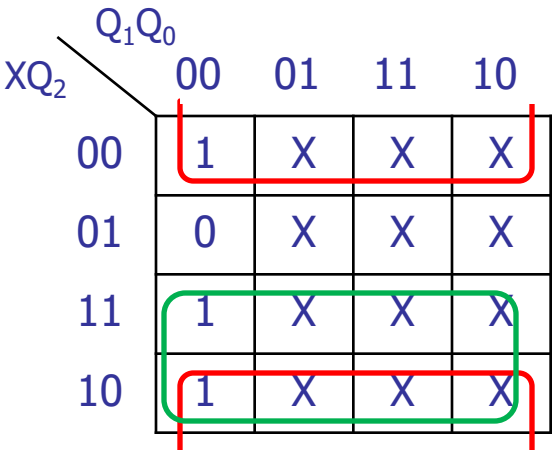
K-maps:



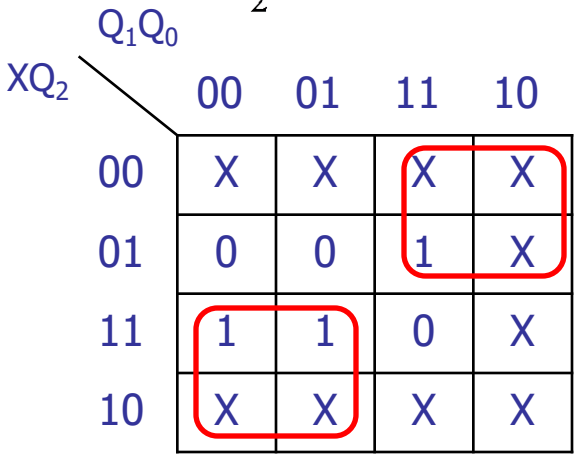
$J_2 =$



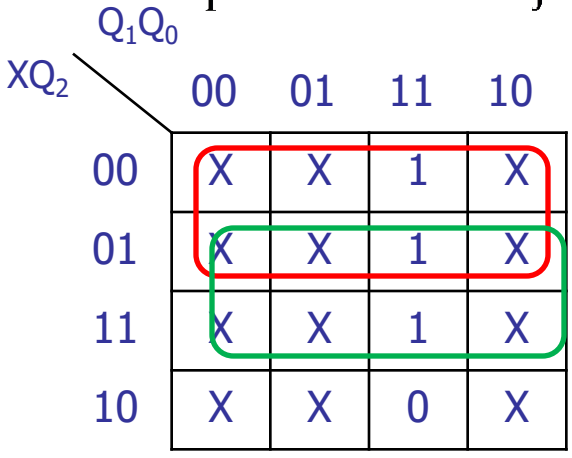
$J_1 =$



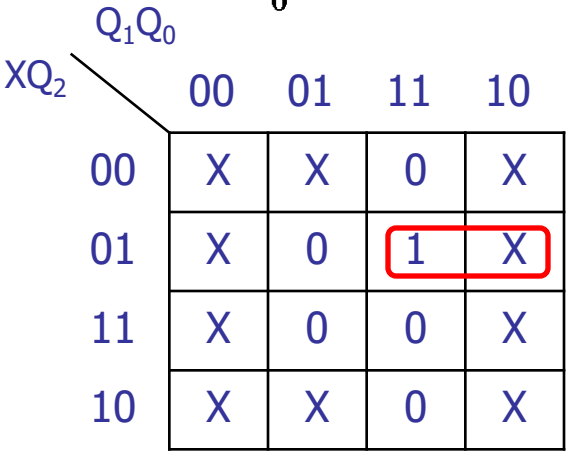
$J_0 =$



$K_2 =$

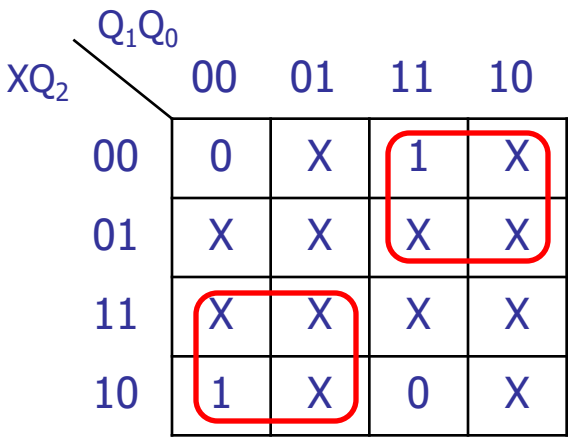


$K_1 =$

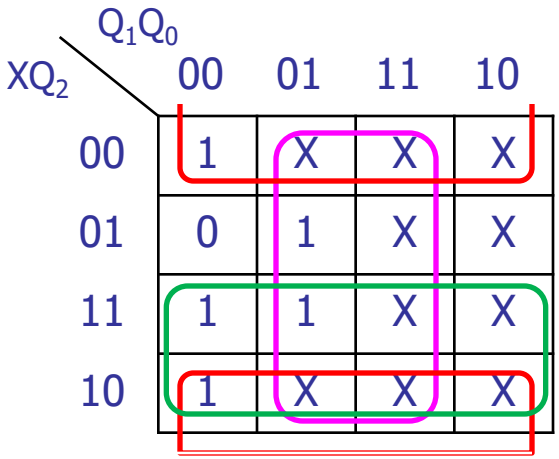


$K_0 =$

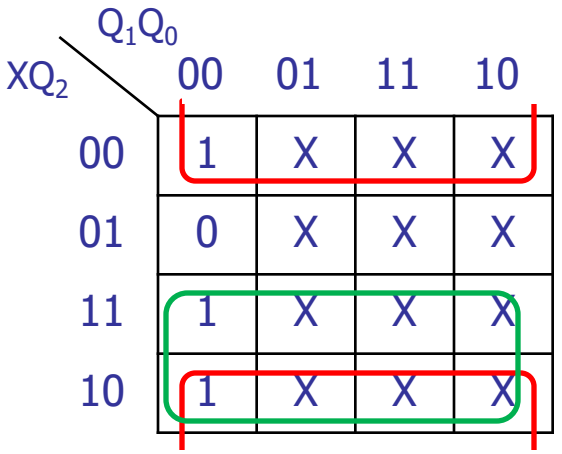
K-maps:



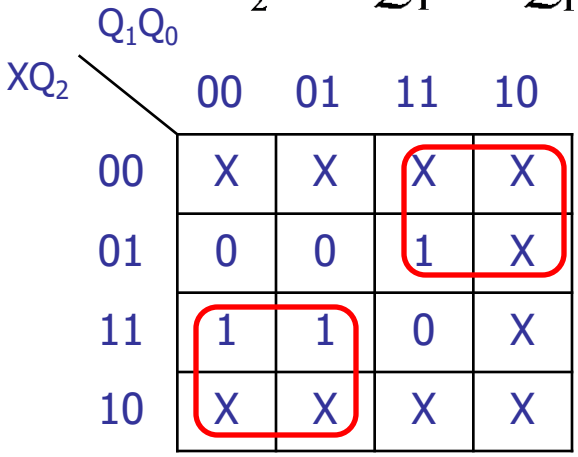
$$J_2 = X\overline{Q}_1 + \overline{X}Q_1$$



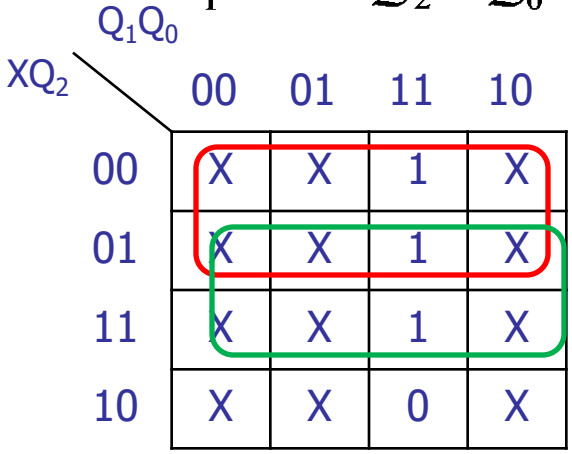
$$J_1 = X + \overline{Q}_2 + Q_0$$



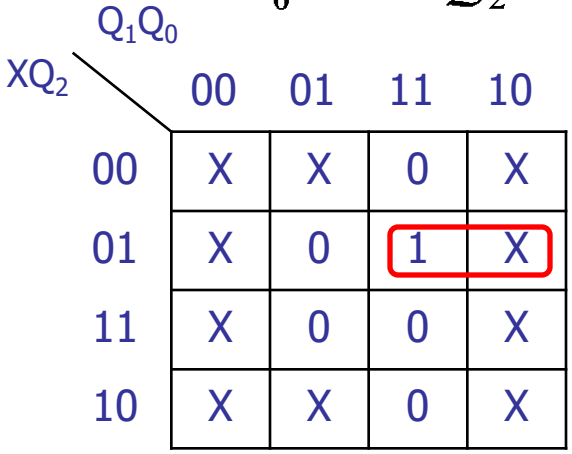
$$J_0 = X + \overline{Q}_2$$



$$K_2 = X\overline{Q}_1 + \overline{X}Q_1$$



$$K_1 = \overline{X} + Q_2$$



$$K_0 = \overline{X}Q_2Q_1$$

Draw the counter design.

FF0

$$J_0 = X + \overline{Q}_2$$

$$K_0 = \overline{X} Q_2 Q_1$$

FF1

$$J_1 = X + \overline{Q}_2 + Q_0$$

$$K_1 = \overline{X} + Q_2$$

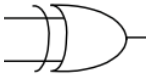
FF2

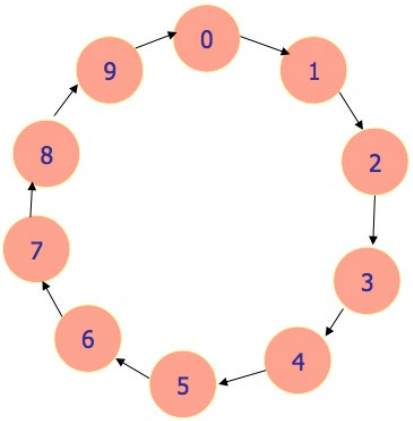
$$J_2 = X\overline{Q}_1 + \overline{X}Q_1$$

$$K_2 = X\overline{Q}_1 + \overline{X}Q_1$$

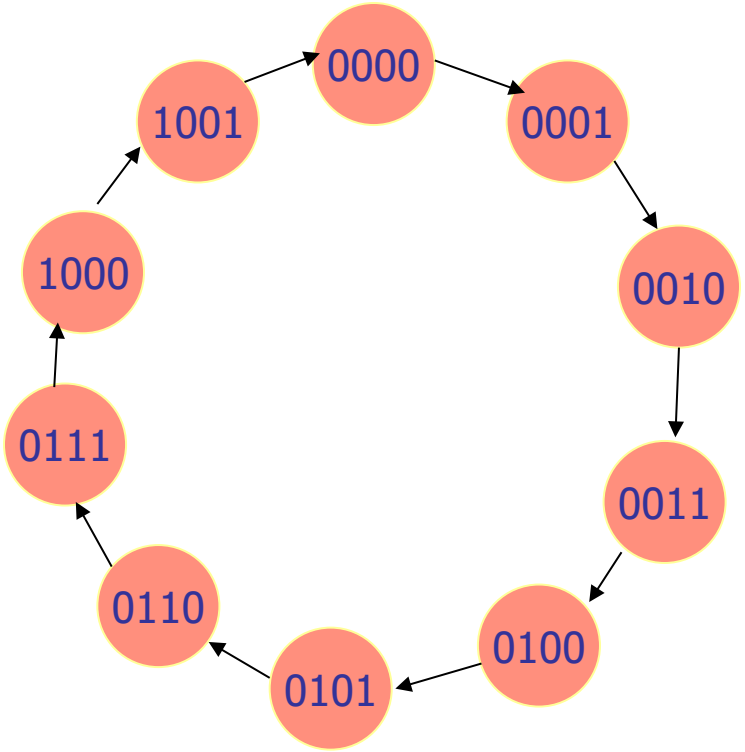
$$J_2 = K_2 = X \oplus Q_1$$

(XOR)





Synchronous BCD Decade Counter



- Synchronous decade counter counts from 0 to 9 and then recycles to 0 again.
- 4 flip-flops are required, and the unused states (10 to 15) are taken as don't care terms.

Exercise 8b.17: Draw the design a synchronous BCD decade counter using the T flip-flop.

Present State				Next State				T FF Transition			
Q_3	Q_2	Q_1	Q_0	Q_{3+}	Q_{2+}	Q_{1+}	Q_{0+}	T_3	T_2	T_1	T_0
0	0	0	0	0	0	0	1	0	0	0	**1**
0	0	0	1	0	0	1	0	0	0	1	**1**
0	0	1	0	0	0	1	1	0	0	0	**1**
0	0	1	1	0	1	0	0	0	1	1	**1**
0	1	0	0	0	1	0	1	0	0	0	**1**
0	1	0	1	0	1	1	0	0	0	1	**1**
0	1	1	0	0	1	1	1	0	0	0	**1**
0	1	1	1	1	0	0	0	1	1	1	**1**
1	0	0	0	1	0	0	1	0	0	0	**1**
1	0	0	1	0	0	0	0	1	0	0	**1**
1	0	1	0	X	X	X	X	X	X	X	**X**
1	0	1	1	X	X	X	X	X	X	X	**X**
1	1	0	0	X	X	X	X	X	X	X	**X**
1	1	0	1	X	X	X	X	X	X	X	**X**
1	1	1	0	X	X	X	X	X	X	X	**X**
1	1	1	1	X	X	X	X	X	X	X	**X**

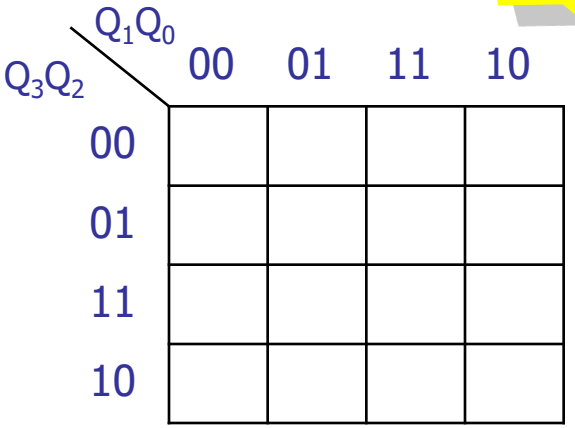
**Fill in the T0 column

Home work

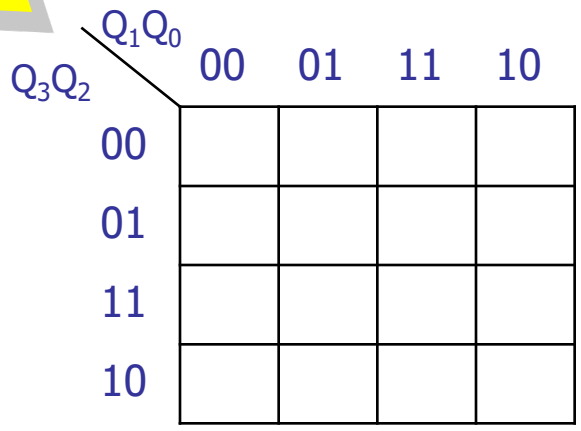
**Fill in the K-maps

Self-Test:

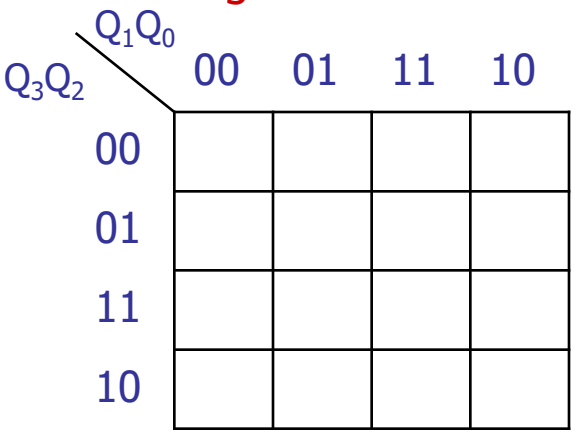
Fill in the K-map to simplify the equations.



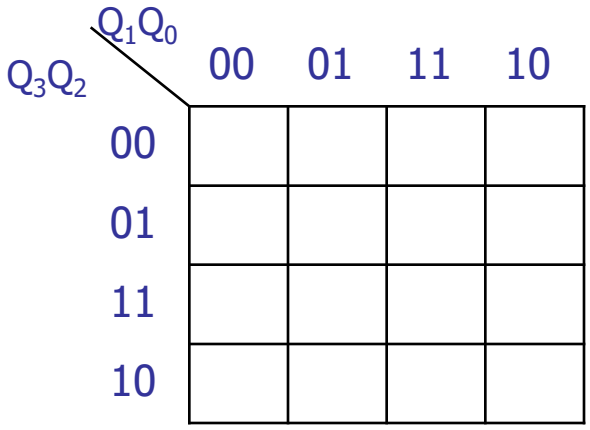
$T_3 =$



$T_2 =$



$T_1 =$



$T_0 =$

Exercise 8b.18: Design a synchronous BCD decade counter using the D flip-flop.

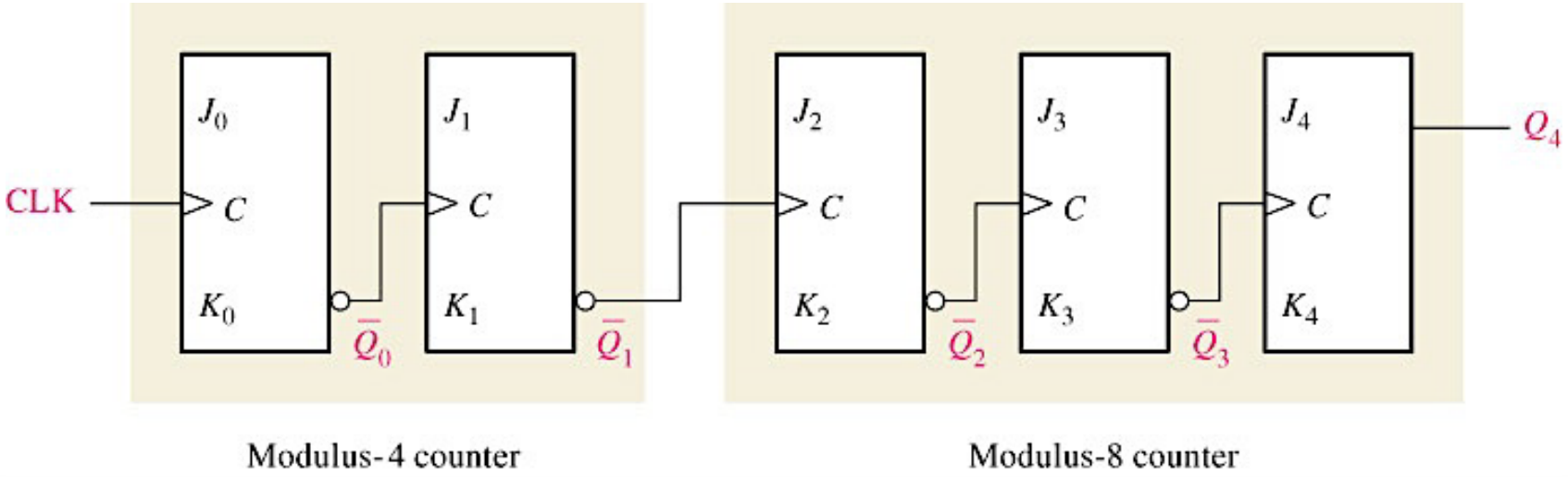
Cascaded Counter

Cascaded Counter

- Counter can be connected to achieve higher modulus operation.
- Cascading means that the last-stage output of one counter drives the input of the next counter.

Example:

- Two counters, modulus-4 and modulus-8 connected in cascade, can achieve count until 32 CLK (modulus-32). (*i.e* 4 x 8)



Recap: Modulus

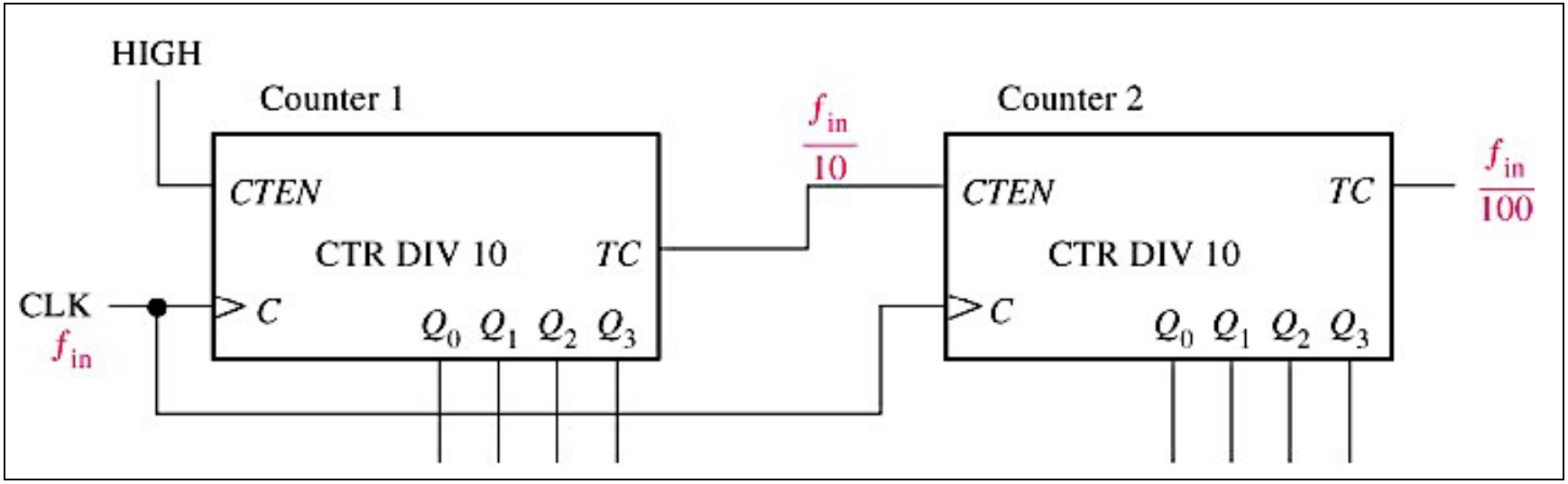
- The modulus → number of unique states through which the counter will sequence.
- Maximum possible number of states = 2^N,

  N is the number of flip-flops in the counter.
- Example : Modulus 8 = 2^3 (Need 3 flip flops)

- Counter can be designed to have less number of states in their sequence → Truncated sequence.
  - One common modulus for counters → ten (Modulus 10).
  - It called BCD decade counters (as explained in previous slides).

Cascaded Counter:
Modulus-100 Counter

- Modulus-100 counter using 2 cascaded decade counters.
- This counter can be viewed as a frequency divider.
- It divides the input clock frequency by 100.



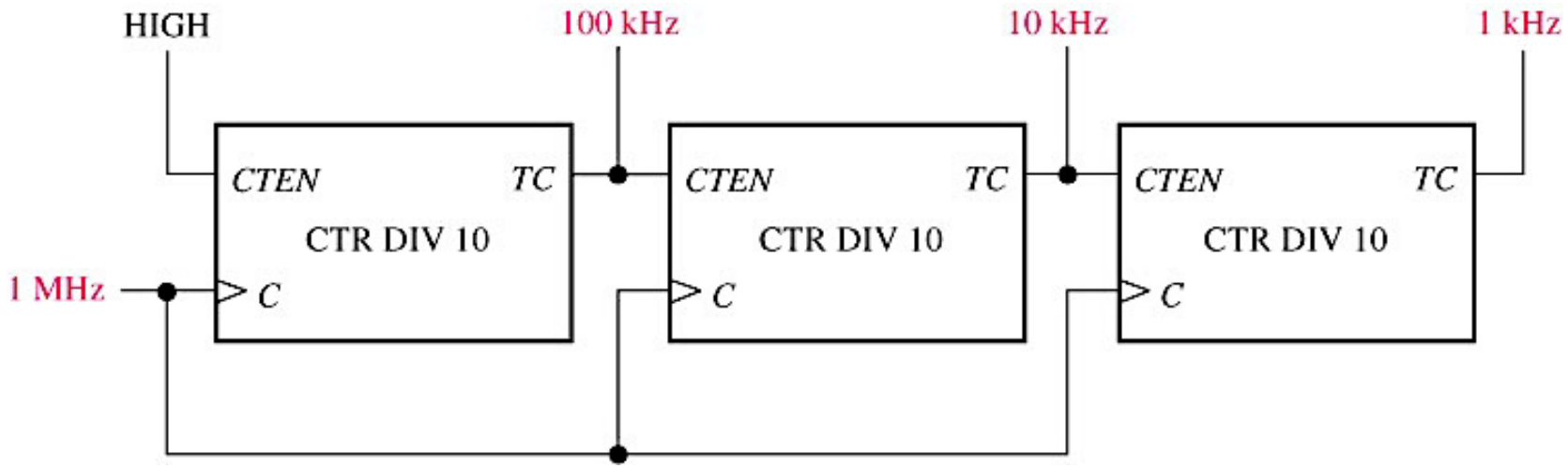
CTEN – Count Enable function
TC – Terminal Count function

(Total MOD = 10 x 10 = 100)

Cascaded Counter:

Modulus-1000 Counter

- Three cascaded decade counters forming a divide-by-1000 frequency divider.



Total MOD = 10 x 10 x 10
= 1000

Basis clock frequency of 1 MHz and you wish to obtain 100kHz, 10Hz, and 1kHz, a series of cascaded decade counters can be used.

- If 1 MHz signal is divided by 10, the output is 100kHz.
- Then if the 100 kHz signal is divided by 10, the output is 10kHz.
- Further division by 10 gives the 1 kHz frequency.

Exercise 8b.19: Two type of counters, modulus-4 and modulus-8 need to be used to achieve count up to modulus-*n* (*n* CLK).

a) How to cascade the counters to achieve count until 32 CLK (modulus-32)?
b) What is the frequency produced by each counter given an initial frequency is 800MHz?

Solutions:

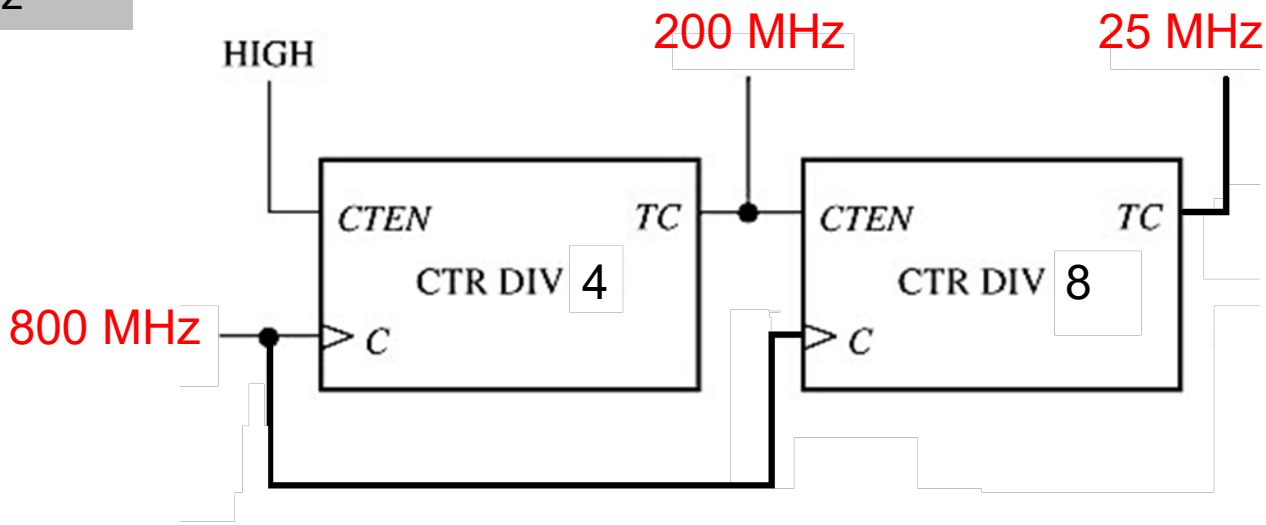
a) Modulus-4 x Modulus-8, or

Modulus-8 x Modulus-4.

b)

Modulus-4:
= 800MHz / 4
= 200MHz

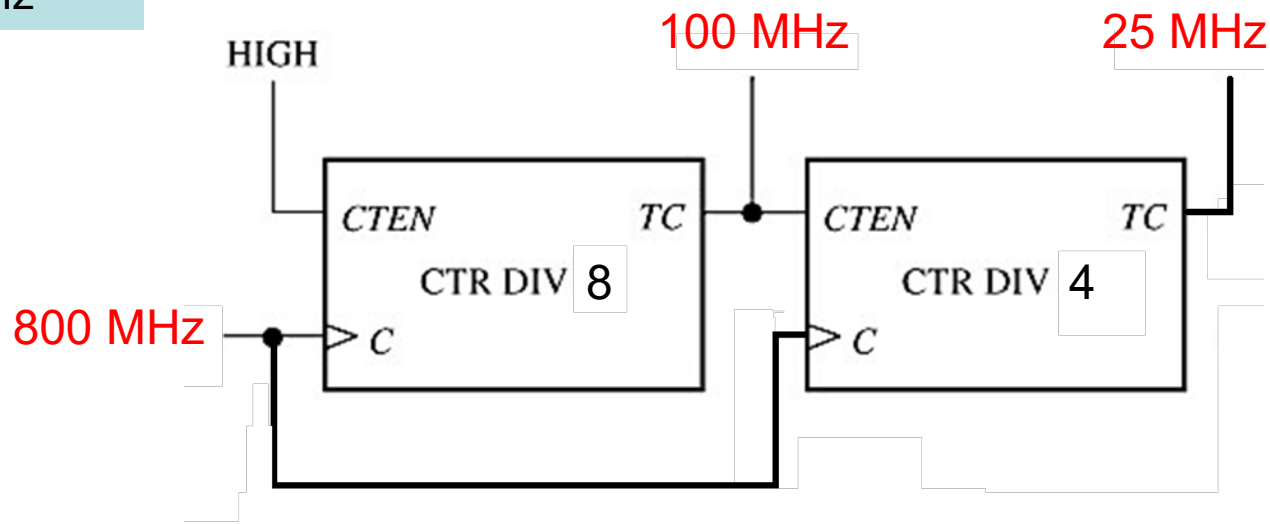
Modulus-8:
= 200MHz / 8
= 25MHz



b)

Modulus-8:
= 800MHz / 8
= 100MHz

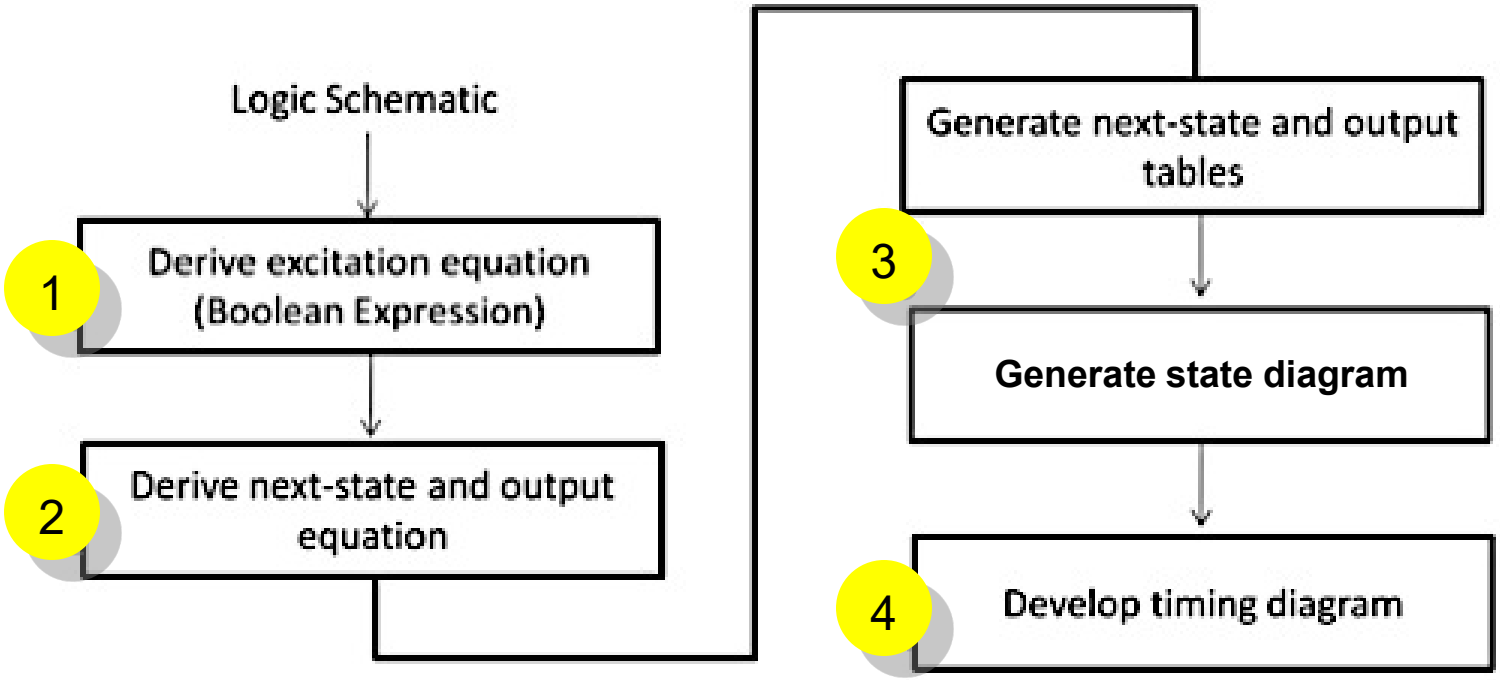
Modulus-4:
= 100MHz / 4
= 25MHz



Analysis of Sequential Circuits

Analysis of Sequential Circuits

- Behavior of a sequential circuit is determined from the inputs, the outputs and the states of its flip-flops.
- Both the output and the next state are a function of the inputs and the present state.



- Step 1:
  Start with the logic schematic from which we can derive **excitation equations** for each flip-flop input.

- Step 2:
  To obtain **next-state equations**, we insert the excitation equations into the characteristic equations. The **output equations** can be derived from the schematic:

Flip-flop characteristic equation:

active HIGH

$$JK: Q_{next} = J\overline{Q} + \overline{K}Q$$

$$D: Q_{next} = D$$

$$T: Q_{next} = T\overline{Q} + \overline{T}Q$$

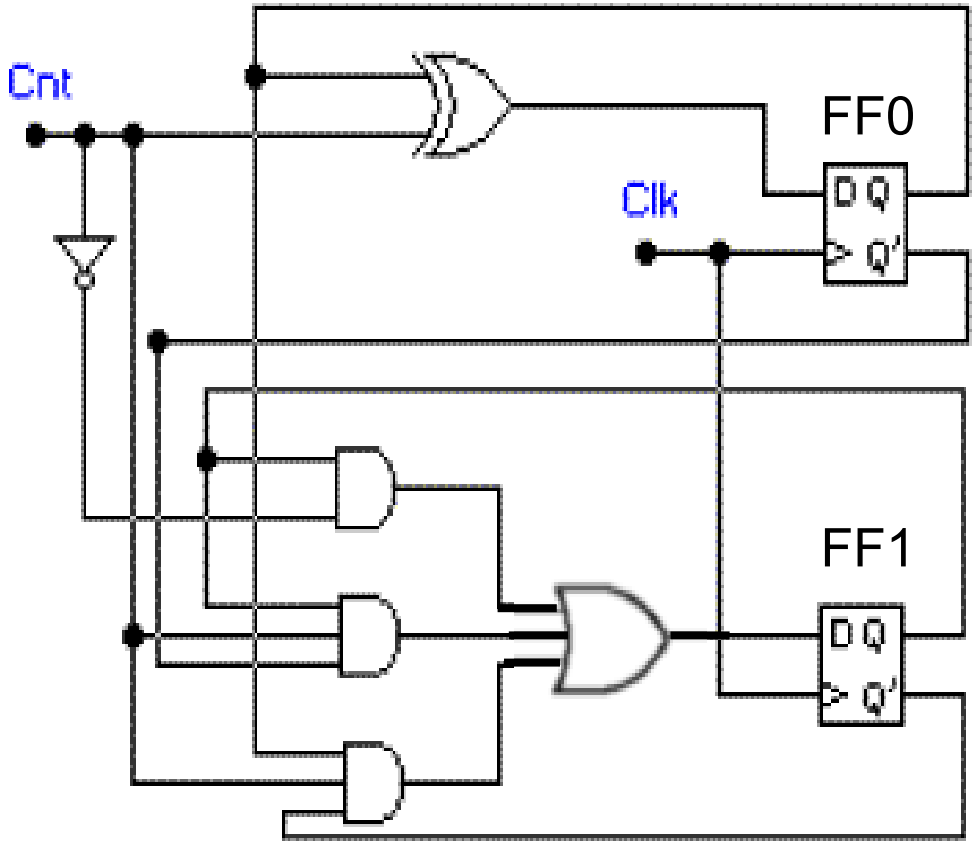
- Step 3:
  Once we have our output and next-state equations, we can generate the **next-state and output tables** as well as **state diagrams**.

- Step 4:
  When we reach this stage, we use either the table or the state diagram to develop a **timing diagram** which can be verified through simulation.

Analysis of Sequential Circuits:
Modulo-4 Counter

Example:

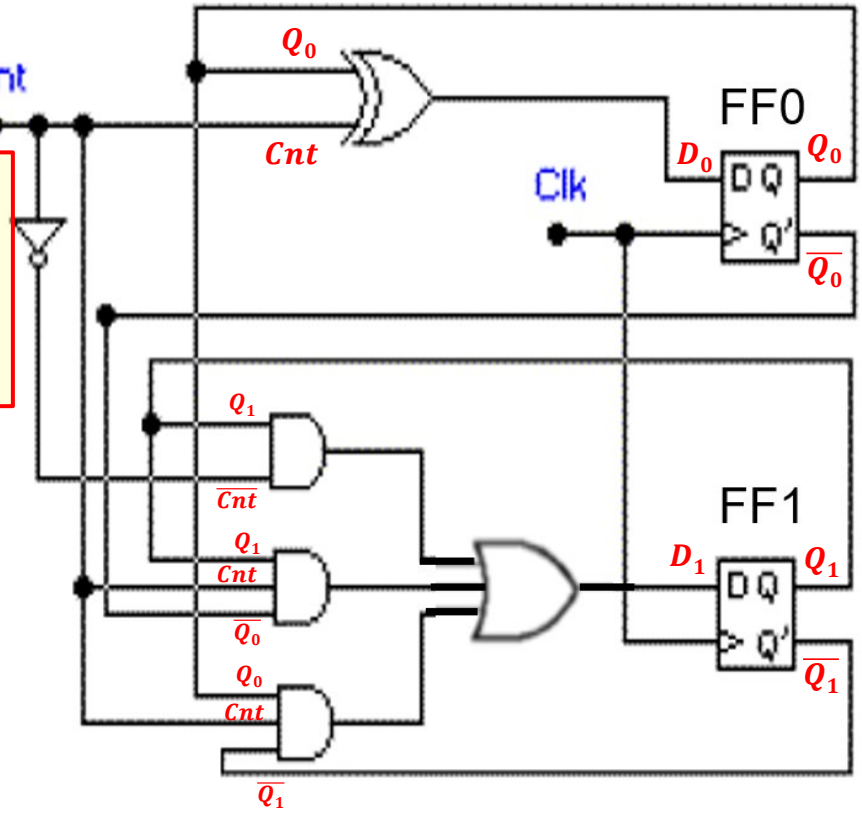
Derive the state table and state diagram for the sequential circuit below.



- Step 1: **Boolean expressions** for the inputs of each flip-flops in the schematic.

$$D_0 = Cnt \oplus Q_0 = \overline{Cnt} \cdot Q_0 + Cnt \cdot \overline{Q_0}$$

$$D_1 = \overline{Cnt} \cdot Q_1 + Cnt \cdot \overline{Q_1} \cdot Q_0 + Cnt \cdot Q_1 \cdot \overline{Q_0}$$



active HIGH

$JK: Q_{next} = JQ + KQ$

$D: Q_{next} = D$

$T: Q_{next} = T\overline{Q} + \overline{T}Q$

- Step 1: **Boolean expressions** for the inputs of each flip-flops in the schematic.

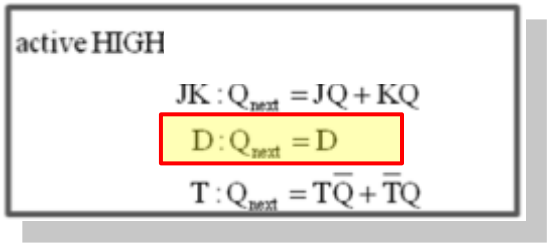
$$D_0 = Cnt \oplus Q_0 = \overline{Cnt} \cdot Q_0 + Cnt \cdot \overline{Q_0}$$

$$D_1 = \overline{Cnt} \cdot Q_1 + Cnt \cdot \overline{Q_1} \cdot Q_0 + Cnt \cdot Q_1 \cdot \overline{Q_0}$$

- Step 2: Derive the **next-state equations** by converting these excitation equations into flip-flop characteristic equations. In the case of D flip-flops, $Q_+ =$

$$Q_{0+} = D_0$$

$$Q_{1+} = D_1$$



- Step 1: **Boolean expressions** for the inputs of each flip-flops in the schematic.

$$D_0 = Cnt \oplus Q_0 = \overline{Cnt} \cdot Q_0 + Cnt \cdot \overline{Q_0}$$

$$D_1 = \overline{Cnt} \cdot Q_1 + Cnt \cdot \overline{Q_1} \cdot Q_0 + Cnt \cdot Q_1 \cdot \overline{Q_0}$$

- Step 2: Derive the **next-state equations** by converting these excitation equations into flip-flop characteristic equations. In the case of D flip-flops, $Q_+ =$

$$Q_{0_+} = D_0 = Cnt \oplus Q_0 = \overline{Cnt} \cdot Q_0 + Cnt \cdot \overline{Q_0}$$

$$Q_{1_+} = D_1 = \overline{Cnt} \cdot Q_1 + Cnt \cdot \overline{Q_1} \cdot Q_0 + Cnt \cdot Q_1 \cdot \overline{Q_0}$$

$$D_0 = Cnt \oplus Q_0 = \overline{Cnt} \cdot Q_0 + Cnt \cdot \overline{Q_0}$$

$$D_1 = \overline{Cnt} \cdot Q_1 + Cnt \cdot \overline{Q_1} \cdot Q_0 + Cnt \cdot Q_1 \cdot \overline{Q_0}$$

- Step 3:
  Construct the **next-state table**.

Input, Cnt	Present State		Next State	
	Q_1	Q_0	$Q_{1+} = D_1$	$Q_{0+} = D_0$
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

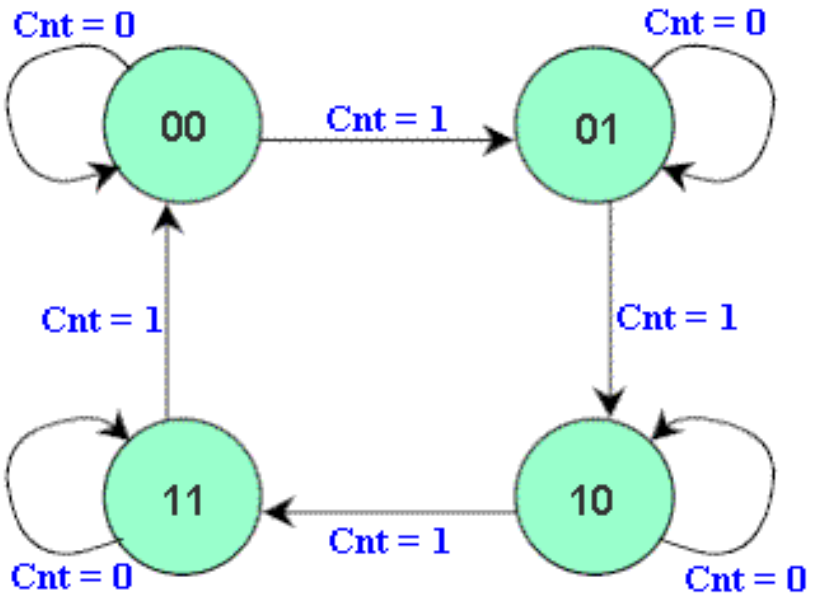
$$Q_{0_+} = D_0 = Cnt \oplus Q_0 = \overline{Cnt} \cdot Q_0 + Cnt \cdot \overline{Q_0}$$

$$Q_{1_+} = D_1 = \overline{Cnt} \cdot Q_1 + Cnt \cdot \overline{Q_1} \cdot Q_0 + Cnt \cdot Q_1 \cdot \overline{Q_0}$$

- Step 3:
  Construct the **next-state table**.

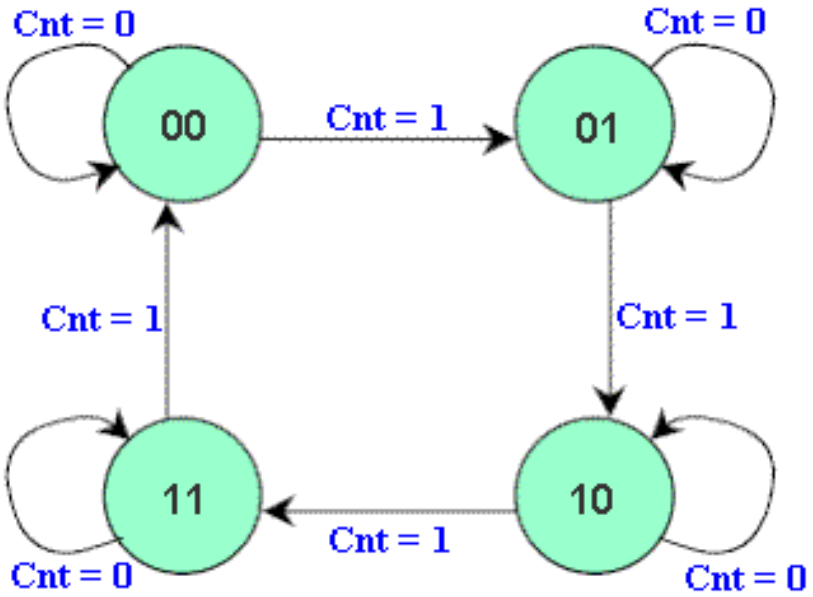
Input, Cnt	Present State		Next State	
	Q_1	Q_0	$Q_{1+} = D_1$	$Q_{0+} = D_0$
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	0

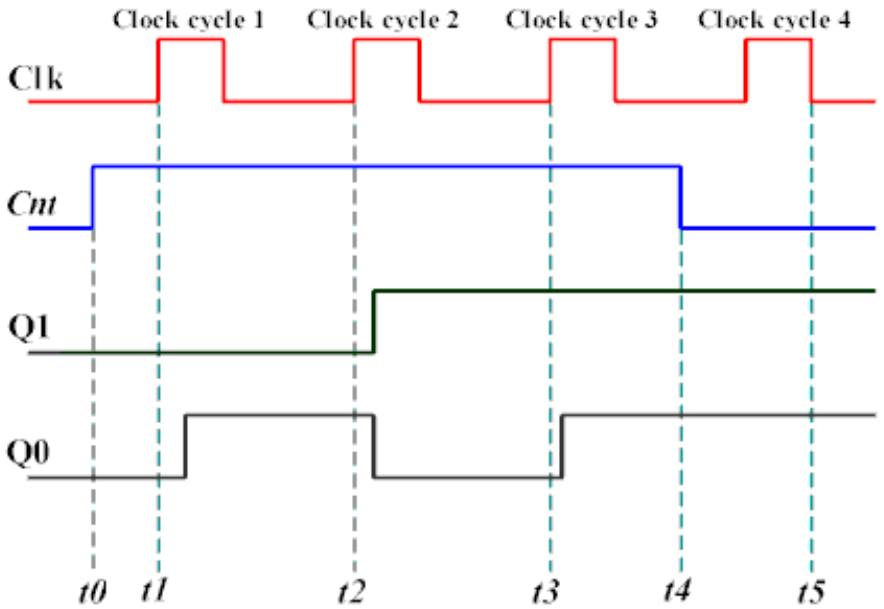
- Step 4:
- The **state diagram** is generated directly from the next-state table.



Input, Cnt	Present State		Next State	
	Q_1	Q_0	$Q_{1+} = D_1$	$Q_{0+} = D_0$
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	0

- Step 4:
- The **state diagram** is generated directly from the next-state table.
- Next get the **timing diagram**





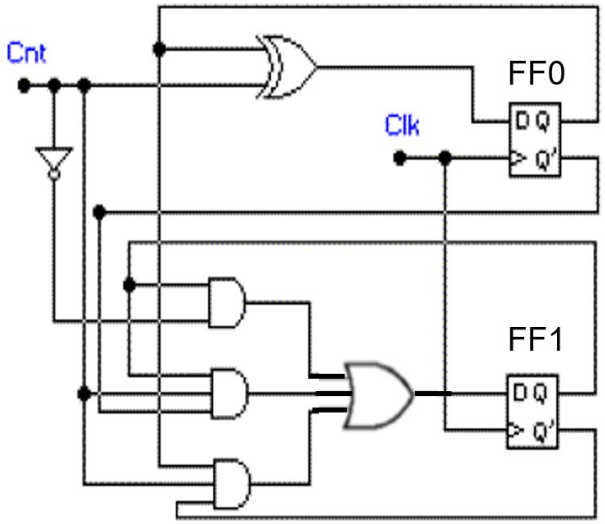
We can conclude:

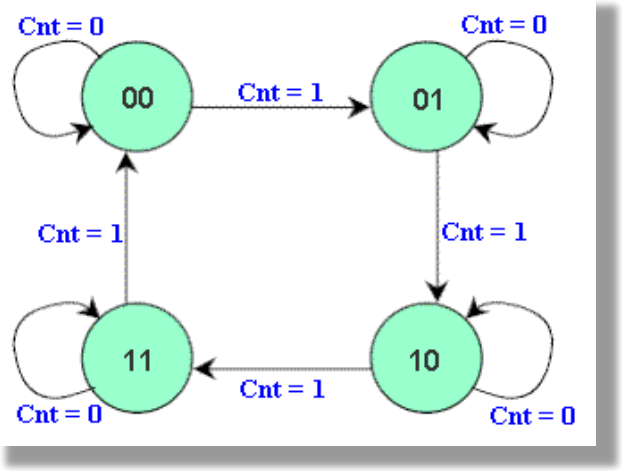
a) From the counter circuit:

- 2- bit counter because there are 2 FFs in the design.
- Sycnhronous counter because the FFs have a common clock.

b) From the counter state diagram:

- MOD 4 because has 4 state (i.e. $2^2=4$), not a truncated counter.
- Count Up counter when Cnt=1, and stay in the previous state when Cnt=0.



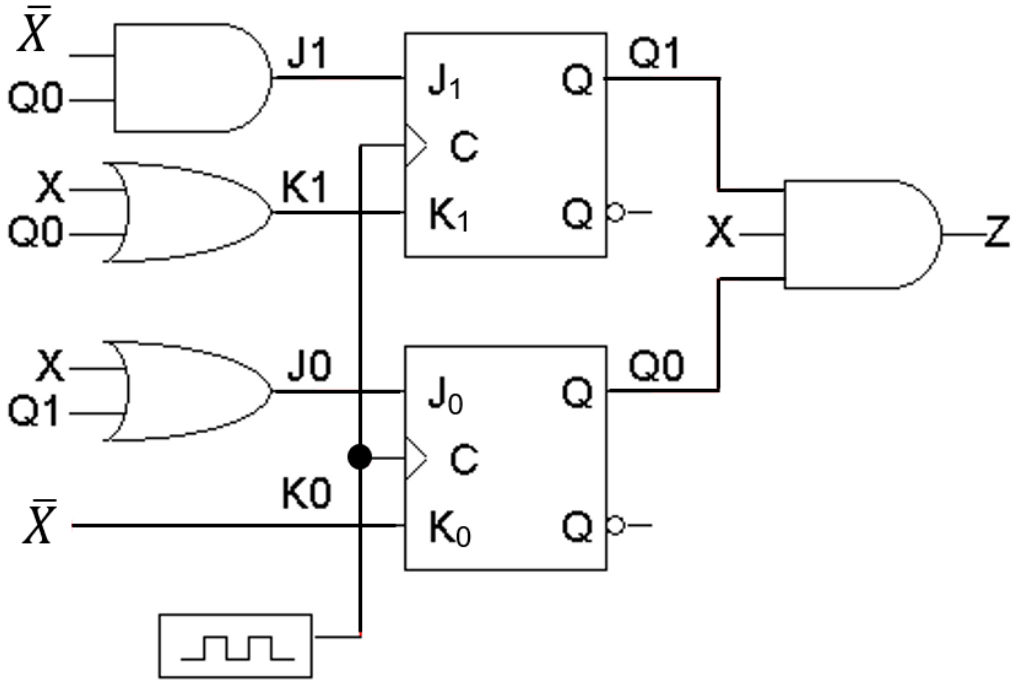


Analysis of Sequential Circuits:

JK Circuit Analysis

Assume:

- Sequential circuit with two JK flip-flops.
- There is one input, X, and one output, Z.



$$J_1 = \bar{X}Q_0 \qquad J_0 = X + Q_1 \qquad Z = Q_1Q_0X$$

$$K_1 = X + Q_0 \qquad K_0 = \bar{X}$$

- Remember that there is one input X, one output Z, and two flip-flops Q_1Q_0.
- The present state Q_1Q_0 and the input will determine the next state and the output.
- From the diagram, $Z = Q_1Q_0X$

Input, X	Present State		Next State		Output, Z
	Q_1	Q_0	Q_{1+}	Q_{0+}	
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

**Fill in the Z

- Remember that there is one input X, one output Z, and two flip-flops Q_1Q_0.
- The present state Q_1Q_0 and the input will determine the next state and the output.
- From the diagram, $Z = Q_1Q_0X$

Input, X	Present State		Next State		Output, Z
	Q_1	Q_0	Q_{1+}	Q_{0+}	
0	0	0			0
0	0	1			0
0	1	0			0
0	1	1			0
1	0	0			0
1	0	1			0
1	1	0			0
1	1	1			1

**Fill in the Z

$J_1 = \bar{X}Q_0 \qquad J_0 = X + Q_1 \qquad Z = Q_1Q_0X$

$K_1 = X + Q_0 \qquad K_0 = \bar{X}$

active HIGH SR : $Q_{next} = S + \bar{R}Q, SR = 0$

JK : $Q_{next} = J\bar{Q} + \bar{K}Q$

D : $Q_{next} = D$

T : $Q_{next} = T\bar{Q} + \bar{T}Q$

$$Q_{0_+} = J_0\overline{Q_0} + \overline{K_0}Q_0 = (X + Q_1)\overline{Q_0} + \bar{\bar{X}}Q_0 = X\overline{Q_0} + Q_1\overline{Q_0} + XQ_0$$

$$Q_{1_+} = J_1\overline{Q_1} + \overline{K_1}Q_1 = (\bar{X}Q_0)\overline{Q_1} + (\overline{X + Q_0})Q_1 = \bar{X}Q_0\overline{Q_1} + (\bar{X}\,\overline{Q_0})Q_1 = \bar{X}Q_0\overline{Q_1} + \bar{X}\,\overline{Q_0}\,Q_1$$

$$= \bar{X}(Q_0\overline{Q_1} + \overline{Q_0}\,Q_1)$$

Input, X	Present State		Next State		Output, Z
	Q_1	Q_0	Q_{1+}	Q_{0+}	
0	0	0			0
0	0	1			0
0	1	0			0
0	1	1			0
1	0	0			0
1	0	1			0
1	1	0			0
1	1	1			1

**Fill in the next state column

active HIGH SR : $Q_{next} = S + \overline{R}Q, SR = 0$

JK : $Q_{next} = J\overline{Q} + \overline{K}Q$

D : $Q_{next} = D$

T : $Q_{next} = T\overline{Q} + \overline{T}Q$

$$Q_{0_+} = X\overline{Q_0} + Q_1\overline{Q_0} + XQ_0$$

$$Q_{1_+} = \bar{X}(Q_0\overline{Q_1} + \overline{Q_0}\,Q_1)$$

Input, X	Present State		Next State		Output, Z
	Q_1	Q_0	Q_{1+}	Q_{0+}	
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	1	1	0
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	1	1

**Fill in the next state column

Method 2 –

- Fill up JK input values based on input equations
- Fill up Next State columns by observing JK input values

$$J_1 = \bar{X}Q_0 \qquad J_0 = X + Q_1 \qquad Z = Q_1Q_0X$$

$$K_1 = X + Q_0 \qquad K_0 = \bar{X}$$

Input, X	Present State		Next State		J1	K1	J0	K0	Output, Z
	Q_1	Q_0	Q_{1+}	Q_{0+}					
0	0	0							0
0	0	1							0
0	1	0							0
0	1	1							0
1	0	0							0
1	0	1							0
1	1	0							0
1	1	1							1

Method 2 –

- Fill up JK input values based on input equations
- Fill up Next State columns by observing JK input values

$$J_1 = \bar{X}Q_0 \qquad J_0 = X + Q_1 \qquad Z = Q_1Q_0X$$

$$K_1 = X + Q_0 \qquad K_0 = \bar{X}$$

Input, X	Present State		Next State		J1	K1	J0	K0	Output, Z
	Q_1	Q_0	Q_{1+}	Q_{0+}					
0	0	0			**0**				0
0	0	1			**1**				0
0	1	0			**0**				0
0	1	1			**1**				0
1	0	0			**0**				0
1	0	1			**0**				0
1	1	0			**0**				0
1	1	1			**0**				1

Method 2 –

- **Fill up JK input values based on input equations**
- **Fill up Next State columns by observing JK input values**

$$J_1 = \bar{X}Q_0 \qquad J_0 = X + Q_1 \qquad Z = Q_1Q_0X$$

$$K_1 = X + Q_0 \qquad K_0 = \bar{X}$$

Input, X	Present State		Next State		J1	K1	J0	K0	Output, Z
	Q_1	Q_0	Q_{1+}	Q_{0+}					
0	0	0			0	**0**			0
0	0	1			1	**1**			0
0	1	0			0	**0**			0
0	1	1			1	**1**			0
1	0	0			0	**1**			0
1	0	1			0	**1**			0
1	1	0			0	**1**			0
1	1	1			0	**1**			1

Method 2 –

- **Fill up JK input values based on input equations**
- **Fill up Next State columns by observing JK input values**

$$J_1 = \bar{X}Q_0 \qquad J_0 = X + Q_1 \qquad Z = Q_1Q_0X$$

$$K_1 = X + Q_0 \qquad K_0 = \bar{X}$$

Input, X	Present State		Next State		J1	K1	J0	K0	Output, Z
	Q_1	Q_0	Q_{1+}	Q_{0+}					
0	0	0			0	0	**0**		0
0	0	1			1	1	**0**		0
0	1	0			0	0	**1**		0
0	1	1			1	1	**1**		0
1	0	0			0	1	**1**		0
1	0	1			0	1	**1**		0
1	1	0			0	1	**1**		0
1	1	1			0	1	**1**		1

Method 2 –

- **Fill up JK input values based on input equations**
- **Fill up Next State columns by observing JK input values**

$$J_1 = \bar{X}Q_0 \qquad J_0 = X + Q_1 \qquad Z = Q_1Q_0X$$

$$K_1 = X + Q_0 \qquad K_0 = \bar{X}$$

Input, X	Present State		Next State		J1	K1	J0	K0	Output, Z
	Q_1	Q_0	Q_{1+}	Q_{0+}					
0	0	0			0	0	0	1	0
0	0	1			1	1	0	1	0
0	1	0			0	0	1	1	0
0	1	1			1	1	1	1	0
1	0	0			0	1	1	0	0
1	0	1			0	1	1	0	0
1	1	0			0	1	1	0	0
1	1	1			0	1	1	0	1

Method 2 –

- **Fill up JK input values based on input equations**
- **Fill up Next State columns by observing JK input values**

$$J_1 = \bar{X}Q_0 \qquad J_0 = X + Q_1 \qquad Z = Q_1Q_0X$$

$$K_1 = X + Q_0 \qquad K_0 = \bar{X}$$

Input, X	Present State		Next State		J1	K1	J0	K0	Output, Z
	Q_1	Q_0	Q_{1+}	Q_{0+}					
0	0	0			0	0	0	1	0
0	0	1			1	1	0	1	0
0	1	0			0	0	1	1	0
0	1	1			1	1	1	1	0
1	0	0			0	1	1	0	0
1	0	1			0	1	1	0	0
1	1	0			0	1	1	0	0
1	1	1			0	1	1	0	1

Method 2 –

- Fill up JK input values based on input equations
- Fill up Next State columns by observing JK input values

$$J_1 = \bar{X}Q_0 \qquad J_0 = X + Q_1 \qquad Z = Q_1Q_0X$$

$$K_1 = X + Q_0 \qquad K_0 = \bar{X}$$

Input, X	Present State		Next State		J1	K1	J0	K0	Output, Z
	Q_1	Q_0	Q_{1+}	Q_{0+}					
0	0	0	0	0	**0**	**0**	0	1	0
0	0	1	1	0	**1**	**1**	0	1	0
0	1	0	1	1	**0**	**0**	1	1	0
0	1	1	0	0	**1**	**1**	1	1	0
1	0	0	0	1	**0**	**1**	1	0	0
1	0	1	0	1	**0**	**1**	1	0	0
1	1	0	0	1	**0**	**1**	1	0	0
1	1	1	0	1	**0**	**1**	1	0	1

Method 2 –

- **Fill up JK input values based on input equations**
- **Fill up Next State columns by observing JK input values**

$$J_1 = \bar{X}Q_0 \qquad J_0 = X + Q_1 \qquad Z = Q_1Q_0X$$

$$K_1 = X + Q_0 \qquad K_0 = \bar{X}$$

Input, X	Present State		Next State		J1	K1	J0	K0	Output, Z
	Q_1	Q_0	Q_{1+}	Q_{0+}					
0	0	0	0	0	0	0	0	1	0
0	0	1	1	0	1	1	0	1	0
0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0
1	0	1	0	1	0	1	1	0	0
1	1	0	0	1	0	1	1	0	0
1	1	1	0	1	0	1	1	0	1

Method 2 –

- **Fill up JK input values based on input equations**
- **Fill up Next State columns by observing JK input values**

$$J_1 = \bar{X}Q_0 \qquad J_0 = X + Q_1 \qquad Z = Q_1Q_0X$$

$$K_1 = X + Q_0 \qquad K_0 = \bar{X}$$

Input, X	Present State		Next State		J1	K1	J0	K0	Output, Z
	Q_1	Q_0	Q_{1+}	Q_{0+}					
0	0	0	0	0	0	0	**0**	**1**	0
0	0	1	1	0	1	1	**0**	**1**	0
0	1	0	1	1	0	0	**1**	**1**	0
0	1	1	0	0	1	1	**1**	**1**	0
1	0	0	0	1	0	1	**1**	**0**	0
1	0	1	0	1	0	1	**1**	**0**	0
1	1	0	0	1	0	1	**1**	**0**	0
1	1	1	0	1	0	1	**1**	**0**	1

Method 2 –

- Fill up JK input values based on input equations
- Fill up Next State columns by observing JK input values

$$J_1 = \bar{X}Q_0 \qquad J_0 = X + Q_1 \qquad Z = Q_1Q_0X$$

$$K_1 = X + Q_0 \qquad K_0 = \bar{X}$$

Input, X	Present State		Next State		J1	K1	J0	K0	Output, Z
	Q_1	Q_0	Q_{1+}	Q_{0+}					
0	0	0	0	0	0	0	0	1	0
0	0	1	1	0	1	1	0	1	0
0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0
1	0	1	0	1	0	1	1	0	0
1	1	0	0	1	0	1	1	0	0
1	1	1	0	1	0	1	1	0	1

Method 2 –

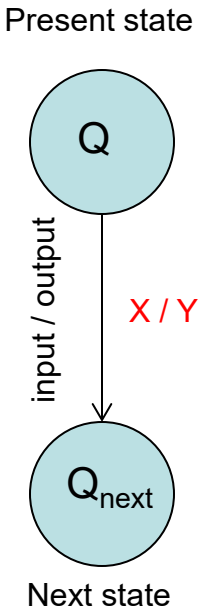
- Fill up JK input values based on input equations
- Fill up Next State columns by observing JK input values

$$J_1 = \bar{X}Q_0 \qquad J_0 = X + Q_1 \qquad Z = Q_1Q_0X$$

$$K_1 = X + Q_0 \qquad K_0 = \bar{X}$$

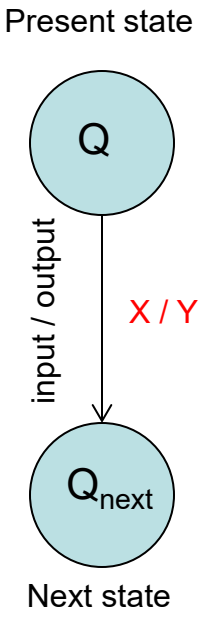
Input, X	Present State		Next State		J1	K1	J0	K0	Output, Z
	Q_1	Q_0	Q_{1+}	Q_{0+}					
0	0	0	0	0	0	0	0	1	0
0	0	1	1	0	1	1	0	1	0
0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0
1	0	1	0	1	0	1	1	0	0
1	1	0	0	1	0	1	1	0	0
1	1	1	0	1	0	1	1	0	1

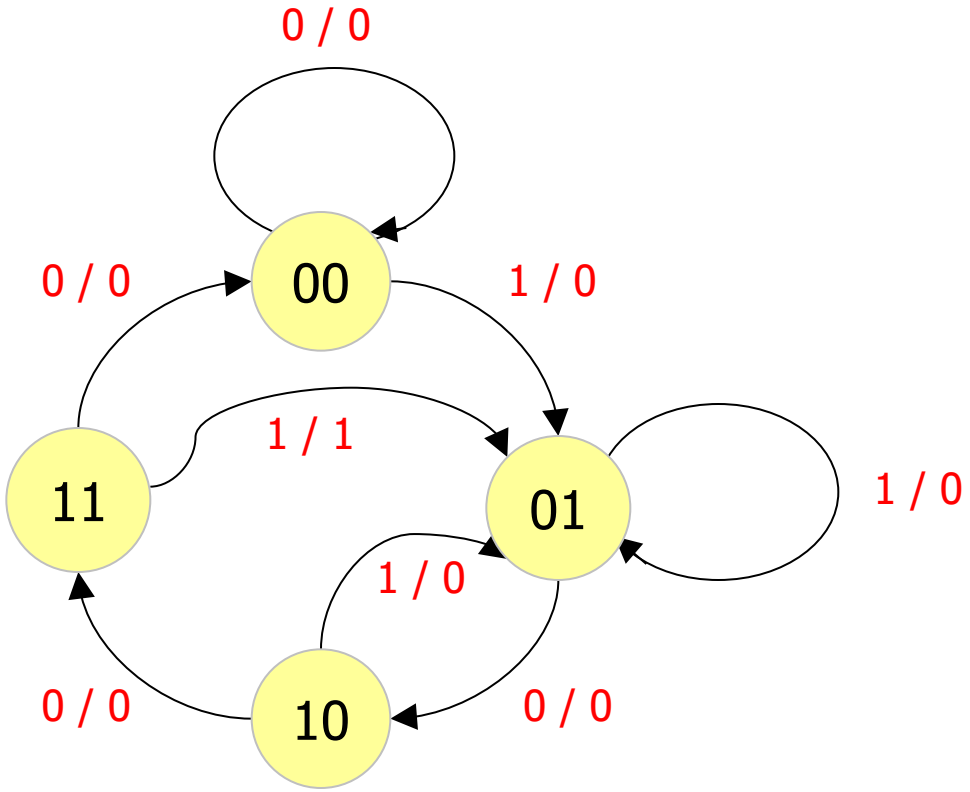
Exercise 8b.20: Draw the state diagram for the example in previous slide.



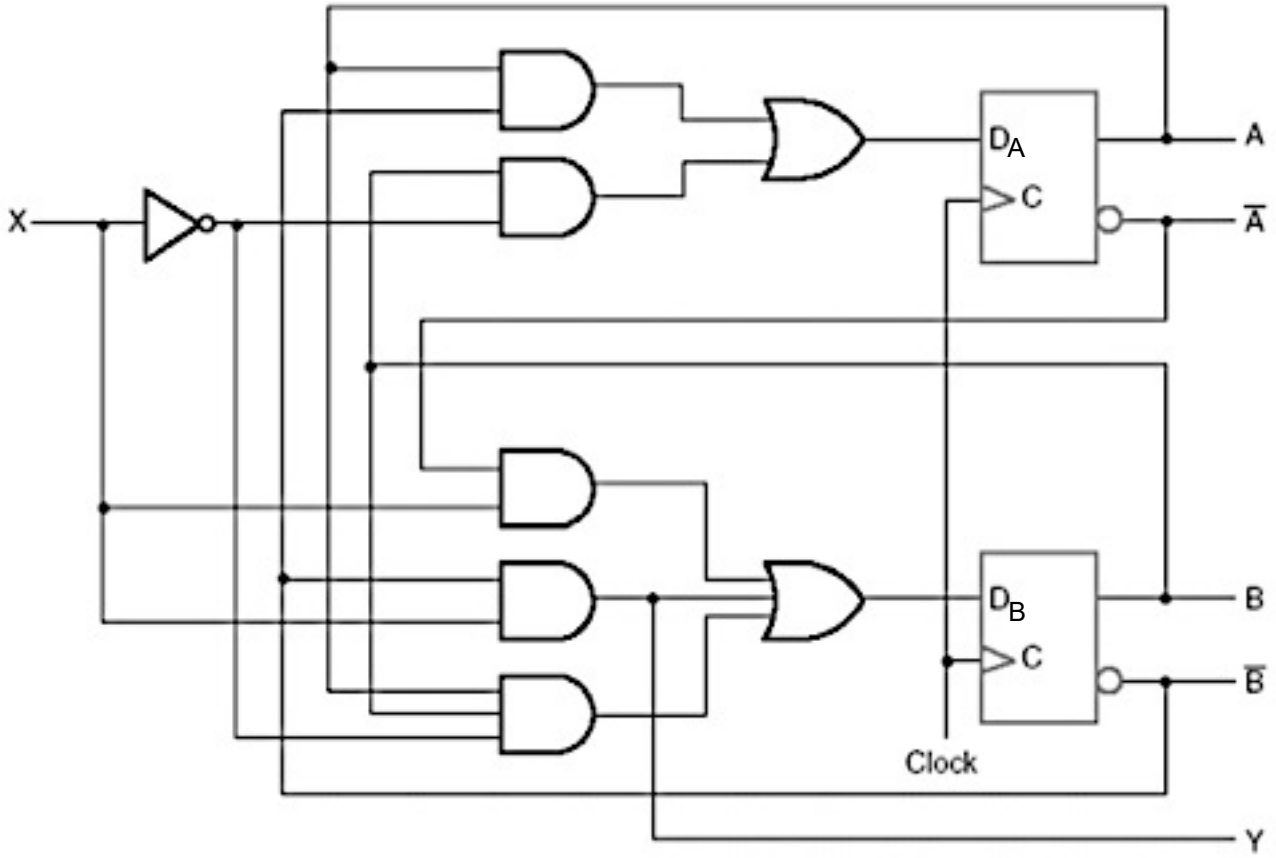
Input, X	Present State		Next State		Output, Z
	Q_1	Q_0	Q_{1+}	Q_{0+}	
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	1	1	0
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	1	1

Solution : Draw the state diagram for the example in previous slide.

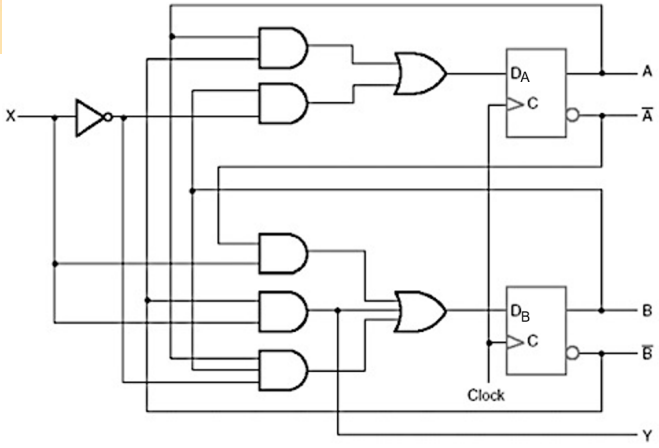




Exercise 8b.21: Analysis for the following sequential circuit.



Solution:



Step 1: The equation of each FF and output, Y

$$D_A = \overline{X}B + A\overline{B}$$

$$D_B = \overline{A}X + \overline{B}X + AB\overline{X}$$

$$Y = \overline{B}X$$

active HIGH SR : $Q_{next} = S + \overline{R}Q, SR = 0$

JK : $Q_{next} = J\overline{Q} + \overline{K}Q$

D : $Q_{next} = D$

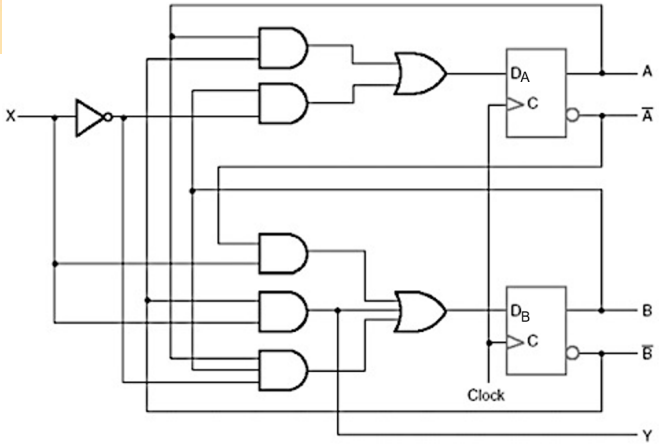
T : $Q_{next} = T\overline{Q} + \overline{T}Q$

Step 2: Derive the next state equations by converting these excitation equation into FF characteristic equations.

$$D_{A+} = D_A$$

$$D_{B+} = D_B$$

Solution:



Step 1: The equation of each FF and output, Y

$$D_A = \overline{X}B + A\overline{B}$$

$$D_B = \overline{A}X + \overline{B}X + AB\overline{X}$$

$$Y = \overline{B}X$$

active HIGH SR : $Q_{next} = S + \overline{R}Q, SR = 0$

JK : $Q_{next} = J\overline{Q} + \overline{K}Q$

D : $Q_{next} = D$

T : $Q_{next} = T\overline{Q} + \overline{T}Q$

Step 2: Derive the next state equations by converting these excitation equation into FF characteristic equations.

$$D_{A+} = D_A = \overline{X}B + A\overline{B}$$

$$D_{B+} = D_B = \overline{A}X + \overline{B}X + AB\overline{X}$$

Step 3: Produce a Next State Table.

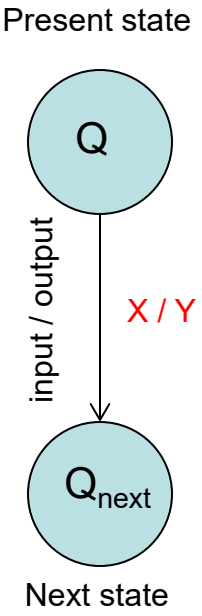
$$D_{A+} = D_A = \overline{X}B + A\overline{B}$$

$$D_{B+} = D_B = \overline{A}X + \overline{B}X + AB\overline{X}$$

$$Y = \overline{B}X$$

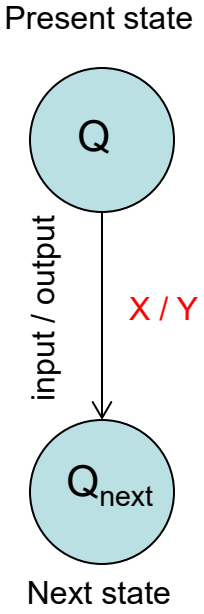
Input, X	Present State		Next State		Output, Y
	A	B	A_+	B_+	
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	1	0	0
0	1	1	1	1	0
1	0	0	0	1	1
1	0	1	0	1	0
1	1	0	1	1	1
1	1	1	0	0	0

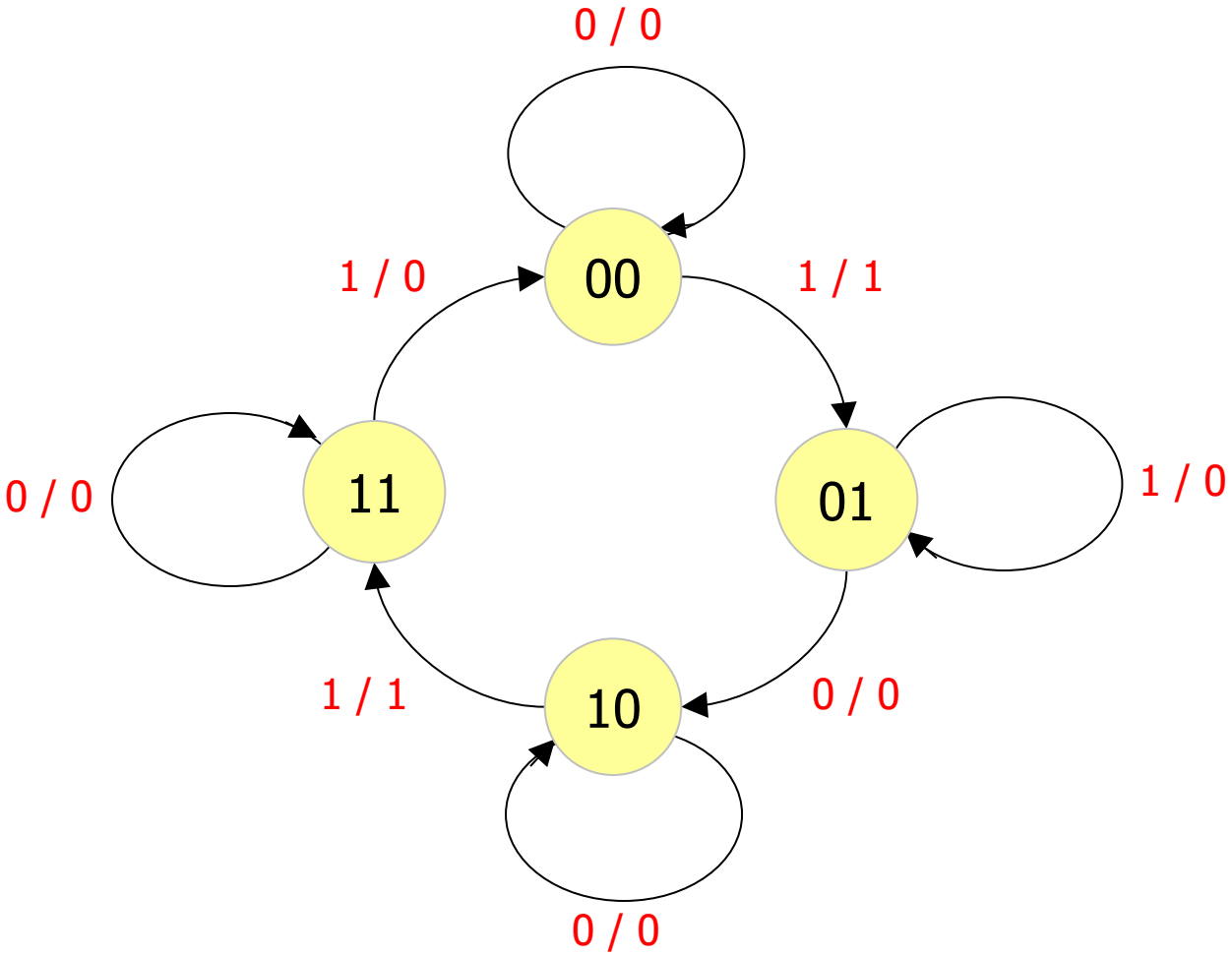
Exercise 8b.22: Draw the state diagram for the example in previous slide.



Input, X	Present State		Next State		Output, Y
	A	B	A_+	B_+	
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	1	0	0
0	1	1	1	1	0
1	0	0	0	1	1
1	0	1	0	1	0
1	1	0	1	1	1
1	1	1	0	0	0

Solution : Draw the state diagram for the example in previous slide.



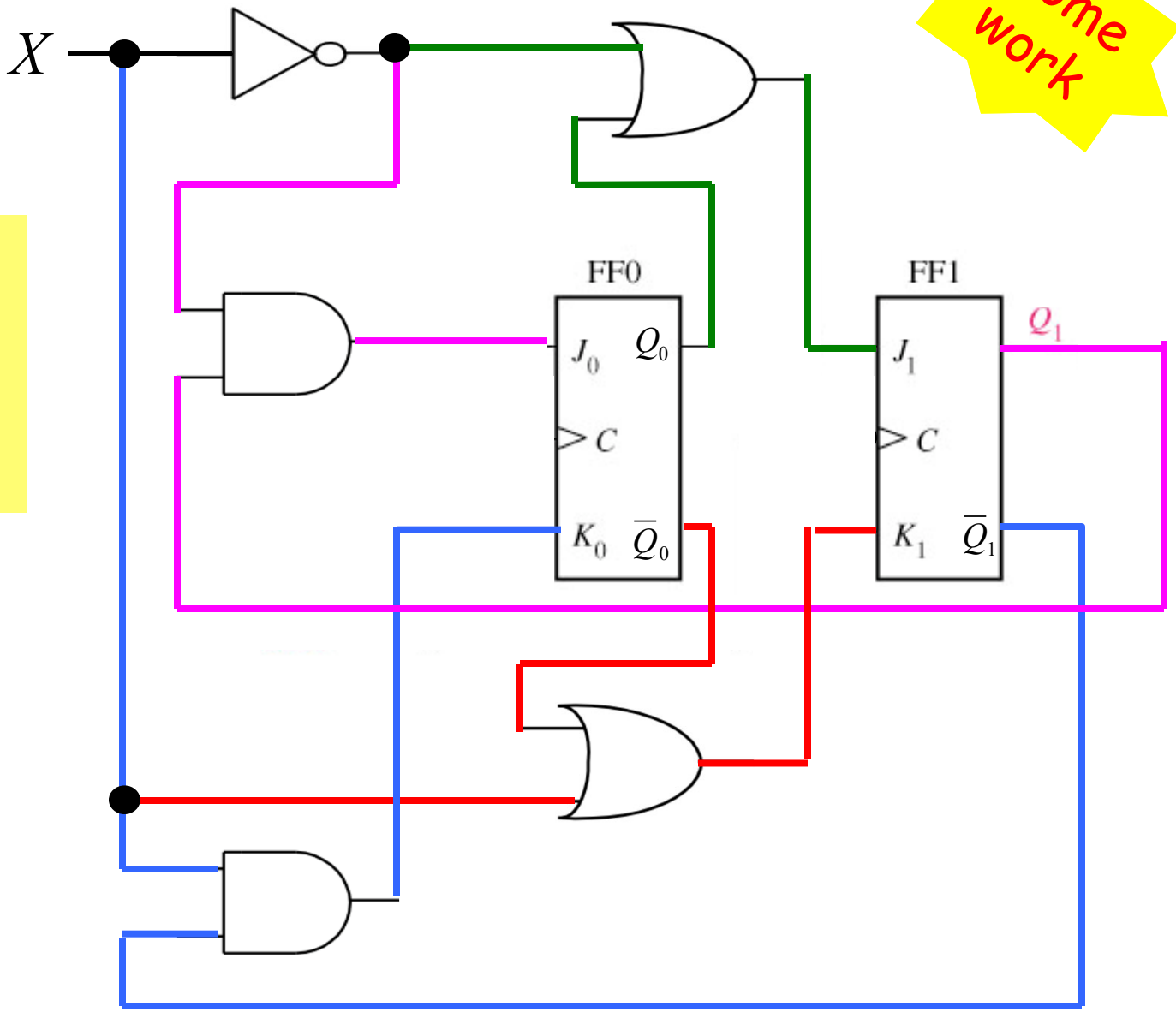


End of Module 8

Home work

Exercise 8b.23:

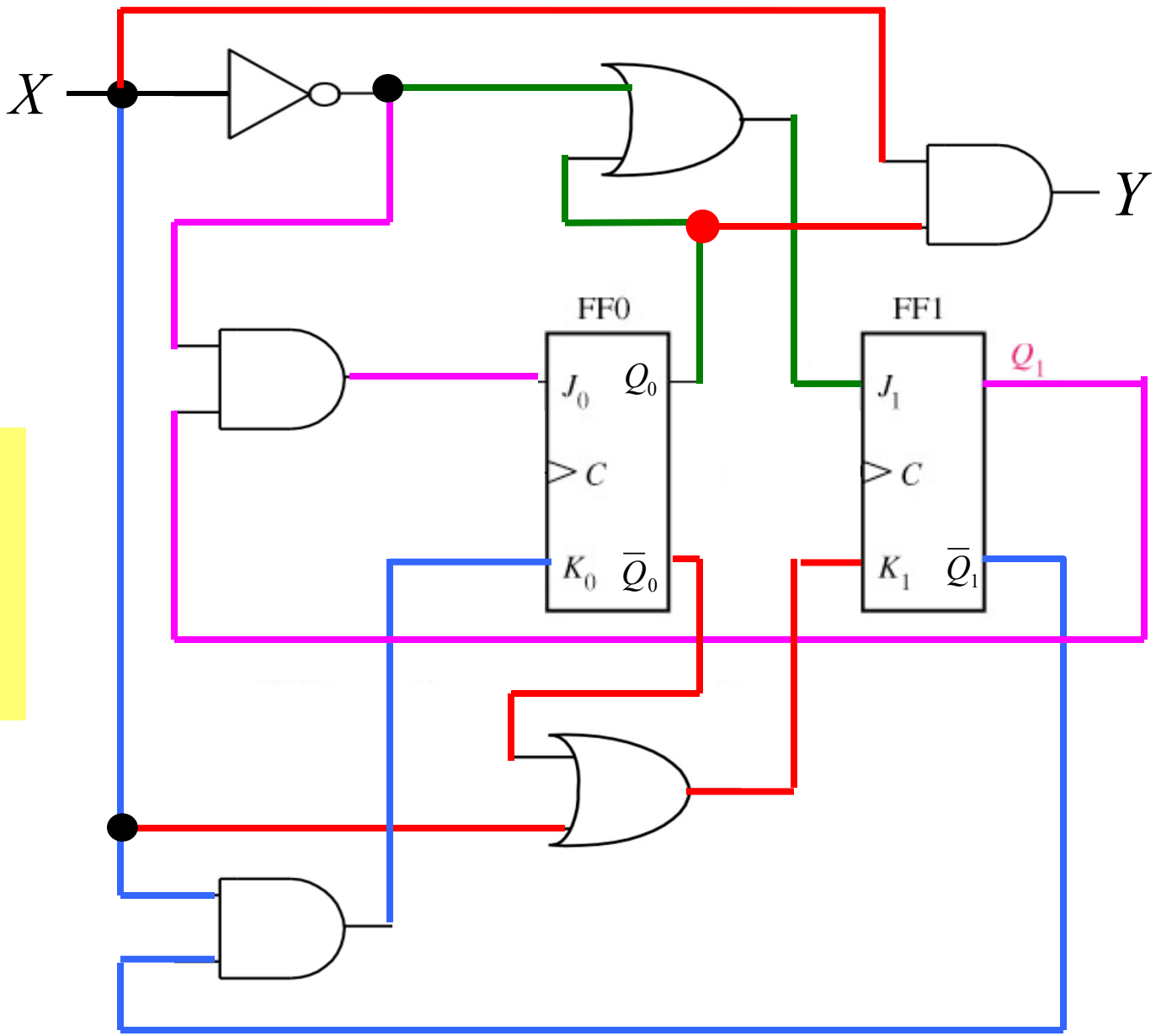
Derive the state table and state diagram for the sequential circuit below.



Home work

Exercise 8b.24:

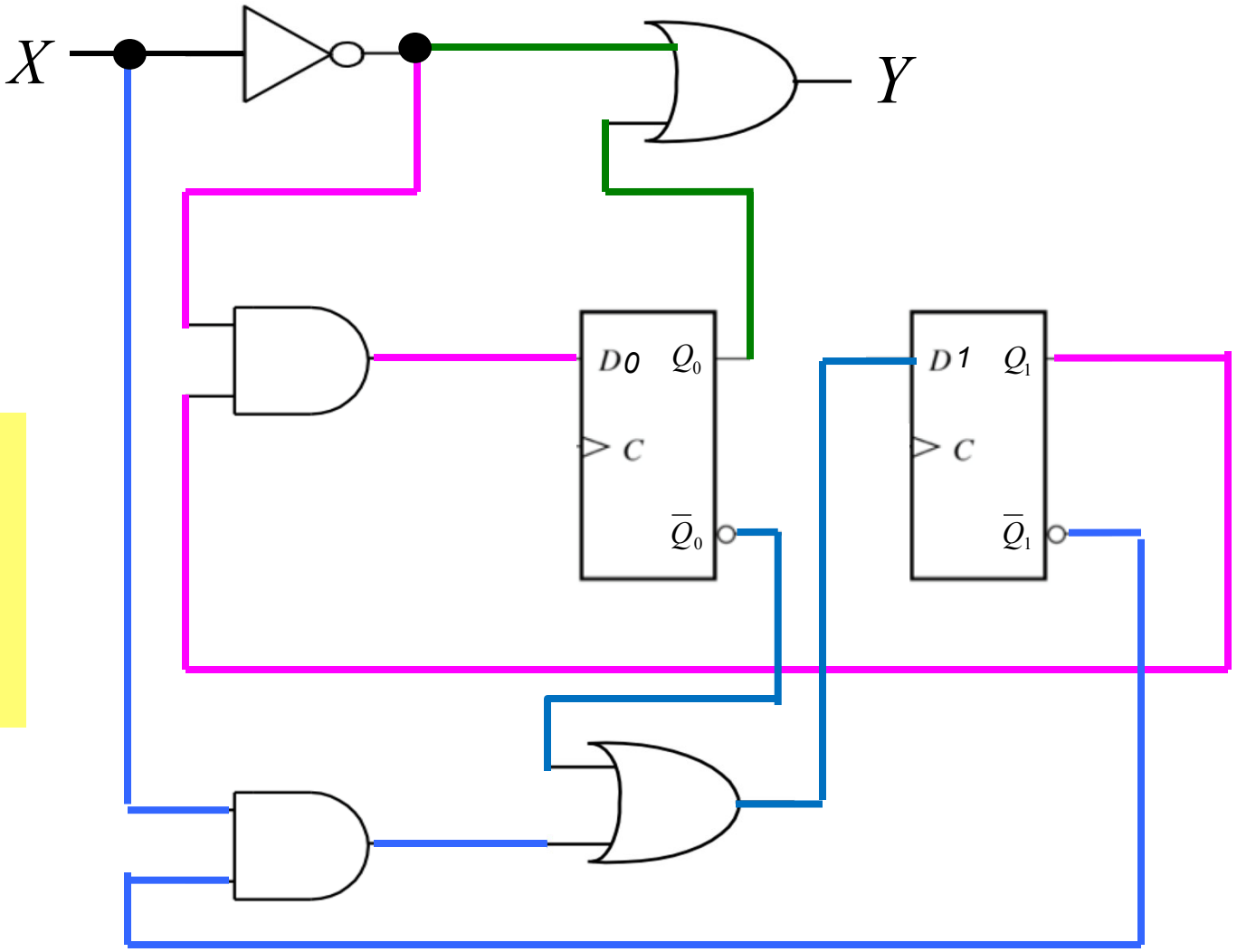
Derive the state table and state diagram for the sequential circuit below.



Home work

Exercise 8b.25:

Derive the state table and state diagram for the sequential circuit below.



Exercise 8b.27:

Home work

Derive the state table and state diagram for the sequential circuit below.