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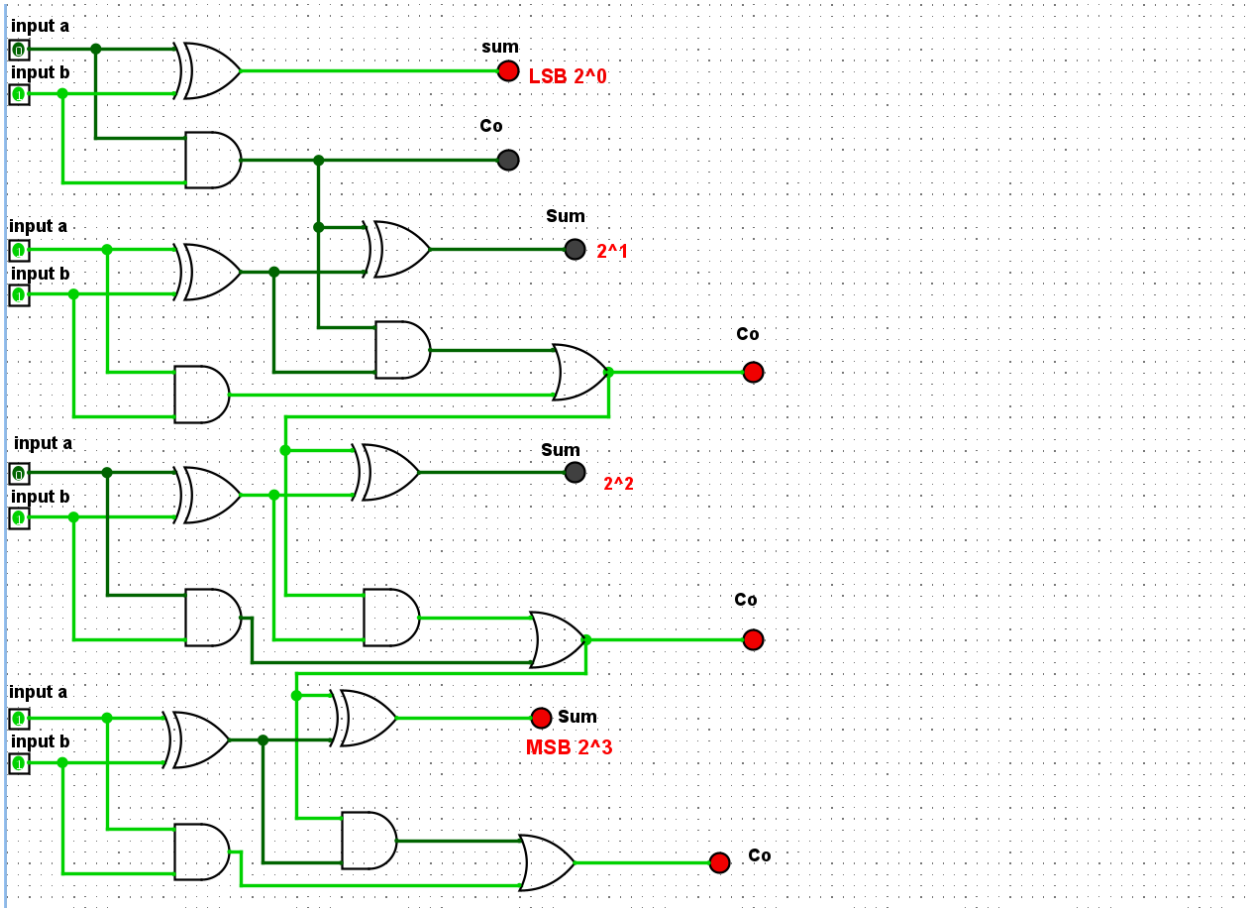
Lab02

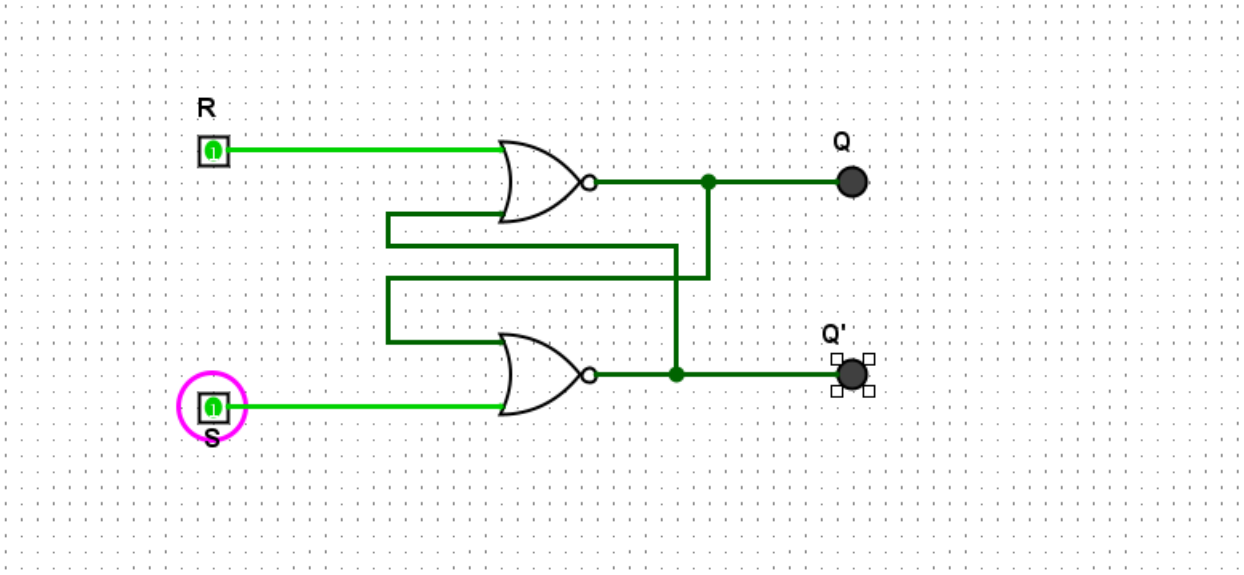
1. 4-bit adder



Input A	Input B	Output
0101	0000	0101
0101	0001	0110
0101	0010	0111
0101	0011	1000
0101	0100	1001
0101	0101	1010
0101	0110	1011
0101	0111	1100
0101	1000	1101
0101	1001	1110
0101	1010	1111
0101	1011	0000
0101	1100	0001
0101	1101	0010
0101	1110	0011
0101	1111	0100

Part 2: Storing bits with Flip Flops

I. R-S flip flop



Set	Reset	Q	Q'
1	0	1	0
1	1	indeterminate	indeterminate
0	1	0	1
1	1	indeterminate	indeterminate

11. Describe in a sentence, the behaviour of the circuit when one of the inputs is 1 (but not both) and why this is useful for digital circuit design.

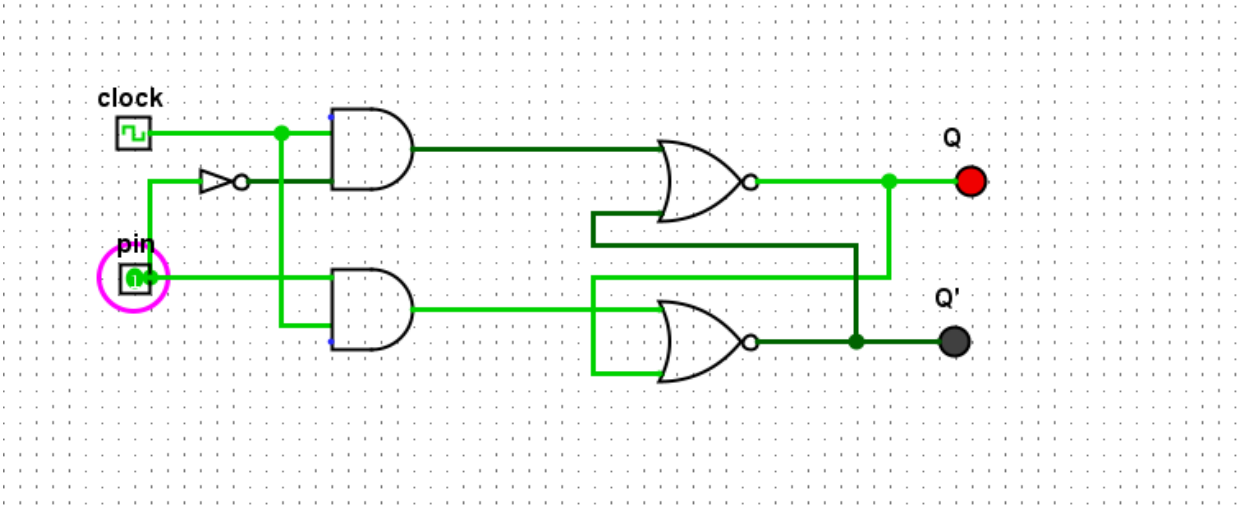
Based on the screenshot of the RS flip flop you provided earlier, if I set the Set input to high (1) and turn off the Reset input to 0, then Q will become 1 and Q' will become 0. Conversely, if we set Reset to high (1) and turn off Set, then Q will return to 0 and Q' will become 1. This is useful for digital circuit design because it's allow to hold and store binary information.

12. What do you notice about the two times you set both inputs to 1. Briefly explain what is happening here and why this is an issue for digital circuit design?

If both inputs of an RS flip flop are set to 1, it becomes indeterminate and is also referred to as the forbidden state. It will cause abrupt changes in the output signal, leading to an undefined and unstable state of the output. Therefore, it is highly dangerous for circuit design.

II. D flip flop

Clock	Pin	Q	Q'
0	0	0	0
0	1	0	0
1	1	1	0
1	0	0	1



15. Briefly explain the behaviour of a D Flip Flop and how it is useful for digital circuit design.

- When the clock is not active (0), the circuit will not respond to any input, and the outputs Q and Q' will hold the same values as the previous input state. When the clock is active (1), the output Q will change to match the input, while the output Q' will be the complement of Q. It is useful in controlling data transmission time and implementing sequential logic in digital circuits

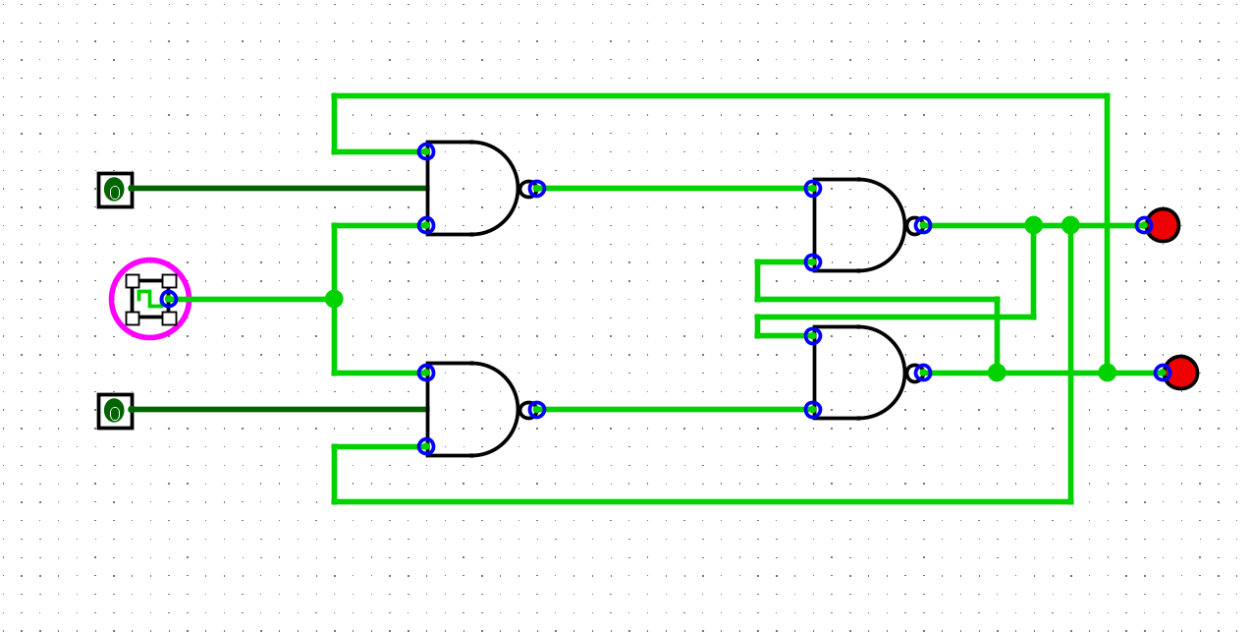
16. What is the role of the clock ? How does it impact the changing of state of Q and Q' ?

The role of the clock is synchronize data flow in circuit. The clock will control and determine the timing at which the inputs of the flip flop are processed, while the value of the output will change based on the changes in the inputs. Therefore, when the inputs change, it also affects the state changes of the output.

17. Why is it generally preferred over the R-S Flip Flop?

D flip flop is often preferred over R-S Flip Flop because it prevents the occurrence of the forbidden state. D flip flop does not allow both inputs to be set to 1 because its two inputs are complementary to each other.

19. Complete and include this truth table for JK Flip Flops in your submission document.



J	K	Q (when clocked)	Q' (when clocked)
0	0	no change	no change
1	0	1	0
0	1	0	1
1	1	toggle	toggle

20. How can a J-K Flip Flop be made to behave like a D Flip Flop ?

To make a JK flip flop behave like a D flip flop, we need to connect the D input together with the J input, and the complement of D as the K input, which means that K is connected to D through a NOT gate.

21. How can a J-K Flop Flop be made to behave like a toggle (T Flip Flop) ?

JK flip flop can be made to behave like a toggle(T flip flop) when 2 input is high(1).