TIMER RTL

start_bit_detected

packet_done

framing_error

See
state
diagram

next_state

\3

D  Q

reg

Clk

state

\3

nRst

Output logic
See
Diagram

enable_timer

sbc_clear

sbc_enable

load_buffer

nRst

start_bit_detected=0

IDLE

start_bit_det
ected = 1

START

sbc_clear=1

packet_done
= 0

PACK

enable_tim
er=1

packet
_done
=1

framing_error
= 1

framing_error
= 0

FRAME

_____

STORE

_____

load_buffer =
1

STOP

sbc_enable
=1