7.2. "1101 detector"
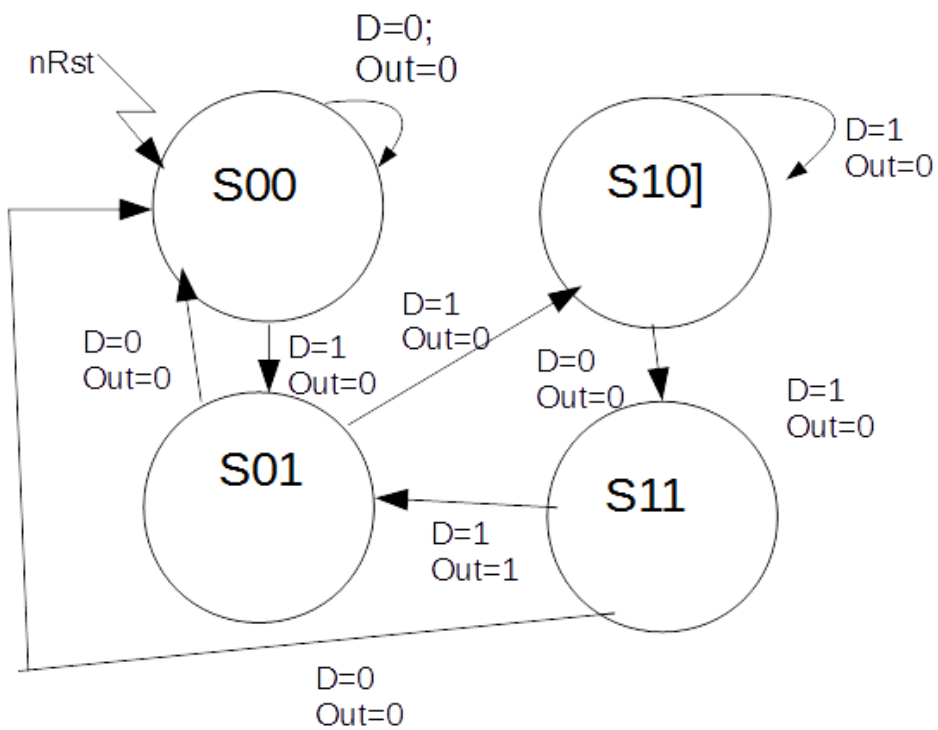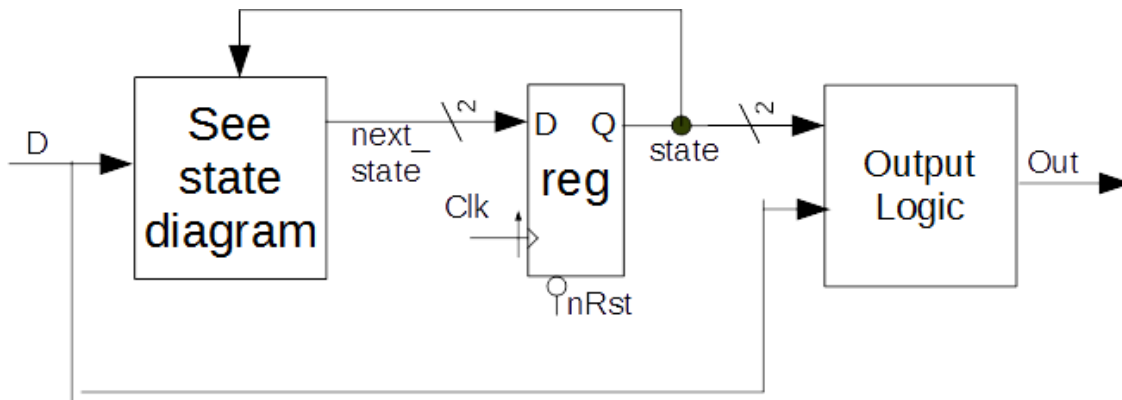
MEALY MODEL

D → See state diagram → next_state /2 → D Q reg state /2 → Output Logic → Out

Clk

nRst

State diagram:

nRst → S00

S00: D=0; Out=0 (self loop)

S10]: D=1 Out=0 (self loop)

S00 → S01: D=1 Out=0

S01 → S00: D=0 Out=0

S01 → S10]: D=1 Out=0

S10] → S11: D=0 Out=0

S11: D=1 Out=0 (self loop)

S11 → S01: D=1 Out=1

S11 → S00: D=0 Out=0

MOORE MODEL

See state diagram → next_state →\3→ D Q reg state →\3→ Output Logic → Output

D →

Clk

nRst

nRst → S000 —0—

D=0 (self loop on S000)

D=0 → (from S110 to S000)

S110 —0—

D=0 (from top to S101)

S101 —1—

D=1 (from S110 to S101)

D=0 (from S000 down) / D=1 (from S000 down)

D=1 → S011 —0—

D=0 (from S011 up to S110)

D=1 (self loop on S011)