PIRAQ III User's Guide

Description

PIRAQ III is a PCI based data acquisition and signal processing system on a single printed circuit board. Figure 1 shows a basic block diagram of the PIRAQ III. The card features two 14 bit analog to digital converters running at up to 64 MHz. Each ADC feeds a pair of GC2011A FIR Filter chips, which can be used to perform quadrature down conversion, filtering and decimation of the input stream. 18 bit Inphase and Quadrature data are output from the FIR chips and stored in separate FIFO buffers where they are available to the DSP for further processing. The DSP used is a TMS320C6701, running at 160MHz and capable of 900 MFLOPS peak processing performance. In addition to the DSPs 64KB internal program RAM and 64KB data RAM, there is 256KB of full-speed SBSRAM and 16MB of ½ speed SDRAM. The Card supports 32bit 33MHz PCI bus initiator and target interfaces and can interrupt the PC's CPU as well be interrupted. In addition, the PIRAQ III provides all the necessary timing signals to control data acquisition and to synchronize multiple boards.

Theory of Operation

The PIRAQ III has been developed to acquire high speed wide dynamic range data and to have the onboard processing capability to deliver a very high quality raw data stream (I,Q) for subsequent processing by multiple PCs. If less processing is required on the raw data then the on-board DSP can be used for Autocovariance and/or other signal processing.

For traditional Radar applications, the Piraq III offers two data acquisition channels to provide overlapping dynamic range of the input. Either a 60 MHz or a 16 MHz Intermediate Frequency (IF) can be used. For a 60 MHz IF, each channel sub-samples the IF at 48 MHz; this yields a signal centered at 12 MHz oversampled 4 times. If a 16 MHz IF is used, then each channel is sampled at 64 MHz. This also yields a signal oversampled by a factor of 4. The samples are divided into even and odd sampled streams. This forms the basis for the inphase and quadrature data outputs. By judiciously choosing the signs and weights of the coefficients within the FIR chips, decimated (to the desired gate spacing) inphase and quadrature data streams are available to the user. The DSP can be used to perform further filtering, phase noise compensation, high or low dynamic range channel selection, and other user defined tasks.

Upon power up the PCI bridge chip is initialized via an on-board serial EEPROM. Once this occurs, the PCI interface can be accessed via the PC. The DSP program is loaded from the PC using the DSP's 16 bit Host Port Interface (HPI), which is memory mapped to the PCI bus. The program can reside in either internal program memory or external SBSRAM or SDRAM. The best performance will probably be obtained using the internal memory, followed by SBSRAM and then SDRAM. The SDRAM is intended for storing and operating on large data arrays. When processing is completed, the data can be transferred to the PC's memory via the PCI bus. In this instance the PIRAQ III becomes the PCI initiator and the DSP transfers the data via the PCI bridge chip. This can be done as a DMA operation on the DSP, so very little processing power will be lost. The DSP can also interrupt the PC upon completion of the transfer. The interrupt can be implemented in hardware or via the PCI bridge chips mailbox or doorbell interrupts.

PIRAQ III control and status can be read via the PCI bus from two 16bit registers. In addition, two programmable timer chips can be accessed from the PCI interface to set PRF, gate spacing and number of range gates.

Programming Model

The intent here is to present memory map and data width information for all PCI mapped locations. All addresses presented here are in bytes and relative to PIRAQ III base address. The base address for the card is assigned by the PCI bios upon power up and can be obtained by reading from address (0x?????).

PCI Address Map

NAME	ADDRESS	WIDTH	TYPE
FIR – CH1 I	0x0 - 0x3FF	16 bits	R/W
FIR – CH1 Q	0x400 - 0x7FF	16 bits	R/W
FIR – CH2 I	0x800 - 0xBFF	16 bits	R/W
FIR – CH2 Q	0xC00-0xFFF	16 bits	R/W
Timer 0	0x1000-0x100F	16 bits	W
Timer 1	0x1010 - 0x13FF	16 bits	W
Control/Status Register 0	0x1400	16 bits	R/W
Control/Status Register 1	0x1410	16 bits	R/W
HPI	0x1800-0x180F	16 bits	R/W

Configuration of the PCI target and initiator interfaces occur on power up via the serial EEPROM, although modifications can be made by the PC or the DSP.

FIR Filter Chips

The FIR filter chip used is the Graychip GC2011A, for more detailed information refer to the datasheet at the Graychip's website (www.graychip.com). Each chip has 512 registers; each register is 16 bits wide. The following table gives a brief description of the registers for a single GC2011A. The addresses given are relative to the base address for a given FIR filter chip.

FIR Filter Addresses

NAME	ADDRESS
Apath_reg0	0x0
Apath_reg1	0x2
Bpath_reg0	0x4
Bpath_reg1	0x6
Cascade_reg	0x8
Counter_reg	0xA
Gain_reg	0xC
Output_reg	0xE
Snap_regA	0x10
Snap_regB	0x12
Snap_regC	0x14
One_Shot	0x16
New_Modes	0x18
Unused	0x1A – 0xFE
Coefficient Registers	0x100 – 0x1FE
Snapram	0x200 – 0x3FE

Timers

There are two 82C54 timer chips on the PIRAQ III. They are responsible for generating all the user programmable timing signals required for data acquisition. Each timer chip has three independent 16 bit counters and can operate in one of 6 user selectable modes. An 8 bit control word determines counter operation. Programming of the 82C54 is very flexible; there are only two rules. For each counter, the control word must be written before the initial count is written. The initial count must follow the count format specified in the control word (least significant byte only, most significant byte only, or least significant byte followed by most significant byte).http://www.intersil.com The following table provides more detailed address information for the timers.

Timer Addressing

NAME	ADDRESS	WIDTH	TYPE
Timer 0 - Control Word	0x1006	8 bits	W
Timer 0 - Counter 0	0x1000	8 bits	W
Timer 0 - Counter 1	0x1002	8 bits	W
Timer 0 - Counter 2	0x1004	8 bits	W
Timer 1 - Control Word	0x1016	8 bits	W
Timer 1 - Counter 0	0x1010	8 bits	W
Timer 1 - Counter 1	0x1012	8 bits	W
Timer 1 - Counter 2	0x1014	8 bits	W

The 8 bit control word is structured as follows.

Control Word

NAME	BIT	.FUNCTION
BCD	0	if BCD = 0; then counter is 16 bit binary if BCD = 1; then counter is binary coded decimal
M0,M1,M2	1-3	the binary value of these three bits define the mode (0-5)
RW0,RW1	4,5	00 = counter latch command 01 = read/write ls byte only 10 = read/write ms byte only 11 = read/write ls byte first then ms byte
SC0,SC1	6,7	00 = select counter 0 01 = select counter 1 10 = select counter 2 11 = read back command

For more detailed information on the 82C54 refer to www.intersil.com .

Control/Status Registers

There are two 16 bit Control/Status registers on the PIRAQ III. Control/Status register 0 is at offset 0x1400 and Control/Status register 1 is at 0x1410. The bits of each are defined below.

Control/Status Register 0

NAME	BIT	FUNCTION
SW_RESET	0	
TRESET	1	
TMODE	2	
DELAY_SIGN	3	
EVEN_TRIG	4	
ODD_TRIG	5	
EVEN_TP	6	
ODD_TP	7	
PCLED	8	
GLEN0	9	
GLEN1	10	
GLEN2	11	
GLEN3	12	
GLEN4	13	
GATE0MODE	14	
SAMPLE_CTRL	15	

Control/Status Register 1

NAME	BIT	FUNCTION
PLL_CLOCK	0	
PLL_LE	1	
PLL_DATA	2	
WATCHDOG	3	
PCI_INT	4	
EXTTRIGEN	5	
FIRST_TRIG	6	Read Only

PHASELOCK	7	Read Only

HPI

The 16 bit Host Port Interface allows the user to test and program DSP memory via the PCI bus. From the programmer's view the HPI is made up of three registers. The HPI Control Register (HPIC), the HPI Address Register (HPIA) and the HPI Data Register (HPID). The registers map as follows:

HPIC 0x1800
HPIA 0x1804
HPID 0x1808 (HPIA auto-increment), 0x180C (HPIA not effected)

The HPIC is organized as a 32 bit register whose high halfword and low halfword contents are identical. On a PCI target write, both halfwords must be the same. Only DSP writes to the lower halfword affect HPIC values and operation. The bits of the HPIC are defined in the table.

HPIC

NAME	BIT	FUNCTION
HWOB	0	if HWOB =1, the first halfword is least significant if HWOB = 0, the first halfword is most significant
DSPINT	1	the PC to DSP interrupt
HINT	2	DSP to PC interrupt; the inverted value determines the state of the HINT output, read only
HRDY	3	Ready Signal to PC, read only
FETCH	4	PC fetch request
rsvd	5-15	RESERVED
HWOB	16	if HWOB =1, the first halfword is least significant if HWOB = 0, the first halfword is most significant
DSPINT	17	the PC to DSP interrupt
HINT	18	DSP to PC interrupt; the inverted value determines the state of the HINT output, read only
HRDY	19	Ready Signal to PC, read only
FETCH	20	PC fetch request

rsvd	21-31	RESERVED

PCI access of the HPI begins with the initialization of the HWOB bit of the HPIC, followed by setting of the address in the HPIA. Then the HPID can be accessed in either address autoincrement mode or not.
For further information on the HPI consult document spru190c.pdf available at www.ti.com

DSP Details

The TMS3206701 DSP chip supports a wide variety of memory types through its External Memory Interface (EMIF). On the PIRAQ III, these include SBSRAM, SDRAM, FIFOs and other asynchronous devices. The user has two choices of memory maps, Map 0 and Map 1. Map 0 has SBSRAM mapped at address 0, while Map 1 has internal program memory mapped to address 0. These are selected at reset by the status of Bootmode(0:4) which is directly effected by jumpers **JP2**, **JP3**, and **JP4**. The PIRAQ III DSP supports the following 5 boot configurations according to the jumper settings selected. An X indicates the jumper is in place.

Boot Jumper Settings

JP2	JP3	JP4	Boot Process/Memory Map
			HPI/Map 1– internal program memory
		X	HPI/Map 0 – external SBSRAM
X			None (load via JTAG)/Map 1 – internal program memory
X		X	None (load via JTAG)/Map 0 – external SBSRAM 1x rate
	X		None (load via JTAG)/Map 0 – external SBSRAM 1/2x rate

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DSP Memory Maps

ADDRESS RANGE (hex)	SIZE (bytes)	MAP 0	MAP 1
0000 0000 – 0000 FFFF	64K	SBSRAM	Internal Program RAM
0001 0000 – 0003 FFFF	192K	SBSRAM	Reserved
0004 0000 – 003F FFFF	4M - 256K	–	Reserved
0040 0000 – 0043 FFFF	256K	–	SBSRAM
0044 0000 – 00FF FFFF	12M - 256K	–	–

ADDRESS RANGE (hex)	SIZE (bytes)	MAP 0	MAP 1
0100 0000 – 0100 007F	128	PLX 9054 PCI configuration registers	–
0100 0080 - 0100 017F	256	PLX 9054 local configuration registers	–
0100 0180 – 0100 01FF	128	–	–
0100 0200 – 0100 0203	4	FIFO Reset	–
0100 0204 – 0100 0207	4	FIFO 1 read enable	–
0100 0208 – 0100 020B	4	FIFO 2 read enable	–
0100 020C – 0100 020F	4	FIFO 3 read enable	–
0100 0210 - 0100 0213	4	FIFO 4 read enable	–
0100 00214 - 0100 02FF	236	–	–
0100 0300 - 0100 0303	4	PCI Address bit 20	–
0100 0304 – 0100 0307	4	PCI Address bit 21	–
0100 0308 – 0100 030B	4	LED 0	–
0100 030C – 0100 030F	4	LED 1	–
0100 0310 – 013F FFFF	4M - 784	–	–
0140 0000 – 0140 007F	128	Internal Program RAM	PLX 9054 PCI configuration registers
0140 0080 - 0140 017F	256	Internal Program RAM	PLX 9054 local configuration registers
0140 0180 – 0140 01FF	128	Internal Program RAM	–
0140 0200 – 0140 0203	4	Internal Program RAM	FIFO Reset
0140 0204 – 0140 0207	4	Internal Program RAM	FIFO 1 read enable
0140 0208 – 0140 020B	4	Internal Program RAM	FIFO 2 read enable

ADDRESS RANGE (hex)	SIZE (bytes)	MAP 0	MAP 1
0140 020C – 0140 020F	4	Internal Program RAM	FIFO 3 read enable
0140 0210 – 0140 0213	4	Internal Program RAM	FIFO 4 read enable
0140 0214 – 0140 02FF	236	Internal Program RAM	–
0140 0300 - 0140 0303	4	Internal Program RAM	PCI Address bit 20
0140 0304 – 0140 0307	4	Internal Program RAM	PCI Address bit 21
0140 0308 – 0140 030B	4	Internal Program RAM	LED 0
0140 030C – 0140 030F	4	Internal Program RAM	LED 1
0140 0310 – 0140 FFFF	64K - 784	Internal Program RAM	–
0141 0000 – 017F FFFF	4M - 64K	Reserved	–
0180 0000 – 0183 FFFF	256K	Internal EMIF registers	Internal EMIF registers
0184 0000 – 0187 FFFF	256K	Internal DMA controller registers	Internal DMA controller registers
0188 0000 - 018B FFFF	256K	Internal HPI registers	Internal HPI registers
018C 0000 – 018F FFFF	256K	Internal McBSP 0 registers	Internal McBSP 0 registers
0190 0000 – 0193 FFFF	256K	Internal McBSP 1 registers	Internal McBSP 1 registers
0194 0000 – 0197 FFFF	256K	Internal Timer 0 registers	Internal Timer 0 registers
0198 0000 – 019B FFFF	256K	Internal Timer 1 registers	Internal Timer 1 registers
019C 0000 – 019F FFFF	256K	Internal Interrupt Selector registers	Internal Interrupt Selector registers

ADDRESS RANGE (hex)	SIZE (bytes)	MAP 0	MAP 1
01A0 0000 – 01FF FFFF	6M	Internal peripheral bus (reserved)	Internal peripheral bus (reserved)
0200 0000 – 02FF FFFF	16M	SDRAM	SDRAM
0300 0000 – 03FF FFFF	16M	PCI bus (initiator)	PCI bus (initiator)
0400 0000 – 7FFF FFFF	2G - 64M	Reserved	Reserved
8000 0000 – 803F FFFF	64K	Internal Data RAM	Internal Data RAM
8040 0000 – FFFF FFFF	2G - 64K	Reserved	Reserved

In order for the external memory interfaces to function correctly, the user must correctly configure the 7 EMIF configuration registers, prior to any external memory accesses. The EMIF registers and the correct values for PIRAQ III are given below. For more detailed information refer to document spru190c.pdf available at www.ti.com

EMIF Registers

NAME	ADDRESS	VALUE
EMIF Global Control	0x1800000	0x6C
EMIF CE1 Space Control	0x1800004	TBD (FIFOs,etc.)
EMIF CE0 Space Control	0x1800008	0x40 (SBSRAM)
Reserved	0x180000C	--
EMIF CE2 Space Control	0x1800010	0x30 (SDRAM)
EMIF CE3 Space Control	0x1800014	TBD (PCI I/F)
EMIF SDRAM Control	0x1800018	0x7115000
EMIF SDRAM Timing	0x180001C	0x518

PCI Interface

The PIRAQ III supports both initiator and target interfaces to the PCI bus. The target interface is used primarily to configure the board and program the DSP. The initiator interface is used to transfer data from DSP memory to PC memory.

Target Interface

The target interface is configured upon power up by the serial EEPROM and should not require modification. The user can access all configuration registers using the PC via the PCI bus or the DSP via the local bus. Refer to 9054db-20.pdf at www.plxtech.com for more information.

Initiator Interface

The initiator interface supports type 0 and type 1 PCI configuration cycles, single cycle I/O, and single and burst memory transfers across the PCI bus. The PLX 9054 PCI bridge chip must be configured by the PC or the DSP prior to any data transfer. The data transfer itself can be done using the DSP's CPU or one of the DSP's internal DMA engines. To set up a data transfer, the following procedure should be followed.

Interrupts

Several mechanisms exist for the DSP to interrupt the host PC and vice versa. These include hardware interrupts, mailbox interrupts and doorbell interrupts. All involve using the PLX 9054 PCI bridge chip.

DSP to host PC

Hardware interrupts from the DSP to the PC are achieved via the PCI bus INTA line. The DSP writes a 1 to the HINT bit in the HPIC. This lowers INTA. The ISR running on the PC clears the interrupt by writing a 1 to the HINT bit of the HPIC. Mailbox registers in the PLX 9054 can be used to communicate status if interrupts are shared by other devices.

Mailbox interrupts can also be used. In this case the DSP would write a mailbox register, which would generate a PCI interrupt on INTA. The PC's ISR would read the mailbox register, thus clearing the interrupt. It should be noted that writing to the mailbox register doesn't automatically result in a PCI interrupt, but must be configured to do so.

Doorbell interrupts work much the same way as mailbox interrupts do. In this case, the DSP writes a doorbell register, which automatically generates a PCI Interrupt. The interrupt is cleared by an ISR that reads the doorbell register.

Host PC to DSP

Hardware is the only means that the PC can use to interrupt the DSP, but three options with some variations exist to do so.