USER MANUAL

Accessory 14P

PCI Format TTL 48/96 Input/Output Board

3Ax-603755-xUxx

January 13, 2004

DELTA TAU
Data Systems, Inc.
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INTRODUCTION

The PMAC Accessory-14P is a general-purpose input/output board for the PMAC family of motion controllers. Accessory-14P provides expanded and flexible digital I/O capabilities for the controller and can be configured for a wide variety of different uses to serve many diverse applications. It is commonly used for discrete I/O and for parallel binary feedback or gray scale code (absolute encoders and laser interferometers). This accessory also allows easy connection to OPTO22 and Grayhill Module I/O cards for general purpose I/O. This accessory provides PMAC with 48 or 96 bits of digital I/O which may be configured according to specific needs. The ACC-14P is connected to the PMAC through its JEXP port connector.

The ACC-14P can be ordered as a 48-bit I/O card or fully populated as a 96-bit I/O card. The ACC-14P uses the Delta Tau IOGATE IC, which can provide sophisticated I/O control for the application. The Delta Tau IOGATE IC has the following main features:

- 48 I/O points
- Individual direction control for I/O points
- Individual inversion control for each I/O point
- Individual control on inputs of latched or transparent read
- Automatic conversion of latched Gray code inputs
- Eight additional inputs for latch control, maskable interrupts, or general inputs

Up to six fully populated ACC-14P cards can be used to process 576 bits of real time I/O.

Warning

The Non-Turbo PMAC Encoder conversion table does not support the byte-wide parallel word feedback entries as of Non-Turbo PMAC Firmware release 1.17B. At this time, the Non-Turbo PMAC can only use the ACC-14P for general purpose I/O.

Configuration

The ACC-14P, ordered without options, provides 48 user I/O points through a single IOGATE IC. Two 50-pin IDC headers (J3 and J4) are provided, each for 24 I/O points with returns and clock latching signals.

If Option 1 is ordered, 48 additional I/O points are provided through a second IOGATE IC, for a total of 96 I/O points. Two additional 50-pin IDC headers (J5 and J6) are provided for the additional I/O points.

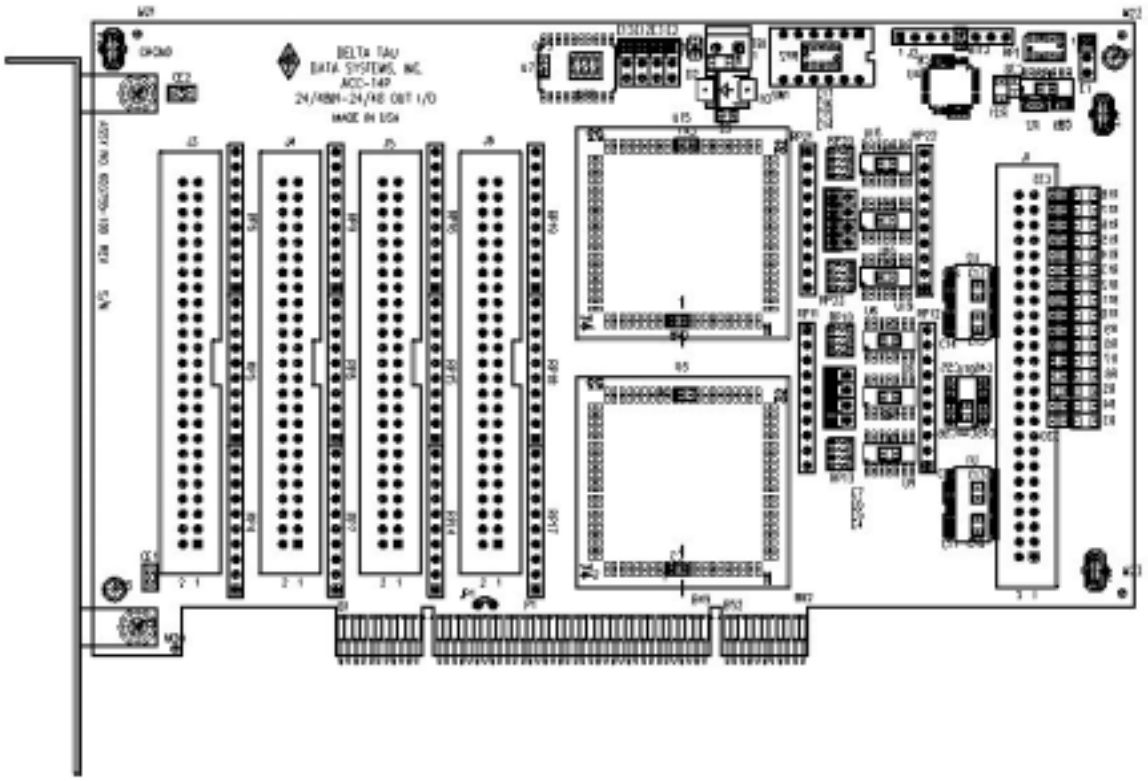
HARDWARE SETUP

The ACC-14P uses PMAC expansion port memory locations defined by the type of PMAC (non-Turbo or Turbo).

Non-Turbo PMAC Memory Locations	Turbo PMAC Memory Locations
$FFD0	$78A00
$FFD8	$78B00
$FFE0	$78C00
$FFE8	$78D00
$FFF0	$78E00
$FFF8	$78F00

The ACC-14P has a set of dip switches telling it where to process its data. Once the information is at these locations, the binary word can be processed in the encoder conversion table to use for servo loop closure. Proper setting of the dip switches ensures all of the I/O boards used in the application do not interfere with each other.

Layout Diagram



Address Select DIP Switch S1

The switch one (S1) settings will allow the selection of the starting address location for the first I/O gate on the ACC-14P. The following table shows the dip switch settings for both the non-Turbo and Turbo PMAC.

ACC-14P Switch Settings

Non-Turbo PMAC	Turbo PMAC Address	DIP Switch SW1 Position					
		6	5	4	3	2	1
Y:$FFD0*	Y:$78A00*	Close	Close	Close	Close	Open	Close
Y:$FFD8	Y:$78B00	Close	Close	Close	Close	Open	Open
Y:$FFE0	Y:$78C00	Close	Close	Close	Open	Close	Close
Y:$FFE8	Y:$78D00	Close	Close	Close	Open	Close	Open
Y:$FFF0	Y:$78E00	Close	Close	Close	Open	Open	Close
Y:$FFF8	Y:$78F00	Close	Close	Close	Open	Open	Open
* default setting							

Jumpers

Refer to the layout diagram of ACC-14E for the location of the jumpers on the board.

E-Point Jumpers

Jumper	Config	Description	Settings	Default
E1	1-2	Sample Clock Select	1-2 Phase clock is Sample clock 2-3 Servo clock is Sample clock	2-3
E2	1-2-3	Output Clock Polarity for J3 and J4	1-2 OCLK_1_2 is Sample clock- 2-3 OCLK_1_2 is Sample clock+	1-2
E3	1-2-3	Latch Clock Polarity for J3 and J4	1-2 ENA_CLK_1_2 is Sample clock+ 2-3 ENA_CLK_1_2 is Sample clock-	2-3
E4	1-2	Input Latch Signal for bits 0-23	On passes the ICLK1 5V input from J3 to latch port A I/O Off passes the ICLK1 0V input from J3 to latch port A I/O	1-2
E5	1-2	Error Latch Signal for bits 0-23	On allows a low ERR1/ input to disable the J3 latch Off allows a high ERR1/ input to disable the J3 latch	1-2
E6	1-2	Input Latch Signal for bits 24-47	On passes the ICLK2 5V input from J5 to latch port B I/O Off passes the ICLK2 0V input from to latch port B I/O	1-2
E7	1-2	Error Latch Signal for bits 24-47	On allows a low ERR2/ input to disable the J4 latch Off allows a high ERR2/ input to disable the J4 latch	1-2
E12	1-2-3	Output Clock Polarity for J5 and J6	1-2 OCLK_3_4 is Sample clock- 2-3 OCLK_3_4 is Sample clock+	1-2
E13	1-2-3	Latch Clock Polarity for J5 and J6	1-2 ENA_CLK_3_4 is Sample clock+ 2-3 ENA_CLK_3_4 is Sample clock-	2-3
E14	1-2	Input Latch Signal for bits 48-71	On passes the ICLK3 5V input from J5 to latch port A I/O Off passes the ICLK3 0V input from J5 to latch port A I/O	1-2
E15	1-2	Error Latch Signal for bits 48-71	On allows a low ERR3/ input to disable the J5 latch Off allows a high ERR3/ input to disable the J5 latch	1-2
E16	1-2	Input Latch Signal for bits 72-95	On passes the ICLK4 5V input from J6 to latch port B I/O Off passes the ICLK4 0V input from J6 to latch port B I/O	1-2
E17	1-2	Error Latch Signal for bits 72-95	On allows a low ERR4/ input to disable the J6 Latch Off allows a high ERR4/ input to disable the J6 Latch	1-2
If ICLK or ERR inputs from the encoder are not present, the E4, E5, E6, E7, E14, E15, E16, E17 jumpers are pulled up to 5V.				

USING ACC-14P WITH PMAC

The ACC-14P can be used with the PMAC for either general purpose I/O or as latched inputs for servo loop position or velocity feedback. The registers used for general I/O use are 8-bit registers. Three 8-bit registers can be user-defined for each 24-bit I/O port. To use the ACC-14P for closed loop servo data, set up various I-variables for the encoder conversion table and power-on position variables. The encoder conversion table is set up using variables I8000 through I8191. Each variable is an entry in the conversion table and its setup is described in the Turbo PMAC Software Reference Manual.

Warning

Presently, the non-Turbo PMAC Encoder conversion table does not support the byte-wide parallel word feedback entries (as of the non-Turbo PMAC Firmware release 1.17B).

PMAC Memory Mapping for ACC-14P

The Delta Tau IOGATE ASIC used on the ACC-14P has an 8-bit data bus and therefore the memory mapping to the I/O bits is processed as 8-bit words at the PMAC. Using this simple scheme up to 576 (96×8) bits of data for general purpose I/O can be processed. In the example below, assume the card is addressed to its default setting at base address $78A00.

The data for the first IOGATE is in the lower eight bits of the base address and is mapped as follows:

Data	Location	Turbo Address	Non-Turbo Address
Bits 0-7	Y word of Base Address + 0	Y:$78A00,0,8	Y:$FFD0,0,8
Bits 8-15	Y word of Base Address + 1	Y:$78A01,0,8	Y:$FFD1,0,8
Bits 16-23	Y word of Base Address + 2	Y:$78A02,0,8	Y:$FFD2,0,8
Bits 24-31	Y word of Base Address + 3	Y:$78A03,0,8	Y:$FFD3,0,8
Bits 32-39	Y word of Base Address + 4	Y:$78A04,0,8	Y:$FFD4,0,8
Bits 40-47	Y word of Base Address + 5	Y:$78A05,0,8	Y:$FFD5,0,8
Latch/Mask	Y word of Base Address + 6	Y:$78A06,0,8	Y:$FFD6,0,8
Control Word	Y word of Base Address + 7	Y:$78A07,0,8	Y:$FFD7,0,8

The data for the second IOGATE is in the middle eight bits of the base address and is mapped as follows:

Data	Location	Turbo Address	Non-Turbo Address
Bits 48-55	Y word of Base Address + 0	Y:$78A00,8,8	Y:$FFD0,8,8
Bits 56-63	Y word of Base Address + 1	Y:$78A01,8,8	Y:$FFD1,8,8
Bits 64-71	Y word of Base Address + 2	Y:$78A02,8,8	Y:$FFD2,8,8
Bits 72-79	Y word of Base Address + 3	Y:$78A03,8,8	Y:$FFD3,8,8
Bits 80-87	Y word of Base Address + 4	Y:$78A04,8,8	Y:$FFD4,8,8
Bits 88-95	Y word of Base Address + 5	Y:$78A05,8,8	Y:$FFD5,8,8
Latch/Mask	Y word of Base Address + 6	Y:$78A06,8,8	Y:$FFD6,8,8
Control Word	Y word of Base Address + 7	Y:$78A07,8,8	Y:$FFD7,8,8

Read or write to the data by either pointing M-variables to the memory locations associated with the I/O word or processing it in the encoder conversion table. To use the data properly, set up the control word to process it as inverted/non-inverted logic, binary/grayscale, or latched/transparent data.

ACC-14P IOGATE Control Word

The control register at address {Base + 7} permits the configuration of the IOGATE IC to a variety of applications. The control register consists of eight write/read-back bits – Bits 0 - 7. The control register consists of two sections: Direction Control and Register Select.

The direction control allows the setting of input bytes to be read only. One of the advantages of the IOGATE IC is the ability to define the bits as inputs or outputs. This control mechanism ensures that the inputs will always be read properly. (Traditional I/O accessories have defined the inputs and outputs by hardware.)

The register select bits allow the input or output bytes inversion control or the latching input features to be defined.

Direction Control Bits

Bits 0 to 5 of the control register simply control the direction of the I/O for the matching numbered data register. That is, Bit *n* controls the direction of the I/O at {Base + *n*}. A value of 0 in the control bit (the default) permits a write operation to the data register, enabling the output function for each line in the register. Enabling the output function does not prevent the use of any or all of the lines as inputs, as long as the outputs are off (non-conducting). A value of 1 in the control bit does not permit a write operation to the data register, disabling the output, reserving the register for inputs.

For example, a value of 1 in Bit 3 disables the write function into the data register at address {Base + 3}, ensuring that lines I/O24 – I/O31 can always be used as inputs.

Register Select Control Bits

The control register also allows access to each of the setup registers for each of the 8-bit I/O words. Bits 6 and 7 of the control register together select which of four possible registers can be accessed at each of the addresses {Base + 0} through {Base + 5}. They also select which of two possible registers can be selected at {Base + 6}. The setup registers are accessed only when setting the 8-bit I/O words for:

- Individual inversion control for each I/O point (bit 7 = 0, bit 6 = 1)
- Individual control on inputs of latched or transparent read (bit 7 = 1, bit 6 = 0)
- Automatic conversion of latched Gray code inputs (bit 7 = 1, bit 6 = 1)
- Eight additional inputs for latch control, maskable interrupts, or general inputs

The following table explains how these bits select registers:

Bit 7	Bit 6	Combined Value	{Base + 0} to {Base + 5} Register Selected	{Base + 6} Register Selected
0	0	0	Data Register	Data Register
0	1	1	Setup Register 1	Setup Register
1	0	2	Setup Register 2	n. a.
1	1	3	Setup Register 3	n. a.

In a typical application, non-zero combined values of Bits 6 and 7 are used only for initial configuration of the IC. These values are used to access the setup registers at the other addresses. After the configuration is finished, zeros are written to both Bits 6 and 7, so the data registers at the other registers can be accessed.

Setup Registers

There are four registers accessible at each of the IC addresses {Base + 0} to {Base + 5}: three 8-bit setup registers and an 8-bit data register. The setup registers control how data is written to and read from the data registers.

Setup Register 1: Inversion Control

Setup Register 1 at each address {Base + 0} through {Base + 5} by writing a 1 to Bit 6 of the Control Word at {Base + 7} and a 0 to Bit 7. Register 1 is the inversion control register for the data register at the same address. Each bit of Setup Register 1 controls the inversion of the matching bit of the data register at the same address.

A value of 0 in a bit of Setup Register 1 specifies an inverting I/O point for the matching bit of the data register at the same address. That is, for an output, a value of 0 produces a low (conducting) output, and a value of 1 produces a high (non-conducting) output. For an input, a line pulled low produces a 1 value, and a line pulled high or permitted to float high, produces a 0 value.

A value of 1 in a bit of Setup Register 1 specifies a non-inverting I/O point for the matching bit of the data register at the same address. That is, for an output, a value of 0 produces a high (non-conducting) output, and a value of 1 produces a low (conducting) output. For an input, a line pulled low produces a 0 value, and a line pulled high or permitted to float high, produces a 1 value.

Setup Register 2: Read Control

Setup Register 2 at each address {Base + 0} through {Base + 5} by writing a 0 to Bit 6 of the Control Word at {Base + 7} and a 1 to Bit 7. Register 2 is the read control register for the data register at the same address. Each bit of Setup Register 2 controls what data is read from the matching bit of the data register at the same address.

The action of a bit of Setup Register 2 is dependent on the setting of the matching bit of Setup Register 3 for the same address. If the matching bit of Setup Register 3 is 0, selecting unlatched inputs, the bit of Setup Register 2 controls whether the pin value is read, or the value in the writeable register is read. A value of 0 in the bit of Setup Register 2 selects the pin value to be read from the matching bit of the Data Register at the same address; a value of 1 in the bit selects the writeable register value.

If the matching bit of Setup Register 3 is 1, selecting latched inputs, the bit of Setup Register 2 controls whether the directly latched data is read, or the value that is the result of a Gray-code-to-binary conversion. A value of 0 in the bit of Setup Register 2 selects the directly latched value to be read from the matching bit of the data register at the same address; a value of 1 in the bit selects the value that is the result of a Gray-code-to-binary conversion.

Setup Register 3: Latch Control

Setup Register 3 at each address {Base + 0} through {Base + 5} by writing a 1 to Bit 6 of the Control Word at {Base + 7} and a 1 to Bit 7. Register 3 is the latch control register for the data register at the same address. Each bit of Setup Register 3 controls whether latched or unlatched data is read from the matching bit of the data register at the same address.

A value of 0 in the bit of Setup Register 3 selects unlatched data to be read from the matching bit of the data register at the same address; a value of 1 in the bit selects latched data to be read.

For both the latched and unlatched settings, the matching bit of Setup Register 2 controls exactly what type of data is read from the data register.

Data Registers

The data register at each address {Base + 0} through {Base + 5}, which is selected by writing a 0 to Bit 6 of the Control Register at {Base + 7} and a 0 to Bit 7, provides the working interface for the eight input/output lines matched to that address. The processor reads from or writes to the data register to access the input/output lines.

If there is a value of 1 in Bit *n* (*n* = 0 to 5) of the Control Word, a write operation to the data register at address {Base + *n*} has no effect on the I/O line, effectively disabling the output function for all eight lines associated with the register.

A read operation from a data register can access one of four types of data for each I/O line associated with the register (individually selectable), depending on how the Setup Registers 2 and 3 at the same address have been configured.

The following table summarizes how the Setup Register bits control what data is read in the matching bit of the Data Register:

Setup Register 3 Bit Value	Setup Register 2 Bit Value	Data Type Read
0	0	Pin Value Read
0	1	Writeable Register Read
1	0	Latched Input Read
1	1	Converted Gray Code Read

Inversion Control Example:

```
M2007->Y:$078A07,0,8     ;control word for bits 0-47
M2000->Y:$078A00,0,8     ;I/O bits 0-7
M2001->Y:$078A01,0,8     ;I/O bits 8-15
M2002->Y:$078A02,0,8     ;I/O bits 16-23

M2007=$40                ;access inversion control (Setup Register 1)
M2000=$00                ;inverting logic for bits 0-7 (default)
M2001=$00                ;inverting logic for bits 8-15 (default)
M2002=$FF                ;non-inverting logic for bits 16-23
```

Latch-Gray and Latch-Binary Scale Example:

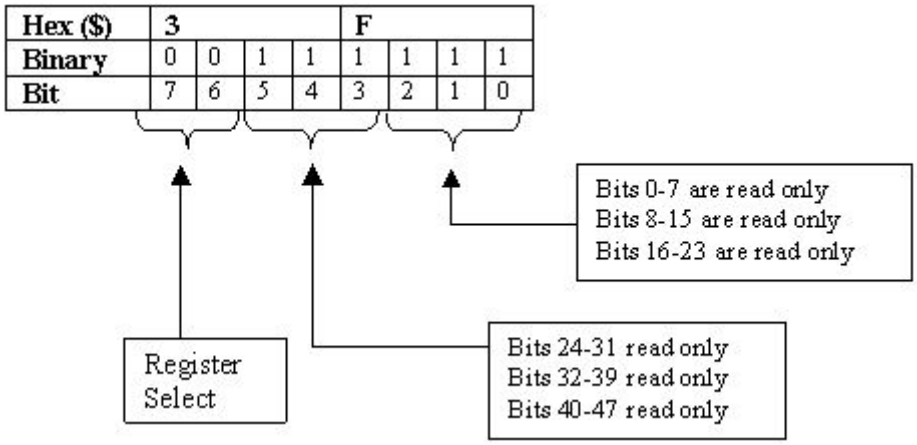
```
M2007->Y:$078A07,0,8     ;control word for bits 0-47
M2000->Y:$078A00,0,8     ;I/O bits 0-7
M2001->Y:$078A01,0,8     ;I/O bits 8-15
M2002->Y:$078A02,0,8     ;I/O bits 16-23
M2003->Y:$078A03,0,8     ;I/O bits 24-31
M2004->Y:$078A04,0,8     ;I/O bits 32-39
M2005->Y:$078A05,0,8     ;I/O bits 40-47

M2007=$C0                ;access Read control (Setup Register 3)
M2000=$FF                ;Latch bits 0-7
M2001=$FF                ;Latch 8-15
M2002=$FF                ;Latch 16-23
```

To complete the latch setup, write to the control word.

Control Word Setup Example

The control words for the I/O card must be set up at power up. A simple PLC can be written to setup the control word properly. In this example, a fully populated ACC-14P addressed at $78A00 will be set up. Bits 0-47 will be set up as read only inputs and bits 48-95 as read/write outputs.

Control Word for ACC-14P (M2007->Y:$078A07,0,8)




```
M2000->Y:$078A00,0,8        ;I/O bits 0-7
M2001->Y:$078A01,0,8        ;I/O bits 8-15
M2002->Y:$078A02,0,8        ;I/O bits 16-23
M2003->Y:$078A03,0,8        ;I/O bits 23-31
M2004->Y:$078A04,0,8        ;I/O bits 32-39
M2005->Y:$078A05,0,8        ;I/O bits 40-47
M2006->Y:$078A06,0,8        ;register selected
M2007->Y:$078A07,0,8        ;control register

M2008->Y:$078A00,8,8        ;I/O bits 48-55
M2009->Y:$078A01,8,8        ;I/O bits 56-63
M2010->Y:$078A02,8,8        ;I/O bits 64-71
M2011->Y:$078A03,8,8        ;I/O bits 72-79
M2012->Y:$078A04,8,8        ;I/O bits 80-87
M2013->Y:$078A05,8,8        ;I/O bits 88-95
M2014->Y:$078A06,8,8        ;register selected
M2015->Y:$078A07,8,8        ;control register

M2007->Y:$078A07,0,8        ;control word for $78C00,0,8 - $78C05,0,8
M2015->Y:$078A07,8,8        ;control word for $78A00,0,8 - $79C05,0,8

;**** PLC to initialize read/write I/O bits ****
OPEN PLC 1 CLEAR
M2007=$3F             ;define bits 0-23 and 24-47 as inputs (ACC-14P)
M2015=$00             ;define bits 48-71 and 72-95 as outputs (ACC-14P)
DIS PLC1
CLOSE
```

Accessory-14P I/O M-Variables for Turbo PMAC

The following is a list of suggested M-variables for the default jumper settings is provided. Any M-variables may be assigned to these addresses. For this example, assume 24 inputs and 24 outputs. These M-variable definitions may be used as general purpose I/O for PLCs or motion programs.

M7000->Y:$078A00,0,1	Bit 0	**M7024->Y:$078A03,0,1**	Bit 24
M7001->Y:$078A00,1,1	Bit 1	**M7025->Y:$078A03,1,1**	Bit 25
M7002->Y:$078A00,2,1	Bit 2	**M7026->Y:$078A03,2,1**	Bit 26
M7003->Y:$078A00,3,1	Bit 3	**M7027->Y:$078A03,3,1**	Bit 27
M7004->Y:$078A00,4,1	Bit 4	**M7028->Y:$078A03,4,1**	Bit 28
M7005->Y:$078A00,5,1	Bit 5	**M7029->Y:$078A03,5,1**	Bit 29
M7006->Y:$078A00,6,1	Bit 6	**M7030->Y:$078A03,6,1**	Bit 30
M7007->Y:$078A00,7,1	Bit 7	**M7031->Y:$078A03,7,1**	Bit 31
M7008->Y:$078A01,0,1	Bit 8	**M7032->Y:$078A04,0,1**	Bit 32
M7009->Y:$078A01,1,1	Bit 9	**M7033->Y:$078A04,1,1**	Bit 33
M7010->Y:$078A01,2,1	Bit 10	**M7034->Y:$078A04,2,1**	Bit 34
M7011->Y:$078A01,3,1	Bit 11	**M7035->Y:$078A04,3,1**	Bit 35
M7012->Y:$078A01,4,1	Bit 12	**M7036->Y:$078A04,4,1**	Bit 36
M7013->Y:$078A01,5,1	Bit 13	**M7037->Y:$078A04,5,1**	Bit 37
M7014->Y:$078A01,6,1	Bit 14	**M7038->Y:$078A04,6,1**	Bit 38
M7015->Y:$078A01,7,1	Bit 15	**M7039->Y:$078A04,7,1**	Bit 39
M7016->Y:$078A02,0,1	Bit 16	**M7040->Y:$078A05,0,1**	Bit 40
M7017->Y:$078A02,1,1	Bit 17	**M7041->Y:$078A05,1,1**	Bit 41
M7018->Y:$078A02,2,1	Bit 18	**M7042->Y:$078A05,2,1**	Bit 42
M7019->Y:$078A02,3,1	Bit 19	**M7043->Y:$078A05,3,1**	Bit 43
M7020->Y:$078A02,4,1	Bit 20	**M7044->Y:$078A05,4,1**	Bit 44
M7021->Y:$078A02,5,1	Bit 21	**M7045->Y:$078A05,5,1**	Bit 45
M7022->Y:$078A02,6,1	Bit 22	**M7046->Y:$078A05,6,1**	Bit 46
M7023->Y:$078A02,7,1	Bit 23	**M7047->Y:$078A05,7,1**	Bit 47

```
;****** Sample E-Stop PLC *****
; This PLC will abort all motion programs and kill the bus voltage to
; the motors when E-stop is depressed.  When E-Stop button in pulled out
; the motors will servo to actual position (<ctrl> A command) after
; allowing 5 seconds for proper bus voltage.

;P7000 used as a Latch variable
;M7000 used Emergency Stop Input
;M7024 used as Main Contact for main AC for Bus Voltage
;I5111 used as count down timer (Turbo PMAC)

OPEN PLC 5 CLEAR
IF (M7000=1 and P7000=0)    ;emergency stop condition
    CMD^A                   ;global motion program abort
    I5111=500*8388608/I10   ;500 msec delay for deceleration
    WHILE (I5111>0)//
ENDWHILE
    CMD^K                   ;kill all axes
    M7024=0                 ;turn off BUS voltage
    P7000=1                 ;latch input
ENDIF
```

```
IF (M7000=0 and P7000=1)
    M7024=1                     ;enable BUS voltage
    I5111=5000*8388608/I10      ;5000 msec delay for bus voltage
    WHILE (I5111>0)//
ENDWHILE
    CMD^A                       ;close loop for all servos
    P7000=0                     ;latch input
ENDIF
CLOSE
```

Closed-Loop Control Using Acc-14P

If providing position information to Turbo PMAC as a parallel data word, as from an absolute encoder or processed from a laser interferometer, the encoder conversion table must be configured properly.

The encoder conversion table can be modified using either PMAC's Executive Program Encoder Conversion Table dialog box or the on-line commands in the Executive terminal mode. The following sections describe in detail PMAC's ACC-14P parallel feedback conversion process and actual setup.

Extended Entries ($F):

Encoder conversion table entries in which the first hex digit of the first line is $F are extended entries. In these entries, the actual method is dependent on the first digit of the second line. Extended entries are a minimum of two lines.

Byte-Wide Parallel Feedback Entries ($F/$2, $F/$3):

An ECT entry in which the first hex digit of the first line is $F and the first hex digit of the second line is $2 or $3, processes the result of a parallel data feedback source whose data is in byte-wide pieces in consecutive Y-words. This is used to process feedback from 3U-format parallel-data I/O boards: the ACC-3E in stack form, and the ACC-14E in pack (UMAC) form.

Address Word:

The first setup line (I-variable) of the entry contains $F in the first hex digit (bits 20-23). The bit-19 mode-switch bit in the first line controls whether the least significant bit (LSB) of the source register is placed in bit 5 of the result register (normal shift), providing the standard five bits of (non-existent) fraction, or the LSB is placed in Bit 0 of the result register (unshifted), creating no fractional bits.

Normally, the Bit-19 mode switch is set to 0 to place the source LSB in Bit 5 of the result register. Bit 19 is set to 1 to place the source LSB in Bit 0 of the result register for one of three reasons:

- The data already comes with five bits of fraction, as from a Compact MACRO Station.
- The normal shift limits the maximum velocity too much ($V_{max}<2^{18}$ LSBs per servo cycle)
- The normal shift limits the position range too much (Range$<\pm 2^{47}$/Ix08/32 LSBs)

Unless this is done because the data already contains fractional information, the unshifted conversion will mean that the motor position loop will consider one LSB of the source to be 1/32 of a count, instead of one count.

Bits 0 to 18 of the first line contain the base address of the parallel data to be read. This is the address of the least significant byte in the parallel feedback word. The following table shows the possible entries when an ACC-14P I/O board is used:

When the ACC-14P UMAC I/O board is used, the possible entries are shown below:

$F78A0x	**$F78B0x**
$F78C0x	**$F78D0x**
$F78E0x	**$F78F0x**

In both of these tables, if bit 19 is set to 1 to disable the data shift, the second digit should be changed from a 7 to an F.

The final digit, represented by an x in both of these tables, can take a value of 0 to 5, depending on which I/O point on the board is used for the LSB:

```
x=0:  I/O00-07   I/O48-55   I/O96-103
x=1:  I/O08-15   I/O56-63   I/O104-111
x=2:  I/O16-23   I/O64-71   I/O112-119
x=3:  I/O24-31   I/O72-79   I/O120-127
x=4:  I/O32-39   I/O80-87   I/O128-135
x=5:  I/O40-47   I/O88-95   I/O136-143
```

Width/Offset Word

The second setup line (I-variable) of this parallel read entry contains information about what data is to be read starting at the base address. This 24-bit value, usually represented as six hexadecimal digits, is split into four parts, as shown in the following table.

Hex Digit	**1**	**2**	**3**	**4**	**5**	**6**
Contents	2 or 3	Bit Width		Byte	LSB Location	

The first hex digit contains a 2 or a 3. If it has a 2, there is no filtering of the data, and the entry is a 2-line entry. If it has a 3, the input data is filtered to protect against noise or data corruption, and the entry is a 3-line entry, with the third line controlling the filtering.

The second and third digits represent the width of the parallel data in bits, and can range from $01 (1 bit wide – not of much practical use) to $18 (24 bits wide). If the value of these digits is from $01 to $08, only the base address in the first line is used. If the value of these digits is from $09 to $10 (16), the base address and the next higher-numbered address are used. If the value of these digits is from $11 to $18 (17 to 24), three addresses starting at the base address are used.

The fourth digit represents which byte of the source words is used. It has three valid values:

- 0: Low byte (bits 0 – 7)
- 1: Middle byte (bits 8 – 15)
- 2: High byte (bits 16 – 23)

The fifth and sixth digits contain the bit location of the LSB of the data in the source word at the base address, and can range from $00 (Bit 0 of the source address is the LSB), through $07 (Bit 7 of the source address is the LSB). To calculate this value, divide the number of the I/O point used for the LSB by eight and use the remainder here. For example, if I/O19 is used for the LSB, the remainder of 19/16 is 3.

Maximum Change Word

If the method character for a parallel read is $3 or $7, specifying filtered parallel read, there is a third setup line (I-variable) for the entry. This third line contains the maximum change in the source data in a single cycle that will be reflected in the processed result, expressed in LSBs per servo cycle. The filtering that this creates provides an important protection against noise and misreading of data. This number is effectively a velocity value, and should be set slightly greater than the maximum true velocity ever expected.

Example Turbo Encoder Conversion Table Setup for ACC-14P

Two 18-bit encoders are used in an application with 10000 cts/in and a maximum velocity of 20 in/sec is specified. Accessory-14P port A will be used for the first encoder and port B will be used for the second encoder. The servo update rate is set at the factory default of 2258Hz. For this example, an encoder is set up with filtering, without filtering, and with 24-bit resolution.

First, calculate the maximum velocity per servo cycle:

$$V_{max} = \frac{10000cts}{in} \times \frac{20in}{sec} \times \frac{sec}{2258cyc} = \frac{88.57cts}{cyc}$$

ECT Setup for 18-bit Encoder without Filtering

```
I8000=$F78A00          ;extended feedback entry from $078C00 ($3501)
I8001=$212000          ;18-bit ($12) from $078C00 base 0 ($3502)
I8002=$F78A03          ;extended feedback entry from $078C03 ($3503)
I8003=$212000          ;18-bit ($12) from $078C03 base 0 ($3504)

I103=$3502             ;position feedback for motor 1 from $3502
I104=$3502             ;velocity feedback for motor 1 from $3502
I203=$3504             ;position feedback for motor 2 from $3504
I204=$3504             ;velocity feedback for motor 2 from $3504
```

ECT Setup for 18-bit Encoder with Filtering

```
I8000=$F78A00          ;extended feedback entry from $078C00    ($3501)
I8001=$312000          ;18-bit ($12) from $078C00 base 0        ($3502)
I8002=110              ;filter 110cts/cyc  (88.57*1.25)         ($3503)
I8003=$F78A03          ;extended feedback entry from $078C03    ($3504)
I8004=$312000          ;18-bit ($12) from $078C03 base 0        ($3505)
I8005=110              ;filter 110cts/cyc  (88.57*1.25)         ($3506)

I103=$3503             ;position feedback for motor 1 from $3502
I104=$3503             ;velocity feedback for motor 1 from $3502
I203=$3506             ;position feedback for motor 2 from $3504
I204=$3506             ;velocity feedback for motor 2 from $3504
```

ABSOLUTE ENCODER LATCHING AND HANDSHAKING

When using a parallel-word absolute encoder, it is important to properly latch the encoder data to prevent PMAC from reading the encoder data during an encoder transition. ACC-14P allows several latching and handshaking methods to fit most types of latching schemes.

Note

It is important to set up the Encoder Conversion Table Filter Word as a software protection against bad encoder data.

PMAC reads the encoder data when it processes the Encoder Conversion Tables. This happens shortly (approximately 2 μsec) after the falling edge of the servo clock (the phase calculations are performed first). Therefore, most of the following latching methods will be synchronized to the falling edge of the servo clock.

The error signal inputs (ERR1/ and ERR2/) allow the feedback device to send a signal to the latch circuit to interrupt the latch. Jumpers E8 and E10 are used to set the polarity for the error inputs signals. If the feedback device does not have an error signal output, then set the jumpers E8 and E10 from 1-2 to allow the latch circuit to work properly.

ACC-14P Latching Setup

For the following examples, a standard 24-bit absolute encoder will be read from port A and port B of the first ACC-14P at base address Y:$078A00 for the Turbo PMAC.

The 24-bits of data will be addressed to:

```
M2000->Y:$078A00,0,8  ;Bits 0-7 for absolute encoder port A
M2001->Y:$078A01,0,8  ;Bits 8-15 for absolute encoder port A
M2002->Y:$078A02,0,8  ;Bits 16-23 for absolute encoder port A
M2003->Y:$078A03,0,8  ;Bits 24-31 for absolute encoder port B
M2004->Y:$078A04,0,8  ;Bits 32-39 for absolute encoder port B
M2005->Y:$078A05,0,8  ;Bits 40-47 for absolute encoder port B

M2007->Y:$078A07,0,8  ;Control word to setup Latch
```

Enabling ACC-14P Latching for Turbo PMAC

To enable the ACC-14P latching mechanism, set up each bit of the input word to be latched. This is accomplished by writing to the Setup Variable 2 and Setup Variable 3 when accessed by bits 6 and 7 of the control word.

Setup Variable 2 (Control Word Bit 6=0 and Bit 7=1)

```
M2007=$80             ;Address Setup Variable 2 for Binary or Graycode
M2000=$00             ;Binary Data Read ($FF for Graycode) for bits 0-7
                      ;port A
M2001=$00             ;Binary Data Read ($FF for Graycode) for bits
                      ;8-15 port A
M2002=$00             ;Binary Data Read ($FF for Graycode) for bits
                      ;16-23 port A
M2003=$00             ;Binary Data Read ($FF for Graycode) for bits
                      ;24-31 port B
M2004=$00             ;Binary Data Read ($FF for Graycode) for bits
                      ;32-39 port B
M2005=$00             ;Binary Data Read ($FF for Graycode) for bits
                      ;40-47 port B
```

Setup Variable 3 (Control Word Bit 6=1 and Bit 7=1)

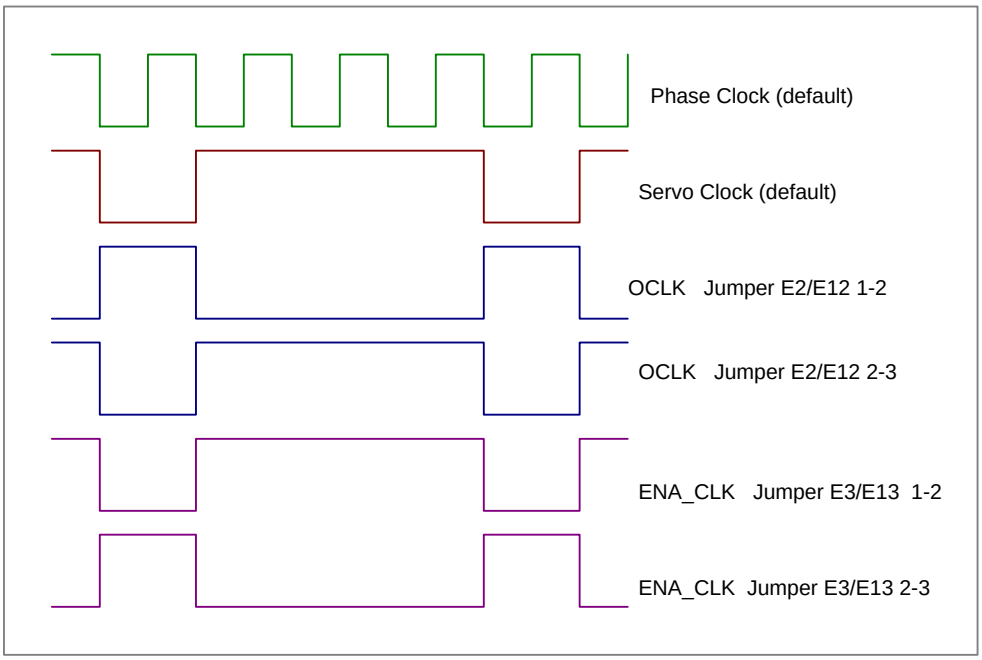
```
M2007=$C0          ;Address Setup Variable 2 for Binary or Graycode
M2000=$FF          ;Latched Data Read ($00 for unlatched) for bits
                   ;0-7 port A
M2001=$FF          ;Latched Data Read ($00 for unlatched) for bits
                   8-15 port A
M2002=$FF          ;Latched Data Read ($00 for unlatched) for bits
                   16-23 port A
M2003=$FF          ;Latched Data Read ($00 for unlatched) for bits
                   24-31 port B
M2004=$FF          ;Latched Data Read ($00 for unlatched) for bits
                   32-39 port B
M2005=$FF          ;Latched Data Read ($00 for unlatched) for bits
                   40-47 port B
```

Once the method of latching has been defined, then set up the control word to read the data. It is also recommended to setup the bits of the encoder inputs to be read only as shown below.

```
M2007=$3F          ;ensure bits 0-23 (portA) and 24-47 (port B) are
                   ;read
```

ACC-14P Latching Examples

The ACC-14P card allows latching the data from the feedback device many different ways. This following section will show how to set up the ACC-14P to latch data on the first two connectors associated with the first IOGATE. In most cases, the data will be latched based on the Servo clock because PMAC will update the data in the encoder conversion table according to the Servo clock. The latching of the data is based on the following clock designations:



Method 1

This method requires the encoder outputs to be latched on the falling edge of the servo clock and no latching to be done on ACC-14P. For latching the encoder outputs, the servo clock is accessed through ACC-14P OCLK_1_2 and/or OCLK_3_4. If the encoder requires a rising edge for its latch, then E2/E12 should be jumpered 1 to 2 for OCLK1_2. If a falling edge is required, E2/E12 should be jumpered 2 to 3.

Required Signal	E2	E3	E4/E6	Latch
Rising edge of OCLK	1 to 2	Off	1 to 2	No
Falling edge of OCLK	2 to 3	Off	1 to 2	No

The advantage of this method is that it is easy to configure and set up. The disadvantage is that typically the encoder's output latch must happen within 2 μsec.

Method 2

This method requires the encoder outputs to be latched on the rising edge of the servo clock and ACC-14P to latch (strobe) the encoder inputs on the falling edge of the servo clock. For latching the encoder outputs, the servo clock is accessed through ACC-14P OCLK1_2 and/or OCLK_3_4. If the encoder requires a rising edge for its latch, then E2 should be jumpered 1 to 2 for OCLK1/OCLK2, respectively. If a falling edge is required, E2 should be jumpered 2 to 3. The control words for the data must be set up for latching to allow the ACC-14E to latch the data. The Input Latch jumper will set up the circuit to latch as either a 5V input or 0V input.

Required Signal	E2	E3	E4/E6	Latch
Rising edge of OCLK	1 to 2	1 to 2	On/Off	Yes
Falling edge of OCLK	2 to 3	1 to 2	On/Off	Yes

The advantage of this method is that the encoder latch time is not critical (almost one servo cycle to latch). The disadvantage is that there is almost a one servo-cycle delay between the encoder output latch and the ACC-14E encoder read.

Method 3

This method requires a self-latching encoder that outputs a signal that indicates it is latched and an ACC-14P that latches (strobes) the encoder inputs on the falling edge of the ICLK only when the servo clock is low. The encoder-latched indicator is brought into ACC-14P via the ICLK. If the encoder outputs a rising edge for its latch indicator, then E4/E6 should be jumpered, so that a rising ICLK latches the data when the servo is low. If a falling edge indicator is output, E4/E6 should not be jumpered, so that a falling ICLK latches the data when the servo is low. The control words for the data must be set up for latching to allow the ACC-14E to latch the data.

Required Signal	E2	E3	E4/E6	Latch
High ICLK means latched	Don't care	2 to 3	On	Yes
Low ICLK means latched	Don't care	2 to 3	Off	Yes

The advantage of this method is that only latched encoder data can be read. The disadvantage is that the encoder latch is asynchronous to PMAC's servo cycle.

Method 4

This method is a combination of 1 and 3. It requires that the encoder outputs be latched on the falling edge of the servo clock and the encoder to signal that it is latched. In addition, ACC-14P must latch (strobe) the encoder inputs on an edge of the ICLK only when the servo clock is low. For latching the encoder outputs, the servo clock is accessed through ACC-14P OCLK_1_2 and/or OCLK_3_4. If the encoder requires a rising edge for its latch, then E2 should be jumpered 1 to 2 for OCLK_1_2. If a falling edge is required, E2 should be jumpered 2 to 3. The encoder latched indicator is brought into ACC-14P via the ICLK inputs. If the encoder outputs a rising edge for its latch indicator, then E4/E6 should be jumpered so that a rising ICLK latches the data when the servo is low. If a falling edge indicator is output, E4/E6 should not be jumpered so that a falling ICLK latches the data when the servo is low. The control words for the data must be set up for latching to allow the ACC-14E to latch the data.

Required Signal	E2	E3	E4/E6	Latch
High OCLK means latch High ICLK means latched	1 to 2	2 to 3	On	Yes
Low OCLK means latch High ICLK means latched	2 to 3	2 to 3	On	Yes
High OCLK means latch Low ICLK means latched	1 to 2	2 to 3	Off	Yes
Low OCLK means latch Low ICLK means latched	2 to 3	2 to 3	Off	Yes

The advantage of this method is that only latched encoder data can be read and there is full handshaking between PMAC and the encoder. The disadvantage of this method is that, typically, the encoder's output latch must happen within 2 μsec and there is more complex wiring and timing involved.

Method 5

This method requires no latching on the encoder outputs and latching on the ACC-14P inputs at the falling edge of the servo clock. For the encoder, no signals are used so the state of the OCLK does not matter. E4 and E6 must be jumpered and latching must be enabled from the control to allow ACC-14P to latch (strobe) its inputs with the falling edge of the servo clock. The control words for the data must be setup for latching to allow the ACC-14P latch the data.

Required Signal	E2	E3	E4/E6	Latch
Latch at Falling Edge	Don't care	2 to 3	On	Yes
Latch at Rising Edge	Don't care	1 to 2	On	Yes

The advantage of this method is that it is easy to configure and set up. The disadvantage is that the encoder data may be latched into ACC-14P at an encoder transition causing bad encoder data for that servo cycle. An Encoder Conversion Table Filter must be set up.

I/O TERMINAL CONNECTOR PINOUTS

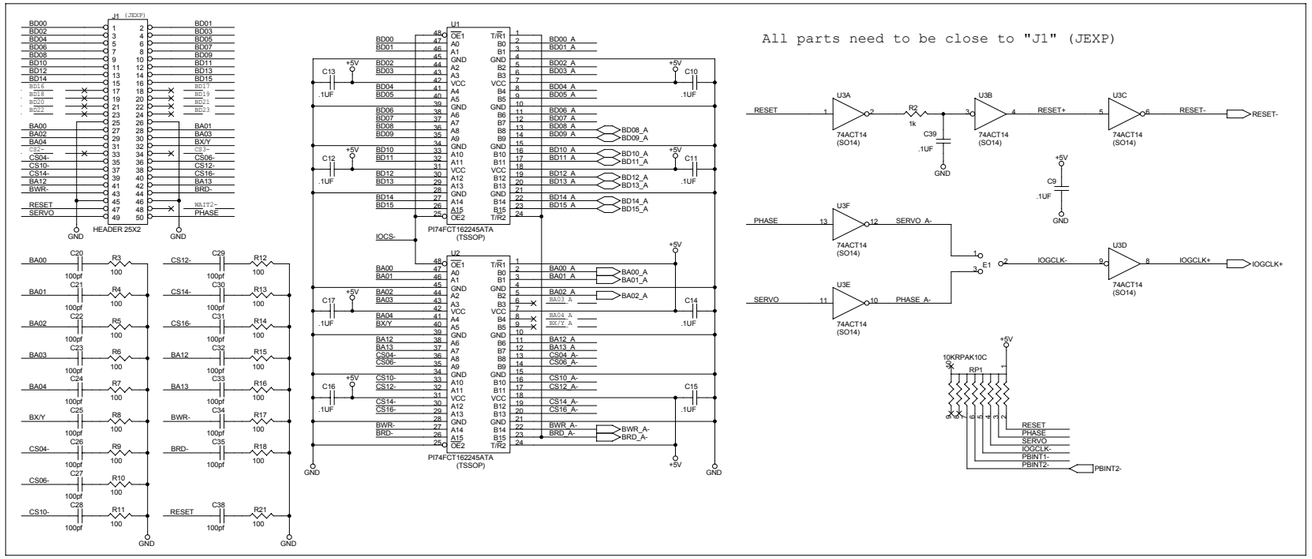
J3 (50 Pin Header)			
Pin	**Symbol**	**Function**	**Description**
1	MI/O23	In/out	I/O at base address, bit 23
2	GND	Common	PMAC common
3	MI/O22	In/out	I/O at base address, bit 22
4	GND	Common	PMAC common
5	MI/O21	In/out	I/O at base address, bit 21
6	GND	Common	PMAC common
7	MI/O20	In/out	I/O at base address, bit 20
8	GND	Common	PMAC common
9	MI/O19	In/out	I/O at base address, bit 19
10	GND	Common	PMAC common
11	MI/O18	In/out	I/O at base address, bit 18
12	GND	Common	PMAC common
13	MI/O17	In/out	I/O at base address, bit 17
14	GND	Common	PMAC common
15	MI/O16	In/out	I/O at base address, bit 16
16	GND	Common	PMAC common
17	MI/O15	In/out	I/O at base address, bit 15
18	GND	Common	PMAC common
19	MI/O14	In/out	I/O at base address, bit 14
20	GND	Common	PMAC common
21	MI/O13	In/out	I/O at base address, bit 13
22	GND	Common	PMAC common
23	MI/O12	In/out	I/O at base address, bit 12
24	GND	Common	PMAC common
25	MI/O11	In/out	I/O at base address, bit 11
26	GND	Common	PMAC common
27	MI/O10	In/out	I/O at base address, bit 10
28	GND	Common	PMAC common
29	MI/O9	In/out	I/O at base address, bit 9
30	GND	Common	PMAC common
31	MI/O8	In/out	I/O at base address, bit 8
32	GND	Common	PMAC common
33	MI/O7	In/out	I/O at base address, bit 7
34	GND	Common	PMAC common
35	MI/O6	In/out	I/O at base address, bit 6
36	GND	Common	PMAC common
37	MI/O5	In/out	I/O at base address, bit 5
38	GND	Common	PMAC common
39	MI/O4	In/out	I/O at base address, bit 4
40	GND	Common	PMAC common
41	MI/O3	In/out	I/O at base address, bit 3
42	GND	Common	PMAC common
43	MI/O2	In/out	I/O at base address, bit 2
44	ERR1	Input	Error signal
45	MI/O1	In/out	I/O at base address, bit 1
46	ICLK1	Input	
47	MI/O0	In/out	I/O at base address, bit 0
48	OCLK1	Output	
49	+V	Output	5V power
50	GND	Common	

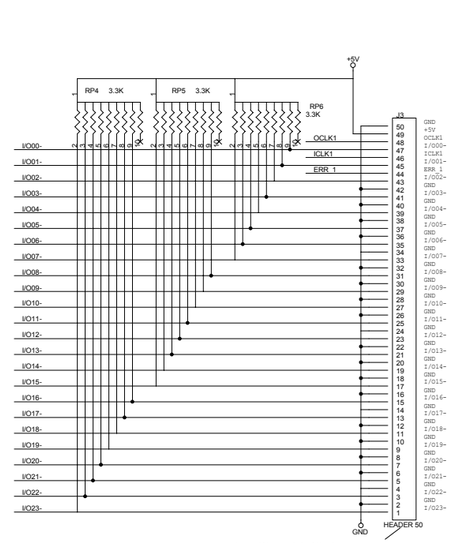
J4 (50 Pin Header)			
Pin	**Symbol**	**Function**	**Description**
1	MI/O47	In/Out	I/O at base address, bit 47
2	GND	Common	PMAC common
3	MI/O46	In/Out	I/O at base address, bit 46
4	GND	Common	PMAC common
5	MI/O45	In/Out	I/O at base address, bit 45
6	GND	Common	PMAC common
7	MI/O44	In/Out	I/O at base address, bit 44
8	GND	Common	PMAC common
9	MI/O43	In/Out	I/O at base address, bit 43
10	GND	Common	PMAC common
11	MI/O42	In/Out	I/O at base address, bit 42
12	GND	Common	PMAC common
13	MI/O41	In/Out	I/O at base address, bit 41
14	GND	Common	PMAC common
15	MI/O40	In/Out	I/O at base address, bit 40
16	GND	Common	PMAC common
17	MI/O39	In/Out	I/O at base address, bit 39
18	GND	Common	PMAC common
19	MI/O38	In/Out	I/O at base address, bit 38
20	GND	Common	PMAC common
21	MI/O37	In/Out	I/O at base address, bit 37
22	GND	Common	PMAC common
23	MI/O36	In/Out	I/O at base address, bit 36
24	GND	Common	PMAC common
25	MI/O35	In/Out	I/O at base address, bit 35
26	GND	Common	PMAC common
27	MI/O34	In/Out	I/O at base address, bit 34
28	GND	Common	PMAC common
29	MI/O33	In/Out	I/O at base address, bit 33
30	GND	Common	PMAC common
31	MI/O32	In/Out	I/O at base address, bit 32
32	GND	Common	PMAC common
33	MI/O31	In/Out	I/O at base address, bit 31
34	GND	Common	PMAC common
35	MI/O30	In/Out	I/O at base address, bit 30
36	GND	Common	PMAC common
37	MI/O29	In/Out	I/O at base address, bit 29
38	GND	Common	PMAC common
39	MI/O28	In/Out	I/O at base address, bit 28
40	GND	Common	PMAC common
41	MI/O27	In/Out	I/O at base address, bit 27
42	GND	Common	PMAC common
43	MI/O26	In/Out	I/O at base address, bit 26
44	ERR2	Input	Error signal
45	MI/O25	In/Out	I/O at base address, bit 25
46	ICLK2	Input	
47	MI/O24	In/Out	I/O at base address, bit 24
48	OCLK2	Output	
49	+V	Output	5v
50	GND	Common	

J5 (50 Pin Header) Option 1 only			
Pin	**Symbol**	**Function**	**Description**
1	MI/O71	In/out	I/O at base address, bit 47
2	GND	Common	PMAC common
3	MI/O70	In/out	I/O at base address, bit 46
4	GND	Common	PMAC common
5	MI/O69	In/out	I/O at base address, bit 45
6	GND	Common	PMAC common
7	MI/O68	In/out	I/O at base address, bit 44
8	GND	Common	PMAC common
9	MI/O67	In/out	I/O at base address, bit 43
10	GND	Common	PMAC common
11	MI/O66	In/out	I/O at base address, bit 42
12	GND	Common	PMAC common
13	MI/O65	In/out	I/O at base address, bit 41
14	GND	Common	PMAC common
15	MI/O64	In/out	I/O at base address, bit 40
16	GND	Common	PMAC common
17	MI/O63	In/out	I/O at base address, bit 39
18	GND	Common	PMAC common
19	MI/O62	In/out	I/O at base address, bit 38
20	GND	Common	PMAC common
21	MI/O61	In/out	I/O at base address, bit 37
22	GND	Common	PMAC common
23	MI/O60	In/out	I/O at base address, bit 36
24	GND	Common	PMAC common
25	MI/O59	In/out	I/O at base address, bit 35
26	GND	Common	PMAC common
27	MI/O58	In/out	I/O at base address, bit 34
28	GND	Common	PMAC common
29	MI/O57	In/out	I/O at base address, bit 33
30	GND	Common	PMAC common
31	MI/O56	In/out	I/O at base address, bit 32
32	GND	Common	PMAC common
33	MI/O55	In/out	I/O at base address, bit 31
34	GND	Common	PMAC common
35	MI/O54	In/out	I/O at base address, bit 30
36	GND	Common	PMAC common
37	MI/O53	In/out	I/O at base address, bit 29
38	GND	Common	PMAC common
39	MI/O52	In/out	I/O at base address, bit 28
40	GND	Common	PMAC common
41	MI/O51	In/out	I/O at base address, bit 27
42	GND	Common	PMAC common
43	MI/O50	In/out	I/O at base address, bit 26
44	ERR3	Input	Error signal
45	MI/O49	In/out	I/O at base address, bit 25
46	ICLK3	Input	
47	MI/O48	In/out	I/O at base address, bit 24
48	OCLK3	Output	
49	+V	Output	5v
50	GND	Common	

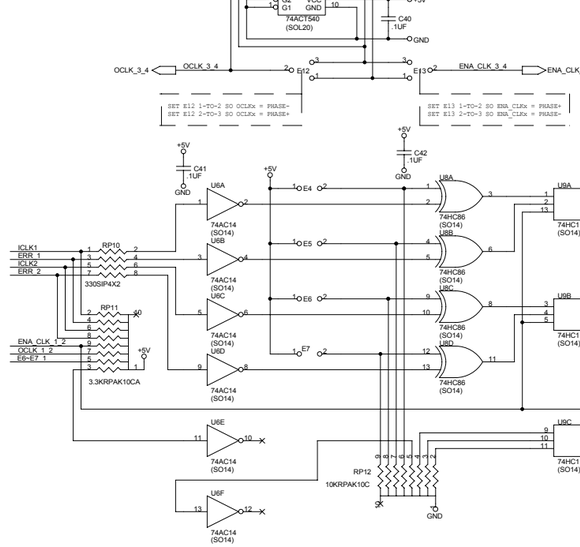
J6 (50 Pin Header) Option 1 only			
Pin	**Symbol**	**Function**	**Description**
1	MI/O95	In/out	I/O at base address, bit 47
2	GND	Common	PMAC common
3	MI/O94	In/out	I/O at base address, bit 46
4	GND	Common	PMAC common
5	MI/O93	In/out	I/O at base address, bit 45
6	GND	Common	PMAC common
7	MI/O92	In/out	I/O at base address, bit 44
8	GND	Common	PMAC common
9	MI/O91	In/out	I/O at base address, bit 43
10	GND	Common	PMAC common
11	MI/O90	In/out	I/O at base address, bit 42
12	GND	Common	PMAC common
13	MI/O89	In/out	I/O at base address, bit 41
14	GND	Common	PMAC common
15	MI/O88	In/out	I/O at base address, bit 40
16	GND	Common	PMAC common
17	MI/O87	In/out	I/O at base address, bit 39
18	GND	Common	PMAC common
19	MI/O86	In/out	I/O at base address, bit 38
20	GND	Common	PMAC common
21	MI/O85	In/out	I/O at base address, bit 37
22	GND	Common	PMAC common
23	MI/O84	In/out	I/O at base address, bit 36
24	GND	Common	PMAC common
25	MI/O83	In/out	I/O at base address, bit 35
26	GND	Common	PMAC common
27	MI/O82	In/out	I/O at base address, bit 34
28	GND	Common	PMAC common
29	MI/O81	In/out	I/O at base address, bit 33
30	GND	Common	PMAC common
31	MI/O80	In/out	I/O at base address, bit 32
32	GND	Common	PMAC common
33	MI/O79	In/out	I/O at base address, bit 31
34	GND	Common	PMAC common
35	MI/O78	In/out	I/O at base address, bit 30
36	GND	Common	PMAC common
37	MI/O77	In/out	I/O at base address, bit 29
38	GND	Common	PMAC common
39	MI/O76	In/out	I/O at base address, bit 28
40	GND	Common	PMAC common
41	MI/O75	In/out	I/O at base address, bit 27
42	GND	Common	PMAC common
43	MI/O74	In/out	I/O at base address, bit 26
44	ERR4	Input	Error signal
45	MI/O73	In/out	I/O at base address, bit 25
46	ICLK4	Input	
47	MI/O72	In/out	I/O at base address, bit 24
48	OCLK4	Output	
49	+V	Output	5v
50	GND	Common	

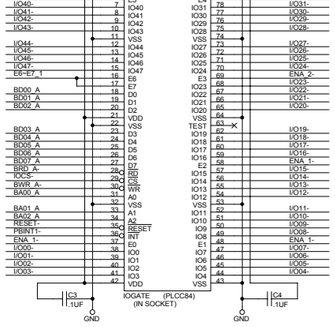
All parts need to be close to "J1" (JEXP)

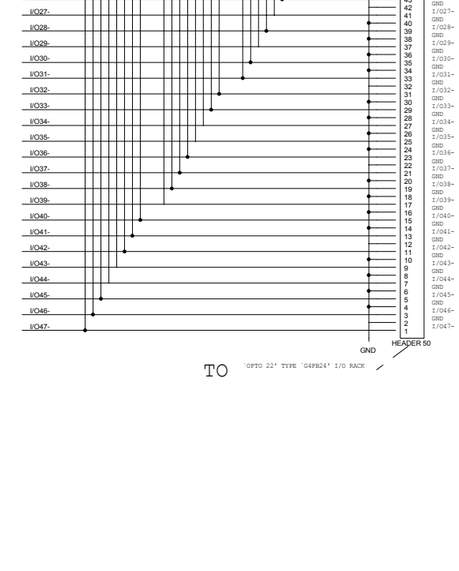




TO 'OPTO 22' TYPE 'G4PB24' I/O RACK







TO 'OPTO 22' TYPE 'G4PB24' I/O RACK

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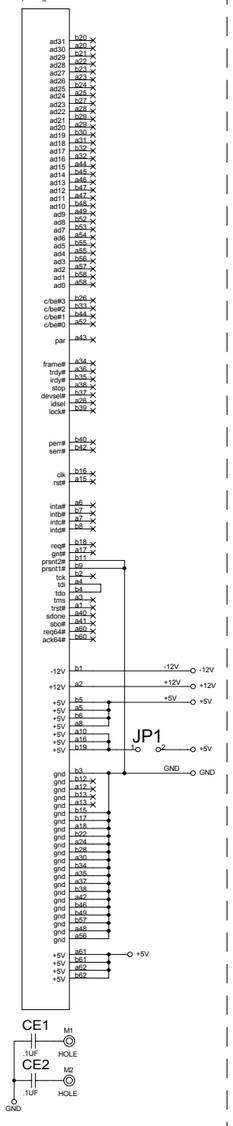
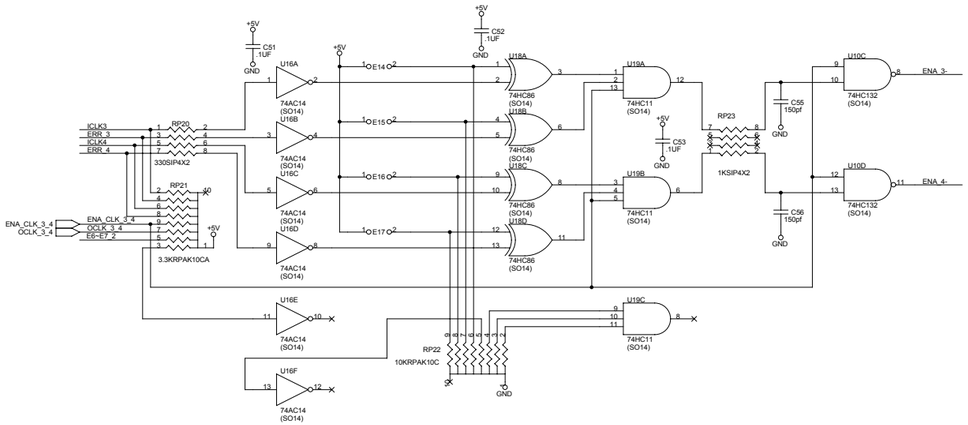
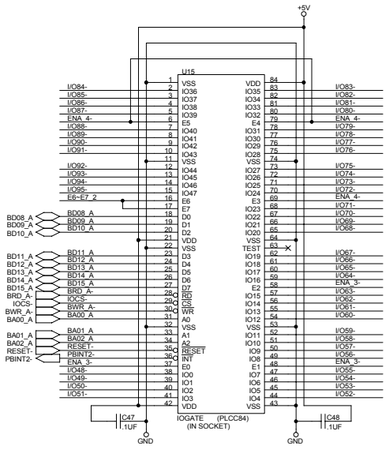
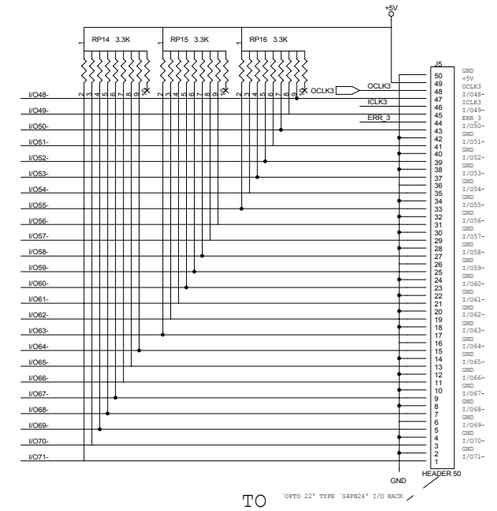
Install on all boards









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OPTION#1

Extra 24in / 24out

Delta Tau Data Systems, Inc.		
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