# DRV8313 Triple Half-H-Bridge Driver IC

## 1 Features

- Three Half-H-Bridge Driver IC
  - Drives 3-Phase Brushless DC Motors
  - Individual Half-Bridge Control
  - Pins for Low-Side Current Sensing
  - Low MOSFET ON-Resistance
- 2.5-A Maximum Drive Current at 24 V, 25°C
- Uncommitted Comparator can be Used for Current Limit or Other Functions
- Built-In 3.3-V 10-mA LDO Regulator
- 8-V to 60-V Operating Supply Voltage Range
- Thermally Enhanced Surface-Mount Package

## 2 Applications

- HVAC Motors
- Consumer Products
- Office Automation Machines
- Factory Automation
- Robotics

## 3 Description

The DRV8313 provides three individually controllable half-H-bridge drivers. The device is intended to drive a three-phase brushless DC motor, though it can also be used to drive solenoids or other loads. Each output driver channel consists of N-channel power MOSFETs configured in a half-H-bridge configuration. The design brings the ground terminals of each driver to pins, thus allowing one driver to perform current sensing on each output.

Current-limit circuitry or other functions are possible uses of an uncommitted comparator.

The DRV8313 can supply up to 2.5-A peak or 1.75-A rms output current per channel (with proper PCB heatsinking at 24 V and 25°C) per half-H-bridge.

The device provides internal shutdown functions for overcurrent protection, short-circuit protection, undervoltage lockout, and overtemperature.

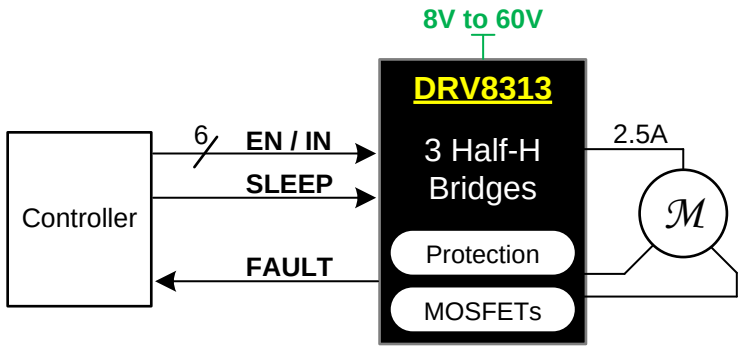
The DRV8313 comes in a 28-pin HTSSOP PowerPAD™ package.

**Device Information**[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| DRV8313 | HTSSOP (28) | 9.70 mm × 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## 4 Simplified Schematic



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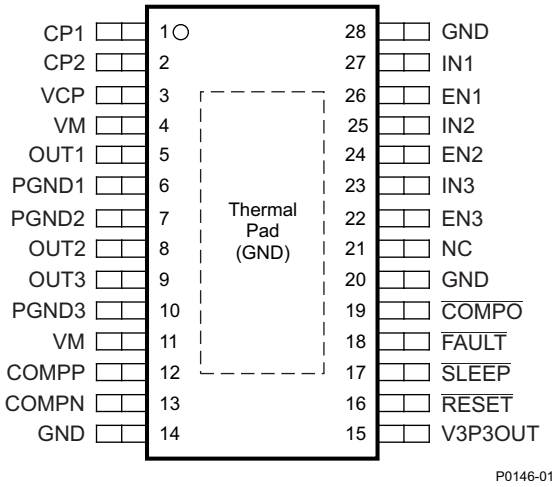
## 5 Revision History

**Changes from Revision A (November 2012) to Revision B** **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 4

# 6 Pin Configuration and Functions

**PWP Package**
**(Top View)**




**Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION | EXTERNAL COMPONENTS OR CONNECTIONS |
|---|---|---|---|---|
| NAME | NO. | | | |
| **POWER AND GROUND** | | | | |
| CP1 | 1 | P | Charge-pump flying capacitor | Connect a 0.01-µF 100-V capacitor between CP1 and CP2. |
| CP2 | 2 | P | Charge-pump flying capacitor | |
| GND | 12, 20, 28, PPAD | P | Device ground | Connect to system ground |
| V3P3OUT | 15 | P | 3.3-V regulator output | Bypass to GND with a 0.47-µF 6.3-V ceramic capacitor. Use for suppling external loads is permissible. |
| VCP | 3 | P | High-side gate drive voltage | Connect a 0.1-µF 16-V ceramic capacitor to VM. |
| VM | 4, 11 | P | Main power supply | Connect to power supply (8.2 V–60 V). Connect both pins to the same supply. Bypass to GND with a 10-µF (minimum) capacitor. |
| **CONTROL** | | | | |
| EN1 | 26 | I | Channel 1 enable | Logic high enables OUT1. Internal pulldown |
| EN2 | 24 | I | Channel 2 enable | Logic high enables OUT2. Internal pulldown |
| EN3 | 22 | I | Channel 3 enable | Logic high enables OUT3. Internal pulldown |
| IN1 | 27 | I | Channel 1 input | Logic input controls state of OUT1. Internal pulldown |
| IN2 | 25 | I | Channel 2 input | Logic input controls state of OUT2. Internal pulldown |
| IN3 | 23 | I | Channel 3 input | Logic input controls state of OUT3. Internal pulldown |
| nRESET | 16 | I | Reset input | Active-low reset input initializes internal logic and disables the outputs. Internal pulldown |
| nSLEEP | 17 | I | Sleep-mode input | Logic high to enable device, logic low to enter low-power sleep mode. Internal pulldown |
| **STATUS** | | | | |
| nFAULT | 18 | OD | Fault | Logic low when in fault condition (overtemperature, overcurrent, UVLO) |
| **COMPARATOR** | | | | |
| COMPN | 13 | I | Comparator negative input | Negative input of comparator |
| COMPP | 12 | I | Comparator positive input | Positive input of comparator |
| nCOMPO | 19 | OD | Comparator out | Output of comparator. Open-drain output |

(1) I = input, O = output, OD = open-drain output, P = power

**Pin Functions (continued)**

| PIN | | TYPE(1) | DESCRIPTION | EXTERNAL COMPONENTS OR CONNECTIONS |
|---|---|---|---|---|
| NAME | NO. | | | |
| **OUTPUT** | | | | |
| OUT1 | 5 | O | Output 1 | Connect to loads. |
| OUT2 | 8 | O | Output 2 | |
| OUT3 | 9 | O | Output 3 | |
| PGND1 | 6 | P | Ground for OUT1 | Connect to ground, or to low-side current-sense resistors. |
| PGND2 | 7 | P | Ground for OUT2 | |
| PGND3 | 10 | P | Ground for OUT3 | |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| | Power-supply voltage ($V_M$) | –0.3 | 65 | V |
| | Digital-pin voltage | –0.5 | 7 | V |
| | Comparator input-voltage | –0.5 | 7 | V |
| | Peak motor-drive output current | Internally limited | | A |
| | Pin voltage (GND1, GND2, GND3) | –600 | 600 | mV |
| | Continuous motor-drive output current(3) | | 2.5 | A |
| $T_J$ | Operating virtual junction temperature | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature | –60 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.
(3) Observe power dissipation and thermal limits.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±3000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_M$ | Motor power-supply voltage range(1) | 8 | | 60 | V |
| $V_{GNDX}$ | GND1, GND2, GND3 pin voltage | –500 | 0 | 500 | mV |
| $I_{V3P3}$ | V3P3OUT load current | 0 | | 10 | mA |

(1) All $V_M$ pins must be connected to the same supply voltage.

## 7.4 Thermal Information

| THERMAL METRIC(1) | | DRV8313 PWP 28 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 31.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 15.9 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 5.6 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 5.5 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.4 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics

$T_A$ = 25°C, over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES** | | | | | | |
| $I_{VM}$ | VM operating supply current | $V_M$ = 24 V, $f_{PWM}$ < 50 kHz | | 1 | 5 | mA |
| $I_{VMQ}$ | VM sleep-mode supply current | $V_M$ = 24 V | | 500 | 800 | µA |
| $V_{UVLO}$ | VM undervoltage lockout voltage | $V_M$ rising | | 6.3 | 8 | V |
| **V3P3OUT REGULATOR** | | | | | | |
| $V_{3P3}$ | V3P3OUT voltage | $I_{OUT}$ = 0 to 10 mA | 3.1 | 3.3 | 3.52 | V |
| **LOGIC-LEVEL INPUTS** | | | | | | |
| $V_{IL}$ | Input low voltage | | | 0.6 | 0.7 | V |
| $V_{IH}$ | Input high voltage | | 2.2 | | 5.25 | V |
| $V_{HYS}$ | Input hysteresis | | 50 | | 600 | mV |
| $I_{IL}$ | Input low current | VIN = 0 | –5 | | 5 | µA |
| $I_{IH}$ | Input high current | VIN = 3.3 V | | | 100 | µA |
| $R_{PD}$ | Pulldown resistance | | | 100 | | kΩ |
| **nFAULT and COMPO OutputS (OPEN-DRAIN OUTPUTS)** | | | | | | |
| $V_{OL}$ | Output low voltage | $I_O$ = 5 mA | | | 0.5 | V |
| $I_{OH}$ | Output high leakage current | $V_O$ = 3.3 V | | | 1 | µA |
| **COMPARATOR** | | | | | | |
| $V_{CM}$ | Common-mode input-voltage range | | 0 | | 5 | V |
| $V_{IO}$ | Input offset voltage | | –7 | | 7 | mV |
| $I_{IB}$ | Input bias current | | –300 | | 300 | nA |
| $t_R$ | Response time | 100-mV step with 10-mV overdrive | | | 2 | µs |
| **H-BRIDGE FETs** | | | | | | |
| $r_{ds(on)}$ | High-side FET ON-resistance | $V_M$ = 24 V, $I_O$ = 1 A, $T_J$ = 25°C | | 0.24 | | Ω |
| | | $V_M$ = 24 V, $I_O$ = 1 A, $T_J$ = 85°C | | 0.29 | 0.39 | |
| $r_{ds(on)}$ | Low-side FET ON-resistance | $V_M$ = 24 V, $I_O$ = 1 A, $T_J$ = 25°C | | 0.24 | | Ω |
| | | $V_M$ = 24 V, $I_O$ = 1 A, $T_J$ = 85°C | | 0.29 | 0.39 | |
| $I_{OFF}$ | Off-state leakage current | | –2 | | 2 | µA |
| $t_{DEAD}$ | Output dead time | | | 90 | | ns |
| **PROTECTION CIRCUITS** | | | | | | |
| $I_{OCP}$ | Overcurrent protection trip level | | 3 | 5 | | A |
| $t_{OCP}$ | Overcurrent protection deglitch time | | | 5 | | µs |
| $T_{TSD}$ | Thermal shutdown temperature | Die temperature | 150 | 160 | 180 | °C |

## 7.6 Switching Characteristics(1)

$T_A$ = 25°C, $V_M$ = 24 V, $R_L$ = 20 Ω

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_1$ | Delay time, ENx high to OUTx high, INx = 1 | 130 | 330 | ns |
| 2 | $t_2$ | Delay time, ENx low to OUTx low, INx = 1 | 275 | 475 | ns |
| 3 | $t_3$ | Delay time, ENx high to OUTx low, INx = 0 | 100 | 300 | ns |
| 4 | $t_4$ | Delay time, ENx low to OUTx high, INx = 0 | 200 | 400 | ns |
| 5 | $t_5$ | Delay time, INx high to OUTx high | 300 | 500 | ns |
| 6 | $t_6$ | Delay time, INx low to OUTx low | 275 | 475 | ns |
| 7 | $t_r$ | Output rise time, resistive load to GND | 30 | 150 | ns |
| 8 | $t_f$ | Output fall time, resistive load to GND | 30 | 150 | ns |

(1) Not production tested

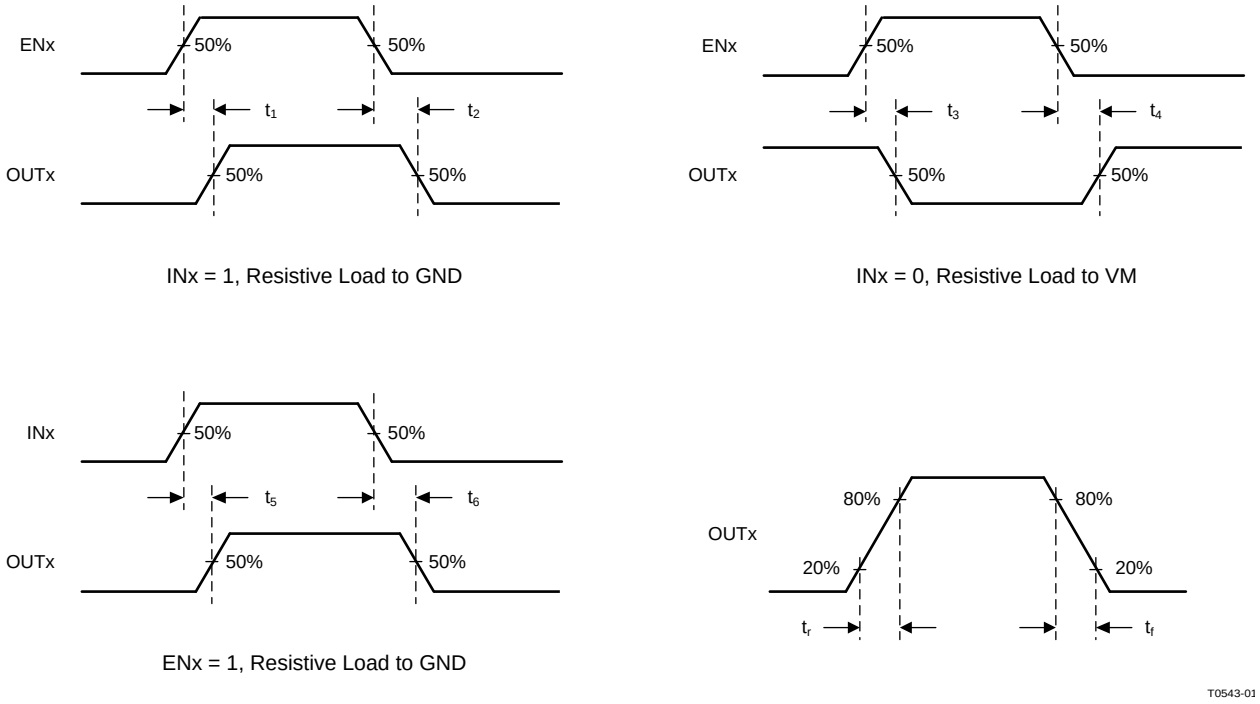



**Figure 1. DRV8313 Switching Characteristics**

## 7.7 Typical Characteristics

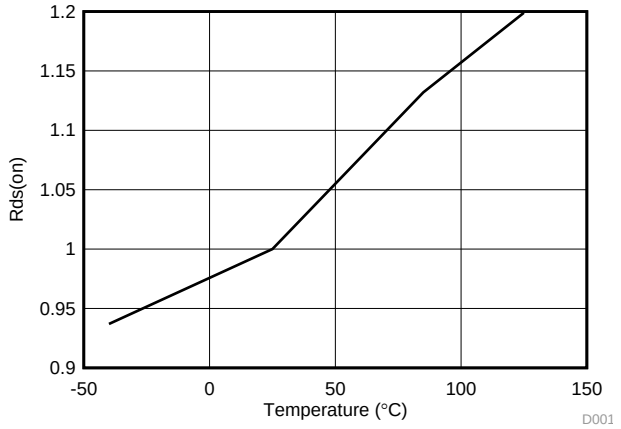



**Figure 2. $r_{DS(on)}$ vs Temperature (Normalized to 25°C)**

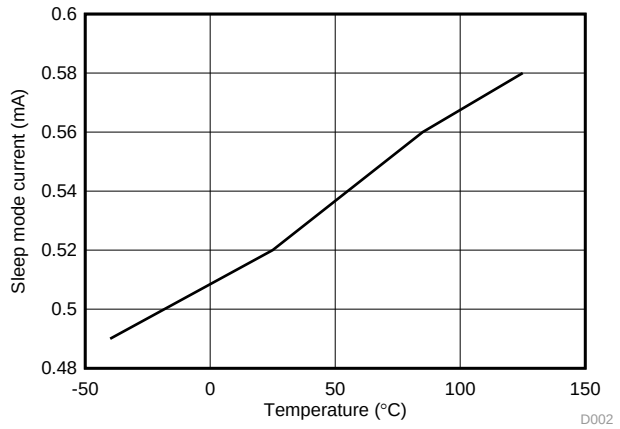


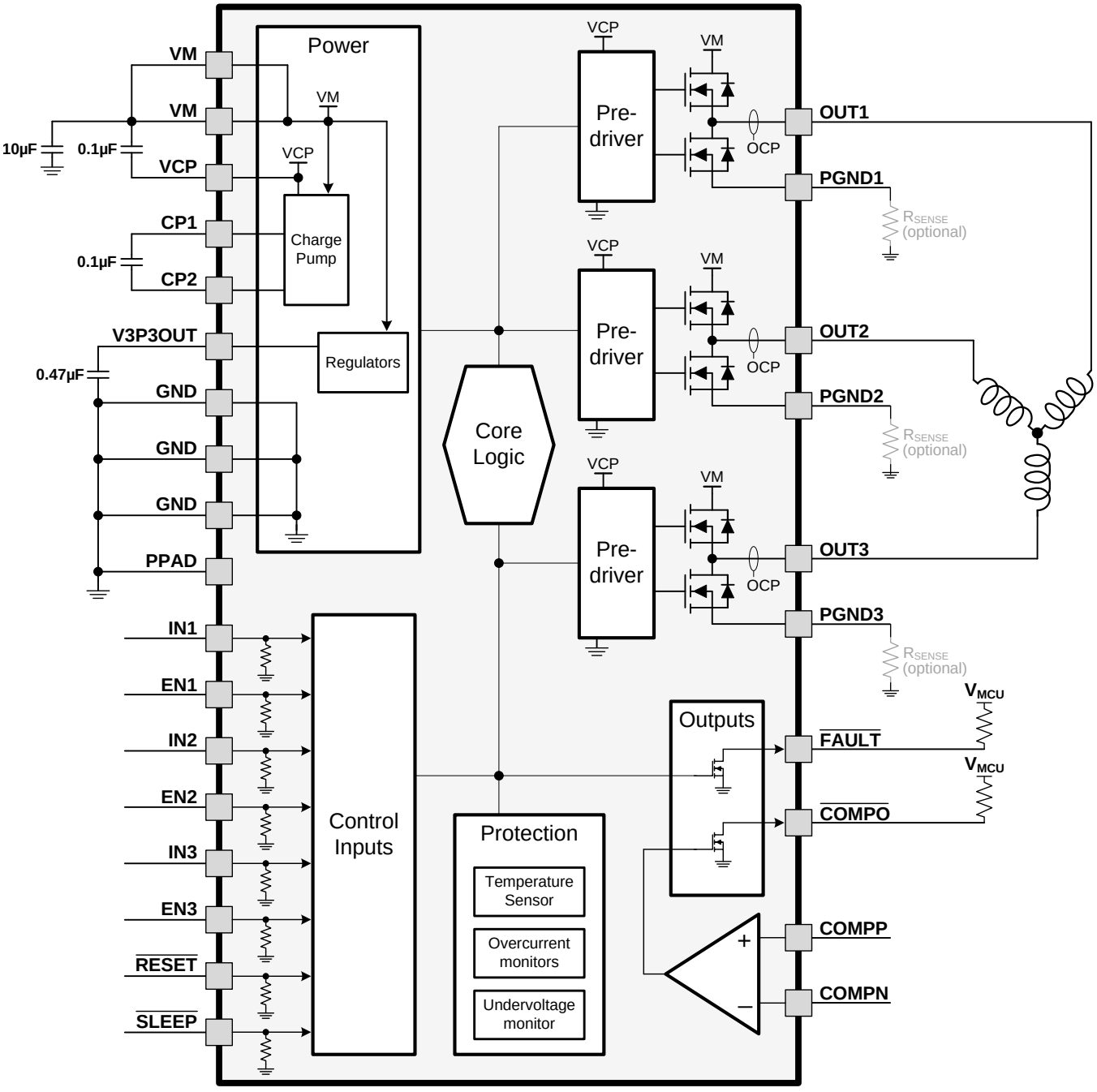

**Figure 3. Sleep-Mode Current vs Temperature**

# 8 Detailed Description

## 8.1 Overview

The DRV8313 integrates three independent 2.5-A half-H bridges, protection circuits, sleep mode, fault reporting, and a comparator. Its single power supply supports a wide 8V to 60V, making it well-suited for motor drive applications.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Output Stage

The DRV8313 contains three half-H-bridge drivers. The source terminals of the low-side FETs of all three half-H-bridges terminate at separate pins (GND1, GND2, and GND3) to allow the use of a low-side current-sense resistor on each output, if desired. The user may also connect all three together to a single low-side sense resistor, or may connect them directly to ground if there is no need for current sensing.

If using a low-side sense resistor, take care to ensure that the voltage on the GND1, GND2, or GND3 pin does not exceed ±500 mV.

There are multiple VM motor power-supply pins. Connect all VM pins together to the motor-supply voltage.

### 8.3.2 Bridge Control

The INx input pins directly control the state (high or low) of the OUTx outputs; the ENx input pins enable or disable the OUTx driver. Table 1 shows the logic:

**Table 1. Logic States**

| INx | ENx | OUTx |
|---|---|---|
| X | 0 | Z |
| 0 | 1 | L |
| 1 | 1 | H |

### 8.3.3 Charge Pump

Because the output stages use N-channel FETs, the device requires a gate-drive voltage higher than the VM power supply to enhance the high-side FETs fully. The DRV8313 integrates a charge-pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires two external capacitors for operation. See the block diagram and pin descriptions for details on these capacitors (value, connection, and so forth).

The charge pump shuts down when nSLEEP is low.

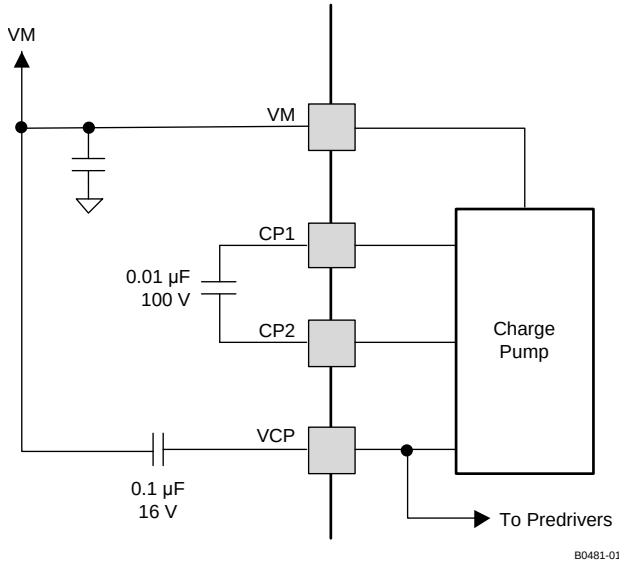



**Figure 4. DRV8313 Charge Pump**

### 8.3.4 Comparator

The DRV8313 includes an uncommitted comparator, which can find use as a current-limit comparator or for other purposes.

Figure 5 shows connections to use the comparator to sense current for implementing a current limit. Current from all three low-side FETs is sensed using a single low-side sense resistor. The voltage across the sense resistor is compared with a reference, and when the sensed voltage exceeds the reference, a current-limit condition is signaled to the controller. The V3P3OUT internal voltage regulator can be used to set the reference voltage of the comparator.

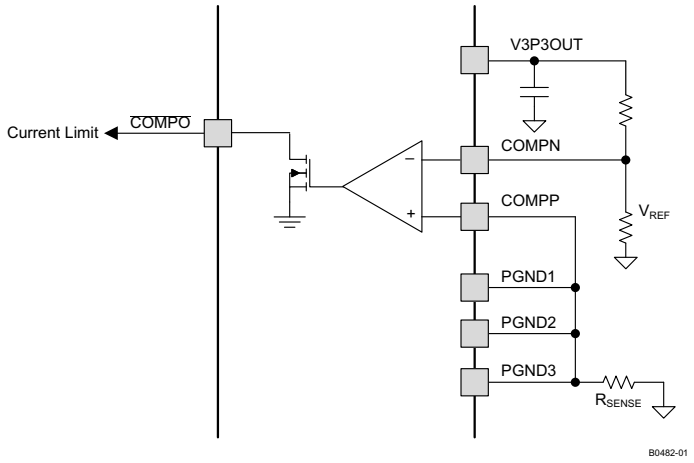



**Figure 5. DRV8313 Comparator**

### 8.3.5 Protection Circuits

The DRV8313 has full protection against undervoltage, overcurrent, and overtemperature events.

#### *8.3.5.1 Overcurrent Protection (OCP)*

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP deglitch time, the device disables the channel experiencing the overcurrent and drives the nFAULT pin low. The driver remains off until either assertion of nRESET or the cycling of VM power.

Overcurrent conditions on both high- and low-side devices, that is, a short to ground, supply, or across the motor winding, all result in an overcurrent shutdown.

#### *8.3.5.2 Thermal Shutdown (TSD)*

If the die temperature exceeds safe limits, the device disables all outputs and drives the nFAULT pin low. Once the die temperature has fallen to a safe level, operation automatically resumes.

#### *8.3.5.3 Undervoltage Lockout (UVLO)*

If at any time the voltage on the VM pins falls below the undervoltage-lockout threshold voltage, the device disables all outputs, resets internal logic, and drives the nFAULT pin low. Operation resumes when VM rises above the UVLO threshold.

## 8.4 Device Functional Modes

### 8.4.1 nRESET and nSLEEP Operation

The nRESET pin, when driven active-low, resets any faults. It also disables the output drivers while it is active. The device ignores all inputs while nRESET is active. Note that there is an internal power-up-reset circuit, so that driving nRESET at power up is not required.

Driving nSLEEP low puts the device into a low-power sleep state. Entering this state disables the output drivers, stops the gate-drive charge pump, resets all internal logic (including faults), and stops all internal clocks. In this state, the device ignores all inputs until nSLEEP returns inactive-high. When returning from sleep mode, some time (approximately 1 ms) must pass before the motor driver becomes fully operational. The V3P3 regulator remains operational in sleep mode.

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The typical application for the DRV8313 is to drive a 3-phase brushless motor. In this application, the three outputs connect to the three motor leads, as shown in Figure 6.

## 9.2 Typical Applications

### 9.2.1 Output Configurations and Connections

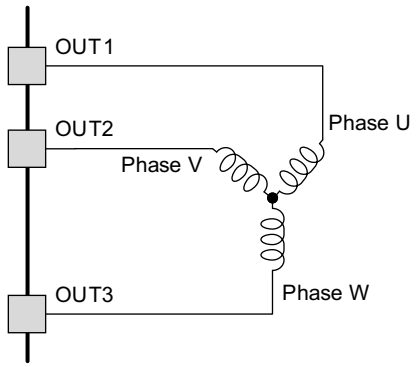



**Figure 6. Three-Phase Motor Connection**

#### *9.2.1.1 Design Requirements*

The device achieves standard 120° (also called trapezoidal or block) commutation, using synchronous rectification, by following the states shown in Table 2.

**Table 2. Three-Phase Motor Signals**

| State | OUT1 (Phase U) | | | OUT2 (Phase V) | | | OUT3 (Phase W) | | |
|---|---|---|---|---|---|---|---|---|---|
| | IN1 | EN1 | OUT1 | IN2 | EN2 | OUT2 | IN3 | EN3 | OUT3 |
| 1 | X | 0 | Z | 1 / PWM | 1 | H / PWM | 0 | 1 | L |
| 2 | 1 / PWM | 1 | H / PWM | X | 0 | Z | 0 | 1 | L |
| 3 | 1 / PWM | 1 | H / PWM | 0 | 1 | L | X | 0 | Z |
| 4 | X | 0 | Z | 0 | 1 | L | 1 / PWM | 1 | H / PWM |
| 5 | 0 | 1 | L | X | 0 | Z | 1 / PWM | 1 | H / PWM |
| 6 | 0 | 1 | L | 1 / PWM | 1 | H / PWM | X | 0 | Z |

The user can implement asynchronous rectification by also applying the PWM signal to the enable inputs.

The DRV8313 can drive other loads, including dc brush motors and solenoids. For example, one could drive a DC brush motor in both directions, plus a single solenoid or unidirectional DC brush motor.

### *9.2.1.2 Detailed Design Procedure*

#### 9.2.1.2.1 Motor Voltage

BLDC motors are typically rated for a certain voltage. Higher voltages generally have the advantage of causing current to change faster through the inductive windings, which allows for higher RPMs. Lower voltages allow for more accurate control of phase currents.

#### 9.2.1.2.2 Sense Resistor

For optimal performance, it is important for a sense resistor to be:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $I_{RMS}^2 \times R$. For example, if peak motor current is 3 A, RMS motor current is 2 A, and a 0.05-Ω sense resistor is used, the resistor will dissipate $2\ A^2 \times 0.05\ \Omega = 0.2$ W. The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a de-rated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. It is always best to measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, it is common practice to use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.

### *9.2.1.3 Application Curves*

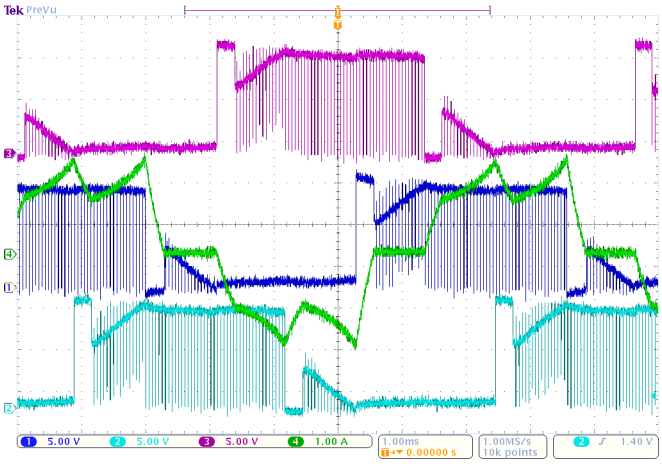



**Figure 7. BLDC Operation**

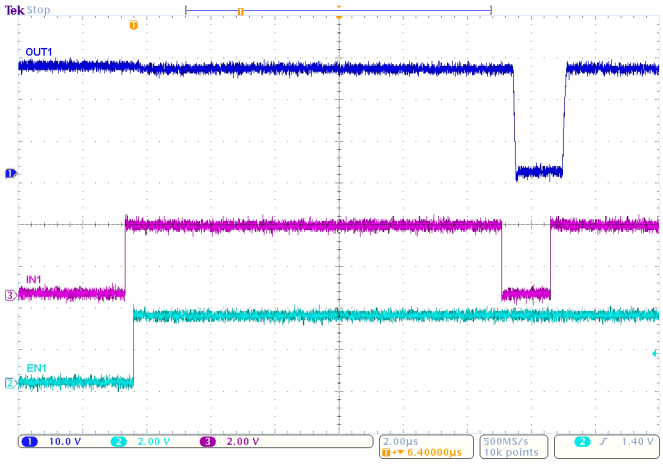



**Figure 8. Input/Output Functionality**

### 9.2.2 Bidirectional Motor Plus Motor or Solenoid Connection

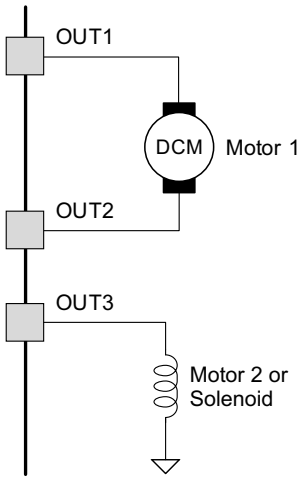



**Figure 9. Bidirectional Motor Plus Motor or Solenoid Connection**

#### *9.2.2.1 Design Requirements*

The functions would be as shown in Table 3.

**Table 3. Bidirectional Motor Plus Motor or Solenoid Signals**

| Motor 1 | | | | | | | Motor 2 or Solenoid | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Function** | **IN1** | **EN1** | **OUT1** | **IN2** | **EN2** | **OUT2** | **Function** | **IN3** | **EN3** | **OUT3** |
| Off or coast | X | 0 | Z | X | X | X | On | 1 / PWM | 1 | 1 |
| Off or coast | X | X | X | X | 0 | X | Off or slow decay | 0 | 1 | 0 |
| Forward | 1 / PWM | 1 | 1 | 0 | 1 | 0 | Off or coast | X | 0 | X |
| Reverse | 0 | 1 | 0 | 1 / PWM | 1 | 1 | | | | |
| Brake or slow decay | 0 | 1 | 0 | 0 | 1 | 0 | | | | |
| Brake or slow decay | 1 | 1 | 1 | 1 | 1 | 1 | | | | |

Applying a PWM signal to the appropriate INx pin(s) as shown in Table 3 could implement PWM speed control.

Another possibility is controlling three different loads. It is possible to return one side of the load either to the power supply (VM) or to ground.

#### *9.2.2.2 Detailed Design Procedure*

##### 9.2.2.2.1 Motor Voltage

The motor voltage to use will depend on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

### 9.2.2.3 Application Curve

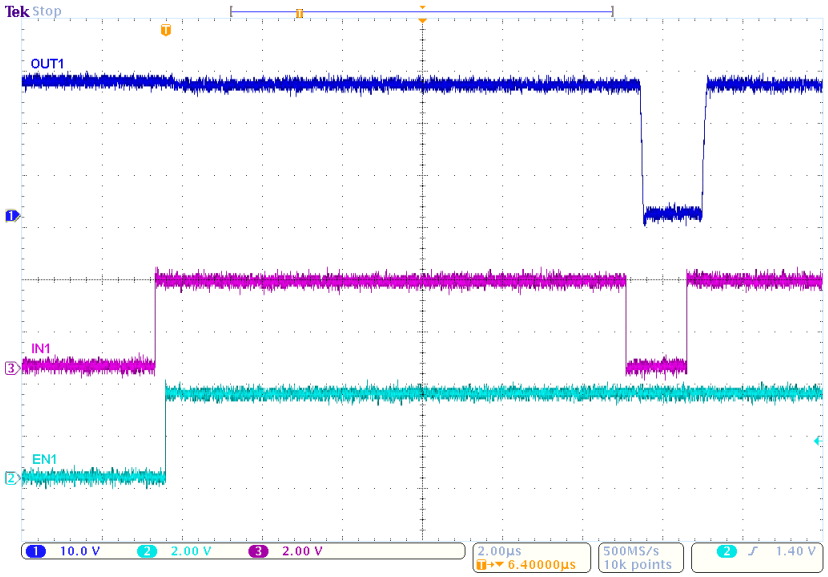



**Figure 10. Input/Output Functionality**

### 9.2.3 Three Independent Load Connections

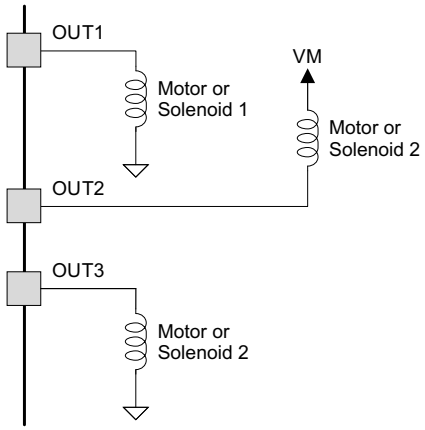



**Figure 11. Three Independent Load Connections Schematic**

#### 9.2.3.1 Design Requirements

**Table 4. Three Independent Load Signals**

| Motor or Solenoid 1 | | | | Motor or Solenoid 2 | | | | Motor or Solenoid 3 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Function | IN1 | EN1 | OUT1 | Function | IN2 | EN2 | OUT2 | Function | IN3 | EN3 | OUT3 |
| On | 1/PWM | 1 | 1 | On | 1/PWM | 1 | 1 | On | 1/PWM | 1 | 1 |
| Off or slow decay | 0 | 1 | 0 | Off or slow decay | 0 | 1 | 0 | Off or slow decay | 0 | 1 | 0 |
| Off or coast | X | 0 | X | Off or coast | X | 0 | X | Off or coast | X | 0 | X |

# 10 Power Supply Recommendations

## 10.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (Brushed DC, Brushless DC, Stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

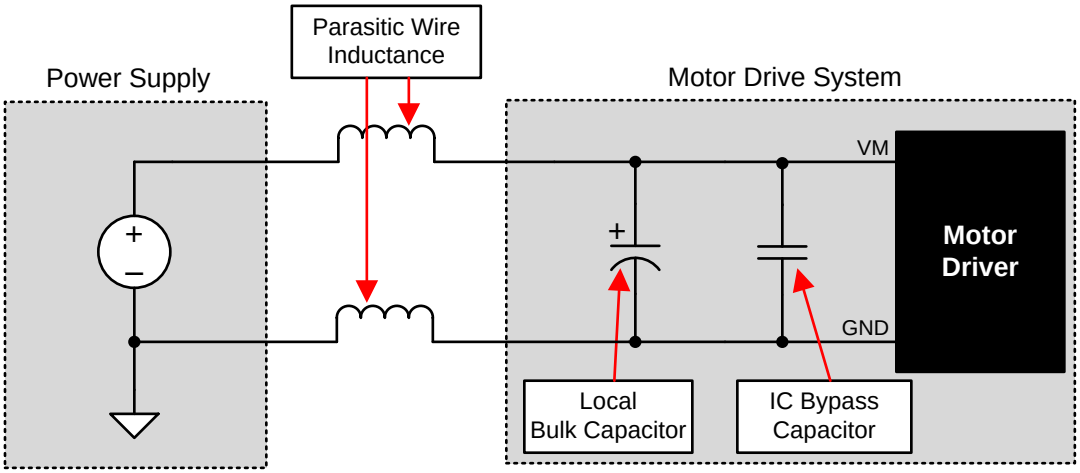



**Figure 12. Example Setup of Motor Drive System With External Power Supply**

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

# 11 Layout

## 11.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times r_{DS(on)}$ heat that is generated in the device.

## 11.2 Layout Example

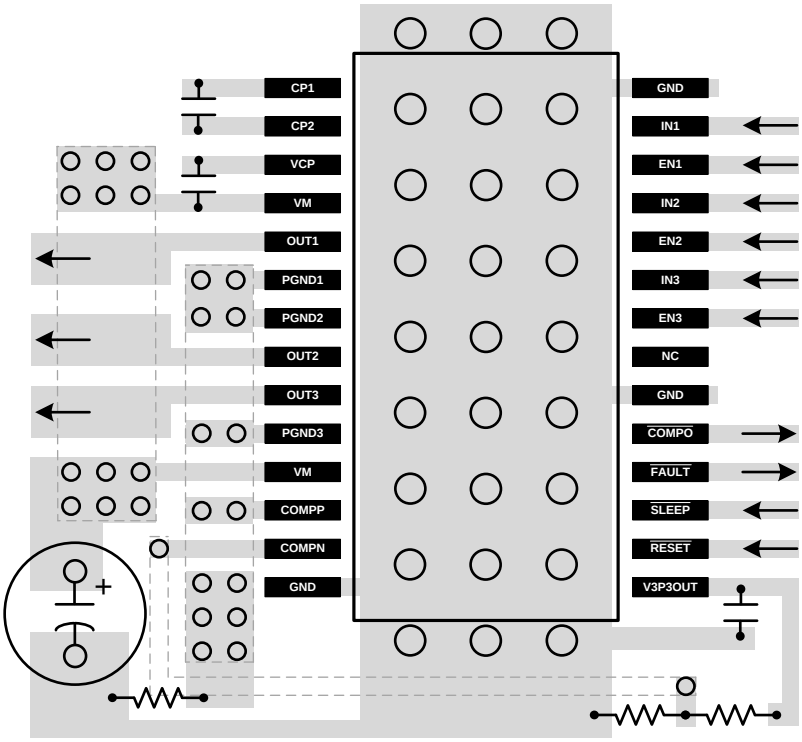



**Figure 13. Recommended Layout Example**

## 11.3 Thermal Considerations

The DRV8313 has thermal shutdown (TSD) as previously described. A die temperature in excess of approximately 150°C disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

### 11.3.1 Heatsinking

The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, add a number of vias to connect the thermal pad to the ground plane to accomplish this. On PCBs without internal planes, add copper area on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, use thermal vias to transfer the heat between the top and bottom layers.

## Thermal Considerations (continued)

For details about how to design the PCB, see TI Application Report SLMA002, *PowerPAD Thermally Enhanced Package* and TI Application Brief SLMA004, *PowerPAD Made Easy*, available at www.ti.com.

In general, providing more copper area allows the dissipation of more power.

## 11.4 Power Dissipation

The power dissipated in the output FET resistance, or $r_{DS(on)}$ dominates power dissipation in the DRV8313. A rough estimate of average power dissipation of each half-H-bridge when running a static load is:

$$P = r_{DS(on)} \times (I_{OUT})^2 \quad (1)$$

where

- P is the power dissipation of one H-bridge,
- $r_{DS(on)}$ is the resistance of each FET, and
- $I_{OUT}$ is equal to the average current drawn by the load.

At start-up and fault conditions, this current is much higher than normal running current; remember to take these peak currents and their duration into consideration.

The total device dissipation is the power dissipated in each of the three half-H-bridges added together.

The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking.

Note that $r_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when sizing the heatsink.

# 12 Device and Documentation Support

## 12.1 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV8313PWP | ACTIVE | HTSSOP | PWP | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | DRV8313 | Samples |
| DRV8313PWPR | ACTIVE | HTSSOP | PWP | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | DRV8313 | Samples |
| DRV8313RHH | PREVIEW | VQFN | RHH | 36 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | DRV8313 | |
| DRV8313RHHR | PREVIEW | VQFN | RHH | 36 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | DRV8313 | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

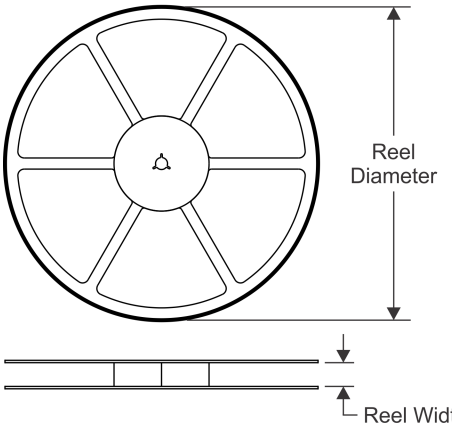
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

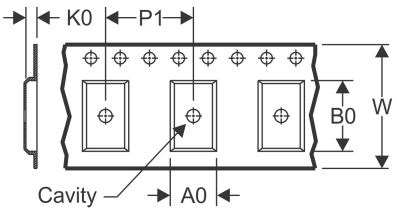
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

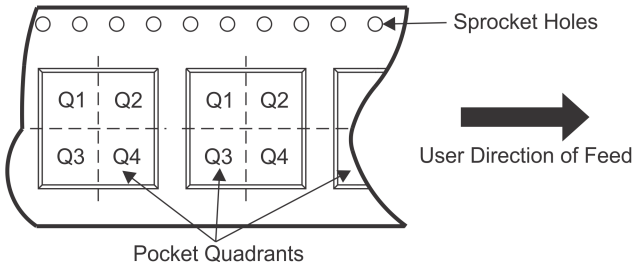



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

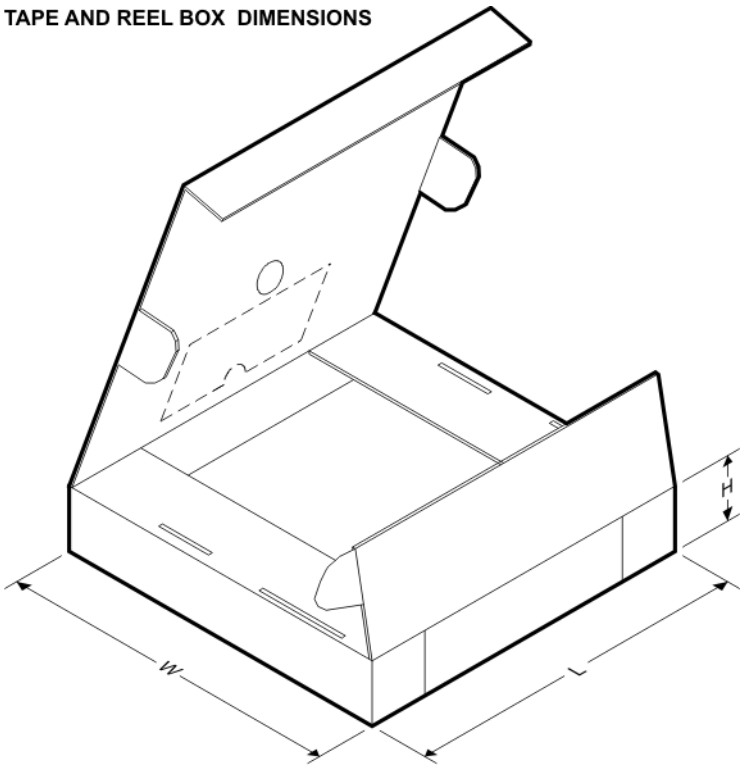
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV8313PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |

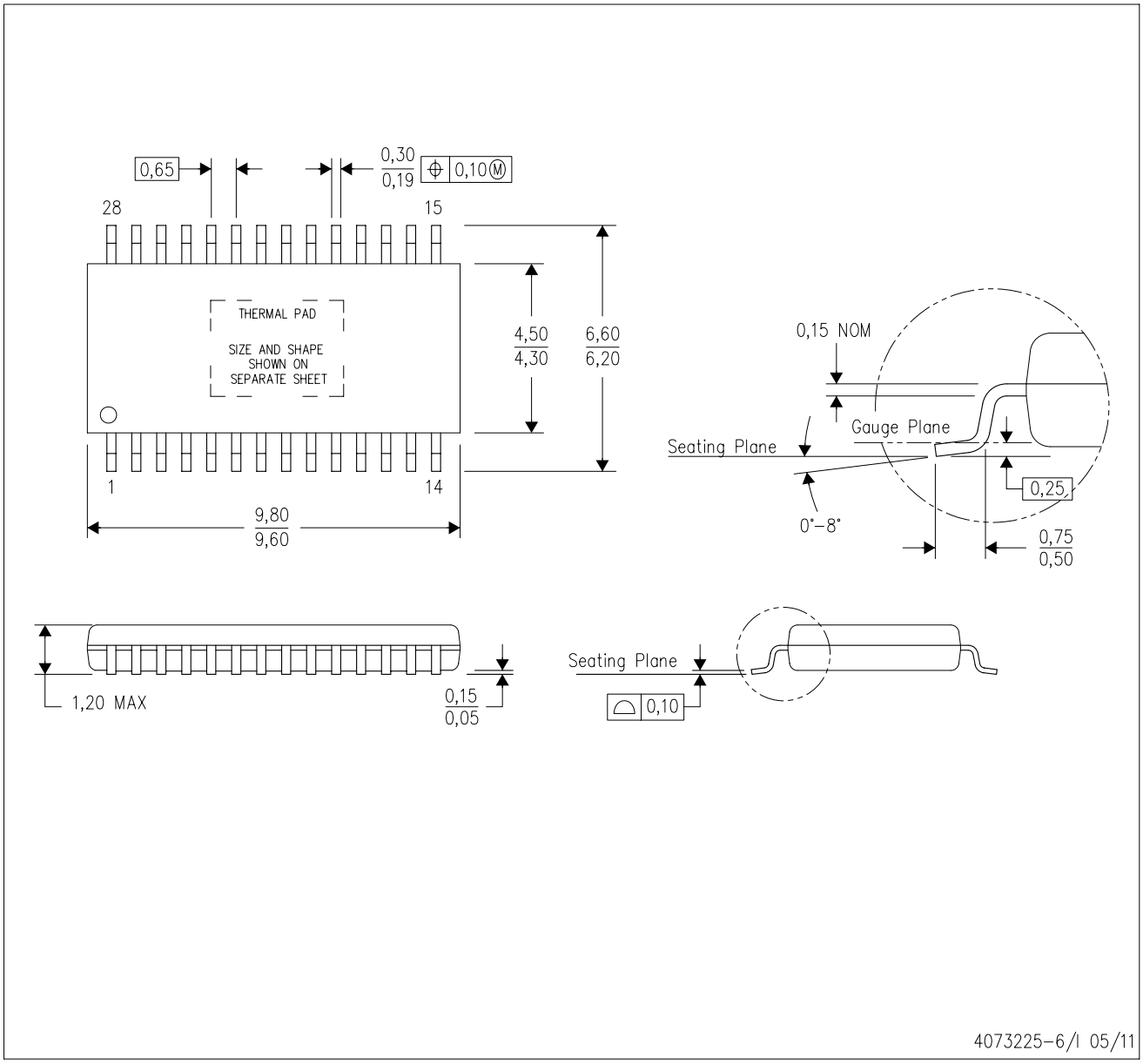
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DRV8313PWPR | HTSSOP | PWP | 28 | 2000 | 367.0 | 367.0 | 38.0 |

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

**PowerPAD is a trademark of Texas Instruments.**

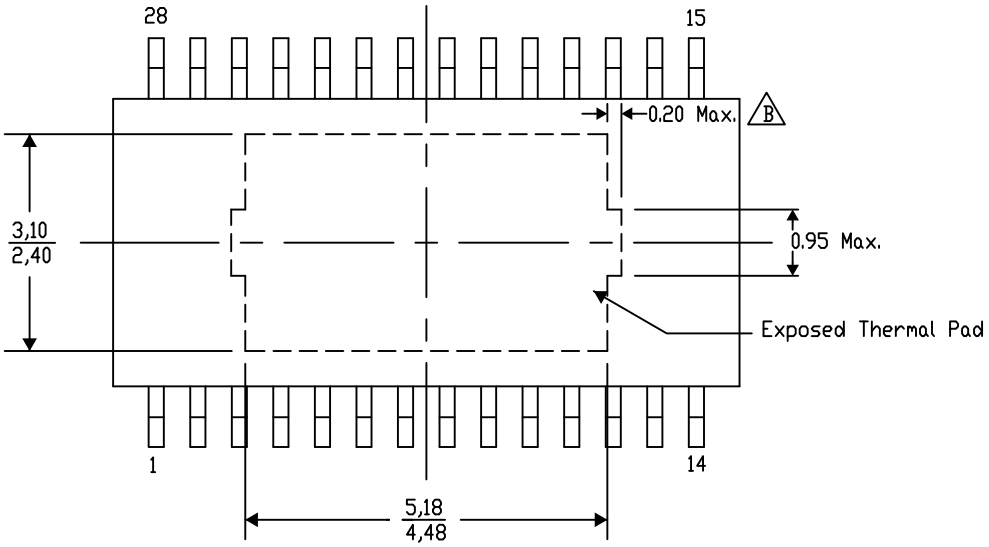
# PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

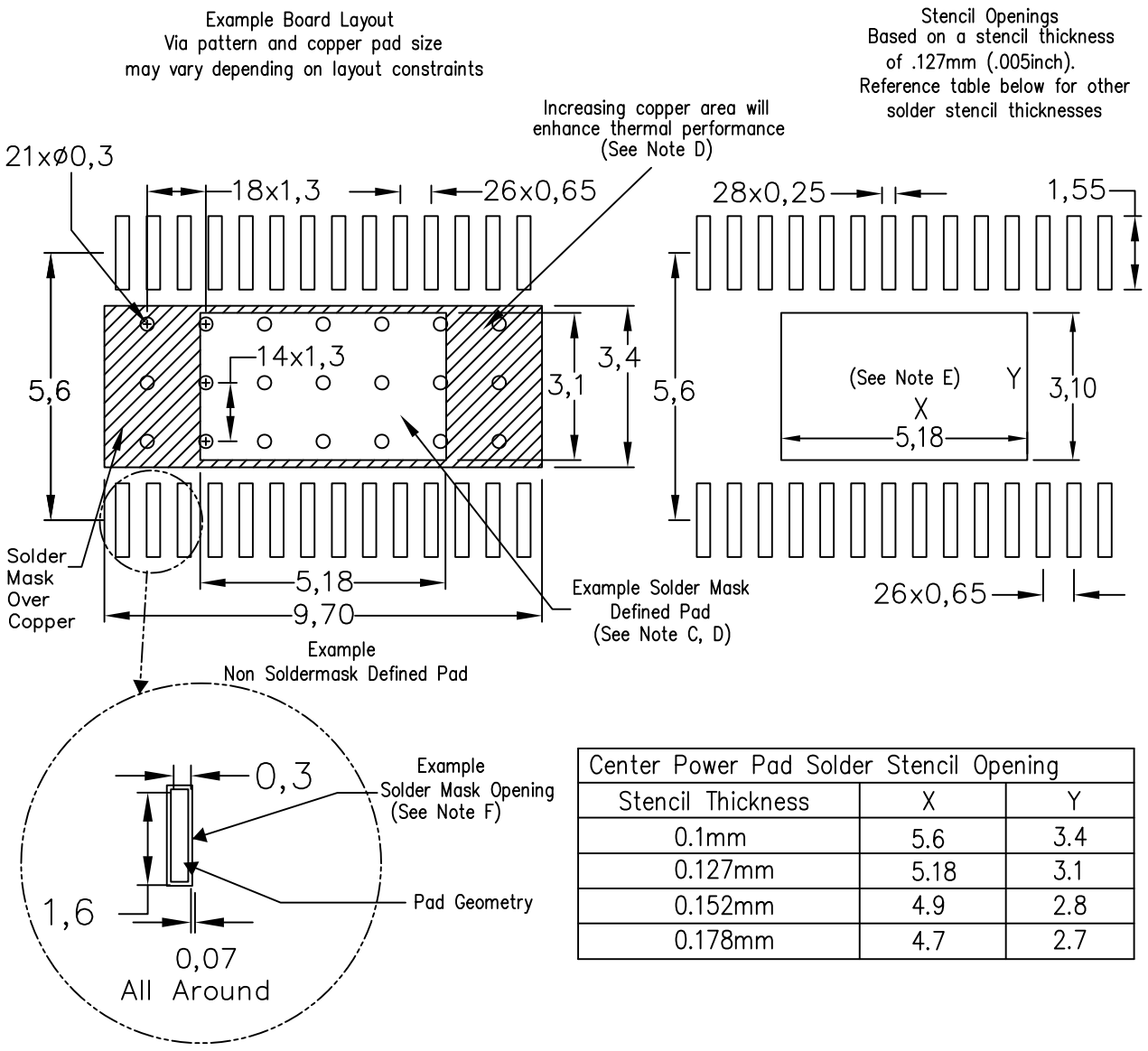
4206332–38/AN 10/15

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

## PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE

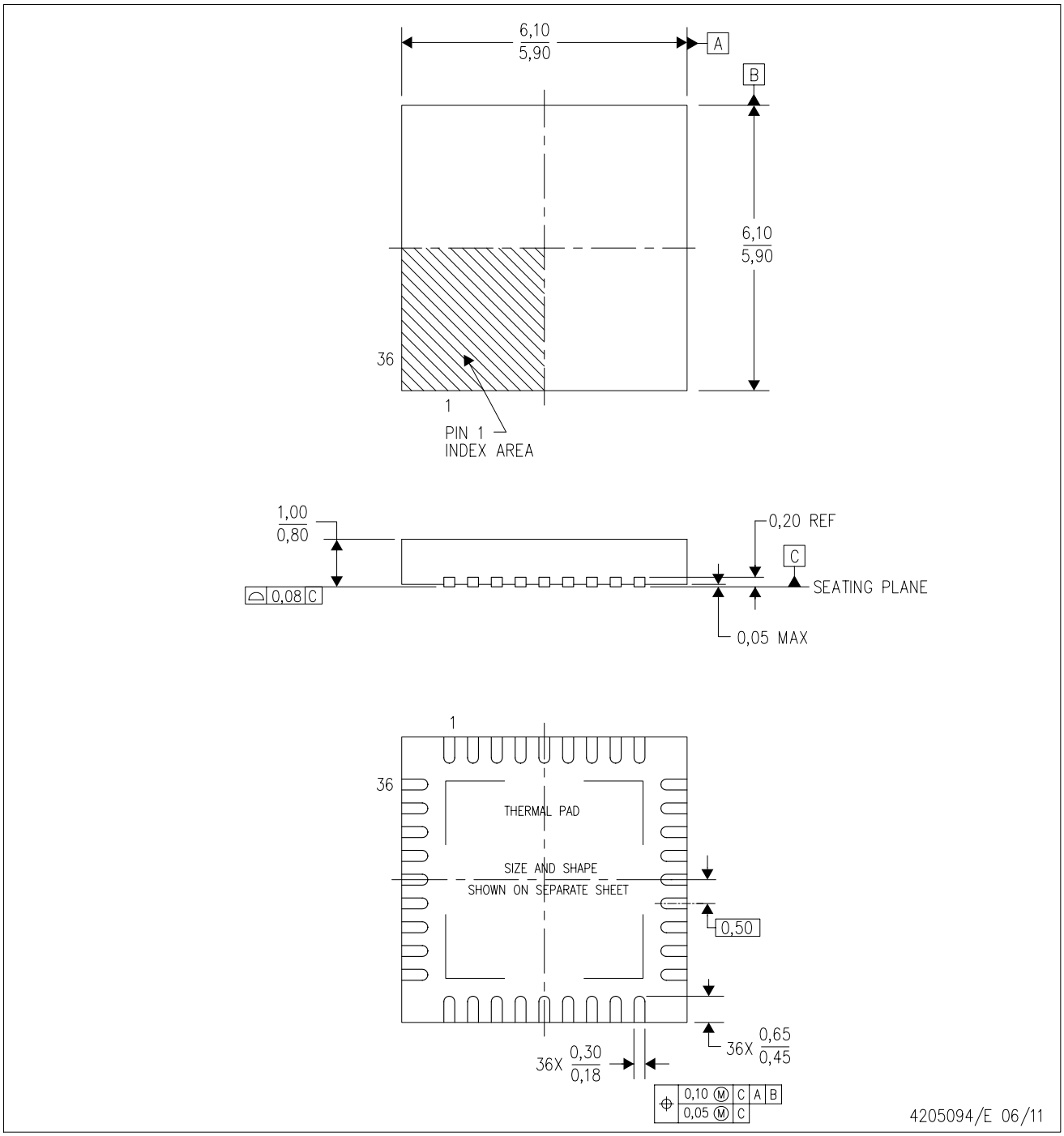



| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 5.6 | 3.4 |
| 0.127mm | 5.18 | 3.1 |
| 0.152mm | 4.9 | 2.8 |
| 0.178mm | 4.7 | 2.7 |

4207609–22/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

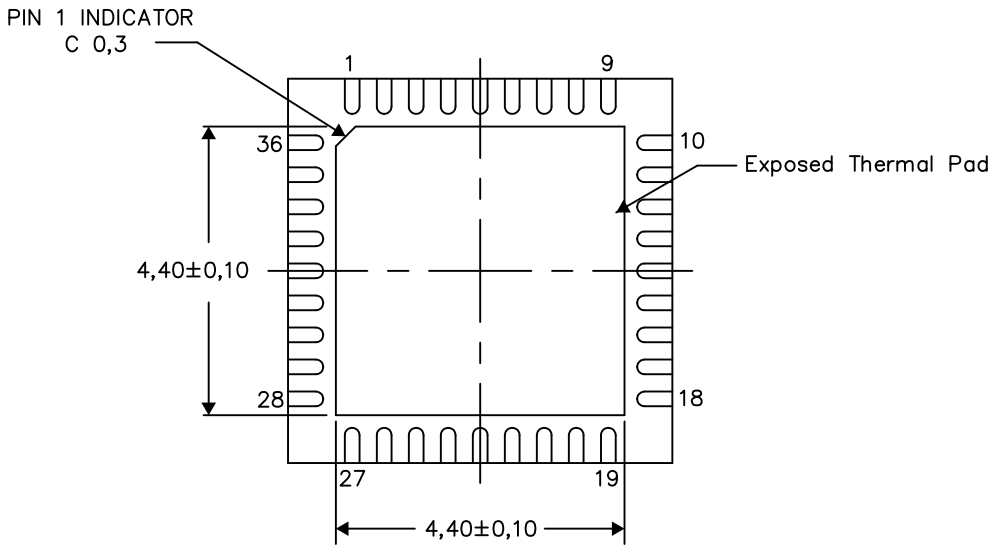
RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



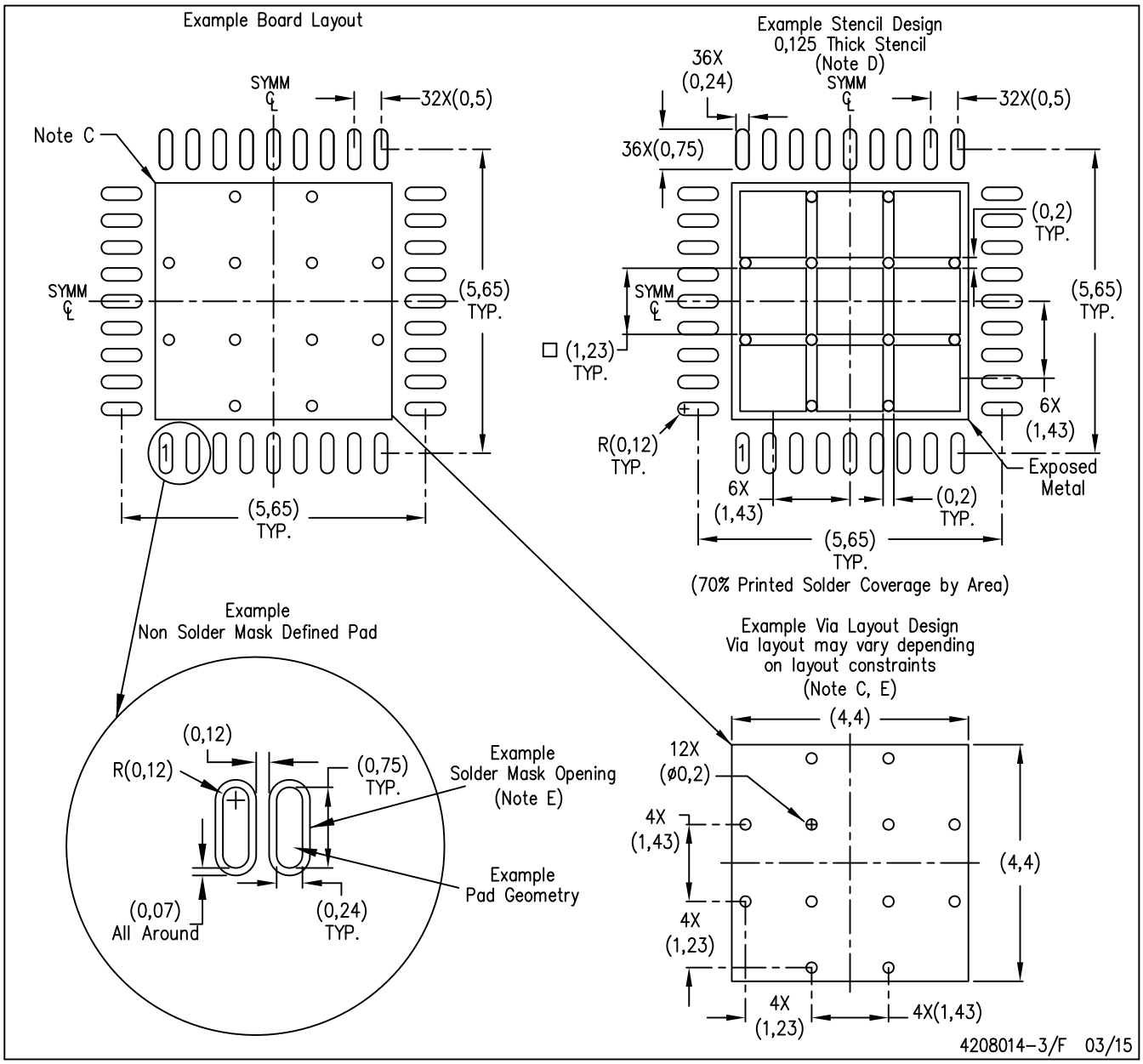

Bottom View

Exposed Thermal Pad Dimensions

4206362–5/M 11/13

NOTE: All linear dimensions are in millimeters

# RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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| **Products** | | **Applications** | |
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| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
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| Logic | logic.ti.com | Security | www.ti.com/security |
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| RFID | www.ti-rfid.com | | |
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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265