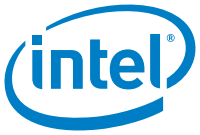
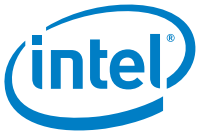


Intel® Joule™ Module

Datasheet

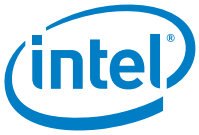
May 2017

Revision 1.6

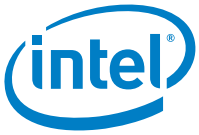


Revision History

Revision	Description	Date
1.6	• Updated required strapping table in section 2.3.3 and power good description in section 3.2.3. Added reference to the online Expansion Board Design Guide.	May 2017
1.5	• Added MIPI* CSI content • Corrected voltage specifications throughout	April 2017
1.3	• Corrected Bluetooth version to 4.2 on page 10	January 2017
1.2	• Updated required strapping table • Edited video encoder information • Added ESD warning • Added links to reference documents • Removed GPIO mapping for Linux* and pointed the reader to the website for this information • Incorporated QA format suggestions.	January 2017
1.1	Update wireless communication statement for end-use equipment integration	September 2016
1.0	Initial release	August 2016



Contents



Tables

Figures

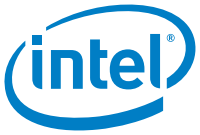
1 Introduction

This datasheet outlines the technical features of the Intel® Joule™ platform which is a system on module (SoM) that combines high-performance computing and graphics with large memory and wireless connectivity in a tiny footprint.

1.1 Acronyms

Table 1 **Acronyms and terminology**

Acronyms	Description
eMMC	embedded Multimedia Card, a lower cost type of boot ROM
GPIO	General Purpose Input/Output
HDMI*	High-Definition Multimedia Interface
I2C	IIC - Inter-Integrated Circuit
I2S	Inter-IC Sound
ISH	Integrated Sensor Hub
LPDDR	Low Power Double Data Rate
LPSS	Low Power Subsystem
MIPI* CSI	Mobile Industry Processor Interface - Camera Serial Interface https://mipi.org/specifications/camera-interface
PCB	Printed Circuit Board
RTC	Real Time Clock
SDIO	Secure Digital Input/Output
SoC	System on Chip; combines compute, graphics and interface in a single device
SoM	System on Module; contains the SoC and additional components in a single package
SPI	Serial Peripheral Interface (Bus)
UART / HSUART	UART - as used in this document, UART ports are to be assumed as only supporting Rxd, TxD signals HSUART - is a full function UART with Clear to Send and Return to Send handshakes for High Speed transfers



1.2 Reference documents

Intel Documents	Intel Document Number or Internet Address
Intel® Joule™ Platform Mechanical Descriptor	http://www.intel.com/content/www/us/en/support/boards-and-kits/000022366.html
Intel® Joule™ Compute Module Expansion Board Hardware Guide	http://www.intel.com/content/www/us/en/support/boards-and-kits/intel-joule-kits/000023394.html
Intel® Joule™ Compute Module Expansion Board Design Guide	http://www.intel.com/content/www/us/en/support/boards-and-kits/intel-joule-kits/000023390.html
Intel® Joule™ Compute Module Thermal Management Guide	http://www.intel.com/content/www/us/en/support/boards-and-kits/000023095.html
Intel® Joule™ Compute Module Website	https://software.intel.com/en-us/iot/hardware/joule
Intel® Joule™ Compute Module Online User Guide	https://software.intel.com/en-us/intel-joule-getting-started
Intel® Joule™ Compute Module Online Community	https://communities.intel.com/community/tech/intel-joule
Intel® Joule™ Compute Module FCC and FAA Regulatory Information	http://www.intel.com/content/www/us/en/support/boards-and-kits/000022313.html
Industry Specifications	**Internet Address**
JEDEC Standard LPDDR4 Specification	http://www.jedec.org
Universal Serial Bus Specification (USB)	http://www.usb.org/developers/doc
USB On-The-Go (OTG) and Embedded Host	http://www.usb.org/developers/onthego
HDMI* Specification v1.4b	http://www.hdmi.org/manufacturer/specification.aspx
MIPI* Specifications	http://mipi.org/specifications

Note: Intel does not control or audit third-party benchmark data or the web sites referenced in this document. You should visit the referenced web site and confirm whether referenced data are accurate.

Warning - Observe proper Electrostatic Discharge (ESD) best practices to protect the module, development kit and accessories. Best practices include keeping devices contained in protective bags and utilizing a grounded wrist strap when handling devices.

2 System on Module Overview

The Intel® Joule™ platform is a system on module (SoM) and is available in multiple configurations that share the same footprint and interface connector placement. This enables accelerated product design by providing multiple levels of compute power, graphics, memory and communication options in a single common footprint that can scale with end-product requirements.

2.1 Intel® Joule™ module configurations

Table 2 **Intel® Joule™ module configurations**

Module	CPU Clock	Graphic Clock	Memory and Storage
Intel® Joule™ 550x module	1.5 GHz	300 MHz	3GB RAM & 8GB eMMC Flash
Intel® Joule™ 570x module	1.7 GHz; Turbo Boost up to 2.4GHz	450 MHz base, 650 MHz Turbo	4GB RAM & 16GB eMMC Flash

2.2 Intel® Joule™ compute module feature summary

Table 3 **Intel® Joule™ compute module features**

Domain	Attribute	Value	Notes
Compute	System on Chip	14nm Intel® Atom™ Processor	Quad-core: 4 cores supporting 2 threads per core
	Address Bus Size	64-Bit (x86-64)	
	Cache	4MB L1	2MB per core-pair
RAM	Type and Speed	LPDDR4 (4 lanes, 3200 MT/sec)	Integrated Package on Package
Graphics	Execution Units	12EUs (2x6) on 550x and 18EUs (3x6) on 570x	
	Open Graphics Libraries	Open GL 3.1ES, Open GL4.3 & Open CL 2.0	
Display	HDMI Output	HDMI 1.4b	1080p
Storage	Type Supported	eMMC 5.0	Max eMMC speed of 400 MB/second
MIPI CSI	Camera connectors	Module accepts Hirose* BM14B(0.8)-400DP-0.4V	Data, clock, power, and GPIO on each connector
	MIPI CSI specification	Two CSI2 D-PHY ports at 1.5 Gb/sec per lane	Supports 2 simultaneous cameras
	Supported resolutions	camera1 (13MP) camera2 (5MP)	
Expansion Connector	Module to expansion board	Two, 2x50 pin connectors	Hirose Electric Co LTD* Part Number DF40C-100DP-0.4V
Audio	Number of DMIC	2	Routed via expansion board connectors
	Number and Speed of I^2S	One I^2S at 9.6 MHz	
USB	USB 3.0 compliant	1 Type C OTG and 1 Host	USB 3, Port 0 is dedicated to Type C USB 3, Port 1 is multiplexed with PCIe
PCIe*	Number of Ports / lanes	1 port / 1 lane	Multiplexed with USB3, Port1
	Max Speed	5 Gb/s	
SIO	I^2C	5 ports (3 LPSS, 2 ISH as LPSS)	Master Mode; max 3.4Mb/s
	UARTS	2 full and 1 half	Maximum rate of 115.2 kb/s for half speed and 3.6864 Mb/s maximum for full speed mode(s)
	SPI	2 ports, 5 chip selects	Up to 25MHz
SDIO	Number of ports	1	For SD Card interface
GPIO	Dedicated GPIO lines	8	Up to 48 when remapping interface pins
	Additional GPIO lines	Up to 48	Interfaces pins can be remapped within BIOS (tool release pending)
	PWM	4	

Table 3 **Intel® Joule™ compute module features**

Domain	Attribute	Value	Notes
Wi-Fi* and Bluetooth®	Integrated wireless module	Intel® Dual Band Wireless-AC 8260	
	Bands	Dual Band MIMO 2x2	2.4 and 5GHz
	Standards	IEEE 802.11agn + ac, BT 4.2 core	
	Security	WPA, WPA2, WPS2, 802.11w, WMM, WMM-PS, WFD, Miracast, Passpoint	
	Dual mode, BT 4.2 Core	Over 15 profiles supported	WPA2, AES-CCMP encryption
Antenna	Dual MHF4 connectors on module	Connection A1 is Wi-Fi* only while connection A2 services both BT and Wi-Fi*	
Power Manager	Integrated PMIC	SoC specific PMIC	Not user programmable

2.3 Expansion board requirements

The Intel® Joule™ Compute Module Expansion Board Design Guide provides design recommendations for designing customer expansion boards. At a minimum, the following elements are required to enable successful module boot and operation.

2.3.1 Method for connecting module to expansion board

The module must be securely mounted to an expansion board in a method that maintains full engagement of the board-to-board interface connectors. See the Intel® Joule™ Platform Mechanical Descriptor for more information.

2.3.2 Method to provide +VSYS power to the module

The subject is covered in Section 3.

2.3.3 Required strapping of module pins

These module pin strappings must be implemented for boot during each rising edge of PMIC_PWRGOOD (J6, pin 33). See 3.2.3 Power good for details.

Table 4 **Required strapping of module pins**

Signal Name	Location	Default	Requirement
UART_0_TXD	J6, pin 93	Internal 20k pull down	Must be Hi-z or pulled down to GND each time PMIC_PWRGOOD asserts
ISH_UART0_RTS	J7, pin 11	Internal 20k pull up	Must be Hi-z or pulled up to +VDD1 each time PMIC_PWRGOOD asserts
ISH_UART0_TXD	J7, pin 15	Internal 20k pull down	Must be Hi-z or pulled down to GND each time PMIC_PWRGOOD asserts
SPI_0_FS1	J7, pin 79	Internal 20k pull up	Must be Hi-z or pulled up to +VDD1 each time PMIC_PWRGOOD asserts
SPI_0_FS0	J7, pin 77	Internal 20k pull down	Must be Hi-z or pulled down to GND each time PMIC_PWRGOOD asserts
SPI_1_FS2	J6, pin 14	Internal 20k pull up	Must be Hi-z or pulled up to +VDD1 each time PMIC_PWRGOOD asserts

2.3.4 BIOS installed onto module

The module requires a Basic Input Output System (BIOS) code to be installed in the device firmware in order to complete the boot and initialization process. The reference configuration loaded during module production can be overwritten with either an updated, approved reference BIOS or a custom BIOS developed by other users, customers or partners.

Caution: Turning off the device during a BIOS update can cause data corruption and loss of functionality.

Warning: End-use equipment integrating the device has to be authorized as required by the U.S. Federal Communications Commission ("FCC") or it has to be operated in accordance with the FCC's rules on operation of unauthorized devices (47 C.F.R. § 2.805), including obtaining approval from any licensed spectrum operator, if the end-use equipment will use such operator's spectrum

Hyperlink: Regulatory Information for the Intel® Joule™ Compute Module

2.4 Expansion board recommendations

2.4.1 External EEPROM for multipurpose pin configuration data

An external EEPROM (recommend ST Microelectronics M24M02-DR* or equivalent) connected to I2C port 0 will hold a specific configuration of the multipurpose pins. During boot, if the BIOS does not find an EEPROM device attached to I2C port 0, then the module will load the default configuration that is stored in BIOS.

2.4.2 Power button

Connect an active low power button to J6 pin 9 to trigger a reset or to power cycle the board.

2.4.3 DnX button

Connect an active high (VDD1) signal to J6, pin 78 to initiate a Download and Execute routine that will update the BIOS via USB 2.0, port 0. This DnX button signal is the only way to initiate the Download and Execute update process.

2.4.4 Real time clock (RTC) backup power source

See section Section 10.1

2.4.5 UART debugging

Include a method to access UART port 2 on the module during boot to collect debug information as this is the only way to access debug messages generated during the power on and boot sequences.

3 Power Delivery, Signaling, and Reset

The power specifications stated herein apply to the capabilities of the Intel® Joule™ module itself. The power specifications will vary for the reference expansion board designed by Intel or for a carrier board that you design yourself. See the Intel® Joule™ Module Expansion Board Design Guide for more details.

3.1 Main power supply (+VSYS)

The Intel® Joule™ module requires +VSYS source routed through 12 pins, 6 on each board-to-board connector, that must all be connected in common to balance the current path.

This is the only power input path; voltage detection at VDCIN_SENSE or VBUS_SENSE will trigger module boot.

Caution: It is NOT possible to supply +VSYS directly from any USB power supply, as the USB operating specification of 4.75V to 5.25V may exceed the safe operational range of the module.

Table 5 **Boot decision per voltage supply condition**

VDCIN_SENSE	VBUS_SENSE	+VSYS	Action
0 VDC	0 VDC	> +VSYS (min)	No Boot
0 VDC	> VBUS_SENSE (min)	> +VSYS (min)	Cold Boot
> VDCIN_SENSE (min)	0 VDC	> +VSYS (min)	Cold Boot
> VDCIN_SENSE (min)	> VBUS_SENSE (min)	> +VSYS (min)	Cold Boot

3.2 Power on signaling

3.2.1 VDCIN_SENSE power sensing

VDCIN_SENSE is the signal that indicates when the module is being powered from an external power source.

When no RTC battery is present, the system will boot when both VDCIN_SENSE and +VSYS are at a valid level.

3.2.2 VBUS_SENSE power sensing

The VBUS_SENSE pin is used by the module to detect if power is present on the USB connector of the attached expansion board. If the VBUS_SENSE pin is within the voltage range specified in Table 7, then the module will initiate a boot.

3.2.3 Power good

The power good signal performs two transitions from LOW to HIGH to fully reset the module. First, the module will assert the PMIC_PWRGOOD signal HIGH after the +VDD1 and +VDD3 rails are within specification. Second, approximately 160 milli-seconds later, power good will transition LOW to complete initialization of internal registers. Then it transitions to HIGH again. Expansion board and mezzanine board designs must insure that circuitry does not interfere with the sate of the compute module boot strap pins. See the Expansion Board Design Guide, online at https://software.intel.com/en-us/node/731146, for details.

3.3 Power button behavior

The Intel® Joule™ module has a single Power Button pin (PMIC_PWRBTN_N) that will:

- trigger a shutdown of the module when held LOW for longer than 10 seconds.
- trigger standby mode on the module when held LOW for more than 2 seconds but less than 10 seconds.

3.4 System voltage rail specifications

Table 6 **Module power rails**

Rail Name	Voltage				Current			Direction	Usage
	Min	Typ	Max	Units	Min	Max	Units		
+VSYS	3.6	4	5.25	V		4	A	Input	Powers the core logic and radios. Recommend using 5V if using the CSI cameras.
+VDD3	3.1	3.3	3.45	V		300	mA	Output	General use. Powers on prior to VDD1
+V5P0V_VCONN	4.75	5	5.25	V		300	mA	Input	Voltage for USB-C VCONN to CC1 or CC2
+VDD1	1.71	1.8	1.89	V		300	mA	Output	General use. Power on after +VDD3
+VRTC	2.05		3.3	V	20	500	uA	Input	RTC backup voltage - supplies voltage to RTC logic when the system is not-powered.

3.5 Power sense signals

Table 7 **Power Sense Signals**

Rail Name	Voltage				Current			Direction	Usage
	Min	Typ	Max	Units	Min	Max	Units		
VBUS_SENSE	4	5	20	V		20	uA	Input	Voltage sense for +VBUS power
VDCIN_SENSE	4	12	20	V	20	20	uA	Input	Voltage sense for +VDC_IN power
VBATT_SENSE	0	3.8	5	V	<20		uA	Input	Voltage detection for battery. May be used to configure battery voltage as a gate to boot.

4 Graphics Specifications

4.1 Intel® Gen9LP features

- Gen9LP graphic engine can run at 450MHz or 650MHz according to model. See Table 2
- Intel 9th generation (Gen 9LP) graphics encoder / decoder engine
- Two or three slices of 6 EUs; each slice supports 6 threads resulting in a total of 12 or 18 available threads, depending on device SKU and configuration. See Table 2 for configurations, and Table 3 for descriptions of the EUs.
- Supports 3D rendering, media composting, and video encoding
- Graphics burst (570x only) enabled through energy counters
- Supports OpenGL* 4.3, OpenGL ES 3.1 and OpenCL 2.0
- 4x anti-aliasing
- Supports content protection using PAVP and HDCP 1.4/2.0
- Hardware capable of (up to) 4k video encode and decode; software dependencies exist.

4.2 Graphic encoder and decoder support

Table 8 **Graphics engine encoders and decoders supported**

Format	Decode Level	Encode Level
H.264	Profiles: CBP, MP, HP Level: L5.2 up to 1080p240, 4kx2kp60 Bit-rate up to 250 Mbps	Profiles: CBP, MP, HP Level: L5.1 up to 1080p120, 4kx2kp30 Bit-rate: up to 250 Mbps
H.265/HEVC	MP L5.1 up to 4kx2kp60 (Bit-rate: up to 40Mbps), MP L5 up to 4kx2kp30 (Bit-rate: up to 100Mbps) 10-bit	MP L4 up to 1080p60
MVC	CBP, MP HPL5.2 up to 4kx2kp60 *see Note*	CBP, MP HPL5.1 up to 4kx2kp30 see Note
VP8	Up to 4kx2kp60	1080p30 *see Note*
VP9	Up to 4kx2kp60	Up to 720p60, 1080p30 *see Note*
MPEG2	HD MPHL (1080p60)	HD MPHL (1080p30) *see Note*
VC-1	AP L4 (1080p60) *see Note*	
WMV9	MP HL (1080p30) *see Note*	
JPEG/MJPEG	1067 Mpps (420), 800 Mpps (422) at 400MHz, 25% non-zero coefficients)	1067 Mpps (420), 800 Mpps (422) (at 400MHz, 25% non-zero coefficients)

Note: Specific formats and configurations may require software support for the chosen operating system.

4.3 HDMI* signal group specifications

The Intel® Joule™ module provides a HDMI 1.4b interface through the board-to-board connectors for expansion board usage.

Refer to the Intel® Joule™ Compute Module Expansion Board Design Guide for the specifications and PCB routing guidance for this interface.

5 Wireless Connectivity

The Intel® Joule™ module contains an integrated Intel® Dual Band Wireless-AC 8260 adapter.

5.1 Intel® Dual Band Wireless-AC 8260 highlights

5.1.1 Wi-Fi features

- Dual-band 2.4 GHz and 5 GHz with MIMO 2x2
- Antenna Diversity is supported
- Radio on/off control via software
- Supports seamless roaming between access points; within respective band and mode of access point
- Compatible with Wi-Fi* Alliance protocols - note, module is NOT Wi-Fi* Alliance certified
  - Wi-Fi* CERTIFIED™ a/b/g/n/ac
  - WMM*, WMM-PS, WPA*, WPA2*, and WPS2*
  - Protected Management Frames
  - Wi-Fi* Direct® for peer to peer device connections
  - Wi-Fi* CERTIFIED™ Miracast Source
- IEEE WLAN Standards:
  - IEEE 802.11abgn, 802.11a/b/g/n/ac, 802.11d, 802.11e, 802.11h, 802.11i, 802.11w, 802.11r, 802.11k

5.2 Bluetooth® highlights

Dual mode Bluetooth® 4.2 Smart (Low Energy) enabling BR/EDR protocols

- Supports Bluetooth® Core Specification Version 4.2 with provisions for supporting future specifications
- Bluetooth® Class 1 or Class 2 transmitter operation

5.2.1 Supported Bluetooth® profiles

- Advanced Audio Distribution Profile (A2DP) (Source/Sink)1
- Audio/Video Remote Control Profile (AVRCP) (Controller/Target)1
- Basic Imaging Profile (BIP) (Initiator/Responder)
- Basic Printing Profile (BPP) (Sender)
- File Transfer Profile (FTP) (Client/Server)
- Generic Access Profile (GAP)
- Generic Attribute Profile (GATT)
- Generic Audio/Video Distribution Profile (GAVDP) (Source/Sink)1
- Generic Object Exchange Profile (GOEP) (Client/Server)
- Hands-Free Profile (HFP) (Audio Gateway) with Wide-Band Speech support (WBS)1
- Hardcopy Cable Replacement Profile (HCRP) (Client)
- Headset Profile (HSP) (Audio Gateway)1
- HID over GATT profile (HOGP) (Host), also known as Low Energy HID profile2
- Object Push Profile (OPP) (Client/Server)
- Phone Book Access Profile (PBAP) (Client)
- Synchronization Profile (SYNC) (Client)

5.3 Security

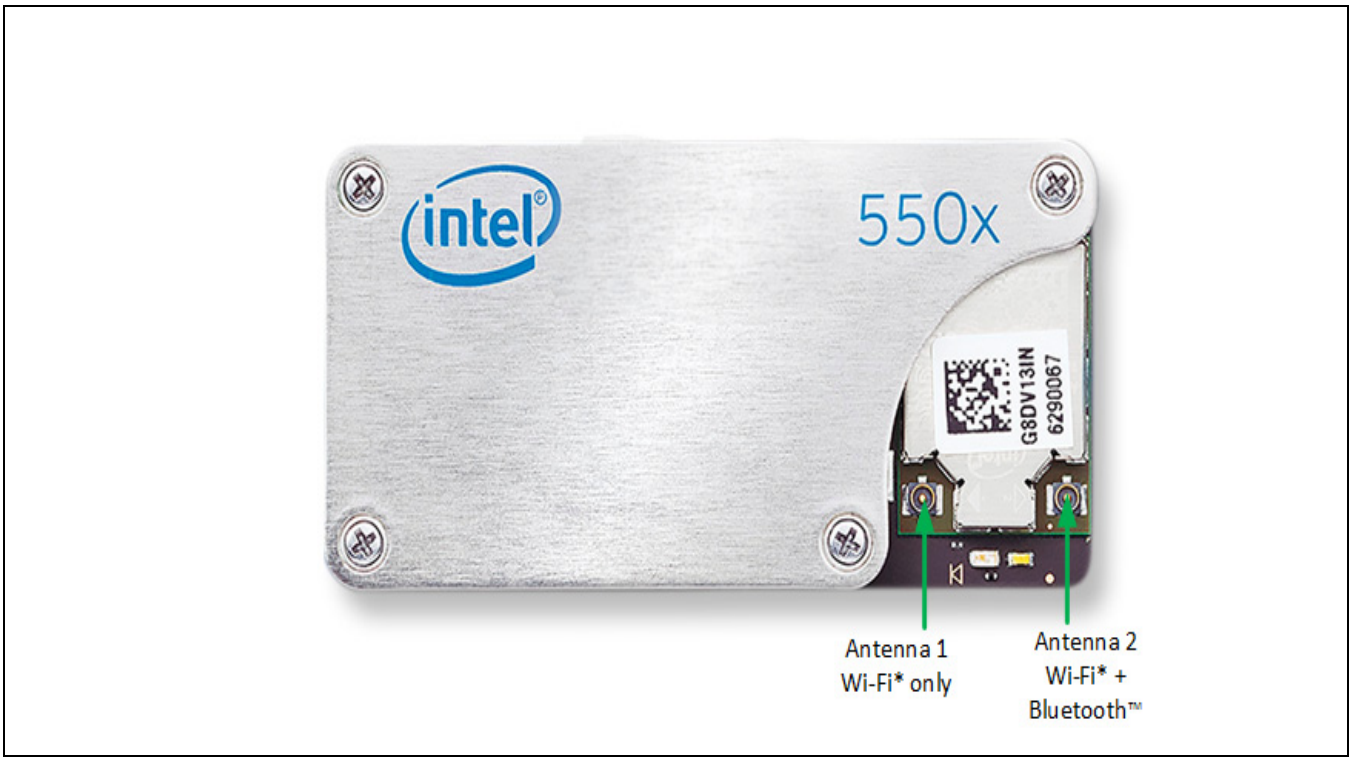
- Authentication: WPA and WPA2, 802.1X (EAP-TLS, TTLS, PEAP, LEAP, EAP-FAST), EAP-SIM, EAP-AKA
- Authentication Protocols: PAP, CHAP, TLS, GTC, MS-CHAP*, MS-CHAPv2
- Encryption: 64-bit and 128-bit WEP, AES-CCMP
- Wi-Fi* Direct® Encryption and Authentication: WPA2, AES-CCMP

5.4 Wireless antenna connectors

The module contains two MHF4 (U.FL compatible) antenna connectors that are labeled 1 and 2 with a triangle-shaped mark.

- A1 is dedicated to the Wi-Fi* service
- A2 supports both Wi-Fi* and Bluetooth® services

Figure 1 **Wireless antenna connector location**



5.5 The Intel® Dual Band Wireless-AC 8260 support site

Hyperlink: http://www.intel.com/content/www/us/en/support/network-and-i-o/wireless-networking/intel-wi-fi-products/intel-dual-band-wireless-ac-8000-series/intel-dual-band-wireless-ac-8260.html

Warning: End-use equipment integrating the device has to be authorized as required by the U.S. Federal Communications Commission ("FCC") or it has to be operated in accordance with the FCC's rules on operation of unauthorized devices (47 C.F.R. § 2.805), including obtaining approval from any licensed spectrum operator, if the end-use equipment will use such operator's spectrum

Hyperlink: Regulatory Information for the Intel® Joule™ Compute Module

6 SD Card Interface

6.1 SD card interface features

- Host clock up to 208 MHz (SDR 104)
- Supports card detection (insertion/removal) with dedicated card detection signal
- Meets SD Host Controller Standard Specification version 3.0
- Meets SD Physical Layer Specification version 3.01
- Only supports SD memory
- Supports 1.8v signal levels directly; requires an external level shifter to support devices that operate above 1.8V

6.1.1 SD card signal group specifications

The Intel® Joule™ module provides a SD Card interface through the board-to-board connectors for expansion board usage.

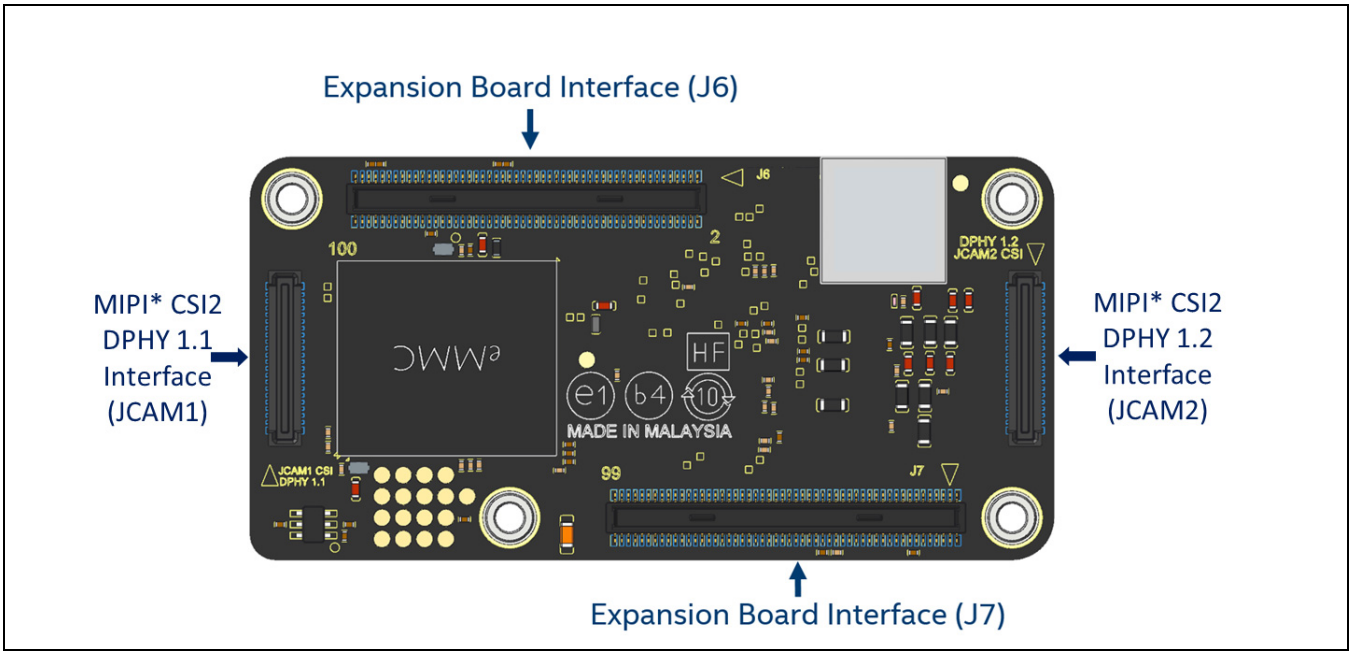
Refer to the Intel® Joule™ Compute Module Expansion Board Design Guide for the specifications and PCB routing guidance for this interface.

7 Module Connectors

The Intel® Joule™ module utilizes two separate, connectors, (J6 & J7) to break out system buses, power and GPIO signals, while two additional connectors (JCAM1 & JCAM2) are dedicated to MIPI-CSI imaging devices.

- All I/O signals are 1.8V with the exception of USB, MIPI CSI, and PCIe which adhere to their respective standards.
- Module connectors J6 and J7 (2x50) are common with Hirose Electric Co LTD* Part Number DF40C-100DP-0.4V and mate with Hirose Electric Co LTD* Part Number DF40C-100DS-0.4V, or compatible.
- JCAM1 and JCAM2 are MIPI CSI based imaging interfaces dedicated to MIPI CSI cameras via 2x20 Hirose* Part Number BM14B(0.8)-40DS-0.4V connectors
  - Mating connector for camera module Flex Printed Circuit Board attach: Hirose* BM14B(0.8)-40DP-0.4V

Figure 2 **Module physical connectors**



7.1 Module dimensions

See the Intel® Joule™ Platform Mechanical Descriptor for complete module and connector dimensions.Module to expansion board connectors

7.1.1 Module electrostatic discharge

ESD testing is performed at the system level, where the module is connected to an expansion board, and not at the module connectors. See the Intel® Joule™ Compute Module Expansion Board Design Guide for more ESD information.

7.1.2 J6 connector interface signals

Table 9 **J6 connector pin descriptions**

Pin	Signal Name	Usage	Description
36	+VDD1	Output	System 1.8 V
30	+VDD3	Output	System 3.3 V
41	+V5P0V_VCONN	Input	Power for USB3.0 CC pins for VCONN-powered accessory.

Table 9 **J6 connector pin descriptions**

Pin	Signal Name	Usage	Description
40	CHRG_INT_N	Input	General purpose input/output for the expansion board charger's interrupt pin, active low. Allows charger to interrupt host to report charger device status and faults. Connected to GPIO_19.
35	CHRG_EN_N	Output	General purpose input/output for the expansion board charger's enable pin, active low. Allows battery to be charged when power is connected to +VDC_IN on the expansion board. Connected to GPIO_15.
43	CODEC_MCLK	Output	MCLK for Master Mode operation for I²S audio
16	ISH_I2C_0_SCL (see note)	Output	I²C clock (open collector) Note: ISH I2C port 0 remapped to I2C port 5 in BIOS
18	ISH_I2C_0_SDA (see note)	Input/Output	I²C data (open collector) Note: ISH I2C port 0 remapped to I2C port 5 in BIOS
21	ISH_I2C_1_SCL (see note)	Output	I²C clock (open collector) Note: ISH I2C port 1 remapped to I2C port 6 in BIOS
23	ISH_I2C_1_SDA (see note)	Input/Output	I²C data (open collector) Note: ISH I2C port 1remapped to I2C port 6 in BIOS
46	HDMI_CLK_DN	Output	HDMI* clock negative
44	HDMI_CLK_DP	Output	HDMI* clock positive
68	DDI1_CTRL_CLK	Output	HDMI* I2C clock
70	DDI1_CTRL_DAT	Input/Output	HDMI* I2C data
62	HDMI_TX_0_DN	Output	HDMI* data lane 0 negative
58	HDMI_TX_1_DN	Output	HDMI* data lane 1 negative
50	HDMI_TX_2_DN	Output	HDMI* data lane 2 negative
64	HDMI_TX_0_DP	Output	HDMI* data lane 0 positive
56	HDMI_TX_1_DP	Output	HDMI* data lane 1 positive
52	HDMI_TX_2_DP	Output	HDMI* data lane 2 positive
74	UART2_CTS	Input	UART port 2 clear to send. UART port 2 is used as a debug port for BIOS messages during boot.
76	UART2_RTS	Output	UART port 2 ready to send. UART port 2 is used as a debug port for BIOS messages during boot.
80	UART2_RXD	Input	UART port 2 receive data. UART port 2 is used as a debug port for BIOS messages during boot.
78	UART2_TXD	Output	UART port 2 transmit data. UART port 2 is used as a debug port for BIOS messages during boot. Pin includes hardware strapping functionality for DNX boot.
4,10,19,42,48,54,60,66,72,73,82,86,96,98,100	GND	Ground	System ground
39	I2S_1_CLK	Input/Output	I²S bit clock. Supplied by the module in master mode and serves as an input in slave mode.
45	I2S_1_FS	Output	I²S frame sync
47	I2S_1_RXD	Input	I²S receive data
49	I2S_1_TXD	Output	I²S transmit data
94	GPIO_22	Input/Output	General purpose input/output
1	PWM_0	Output	Programmable pulse width modulator port 0
3	PWM_1	Output	Programmable pulse width modulator port 1
22	PWM_2	Output	Programmable pulse width modulator port 2
24	PWM_3	Output	Programmable pulse width modulator port 3
65	HPD_SRC	Input	General purpose input/output for HDMI cable hot plug detect. Instantiates a start-up communication between source and sink HDMI devices. Connected to GPIO_200.
84	BTN_N	Input	Connected to general purpose button on the expansion board. Connected to GPIO_17.
57	I2C_0_SCL	Output	I²C port 0 clock
95	I2C_0_SDA	Input/Output	I²C port 0 data

Table 9 **J6 connector pin descriptions**

Pin	Signal Name	Usage	Description
25	ISH_GPIO_0 (see note)	Input/Output	General purpose input/output 0
27	ISH_GPIO_1 (see note)	Input/Output	General purpose input/output 1
32	ISH_GPIO_2 (see note)	Input/Output	General purpose input/output 2
34	ISH_GPIO_3 (see note)	Input/Output	General purpose input/output 3
29	ISH_GPIO_4 (see note)	Input/Output	General purpose input/output 4
38	ISH_GPIO_5 (see note)	Input/Output	General purpose input/output 5
31	ISH_GPIO_6 (see note)	Input/Output	General purpose input/output 6
71	CLK_19P2M	Output	19.2 MHz clock
69	OTG_EN	Output	General purpose input/output controlled by PMIC to enable the module to power a USB OTG device
9	PMIC_PWRBTN_N	Input	System power/sleep button input to PMIC; active low.
33	PMIC_PWRGOOD	Output	Notification to system that all cold boot voltage rails to power the system have ramped up. Transitions high when module rails are within specification.
13	PMIC_RESET_N	Input	Notification to system that PMIC will respond to commands. When asserted, the PMIC will not respond to SoC commands via I2C or SVID because of the PMIC being either in standby or because a TLP is running. This is an active low signal.
79	SDCARD_CD_N	Input	SD card detect. Active low when a card is present, pulled high with internal pull-up when card is not present.
75	SDCARD_CLK	Output	SD card clock
89	SDCARD_CMD	Input/Output	SD card command is used for card initialization and transfer of commands.
81	SDCARD_D0	Input/Output	SD card data 0. By default, during power up or reset, only data 0 is used for data transfer.
83	SDCARD_D1	Input/Output	SD card data 1
85	SDCARD_D2	Input/Output	SD card data 2
87	SDCARD_D3	Input/Output	SD card data 3
77	SDCARD_LVL_CLK_FB	Input	SD card clock feedback for aligning the SDIO data from the level shifter on-board the expansion board via the controller. There is a loopback through the SD card level shifter that drives this pin.
90	SDCARD_LVL_CMD_DIR	Output	SD card command direction indicates whether host is transmitting or receiving over the command pin.
67	SDCARD_LVL_DAT_DIR	Output	SD card data direction indicates whether host is transmitting or receiving over the data.
88	SDCARD_LVL_SEL	Output	SD card level select performs the 1.8V to 3.0V negotiation.
91	SDCARD_PWR_DOWN_N	Output	SD card power down indicates to SDIO device to power down.
53	SPI_1_CLK	Output	SPI port 1 clock
63	SPI_1_MISO	Input	SPI port 1 receive data
55	SPI_1_FS0	Output	SPI port 1 slave select 0
14	SPI_1_FS2	Output	SPI port 1 slave select 2. Hardware strap with disable boot from SD card functionality.
51	SPI_1_MOSI	Output	SPI port 1 transmit data
93	UART_0_TXD	Output	UART port 0 transmit data. Hardware strap with reserved functionality. Note: Goes with UART0 signals on other connector
26	UART_1_RXD	Input	UART port 1 receive data
28	UART_1_TXD	Output	UART port 1 transmit data. Hardware strap with disable boot from eMMC functionality.
20	USB2_ID_PMIC	Input	USB OTG ID for device attach/detach and USB ACA detection via detection of resistance connected to pin. Connected to PMIC USBID pin.
8	USB2_0_DN	Input/Output	USB 2.0 port 0 data negative. Connected to PMIC USB 2.0 port 0.
6	USB2_0_DP	Input/Output	USB 2.0 port 0 data positive. Connected to PMIC USB 2.0 port 0.
59	USB_TYPC_CC1	Input/Output	USB type-C configuration channel 1. Connected to PMIC CC channel 1 pin.
61	USB_TYPC_CC2	Input/Output	USB type-C configuration channel 2. Connected to PMIC CC channel 2 pin.
11	+VRTC	Input	Real-time clock backup battery input to PMIC.
92	VBATT_SENSE	Input	Senses when battery is plugged in
99	VBUS_SENSE	Input	Connected to +VBUS from USB for PMIC detection when USB power source is plugged in.
97	VCONN_DCDC_EN	Output	General purpose input/output controlled by PMIC to enable load switch on expansion board to supply power to USB3.0 CC pins.

Table 9 **J6 connector pin descriptions**

Pin	Signal Name	Usage	Description
37	VDCIN_SENSE	Input	Connected to +VDC_IN from DC jack for PMIC detection when DC jack is plugged in.
2,5,7, 12,15,17	+VSYS	Input	System power
Note: Software enabling the Integrated Sensor Hub (ISH) is not currently available, thus the ISH_I2C_0 and ISH_I2C_1 ports are not functional. Until the ISH is enabled, the ISH_I2C_0 and ISH_I2C_1 ports have been remapped to I2C ports I2C_5 and I2C_6, respectively. Software enabling the Integrated Sensor Hub (ISH) is not currently available, thus the ISH_GPIO_0 through ISH_GPIO_6 are not functional. Until the ISH is enabled, the ISH_GPIO_0 through ISH_GPIO_6 have been remapped to GPIO ports GPIO_146 through GPIO_153, respectively.			

7.1.3 J7 connector interface signals

Table 10 **J7 connector pin descriptions**

Pin	Signal Name	Usage	Description
52	AVS_M_CLK_A1	Output	Microphone clock for channel A (voice trigger microphone)
62	AVS_M_CLK_B1	Output	Microphone clock for channel B (secondary microphone)
66	AVS_M_DATA_1	Input	First microphone pair data
75	FLASH_TORCH	Output	Output from shutter switch when it's pressed full way. This switch state is used to trigger Xenon flash or LED flash
73	FLASH_RST_N	Input	Output from shutter switch when it's pressed halfway. This switch state is used to trigger the Auto focus LED for Xenon Flash or Torch mode for LED flash, active low
71	FLASH_TRIGGER	Input	Control signal to Xenon Flash to start charging capacitor
2,5,8,10,16,17,23,24,29,30,35,36,41,42,54,60,61,67,74,80,84,85,91,90,93,96,99	GND	Ground	System ground
43	I2C_1_SCL	Output	I^2C port 1 clock
45	I2C_1_SDA	Input/Output	I^2C port 1 data
9	ISH_UART_0_CTS (see note)	Input/Output	Remapped by BIOS as GPIO_53, a general purpose input/output
11	ISH_UART_0_RTS (see note)	Input/Output	Remapped by BIOS as GPIO_52, a general purpose input/output
13	ISH_UART_0_RXD (see note)	Input/Output	Remapped by BIOS as GPIO_50, a general purpose input/output
15	ISH_UART_0_TXD (see note)	Input/Output	Remapped by BIOS as GPIO_51, a general purpose input/output
26	I2C_2_SDA	Input/Output	I^2C port 2 data
28	I2C_2_SCL	Output	I^2C port 2 clock
12,14,38, 40,69,81, 83, 92, 94, 98, 100	Reserved	Reserved	Do not use; leave disconnected
88	PCIE1_CLK_DN	Output	PCIe port 1 clock negative
86	PCIE1_CLK_DP	Output	PCIe1 port 1 clock positive
50	PCIE1_CLKREQ_N	Input	PCIe1 port 1 clock request, active low
72	PCIE1_WAKE_N	Input	PCIe1 wake, active low
70	PCIE1_PERST_n	Output	PCIe1 reset, active low
7	PMIC_SLPCLK_1	Output	32kHz RTC

Table 10 **J7 connector pin descriptions**

Pin	Signal Name	Usage	Description
59	SPI_0_CLK	Output	SPI port 0 clock
49	SPI_0_MISO	Input	SPI port 0 receive data
77	SPI_0_FS0	Output	SPI port 0 chip select 0. Hardware strap with reserved functionality.
79	SPI_0_FS1	Output	SPI port 0 chip select 1. Hardware strap with reserved functionality.
53	SPI_0_FS2	Output	SPI port 0 chip select 2
57	SPI_0_MOSI	Output	SPI port 0 transmit data
47	UART_0_CTS	Input	UART port 0 clear to send
55	UART_0_RTS	Output	UART port 0 return to send
51	UART_0_RXD	Input	UART port 0 receive data (note UART_0_TXD is on the other 100p connector)
18	USBC_SEL	Output	PMIC mux control for USB type-C polarity
63	USB2_1_DN	Input/Output	USB 2.0 data negative
65	USB2_1_DP	Input/Output	USB 2.0 data positive
44	USB3_0_RX_DN	Input	USB 3.0 data receive negative
46	USB3_0_RX_DP	Input	USB 3.0 data receive positive
6	USB3_0_TX_DN	Output	USB 3.0 data transmit negative
4	USB3_0_TX_DP	Output	USB 3.0 data transmit positive
95	USB3_1_RX_DP	Input	USB 3.0 data receive negative
97	USB3_1_RX_DN	Input	USB 3.0 data receive positive
89	USB3_1_TX_DN	Output	USB 3.0 data transmit negative
87	USB3_1_TX_DP	Output	USB 3.0 data transmit positive
1,3,20,22, 32,34	+VSYS	Input	System power
Note: Software enabling the Integrated Sensor Hub (ISH) is not currently available, thus the ISH_UART_0 is not functional. Until the ISH is enabled, the ISH_UART_0 port has been remapped to GPIO ports.			

7.2 MIPI* CSI signal group specifications

7.2.1 JCAM1 and JCAM2 connector interface signals

Table 11 **MIPI* CSI connector interface signals (JCAM1 and JCAM2)**

Connector Pin	Signal Name	Usage	Description	Note
21	CAM_CLK	Output	Camera master clock, programmable frequency	8
26	CSI_CLK_0_DN	Input	MIPI CSI Clock 0	3
24	CSI_CLK_0_DP	Input	MIPI CSI Clock 0	3
18	CSI_CLK_2_DN	Input	MIPI CSI Clock 2	4
16	CSI_CLK_2_DP	Input	MIPI CSI Clock 2	4
38	CSI_D0_DN	Input	MIPI CSI Data 0	
36	CSI_D0_DP	Input	MIPI CSI Data 0	
32	CSI_D1_DN	Input	MIPI CSI Data 1	
30	CSI_D1_DP	Input	MIPI CSI Data 1	
6	CSI_D2_DN	Input	MIPI CSI Data 2	5
4	CSI_D2_DP	Input	MIPI CSI Data 2	5
12	CSI_D3_DN	Input	MIPI CSI Data 3	5
10	CSI_D3_DP	Input	MIPI CSI Data 3	5
7	I2C_SCL	Output	I2C clock	7
5	I2C_SDA	Input/Output	I2C data	7
29	RESET1_N	Output	First camera reset, active low	
11	RESET2_N	Output	Second camera reset, active low	

Table 11 **MIPI* CSI connector interface signals (JCAM1 and JCAM2)**

Connector Pin	Signal Name	Usage	Description	Note
9	SID	Output	Second camera I2C ID	2
1	VCAM_A	Supply	Camera analog supply	6
13	VCAM_AF	Supply	Camera autofocus supply	6
31, 33	VCAM_DIG	Supply	Camera digital supply	6
37	VCAM_IO	Supply	Camera I/O supply	1,6
17, 23	VDD3	Supply	VDD3 supply	
27	XSDW	Output	Camera(s) shutdown, active low	

Notes:
1. VCAM_IO is shared between JCAM1 and JCAM2
2. SID is used for setting I2C slave address on the second sensor in a two camera configuration
3. For a single camera configuration, lanes D0-D3 are paired with CLK0
4. For two camera configuration, lanes D0-D1 are paired with CLK0 and lanes D2-D3 are paired with CLK_2
5. Lanes D2 and D3 are optional and may not be needed if using a single low resolution camera
6. Voltage rails are programmable and can be configured in SW driver. However, the module design must be able to withstand voltages described in Table 12 (MIPI* CSI DC specifications). Appropriate decoupling capacitors are required on the camera module side.
7. I2C signals require a 2.7k ohm pull-up to 1.8V, either externally or using the SoC internal pull-ups.
8. For two camera configuration, CAM_CLK is shared between both cameras.

8 MIPI* CSI Interface

8.1 MIPI* CSI DC specification

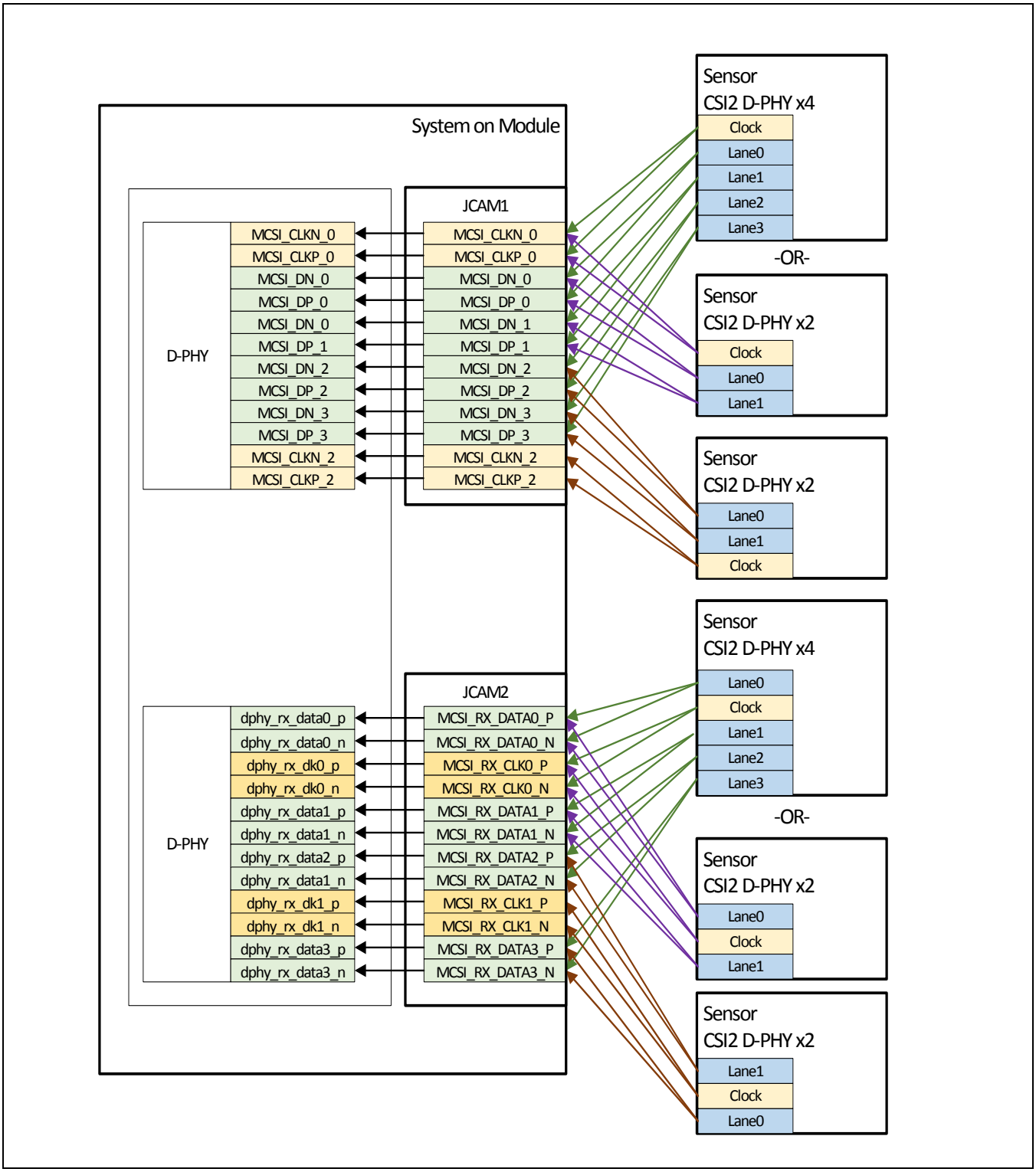
Supported configuration is a 13 mega-pixel camera module on JCAM1 and a 5 mega-pixel camera module on JCAM2. The pin-out is the same for each connector.

Table 12 **MIPI* CSI DC specifications**

Connector Pin #	Signal Name	VR Source	Voltage (V)	Accuracy	Current (mA)
1	VCAM_A	VPROG-3A, VPROG-3B	2.8	5%	200
13	VCAM_AF	VPROG5A, VPROG5B	2.8	5%	200
31, 33	VCAM_DIG	VPROG1E, VPROG1F	1.1	5%	500
37	VCAM_IO	VPROPG1B	1.8	5%	400
17, 23	VDD3	N/A	3.3V	5%	200

8.2 MIPI CSI Lane Mapping Diagram

Figure 3 **MIPI* CSI Lane Mapping**



9 I2C Interfaces

The Intel® Joule™ module provides 7 master I2C interfaces.

9.1 I2C features

- I2C_0 through I2C_6 support standard, full, fast and high-speed modes with a maximum data speed of 3.4Mbps
- I^2C master mode only; no support for multi-master mode
- Clock stretching by slave devices is possible
- Both 7-bit and 10-bit addressing modes are supported

9.2 I2C default configuration

Table 13 **I2C mapping**

Name	Description/Usage	Source	Destination
I2C_0	Dedicated EEPROM on expansion board (holds configuration table)	LPSS	Routed on module J7 for expansion board use
I2C_1	General usage	LPSS	Routed on module J7 for expansion board use
I2C_2	General usage	LPSS	Routed on module J7 for expansion board use
I2C_3	Camera support for JCAM2	LPSS	Module Camera Connector - JCAM2
I2C_4	Camera support for JCAM1	LPSS	Module Camera Connector - JCAM1
ISH_I2C_0	General usage; mapped to LPSS I2C_5	LPSS	Routed on module J6 for expansion board use
ISH_I2C_1	General usage; mapped to LPSS I2C_6	LPSS	Routed on module J6 for expansion board use

10 Clock Specifications

Two module clocks, 19.2 MHz (CLK_19P2M) and 32.768 kHz (PMIC_SLPCLK_1) are routed out through the board-to-board connectors for use on expansion boards.

Refer to the Intel® Joule™ Compute Module Expansion Board Design Guide for the specifications and PCB routing guidance of the clocks.

10.1 RTC backup battery

A backup power source is required for the RTC to operate robustly by preventing RTC data losses during unexpected power events. Implementation options are provided in the Intel® Joule™ Compute Module Expansion Board Design Guide (listed in Section 1.2).

The most common solution is a non-rechargeable coin-cell battery connected to V_RTC at module connector J6, pin 11.

11 UART Specifications

11.1 UART availability

Table 14 **Available UARTS**

Name	Type	Flow Control
UART0	Full HSUART support - dedicated to Boot Mode strapping on expansion board	Yes
UART1	Receive / Transmit only	None
UART2	Full HSUART support	Yes

12 I2S Specifications

One I2S port is provided by the J7 board-to-board connector interface.

12.1 I2S signal group specifications

12.1.1 I2S available formats

The I2S formats listed in Table 15 have not been verified and are subject to change.

Table 15 **I2S available configuration formats**

Mode	Priority	Frame rate	Bits/ sample	Number of slots	Frame to data offset	Frame polarity	Frame width	Frame rate inaccuracy	Notes
I²S master	1	192K,96K, 48K, 16K, 8K	16,24	2	1	0-left , 1-right	50/50	0%	Standard I²S protocol. 50% duty
PCM slave-SFS	1	192K,96K, 48K, 44.1 K, 16K, 8K	16,24	192kHz: 2 96 kHz: 4 All else: 1 to 6	0	High			
PCM slave - LFS	1	192K, 96K, 48K, 44.1K, 16K,8K	16,24	192 kHz: 2 96 kHz: 4 All else: 1 to 6	0	High		0%.	
PCM master -SFS	1	192K, 96K, 48K, 16K, 8K	16, 24	192 kHz: 2 All else: 1 to 4	0	High	1 bit clock wide	0%	Rising edge frame sensitive. Design supports more frame- to-data offset options.
PCM master - LFS	1	192K, 96K, 48K, 16K, 8K	16,24	192 kHz: 2 All else: 1 to 4	0	High	1-bit to n-bit clocks	0%	Design supports width > 1 slot.
Left justified master	2	192K,96K, 48K	16,24	2	0	0-left, 1-right	50/50	0%	Design supports flipping polarity on the frame signal.
I²S slave	3	192K,96K, 48K,44.1K	16,24	2	0	0-left, 1-right	50/50	0%	
Left justified slave	3	192K,96K, 48K	16,24	2	0	0-left, 1-right	50/50	0%	
Right justified	Not supported.								

12.2 Digital microphone ports

The Intel® Joule™ module supports microphones that use the PDM digital microphone standard and attached to the module through the AVS_M interface. Two microphones can share one data line by using time domain multiplexing to the two slots.

PDM microphones are enabled and disabled by the clock signal. Absence of clock signal will switch microphone to sleep mode, which can be utilized in system power management.

Additionally the microphones can be power-gated to cut the power consumption to zero when microphones are not used.

13 GPIO Specifications

13.1 Dedicated GPIO lines

The Intel® Joule™ module provides 9 dedicated GPIO lines (GPIO_0 - 6, GPIO_17 (aka BTN_N signal) and GPIO_22) connected to the core processor.

13.2 Reconfigurable interfaces buses as GPIO

Many interface lines on the module can be reconfigured as GPIO lines by defining a configuration table stored within an EEPROM device on the expansion board.

The BIOS loads a default configuration (see BIOS release notes for more details) if the EEPROM appears empty or is found unreadable by the BIOS. The configuration EEPROM is only read at cold boot and the configuration is retained during reset. Specific outputs can be can be set or cleared before entering a sleep state.

13.3 GPIO internal pull UP / pull DOWN resistors

Each GPIO line can employ an internal pull UP or pull DOWN resistor, this is also defined within the configuration table and stored in the expansion board EEPROM device and read by the BIOS at cold boot.

13.4 Operating System GPIO to function mapping

GPIO signals are configured in BIOS for each supported operating system. The default mapping can change with each iteration of the BIOS. Refer to the Intel Joule compute module website for the current default mapping for each supported operating system.

14 Pulse Width Modulators

The default BIOS configuration table defines four dedicated PWM outputs as PWM_0, PWM_1, PWM_2, and PWM_3, each with programmable frequency and duty cycle.

Table 16 shows examples of hardware (register) based PWM programming:

The PWM variables that control frequency and duty cycle are controlled by the BASE_UNIT_INT, BASE_UNIT_FRAC, and ON_TIME_DIVISOR register settings and the following equations:

14.1 PWM frequency formula:

$$Frequency \approx 19.2\,MHz * \frac{(PWM\ BASE\ UNIT)_d}{256}$$

14.2 PWM duty cycle formula:

$$Duty\ Cycle \approx \frac{(PWM\ ON\ TIME\ DIVISOR)_d}{256}$$

Note: Consult specific operating system documents if manipulating PWM settings at the OS level.

Table 16 **PWM programming examples**

Integer part of BASE_UNIT_INT (bits 29:22)	Fractional part of BASE_UNIT_FRAC (bits 21:8)	Decimal base unit value	ON_TIME_DIVISOR (bits 7:0)	Base unit type	PWM frequency (Hz)	PWM period (uSec)	Duty Cycle
0000_0000b	00_0100_0000_0000b	0.0625	0000_1000b	fractional	4,688	213	50%
0000_0000b	00_0010_0000_0000b	0.03125	0000_0100b	fractional	2,344	427	50%
0000_0000b	00_0001_0000_0000b	0.015625	0000_0001b	fractional	1,172	853	50%

15 Universal Serial Bus

15.1 Available USB ports

The Intel® Joule™ module provides two USB 3.0 ports; one Type C (OTG) and one USB 3.0 host mode and a USB 2 host port.

Table 17 **USB port types**

Signal name	Port	Description
USB2_0_DP	0	USB 2 data positive
USB2_0_DN		USB 2 data negative
USB3_1_RX_DP	1	USB 3 receive data positive
USB3_1_RX_DN		USB 3 receive data negative
USB3_1_TX_DP		USB 3 transmit data positive
USB3_1_TX_DN		USB 3 transmit data negative

Note: The series capacitors required for the TX lines for USB 3.0 signals are already designed into the Intel Joule module itself.