Intel® Joule™ Expansion Board

Design Guide

January 2017

Revision 1.0

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Revision	Description	Date
1.0	Initial release of the Intel® Joule™ Expansion Board Design Guide	January 2017

1 Introduction

1.1 Purpose

This document provides guidance towards designing Intel® Joule™ expansion boards for use with the Intel® Joule™ module.

1.2 Scope

This document provides the minimum information needed to design an expansion board for a module.

Note: The guidelines recommended in this document are based on preliminary simulation work done at Intel while developing systems. This work is ongoing, so the recommendations are subject to change.

Caution: If the guidelines listed in this document are not followed, it is very important the designers perform thorough signal integrity and timing simulations. Even when following these guidelines, Intel recommends the critical signals be simulated to ensure proper signal integrity and propagation time. Simulate any deviation from the guidelines.

1.3 Intended audience

The audience for this document is expected to have a background in electrical engineering, printed circuit board design methodologies, and component selection. The audience is also expected to have operational knowledge of the interface buses and communication protocols chosen to support all the accessories and peripherals anticipated to be part of any final configuration.

1.4 References

Intel Documents	Intel Document Number or Internet Address
Intel® Joule™ Module Datasheet	http://www.intel.com/content/dam/support/us/en/documents/joule-products/intel-joule-module-datasheet.pdf
Intel® Joule™ Expansion Board Schematic	http://www.intel.com/content/dam/support/us/en/documents/joule-products/intel-joule-expansion-board-schematic.pdf
Intel® Joule™ Expansion Board CAD Package	http://www.intel.com/content/dam/support/us/en/documents/joule-products/intel-joule-expansion-board-cad-package.zip
Intel® Joule™ Developer Kit Mechanical Descriptor	http://www.intel.com/content/dam/support/us/en/documents/joule-products/intel-joule-platform-mechanical-descriptor.pdf
Intel® Joule™ Module User Guide	https://software.intel.com/en-us/intel-joule-getting-started

1.5 Acronyms

Acronyms	Description
eMMC	embedded Multimedia Card
EMI	Electro-Magnetic Interference
ESD	Electro-Static Discharge
FPC	Flexible Printed Circuit
GPIO	General Purpose Input Output
GRD	Ground
HDMI*	High-Definition Multimedia Interface
I2C	Inter-Integrated Circuit—also known as IIC
LPDDR	Low Power Double Data Rate
LPSS	Low Power Subsystem
OSC	Oscillator
OTG	On-the-go
PCB or PWA	Printed Circuit Board or Printed Wire Assembly
PCM	Pulse Code Modulation
pF	Picofarads—unit of electrical capacitance
PMIC	Power Management Integrated Circuit
PTC	Positive Temperature Coefficient—a kind of fuse
RTC	Real-Time Clock
RxD	Receive Data
SOC	System on Chip
SOM	System on Module
SPI	Serial Peripheral Interface
TxD	Transmit Data
UART/HSUART	Universal Asynchronous Receiver/Transmitter—as used in this document, UART ports are assumed to only support RxD or TxD signals. High Speed UART—a full-function UART with additional handshake signals to enable faster speeds.
XTAL	Crystal

2 Mechanical Design Guidelines

This section describes keep out zones, mounting methods, and clearances relevant to designing an Intel® Joule™ expansion board.

Refer to the Intel® Joule™ Developer Kit Mechanical Descriptor document for additional details about the reference platform.

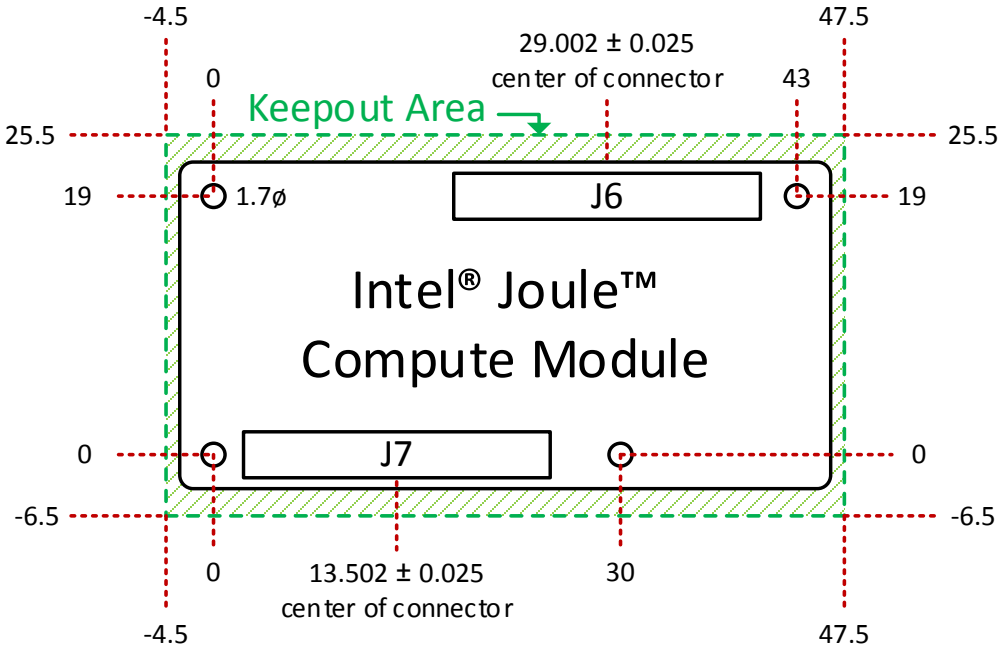
2.1 Module board-to-board connectors

The Intel® Joule™ module uses two board-to-board connectors to separate communication buses, power, and GPIO signals to the expansion board. Module connectors J6 and J7 mate with Hirose* Electric Co LTD part number DF40C-100DS-0.4V or other compatible hardware.

To properly interface with the module, keep the board-to-board connectors parallel, and maintain 19 mm between long-edge centerlines and 15.5 mm between short-edge centerlines, as shown in **Error! Reference source not found.**. The board-to-board interface connectors have a nominal stacking height of 1.5 mm between the inside planes of the module PCB and expansion board; see section 2.4

The following figures provide pertinent dimensional information for the expansion board for reference only. This information can change at any time. Refer to the Intel® Joule™ Developer Kit Mechanical Descriptor for current information.

Figure 2-1: Module key dimensions and keep out area



2.2 Module X-Y keep-out area

The modules require a keep-out area of 52 mm by 32 mm. Provide extra clearance for the installation tooling, accessory cabling, and module removal methods required by service and maintenance.

2.3 Vertical clearance

Vertical clearance is dictated by any thermal management solutions used. Figure 2-2 shows a bare module thermal plate for open-air operation. See the Intel® Joule™ Developer Kit Mechanical Descriptor for additional suggestions.

Figure 2-2: Bare module height

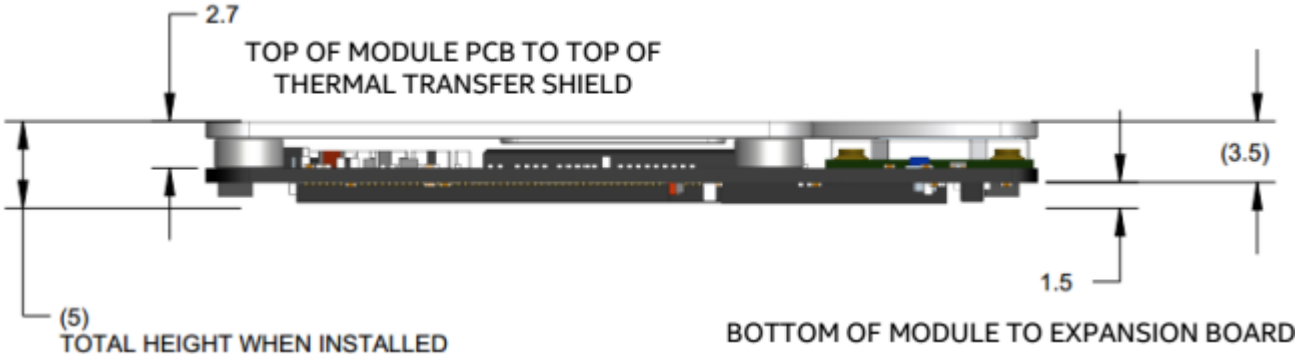
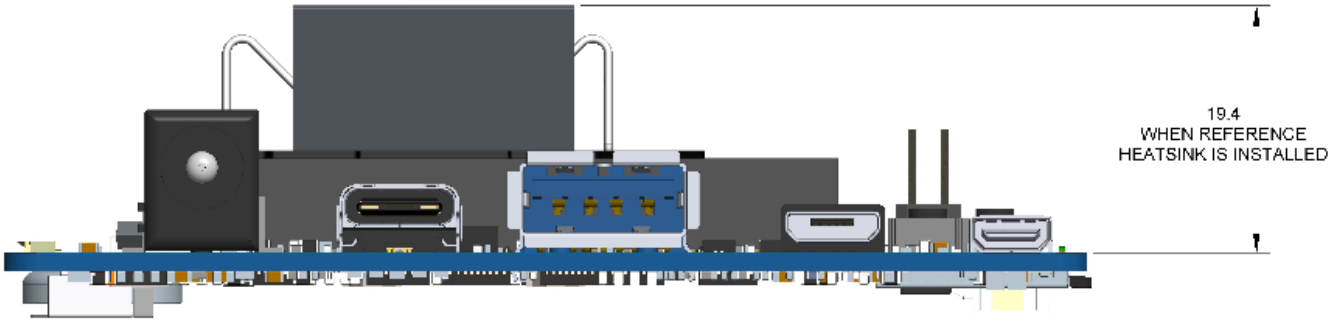


Figure 2-3: Developer kit with reference heatsink installed



2.4 Module retention

The following recommendations outline the elements of a robust and electrically stable module mounting method:

- Use mechanical techniques to maintain a 1.5 mm space between the module PCB and the expansion board.
- Use conductive hardware to provide a ground path between the expansion board and the module thermal plate.
- Apply even force (1.0 newton centimeters, maximum) at each through-hole mounting locations (module inserts).
- Thermal solutions that interface with the module thermal plate must be independently supported to prevent forces that can lift, twist, or crush the module during any movement-transition or vibration during actual, end-device use cases.

2.4.1 Development Kit – module mounting reference design

The following (reference only) images describe the surface mount, threaded standoff used on the development kit expansion board.

Figure 2-4: Cross section of development kit mounting hardware

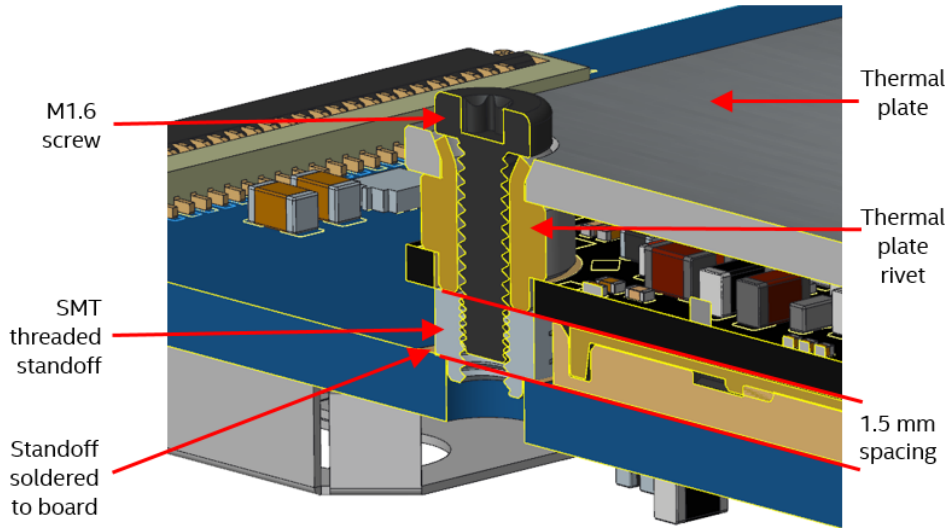
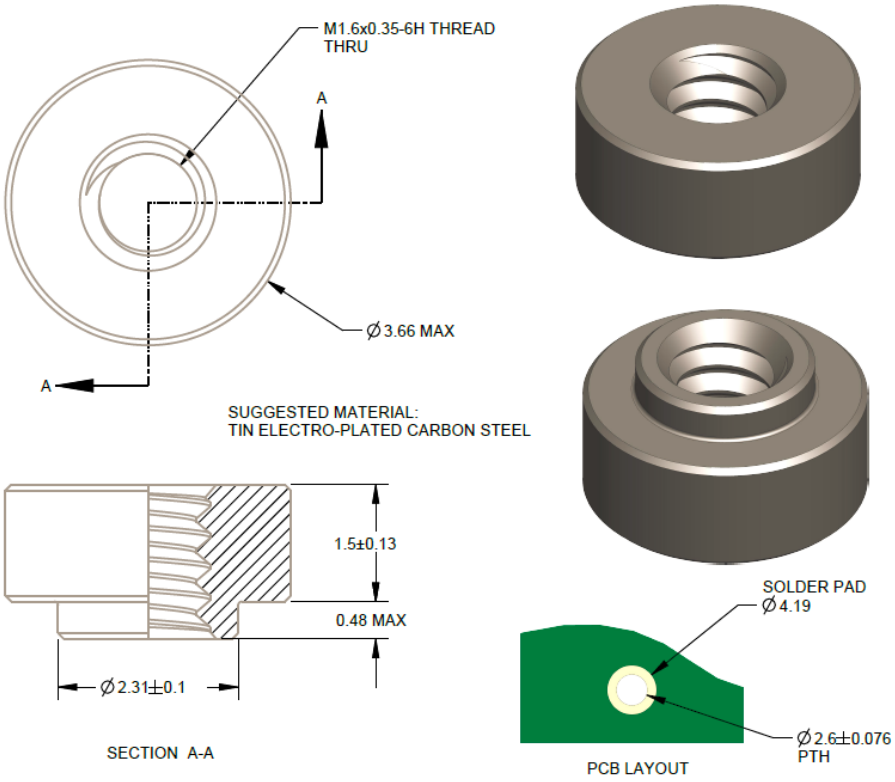


Figure 2-5: Reference design for expansion board SMT threaded standoff



3 Module Board-to-Board Connector Pinout

The Intel® Joule™ module interfaces with the Intel® Joule™ expansion board through two high-density, board-to-board connectors labeled J6 and J7 on the expansion board. The default pin usage of J6 and J7 refers to the vantage point of the expansion board. For example the +VBUS signal originates in the expansion board and is delivered to the module; therefore, +VBUS is an output from the expansion board.

Unless otherwise noted, all I/O signals operate at 1.8 VDC (with the exception of industry standard buses and protocols) each of which must operate within their defining specification parameters.

This pinout is provided as a quick reference; consult the Intel® Joule™ Module Datasheet for the latest information.

Table 3-1: Module J6 connector interface

Pin	Signal Name	Default Usage	Description
41	+V5P0V_VCONN	Output	Power for USB 3.0 CC pins for VCONN-powered accessory
99	+VBUS	Output	+VBUS from USB for PMIC detection when USB power source is plugged in
37	+VDC_IN	Output	+VDC_IN DC source input detection for PMIC
36	+VDD1	Input	System 1.8 VDC
30	+VDD3	Input	System 3.3 VDC
11	+VRTC	Output	Real-time clock backup battery input to PMIC
2, 5, 7, 12, 15, 17	+VSYS	Output	System power
84	BTN_N	Output	Intended for a general purpose (button or signal) that interrupts the processor to perform a priority task or execute a contextually based routine, this input is read at GPIO_17 and driven by a user action, sensor, or subsystem.
71	CLK_19P2M	Input	19.2 MHz clock
43	CODEC_MCLK	Input	MCLK for Master Mode operation of I2S audio
68	DDI1_CTRL_CLK	Input	HDMI I2C clock
70	DDI1_CTRL_DAT	Input/Output	HDMI I2C data
4, 10, 19, 42, 48, 54, 60, 66, 72, 73, 82, 86, 96, 98, 100	GND	Ground	System ground
94	GPIO_22	Output	General purpose input/output
46	HDMI_CLK_DN	Input	HDMI clock negative
44	HDMI_CLK_DP	Input	HDMI clock positive
62	HDMI_TX_0_DN	Input	HDMI data lane 0 negative
64	HDMI_TX_0_DP	Input	HDMI data lane 0 positive
58	HDMI_TX_1_DN	Input	HDMI data lane 1 negative
56	HDMI_TX_1_DP	Input	HDMI data lane 1 positive
50	HDMI_TX_2_DN	Input	HDMI data lane 2 negative
52	HDMI_TX_2_DP	Input	HDMI data lane 2 positive
65	HPD_SRC	Output	General purpose input/output for HDMI cable hot-plug detection This signal sets up a start-up communication between sources and sink HDMI devices; this is also connected to GPIO_200.
57	I2C_0_SCL	Input	I2C port 0 clock, used for configuration EEPROM
95	I2C_0_SDA	Input/Output	I2C port 0 data, used for configuration EEPROM
39	I2S_1_CLK	Input/Output	I2S-bit clock supplied by the module in master mode and serves as an input in slave mode.

Pin	Signal Name	Default Usage	Description
45	I2S_1_FS	Input	I2S frame sync
47	I2S_1_RXD	Output	I2S receive data
49	I2S_1_TXD	Input	I2S transmit data
25	ISH_GPIO_0	Input	General purpose input/output 0, set at output by BIOS until reconfigured[1]
27	ISH_GPIO_1	Input	General purpose input/output 1, set at output by BIOS until reconfigured[1]
32	ISH_GPIO_2	Input	General purpose input/output 2, set at output by BIOS until reconfigured[1]
34	ISH_GPIO_3	Input	General purpose input/output 3, set at output by BIOS until reconfigured[1]
29	ISH_GPIO_4	Input	General purpose input/output 4
38	ISH_GPIO_5	Input	General purpose input/output 5
31	ISH_GPIO_6	Input	General purpose input/output 6
16	ISH_I2C_0_SCL	Input	I2C port 0 clock, mapped to I2C5
18	ISH_I2C_0_SDA	Input/Output	I2C port 0 data, mapped to I2C5
21	ISH_I2C_1_SCL	Input	I2C port 1 clock, mapped to I2C6
23	ISH_I2C_1_SDA	Input/Output	I2C port 1 data, mapped to I2C6
69	OTG_EN	Input	Module generates the OTG enable signal based on the detected port connection.
9	PMIC_PWRBTN_N	Output	Active low output from the expansion board to the module that controls the power state of the module and, by extension, the expansion board, see the Intel® Joule™ Module Datasheet for how the PMIC_PWRBTN_N signal controls the module power state based on duration of the low signal.
33	PMIC_PWRGOOD	Input	Active high output signal from the module to the expansion board that latches the state of the module strapping options (refer to Section 4.6), this signal also indicates if +VDD1 and +VDD3 power supplies from the module are within specification.
13	PMIC_RESET_N	Input	Active low signal output from the module to the expansion board, an expansion board may use this signal to control when the module strapping option signals are driven by the expansion board circuitry. Refer to the module datasheet for additional details of the PMIC_RESET_N signal. Leave the PMIC_RESET_N signal floating if not used on the expansion board.
1	PWM_0	Input	Programmable pulse width modulator port 0
3	PWM_1	Input	Programmable pulse width modulator port 1
22	PWM_2	Input	Programmable pulse width modulator port 2
24	PWM_3	Input	Programmable pulse width modulator port 3
40	Reserved	N/A	No connect
35	Reserved	N/A	No connect
92	Reserved	N/A	No connect
79	SDCARD_CD_N	Output	SD card detect, active low when a card is present, pulled high with internal pull-up when a card is not present
75	SDCARD_CLK	Input	SD card clock
89	SDCARD_CMD	Input/Output	SD card command is used for card initialization and transfer of commands.
81	SDCARD_D0	Input/Output	SD card data 0, by default, during power up or reset, only data 0 is used for data transfer.
83	SDCARD_D1	Input/Output	SD card data 1
85	SDCARD_D2	Input/Output	SD card data 2
87	SDCARD_D3	Input/Output	SD card data 3

[1] During BIOS execution the ISH_GPIO_0-3 signals are configured as outputs and change state to indicate BIOS progression. End users should take this into account in their design.

Pin	Signal Name	Default Usage	Description
77	SDCARD_LVL_CLK_FB	Output	SD card-clock feedback for aligning the SDIO data from the level shifter on-board the expansion board through the controller, there is a loopback through the SD card level shifter that drives this pin.
90	SDCARD_LVL_CMD_DIR	Input	SD card-command direction indicates if the host is transmitting or receiving over the command pin.
67	SDCARD_LVL_DAT_DIR	Input	SD card-data direction indicates if the host is transmitting or receiving over the data.
88	SDCARD_LVL_SEL	Input	SD card-level select performs the 1.8 V-to-3.0 V negotiation.
91	SDCARD_PWR_DOWN_N	Input	SD card-power down tells the SDIO device to power down.
53	SPI_1_CLK	Input	SPI port 1 clock
55	SPI_1_FS0	Input	SPI port 1 slave select 0
14	SPI_1_FS2	Input	SPI port 1 slave select 2, hardware strap with disable boot from SD card functionality
63	SPI_1_MISO	Output	SPI port 1 receive data.
51	SPI_1_MOSI	Input	SPI port 1 transmit data
93	UART_0_TXD	Input	UART port 0 transmit data, hardware strap with reserved functionality Note: This goes with UART0 signals on other connector.
26	UART_1_RXD	Output	UART port 1 receive data.
28	UART_1_TXD	Input	UART port 1 transmit data, hardware strap with disable boot from eMMC functionality
74	UART2_CTS	Output	BIOS configures the UART port 2 lines as the serial debug path. See section 8 for details.
76	UART2_RTS	Input	BIOS configures the UART port 2 lines as the serial debug path. See section 8 for details.
80	UART2_RXD	Output	BIOS configures the UART port 2 lines as the serial debug path. See section 8 for details.
78	UART2_TXD	Input	BIOS configures the UART port 2 lines as the serial debug path. See section 8 for details.
59	USB_TYPC_CC1	Input/Output	Type-C configuration channel 1, connected to PMIC CC channel 1 pin
61	USB_TYPC_CC2	Input/Output	Type-C configuration channel 2, connected to PMIC CC channel 2 pin
8	USB2_0_DN	Bidirectional	USB 2.0 port 0 data negative, connected to PMIC USB 2.0 port 0
6	USB2_0_DP	Bidirectional	USB 2.0 port 0 data positive, connected to PMIC USB 2.0 port 0
20	USB2_ID_PMIC	Output	USB OTG ID for device attach or detach and USB ACA detection through detection of resistance connected to pin, connected to PMIC USBID pin
97	VCONN_DCDC_EN	Input	VCONN_DCDC_EN is a control signal generated by the module to enable expansion board-based supply for USB 3.0 CC pins.

Table 3-2: Module J7 connector interface

Pin	Signal Name	Default Usage	Description
1, 3, 20, 22, 32, 34	+VSYS	Output	System power
52	AVS_M_CLK_A1	Input	Microphone clock for channel A (voice trigger microphone)
62	AVS_M_CLK_B1	Input	Microphone clock for channel B (secondary microphone)
66	AVS_M_DATA_1	Output	Microphone data for channels A and B
73	FLASH_RST_N	Input	Although titled FLASH_RST_N, function is configured as GPIO functionality
75	FLASH_TORCH	Input	Although titled FLASH_TORCH, function is configured as GPIO functionality
71	FLASH_TRIGGER	Input	Although titled FLASH_TRIGGER, function is configured as GPIO functionality
2, 5, 8, 10, 16, 17, 23, 24, 29, 30, 35, 36, 41, 42, 54, 60, 61, 67, 74, 80, 84, 85, 91, 90, 93, 96, 99	GND	Ground	System ground
43	I2C_1_SCL	Input	I2C port 1 clock
45	I2C_1_SDA	Input/Output	I2C port 1 data
28	I2C_2_SCL	Input	I2C port 2 clock
26	I2C_2_SDA	Input/Output	I2C port 2 data
9	ISH_UART_0_CTS	Output	Although titled UART, function is configured as GPIO functionality
11	ISH_UART_0_RTS	Input	Although titled UART, function is configured as GPIO functionality
13	ISH_UART_0_RXD	Output	Although titled UART, function is configured as GPIO functionality
15	ISH_UART_0_TXD	Input	Although titled UART, function is configured as GPIO functionality
7	PMIC_SLPCLK_1	Input	32.768 kHz RTC
68	Reserved	N/A	No connect
82	Reserved	N/A	No connect
27	Reserved	N/A	No connect
25	Reserved	N/A	No connect
21	Reserved	N/A	No connect
19	Reserved	N/A	No connect
33	Reserved	N/A	No connect
31	Reserved	N/A	No connect
39	Reserved	N/A	No connect
37	Reserved	N/A	No connect
76	Reserved	N/A	No connect
78	Reserved	N/A	No connect
12, 14, 38, 40, 69, 81, 83, 92, 94, 98, 100	Reserved	N/A	No connect
56	Reserved	N/A	No connect

Pin	Signal Name	Default Usage	Description
58	Reserved	N/A	No connect
64	Reserved	N/A	No connect
88	Reserved	N/A	No connect
86	Reserved	N/A	No connect
50	Reserved	N/A	No connect
72	Reserved	N/A	No connect
70	Reserved	N/A	No connect
59	SPI_0_CLK	Input	SPI port 0 clock
77	SPI_0_FS0	Input	SPI port 0 chip select 0, hardware strap with reserved functionality
79	SPI_0_FS1	Input	SPI port 0 chip select 1
53	SPI_0_FS2	Input	SPI port 0 chip select 2
49	SPI_0_MISO	Output	SPI port 0 receive data
57	SPI_0_MOSI	Input	SPI port 0 transmit data
47	UART_0_CTS	Output	UART port 0 clear-to-send
55	UART_0_RTS	Input	UART port 0 return-to-send
51	UART_0_RXD	Output	UART port 0 receive data (Note: UART_0_TXD is on the J6 connector)
63	USB2_1_DN	Bidirectional	USB 2.0 port 1 data negative
65	USB2_1_DP	Bidirectional	USB 2.0 port 1 data positive
44	USB3_0_RX_DN	Output	USB 3.0 port 0 data receive negative
46	USB3_0_RX_DP	Output	USB 3.0 port 0 data receive positive
6	USB3_0_TX_DN	Input	USB 3.0 port 0 data transmit negative
4	USB3_0_TX_DP	Input	USB 3.0 port 0 data transmit positive
97	USB3_1_RX_DN	Output	USB 3.0 port 1 data receive positive
95	USB3_1_RX_DP	Output	USB 3.0 port 1 data receive negative
89	USB3_1_TX_DN	Input	USB 3.0 port 1 data transmit negative
87	USB3_1_TX_DP	Input	USB 3.0 port 1 port 1 data transmit positive
18	USBC_SEL	Input	PMIC mux control for Type-C polarity

4 Power Subsystem and Accessory Signaling

4.1 Primary power source and grounding

The Intel® Joule™ module requires a primary power source (+VSYS) routed through 12 pins, 6 on each board-to-board connector. Connect all 12 +VSYS lines in common on the Intel® Joule™ expansion board to balance the input current path to the module.

Connect all ground pins common to board ground planes and the module mechanical mounting solution.

Refer to the Intel® Joule™ Module Datasheet for module-specific information.

Table 4-1: Module power and ground pins

Signal	Module Connector/Pin	Direction	Usage
+VDC_IN	J6 pin 37	Output	Signal module to boot requires +VSYS at acceptable levels
+VSYS	J6 pin (2,5,7,12,15, and 17) J7 pin (1, 3, 20, 22, 32, and 34)	Output	Module power input
+VBUS	J6 pin 99	Output	Signal module USB power is available
+V5P0V_VCONN	J6 pin 41	Output	Provide module a +5 VDC USB CC signal
+VRTC	J6 pin 11	Output	RTC backup voltage supplies voltage to RTC logic when the system is not powered.
Ground	J6 pin (4, 10, 19, 42, 48, 54, 60, 66, 72, 73, 82, 86, 96, 98, 100) J7 pin (2, 5, 8, 10, 16, 17, 23, 24, 29, 30, 35, 36, 41, 42, 54, 60, 61, 67, 74, 80, 84, 85, 91, 90, 93, 96, 99)		Common ground

4.2 Module status signaling

The module boot signal comes from either +VDC_IN or +VBUS, because power applied to +VSYS alone does not enable module operation. If it is necessary for the module to be enabled whenever +VSYS is available or USB power supply is connected, connect the +VDC_IN module signal to the +VSYS net expansion board, and connect +VBUS from the USB connector to the +VBUS signal.

4.2.1 Power rail enabling

The +VDD1 and +VDD3 power rails rise during cold boot of the module PMIC, so both rails are stable before the SoC is taken out of the reset and before code execution starts. They are intended to activate voltage regulators on the expansion board so system devices can be available when the module code execution begins.

Both the +VDD1 and +VDD3 rails can be used directly for powering system components or enabling voltage regulators and supplies on the expansion board if the maximum current limits of Table 4-2 are not exceeded.

If the power consumption of external peripherals is not known, do not use the +VDD1 and +VDD3 power rails directly.

Table 4-2: Power rails available from the module

Voltage Rail Name	Nominal Voltage	Maximum Current	Module Pin	Description
+VDD3	3.3 VDC	300 mA	J2 pin 30	+3.3 V power supply sourced from the module and derived from the +VSYS supply to the module Do not exceed maximum current specified.
+VDD1	1.8 VDC	300 mA	J2 pin 36	+1.8 V power supply sourced from the module and derived from the +VSYS supply to the module Do not exceed maximum current specified.

4.3 Module sideband and GPIO control signals

Sideband signals from the module are used for communicating to, and control of, the expansion board devices.

The PMIC_RESET_N and PMIC_PWRGOOD signals provide module status information to assist debug tasks; it is optional to route these signals on an expansion board or set them as no connect at the module connector if the signals are not used on the expansion board.

The USB signals are necessary to provide connection awareness for various power modes and device state determination.

Table 4-3: PMIC and SoC sideband and GPIO signals

Signal name	From	To	Connector/Pin	Description
PMIC_PWRBTN_N	Expansion Board	Module	J6 pin 9	Active low output from the expansion board to the module that controls the power state of the module and, by extension, the expansion board, see the Intel® Joule™ Module Datasheet for how the PMIC_PWRBTN_N signal controls the module power state based on duration of the low signal.
PMIC_RESET_N	Module	Expansion Board	J6 pin 13	Active low signal output from the module to the expansion board, an expansion board may use this signal to control when the module strapping option signals are driven by the expansion board circuitry. Refer to the Intel® Joule™ Module Datasheet for additional details of the PMIC_RESET_N signal. Leave the PMIC_RESET_N signal floating if not used on the expansion board.
PMIC_PWRGOOD	Module	Expansion Board	J6 pin 33	The module asserts the PMIC_PWRGOOD signal high after the VDD1 and VDD3 rails are within specification.
OTG_EN	Module	USB-C OTG Load Switch	J6 pin 69	Active high, enable 5 V supply for USB OTG
USBC_SEL	Module	Type-C mux	J7 pin 18	Active high or low, Type-C mux port selection signal
VCONN_DCDC_EN	Module	USB-C VCONN Switch	J6 pin 97	Active high, module VCONN input voltage load switch control signal
USB2_ID_PMIC	Expansion Board	Module	J6 pin 20	Active high, indicator for module that a USB OTG cable is connected

Note: Refer to the Intel® Joule™ Module Datasheet for additional electrical specifications.

4.4 Platform power supply (simplistic model)

Figure 4-1 describes a simple power supply for a minimalistic expansion board design using an external 12-VDC, 3-A power supply connected directly to the DC input path.

Any DC input must have adequate protection, for example a reverse-current blocking diode, a fuse, and an ESD transient suppression diode. This DC input path must also have sufficient decoupling capacitors before and after the +VSYS buck regulator.

If the expansion board is designed with +VDC_IN connected to a primary power source, as shown in Figure 4-1, then the module begins to boot when power is applied. For designs not intended to boot when power is connected (remote or secondary enabling), +VDC_IN must be raised to, or above, +VSYS for the module boot sequence to begin.

Refer to the Intel® Joule™ Module Datasheet for the current +VDC_IN and +VSYS voltage ranges.

A buck regulator on the expansion board is necessary to generate module +VSYS power at a controlled 5 V and 5 A regulation. This buck regulator circuit must have a safe input voltage range that is higher than the DC-input supply path provides under any condition.

The +VDD1 and +VDD3 from the module ramp and stabilize before the module code execution begins. These two rails can be used to enable additional voltage regulators and load switches on the expansion board, and those regulator and switches in turn provide power to platform devices.

Figure 4-1: Simple power supply

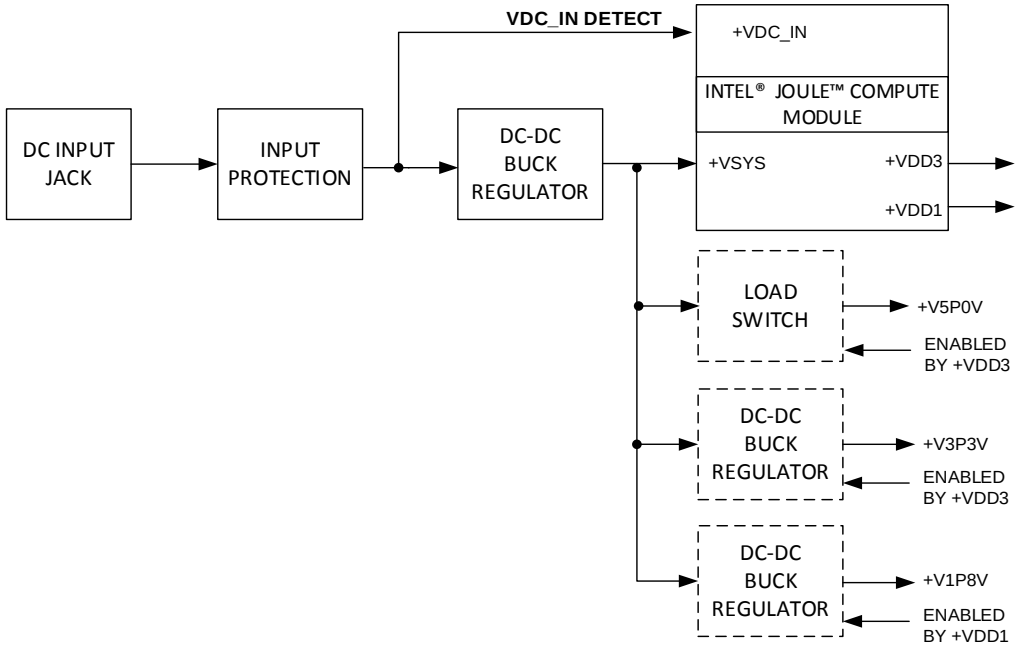
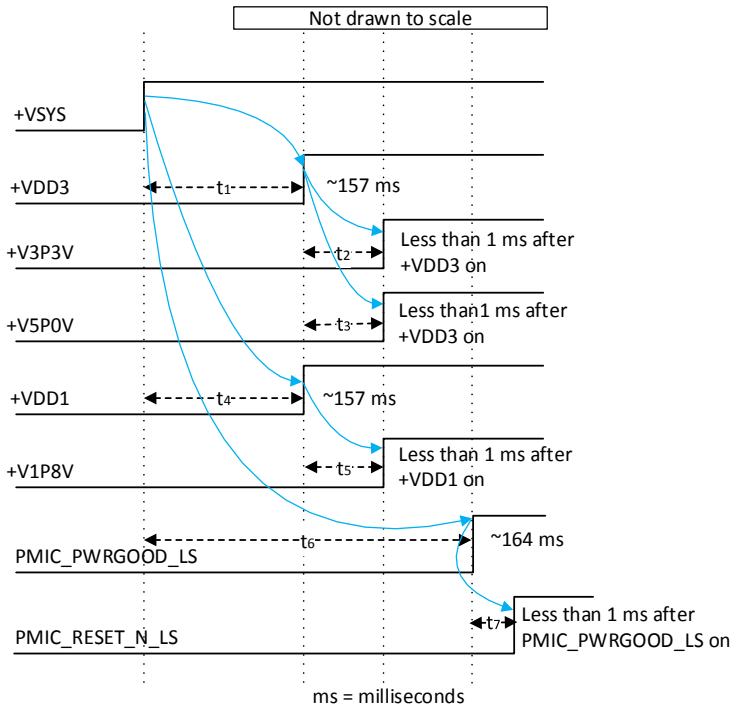


Figure 4-2: Power-on timing sequence



Notes:

- All supplies are off within 2 ms of shutdown event.
- Power up order of rails +VDD1 and +VDD3 is not guaranteed, but does not adversely affect operability.

4.5 Power on, reset, and firmware updating

4.5.1 Power button and reset method

The BIOS defines events initiated by the PMIC_PWRBTN_N button; reference BIOS 161 provides three functions:

- Power on: press for 2 seconds to boot.
- Sleep mode: when powered, press for 2 seconds to put to sleep.
- Mechanical off: press for 10 seconds to power off.

4.5.2 Firmware update on reset

The platform can be configured to enter a BIOS update (download and execute mode) when UART2_TXD (pin 78 on connector J6) is pulled low—and held low until the de-assertion of PMIC_RESET_N.

Additional requirements for the DnX sequence to function:

- A USB device female port, for example a micro receptacle on USB2 port 0 or the Type-C port
- Route +VBUS from the USB connector to the module +VBUS signal (connector J6 pin 99), this allows the module to detect a host connection and mount the media.
- A properly formatted source media with a valid BIOS image in the default partition, see the BIOS setup guide for more information.

4.6 Required straps

The boot behavior of the SoC on the module can be influenced by a number of strap signals. Table 4-4 shows the configuration of the straps for normal operation. It is the designer's responsibility to ensure that their design does not impact the default signal levels in table 4-5; that is, the signals must remain in the default states until the PMIC_RESET_N is de-asserted.

Table 4-4: Required strapping of module pins

Signal Name	Location	Default	Requirement
UART_0_TXD	J6, pin 93	Internal 20k pull down	Must be Hi-Z or pulled down to GND when PMIC_PWRGOOD asserts
ISH_UART_0_RTS	J7, pin 11	Internal 20k pull up	Must be Hi-Z or pulled up to +VDD1 when PMIC_PWRGOOD asserts
ISH_UART_0_TXD	J7, pin 15	Internal 20k pull down	Must be Hi-Z or pulled down to GND when PMIC_PWRGOOD asserts
SPI_0_FS0	J7, pin 77	Internal 20k pull up	Must be Hi-Z or pulled down to GND when PMIC_PWRGOOD asserts
SPI_0_FS1	J7, pin 79	Internal 20k pull up	Must be Hi-Z or pulled up to +VDD1 when PMIC_PWRGOOD asserts
SPI_1_FS2	J6 pin 14	Internal 20k pull up	Must be pulled up when PMIC_PWRGOOD asserts or left floating

4.7 Real-time clock backup battery

A backup power source is necessary for the real-time clock to operate robustly and prevent RTC data losses during unexpected power loss. This can be provided by a non-rechargeable, coin-cell battery connected to +VRTC at module connector J6 pin 11.

5 GPIO Level Transitioning

5.1 Module J2 GPIO connector interface

All module GPIO lines function at 1.8 V levels. Intel® Joule™ expansion board provides appropriate level transition, signal conditioning, and protection for devices on—or devices connected to—the expansion board. The default pin usage of J2 and J3 refers to the vantage point of the module. For example the ISH_GPIO_0 signal originates in the module and is delivered to the expansion board; therefore, ISH_GPIO_0 is an output (as configured by BIOS).

Level transition circuits for GPIO lines must be powered and stable before the module completes the cold boot routine.

Pin	Signal Name	Default Usage	Description
25	ISH_GPIO_0	Input	General purpose input/output 0, set as output by BIOS until reconfigured[1]
27	ISH_GPIO_1	Input	General purpose input/output 1, set as output by BIOS until reconfigured[1]
32	ISH_GPIO_2	Input	General purpose input/output 2, set as output by BIOS until reconfigured[1]
34	ISH_GPIO_3	Input	General purpose input/output 3, set as output by BIOS until reconfigured[1]
29	ISH_GPIO_4	Input	General purpose input/output 4
38	ISH_GPIO_5	Input	General purpose input/output 5
31	ISH_GPIO_6	Input	General purpose input/output 6

5.2 Module J3 GPIO connector interface

Pin	Signal Name	Default Usage	Description
9	ISH_UART_0_CTS	Output	Although titled UART, function is configured as GPIO functionality
11	ISH_UART_0_RTS	Output	Although titled UART, function is configured as GPIO functionality
13	ISH_UART_0_RXD	Input	Although titled UART, function is configured as GPIO functionality
15	ISH_UART_0_TXD	Input	Although titled UART, function is configured as GPIO functionality
73	FLASH_RST_N	Input	Although titled FLASH_RST_N, function is configured as GPIO functionality
75	FLASH_TORCH	Input	Although titled FLASH_TORCH, function is configured as GPIO functionality
71	FLASH_TRIGGER	Input	Although titled FLASH_TRIGGER, function is configured as GPIO functionality

[1] During BIOS execution the ISH_GPIO_0-3 signals are configured as outputs and change state to indicate BIOS progression. End users should take this into account in their design.

6 Configuration EEPROM

6.1 EEPROM usage overview

Intel® Joule™ expansion boards have the option to include an EEPROM device that holds an alternate configuration for the multipurpose pins.

If an EEPROM device is detected by the BIOS, the BIOS attempts to read an alternate configuration table from the EEPROM and reconfigure the Intel® Joule™ module GPIO pins to the description contained in the EEPROM before completing the boot sequence. This sequence is repeated at each cold-boot. If the EEPROM is not found, or if the configuration table contained within the EEPROM is viewed as not accurate or corrupted, the default configuration contained in BIOS is used.

When a pin mode is configured as GPIO, it is also defined as an output or input. When programmed as an input, a GPIO can serve as an interrupt or wake source.

Most GPIO-capable pins are configured as GPIO inputs during the assertion of all resets, and they remain inputs until configured otherwise. As outputs, the GPIOs can be individually cleared or set. They can be preprogrammed to either state when entering standby. External level shifters are necessary if different interface voltage levels are required.

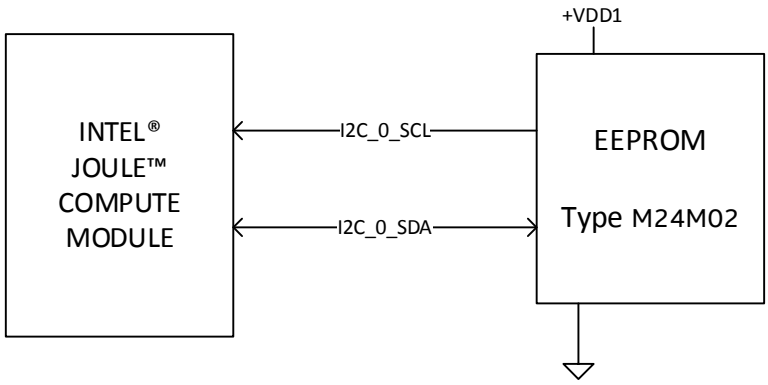
6.2 Multipurpose pin routing considerations

Route multipurpose lines as appropriate for any function they may serve, and ensure that later redefinition of interfaces—if the EEPROM configuration table is changed—does not cause interfaces to fall out of specification.

6.3 EEPROM address and type

The reference firmware is configured to look for a type M24M02 (or equivalent) EEPROM on I2C bus 0, address 0x50 through 0x53 and 0x58 through 0x5B.

Figure 6-1: EEPROM connection



7 I2C – Inter-Integrated Circuit Buses

7.1 I2C overview

Five I2C buses are available across the J6 and J7 board-to-board connectors:

J6 carries the signals for:

- I2C_0, which is used for the configuration EEPROM
- ISH_I2C_0 and ISH_I2C_1 buses mapped to I2C_5 and I2C_6

J7 carries the signals for the general purpose I2C_1 and I2C_2 buses.

By default, internal 2 kΩ pull-ups are enabled on the I2C lines. If additional pull-up strength is needed, an external pull-up can be added, if the I2C electrical specifications—provided in the Intel® Joule™ Module Datasheet—are not exceeded.

The I2C buses can operate in six modes:

- Standard mode (with data rates up to 100 kbps)
- Fast mode (with data rates up to 400 kbps)
- High-speed mode (with data rates up to 3.4 Mbps)
- The SoC is always I2C master. It does not support multi-master mode. The SoC supports clock stretching by slave devices.
- Both 7-bit and 10-bit addressing modes are supported.

Refer to the Intel® Joule™ Module Datasheet for I2C electrical specifications.

7.2 I2C routing

The I2C signals do not need to be routed as differential pairs, but it is recommended not to separate data and clock lines too much. It is not required to route the bus as a daisy chain, because the stub length is not a problem. The maximum trace length is limited by the load capacitance of the traces and attached bus devices. Keep traces short by using a star topology.

7.3 I2C pin mapping

Table 7-1: I2C buses

Signal	Module Connector/Pin	Pin Direction	Use
I2C_0_SCL	J6 pin 57	Input	I2C port 0 clock, used for configuration EEPROM
I2C_0_SDA	J6 pin 95	Input/Output	I2C port 0 data, used for configuration EEPROM
I2C_1_SCL	J7 pin 43	Input	I2C port 1 clock, general purpose
I2C_1_SDA	J7 pin 45	Input/Output	I2C port 1 data, general purpose
I2C_2_SCL	J7 pin 26	Input	I2C port 2 clock, general purpose
I2C_2_SDA	J7 pin 28	Input/Output	I2C port 2 data, general purpose
ISH_I2C_0_SCL	J6 pin 16	Input	I2C port 0 clock, mapped to I2C5
ISH_I2C_0_SDA	J6 pin 18	Input/Output	I2C port 0 data, mapped to I2C5
ISH_I2C_1_SCL	J6 pin 21	Input	I2C port 1 clock, mapped to I2C6
ISH_I2C_1_SDA	J6 pin 23	Input/Output	I2C port 1 data, mapped to I2C6

Note: Refer to the Intel® Joule™ Module Datasheet for additional electrical specifications.

8 UART Interfaces

The Intel® Joule™ module provides two serial UARTs for user modification: UART0 and UART_1.

Refer to the Intel® Joule™ Module Datasheet for additional electrical specifications.

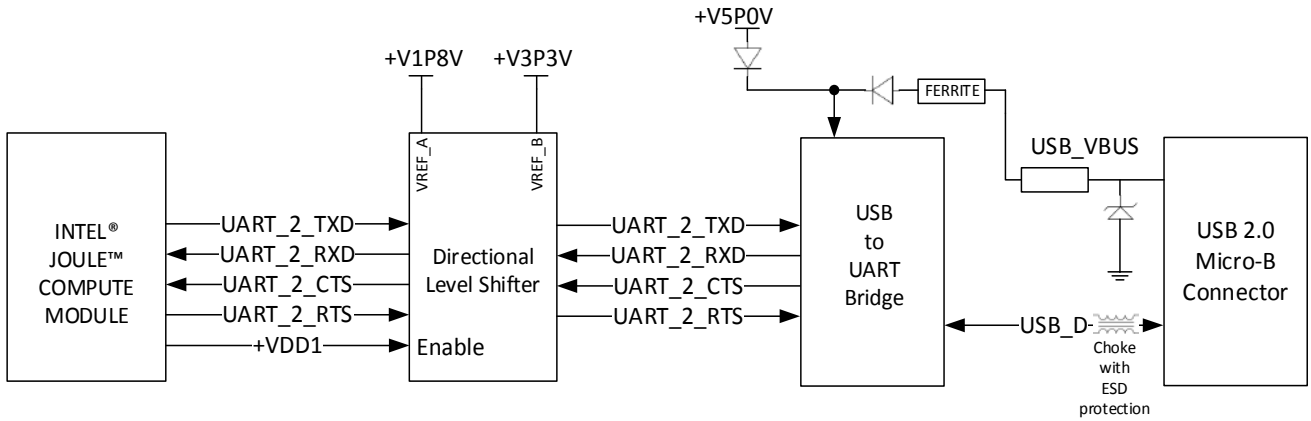
8.1 Debug console port

UART2 is configured in BIOS as the debug UART, allowing BIOS output and console access from the Linux* operating system.

Figure 8-1 shows a typical design with a USB-to-UART bridge and a level shifter for translating the 1.8 V module signals to the 3.3 V levels required by the bridge.

The USB-to-UART bridge is powered either from a 5 V supply (see Figure 4-1), or from the USB device connector; the simplest method for this is a dual source, each with a protection diode.

Figure 8-1: Debug UART



Note: The debug UART uses four pins on J6; these can be routed to a debug connector of choice.

Table 8-1: Debug UART pins

Signal	Module Connector/Pin	Pin Direction	Use
DEBUG_UART2_TXD	J6 pin 78	Input	UART 2 TXD – configured in BIOS as debug output port
DEBUG_UART2_RXD	J6 pin 80	Output	UART 2 RXD – configured in BIOS as debug output port
DEBUG_UART2_CTS	J6 pin 74	Output	UART 2 CTS – configured in BIOS as debug output port
DEBUG_UART2_RTS	J6 pin 76	Input	UART 2 RTS – configured in BIOS as debug output port

8.1.1 UART to USB bridge power

When the module is powered off, it must be isolated from a powered USB-to-UART bridge to prevent current leaking through the UART lines. This can be done by disabling the level shifter through the +VDD1 rail.

To satisfy the pin strap requirements in Table 4-4, the level shifter needs to be directional to prevent the bridge from pulling the TX line high.

If a 1.8 V-compatible USB-to-UART bridge is used, the level shifter can be replaced with a switch enabled by the +VDD1 rail.

The USB differential data lines need a common-mode choke with built-in ESD diodes.

For +VBUS, add ESD protection diodes, a PTC fuse, and a ferrite for EMI filtering.

9 Audio Interface

9.1 Audio codec

The I2S_1 port on J6 is available for audio playback and recording, for example through an audio codec. It can operate in I2S and PCM master or slave modes. The signals are shown in Table 9-1.

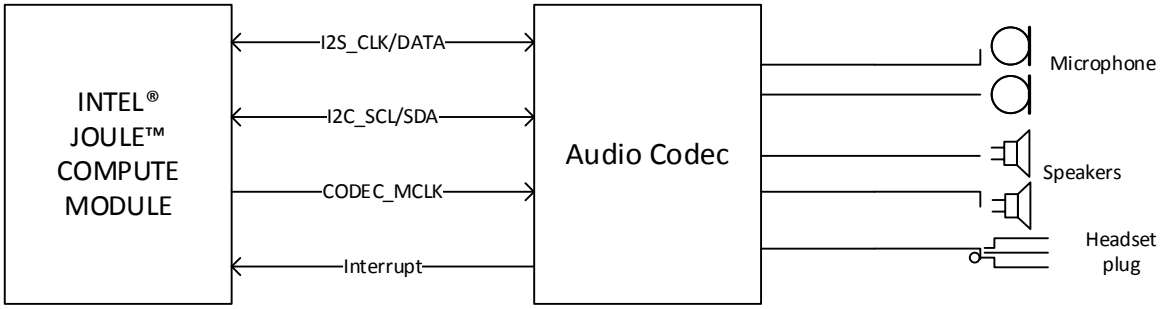
Table 9-1: I2S signals

Signal	Module Connector/Pin	Pin Direction	Use
I2S_1_CLK	J6 pin 39	Input/Output	I2S bit clock, supplied by the module in master mode and serves as an input in slave mode
I2S_1_FS	J6 pin 45	Input/Output	I2S frame sync, supplied by the module in master mode and serves as an input in slave mode
I2S_1_RXD	J6 pin 47	Output	I2S receive data
I2S_1_TXD	J6 pin 49	Input	I2S transmit data

In addition to the audio data over the I2S lines, the Intel® Joule™ module can provide the clock signal for the audio codec over CODEC_MCLK (connector J6 pin 43). The control interface to the audio codec is connected through the I2C or SPI and a possible interrupt line for headset detection from the codec to the module through a standard interrupt capable GPIO (see Figure 9-1).

Refer to the Intel® Joule™ Module Datasheet for additional electrical specifications.

Figure 9-1: Audio codec connection



9.2 Digital microphones

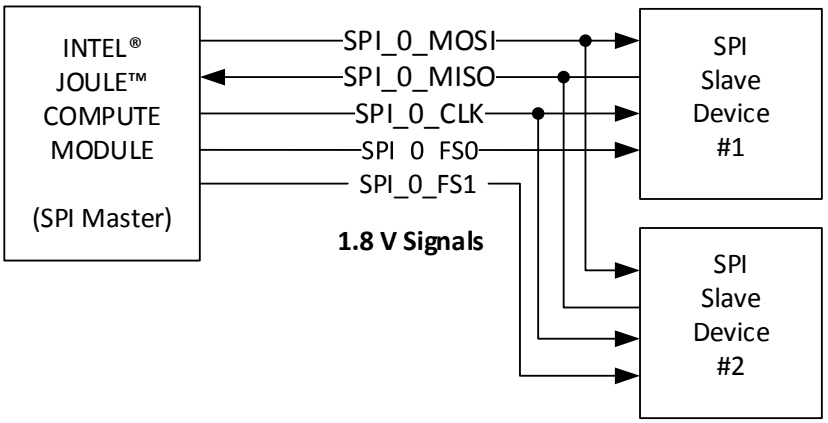
Two digital microphones can be connected to the clock and data signals AVS_M_CLK_A1/AVS_M_CLK_B1 and AVS_M_DATA_1, on connector J7 (pins 52/62 and 66). For a two microphone configuration, using a separate clock signal allows a single microphone to run if a lower power state is needed. Use of the second clock signal is not required.

10 SPI – Serial Peripheral Interface

A 25-MHz SPI bus (SPI_1) is available on the J6 connector with three slave selects and another 25-MHz SPI bus (SPI_0) with two slave selects on the J7 connector. The bus speed is 25 MHz in master mode and 16.67 MHz in slave mode.

In a single-frame transfer, the SoC supports all four possible combinations for the serial clock phase and polarity. In multiple frame transfer, the Intel® Joule™ module supports only a clock phase setting of 1.

Figure 10-1: SPI bus usage example



Note: The SPI interfaces operate 1.8 VDC levels.

Table 10-1: SPI bus usage pin assignments

Signal	Module Connector/Pin	Pin Direction	Use
SPI_0_CLK	J7 pin 59	Input	SPI 0 clock
SPI_0_MOSI	J7 pin 57	Input	SPI 0 master out/slave in
SPI_0_MISO	J7 pin 59	Output	SPI 0 master in/slave out
SPI_0_FS0	J7 pin 77	Input	SPI 0 slave select 0
SPI_0_FS1	J7 pin 79	Input	SPI 0 slave select 1
SPI_0_FS2	J7 pin 53	Input	SPI 0 slave select 2
SPI_1_CLK	J6 pin 53	Input	SPI 1 clock
SPI_1_MOSI	J6 pin 51	Input	SPI 1 master out/slave in
SPI_1_MISO	J6 pin 63	Output	SPI 1 master in/slave out
SPI_1_FS0	J6 pin 55	Input	SPI 1 slave select 0
SPI_1_FS2	J6 pin 14	Input	SPI 1 slave select 1

Note: Refer to the Intel® Joule™ Module Datasheet for additional electrical specifications.

11 USB – Universal Serial Bus

11.1 USB overview

The Intel® Joule™ module provides two USB2 and one USB3 port through the board-to-board connectors:

- USB2 port 0: Used primarily in device mode, also for updating the firmware through the DnX protocol, port 0 also provides signaling of host mode through the USB ID pin.
- USB2 port 1: Used with USB3 port 1 as a backwards compatible USB host port for (keyboard, mouse, HUB) accessories
- USB3 port 0 and 1
- Type-C

The main uses for USBs are to connect hubs, keyboards, and mice when the module is acting as the USB host, or allowing the module to act as a device when communicating with a host.

It is necessary to operate in USB device mode to perform firmware updates.

11.2 USB2 device connectivity

The USB2 port 0 is used as the default port to present the module as a USB device to host systems. This mode is also used for updating the module firmware by reading the code from a connected storage device.

The signals for the USB2 port 0 are on connector J6 (pins 6 and 8 for USB2_0_DP and USB2_0_DN). The USB device connector is a micro connector. USB2 requires a common mode choke with ESD protection on the USB2_0_DP and USB2_0_DN signals. Add ESD protection diodes, and EMI dampening ferrite or a specially designed EMI filter capacitor to USB +VBUS. It is also good design practice to put a PTC fuse in series with +VBUS.

Attach the connector +VBUS pin to the +VBUS signal on the module to wake the module when the USB is inserted. The +VBUS also needs to be connected for the DnX protocol to work. The USB2_ID_PMIC pin can be left unconnected if the USB2 port 0 is not going to be used in host mode.

Figure 11-1: USB2 in device mode

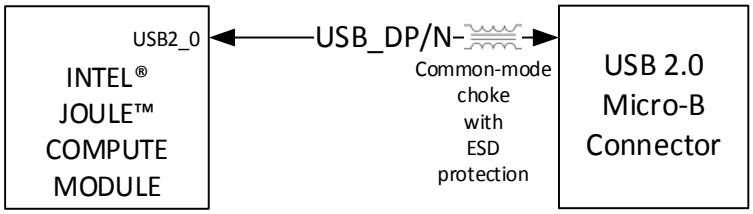


Table 11-1: USB2 port 0 signals

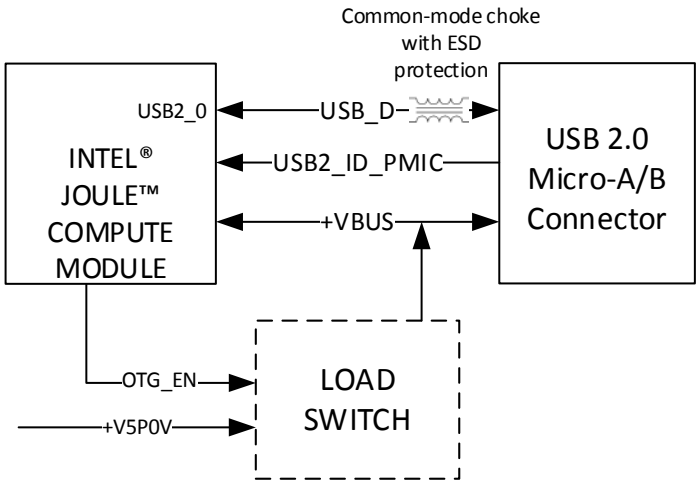
Signal	Module Connector/Pin	Pin Direction	Use
USB2_0_DP	J6 pin 6	Bidirectional	USB 2.0 port 0 data positive
USB2_0_DN	J6 pin 8	Bidirectional	USB 2.0 port 0 data negative
USB2_ID_PMIC	J6 pin 20	Output	Low resistance indicates a USB OTG connection.
+VBUS	J6 pin 99	Output	USB +VBUS power, also wake source for the module

Note: For +VBUS, less than 1 kΩ measured by the module indicates a USB OTG connection. Do not add pull-ups. Leave floating if not connected.

11.2.1 USB2 OTG host connectivity

If a simple design is the goal, USB2 port 0 can serve as a USB host. This allows combining host and device mode to be delivered through just one connector (typically a micro-A or -B connector). The USB2 interface is able to transmit data at 480Mbps. For higher speeds a USB3 is necessary.

Figure 11-2: USB2 OTG setup



Request for host mode is signaled through the ID pin on the USB connector and routed to the USB2_ID_PMIC signal on the module. To power devices in USB host mode, the OTG_EN signal enables +VBUS on the USB connector through a load switch with set 1 A current limit. The +VBUS source can be a dedicated boost regulator fed by +VSYS, or if +VSYS has a minimum of 4.75 V, +VSYS can be used as a +VBUS source. It is good design practice to add an ESD protection diode, a PTC fuse, and EMI filtering to +VBUS, and to add common-mode chokes with built-in ESD diodes to USB data signals. ENDED HERE, add the notes in comments for easier review.

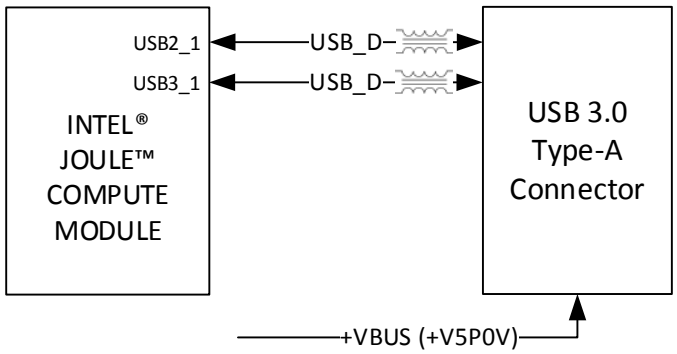
Table 11-2: USB2 OTG setup pin assignments

Signal	Module Connector/Pin	Pin Direction	Use
USB2_1_DN	J7 pin 63	Bidirectional	USB 2.0 port 1 data negative
USB2_1_DP	J7 pin 65	Bidirectional	USB 2.0 port 1 data positive

11.3 USB3 OTG (host) Connectivity

If higher transfer rates are needed, use the USB host functionality through the USB3 port 1. A Type-A receptacle (female USB connector) is, in this case, used to carry the signals from USB3 port 1 and USB2 port 1. Because this setup is not supporting firmware updates, a separate USB2 device connector (see section 11.2) is needed.

Figure 11-3: USB3 OTG setup

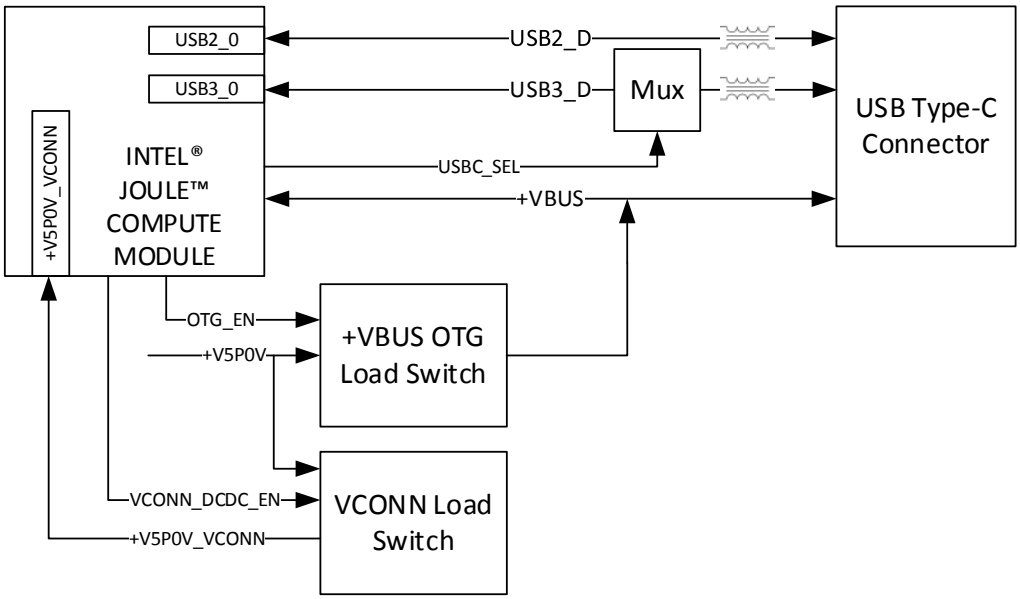


The USB3 OTG connector can provide +VBUS to attached devices by generating a 5 V supply on the Intel® Joule™ expansion board from +VSYS or a 5 V supply. Place a load switch, enabled by +VDD3, between the 5 V supply and USB +VBUS, with a set 1 A current limit. If +VSYS is fixed at 5 V, a boost regulator is not needed and a load switch is sufficient. It is good design practice to add ESD protection diodes, a PTC fuse, and an EMI filter to +VBUS, and to add common-mode chokes that have built-in ESD diodes to USB data signals. **Error! Reference source not found.** shows the signals that are necessary for a USB3 OTG port.

11.3.1 Type-C connector

The module supports Type-C connector through USB2 port 0 and USB3 port 0. Figure 11-4 shows a block diagram of the needed components.

Figure 11-4: Type-C block diagram



When configured as a device, +VBUS is provided from the host side. But in host mode, two load switches can provide power to +VBUS and VCONN, and a mux is necessary on the USB3 port 0 signal lines.

Table 11-3: USB 3.0 Type-C signals

Signal	Module Connector/Pin	Pin Direction	Use
USB3_0_TX_DN	J7 pin 6	Input	USB 3.0 port 0 transmit negative
USB3_0_TX_DP	J7 pin 4	Input	USB 3.0 port 0 transmit positive
USB3_0_RX_DN	J7 pin 46	Output	USB 3.0 port 0 receive negative
USB3_0_RX_DP	J7 pin 44	Output	USB 3.0 port 0 receive positive
USBC_SEL	J7 pin 18	Input	Mux control
OTG_EN	J6 pin 69	Input	OTG power enable
VCONN_DCDC_EN	J6 pin 97	Input	VCONN power enable
USB_TYPC_CC1	J6 pin 59	Input	Type-C configuration channel
USB_TYPC_CC2	J6 pin 61	Output	Type-C configuration channel
USB3_1_TX_DP	J7 pin 87	Input	USB 3.0 port 1 data transmit positive
USB3_1_TX_DN	J7 pin 89	Input	USB 3.0 port 1 data transmit negative
USB3_1_RX_DP	J7 pin 95	Output	USB 3.0 port 1 data receive positive
USB3_1_RX_DN	J7 pin 97	Output	USB 3.0 port 1 data receive negative

12 SD Card Interface

The SD card interface supports SD memory at a maximum of 208MHz (SDR104 mode). An external level shifter is required. The level shifter needs to support dual voltage operation in case UHS-I or faster speeds are required. Signals going to an SD card connector should have ESD protection and EMI filtering.

Figure 12-1: Micro SD card connection

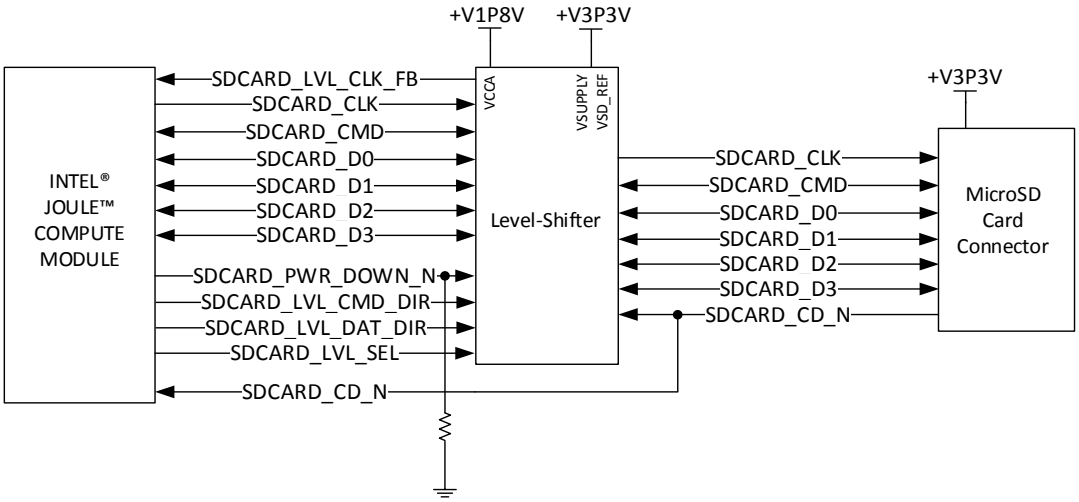


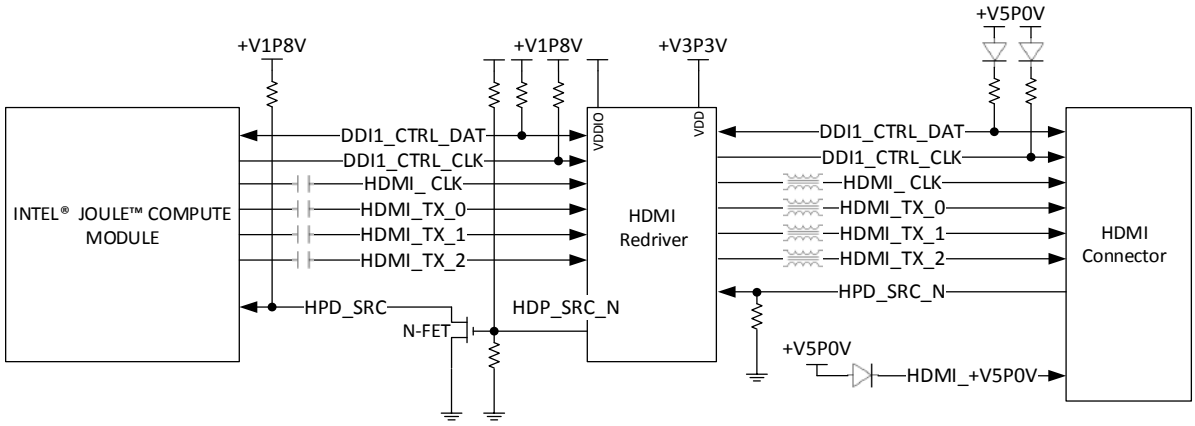
Table 12-1: SD card signals

Signal	Module Connector/Pin	Pin Direction	Use
SDCARD_LVL_CLK_FB	J2 pin 77	Output	SD card clock feedback for aligning the SDIO data from the level shifter on the expansion board through the controller, there is a loopback through the SD card level shifter that drives this pin.
SDCARD_CD_N	J2 pin 79	Output	SD card detect, active low when a card is present, pulled high with internal pull-up when a card is not present
SDCARD_PWR_DOWN_N	J2 pin 91	Input	SD card power down indicates to SDIO device to power down.
SDCARD_LVL_SEL	J2 pin 88	Input	SD card level select performs the 1.8 V to 3.0 V negotiation.
SDCARD_LVL_CMD_DIR	J2 pin 90	Input	SD card command direction indicates whether a host is transmitting or receiving over the command pin.
SDCARD_LVL_DAT_DIR	J2 pin 67	Input	SD card data direction indicates whether a host is transmitting or receiving over the data.
SDCARD_CLK	J2 pin 75	Input	SD card clock
SDCARD_D0	J2 pin 81	Bidirectional	SD card data 0, by default, during power up or reset, only data 0 is used for data transfer.
SDCARD_D1	J2 pin 83	Bidirectional	SD card data 1
SDCARD_D2	J2 pin 85	Bidirectional	SD card data 2
SDCARD_D3	J2 pin 87	Bidirectional	SD card data 3
SDCARD_CMD	J2 pin 89	Bidirectional	SD card command is used for card initialization and transfer of commands.

13 HDMI* - High Definition Multimedia Interface

The HDMI 1.4b compliant port is located on connector J6. A The HDMI DDC signals require a level shifter, which can be either integrated into an HDMI redriver or—if the redriver is omitted—added as a separate component. Figure 13-1 shows an overview of how to add an HDMI connector to an Intel® Joule™ expansion board. HDMI uses three signal lanes and one clock lane for the audio/video content, and two signals at 5V for the DDC protocol. Table 4-12 lists Intel® Joule™ module HDMI signals.

Figure 13-1: HDMI display output



The HDMI signals are located on module connector J6. When routing the signals, the PCB layout guidelines in section 14 must be followed. It is also recommended to add series capacitors to the audio/video signal lines. Common-mode chokes with built-in ESD protection are recommended on clock and data lines between redriver and connector. Add ESD protection diode to hot-plug detect signal coming from HDMI connector.

HDMI hot-plug detect signal needs inverting and level shifting with N-FET transistor. HDMI I2C clock and data signals need to be pulled high to expansion board 5V supply after redriver and 1.8 V on module side. Diodes are added for reverse-current protection on connector side pull-ups and HDMI 5 V supply.

Table 13-1: HDMI signals

Signal	Module Connector/Pin	Pin Direction	Use
HDMI_CLK_DP	J6 pin 44	Input	HDMI clock positive
HDMI_CLK_DN	J6 pin 46	Input	HDMI clock negative
HDMI_TX_0_DP	J6 pin 64	Input	HDMI data lane 0 positive
HDMI_TX_0_DN	J6 pin 62	Input	HDMI data lane 0 negative
HDMI_TX_1_DP	J6 pin 56	Input	HDMI data lane 1 positive
HDMI_TX_1_DN	J6 pin 58	Input	HDMI data lane 1 negative
HDMI_TX_2_DP	J6 pin 52	Input	HDMI data lane 2 positive
HDMI_TX_2_DN	J6 pin 50	Input	HDMI data lane 2 negative
HPD_SRC	J6 pin 63	Output	HDMI cable hot plug detect. Instantiates a start-up communication between source and sink HDMI devices. Connected to GPIO_200.
DDI1_CTRL_DAT	J6 pin 70	Bidirectional	HDMI I2C data
DDI1_CTRL_CLK	J6 pin 68	Input	HDMI I2C clock

14 Trace Layout Guidelines

This section details key layout information for single-ended and differential traces.

14.1 Single-ended trace information

If the Minimum Trace column only has one spacing-to-width ratio, both signals have the same space requirements.

The Typical Signal Loss column presents the specific loss of signal for each interface at the 500-MHz level.

The Kb column describes the coefficient of maximum near-end crosstalk or backwards crosstalk couple factor. Kb refers to a dimensionless ratio representing the voltages between the victim and aggressor traces.

Table 14-1: Definitions for single-ended trace routing

I/O Interfaces	Zo (Ohm) ±12%	Max. Routing Length (mils)	Minimum Trace spacing-to-width ratio	Kb	Typical Signal Loss at Max Routing Length (dB at 500 MHz)	Topology	Note
SD Card	42-47	3900	s:w=1:1	6.5%	0.94	P2P	1, 2
Crystal Oscillator	42-47	900	s:w=5:1	0.1%	0.24		6
GPIO	42-47	7900	s:w=1:1	6.5%	1.87	P2P	
CLK_19P2M, CODEC_MCLK	42-47	6900	s:w=2:1	2.4%	1.63	P2P	
I2C	42-47	Less than 400 pF total load	s:w=1:1	6.5%	N/A		7
I2S	42-47	5900	s:w=1:1	6.5%	1.4	Multi-load P2P	3, 4
HSUART	42-47	6600	s:w=1:1	6.5%	1.59	P2P	
SPI	42-47	6600	clk: s:w=2:1 data per frame: s:w=1:1	clk: 2.4% data: 6.5%	1.59	P2P	5

Notes:

1. Level shifter is needed, and routing between level shifter and SD card connector should be as short as possible, with a maximum of 500 mils. Refer to level shifter vendor's application note.
2. The maximum mismatch of data to clock is 500 mils.
3. The maximum frequency is 4.8 MHz if multi-load is implemented.
4. The maximum mismatch of clock to data per frame is 1000 mils.
5. The maximum mismatch of clock to data per frame is 600 mils.
6. The maximum mismatch is 50 mils.
7. The maximum mismatch of data to clock is 2000 mils.

14.2 Differential trace information

Differential signal pairs need to be routed in parallel with a specific, constant distance. Differential pair signals need to be routed symmetrically. It is not permitted to place any components or vias between the differential pairs, even if the signals are routed symmetrically. Any vias needed on the signal path itself need to be placed in pairs and symmetrically. All traces of a signal and all signals as a whole must be length matched to eliminate skew. It is strongly recommended to route the clock and data lanes on the same layer, between ground and power planes.

Table 14-2: Definitions for differential trace routing

I/O	Zo (Ohm) ± 12%	Max. Routing Length (mils)	Min. Ratio Intra-Pair Space	Min. Ratio Inter-Pair Space	Note
HDMI	80-85	4200	1:1	4:1	
USB 3.0	80-85	5900	1:1	4:1	1
USB 2.0 OTG	80-85	9900	1:1	4:1	1

Note: Spacing to adjacent interfaces to follow Min. Ratio Inter-Pair Spacing.

USB maximum length is for OTG detection topology without FPC.

Appendix A Minimal Board Design

Intel® Joule™ Expansion Board Minimum Requirements:

1. Method for connecting Intel® Joule™ module to expansion board:

   The module must be securely mounted to an expansion board in a method that maintains full engagement of the board-to-board interface connectors. See section 2.4 for more details.

2. Method to provide +VSYS power to the module:
   - The module requires a +VSYS source routed through 12 pins, 6 on each board-to-board connector, which must all be connected in common to balance the current path.
   - Connect +VSYS to +VDC_IN or USB +VBUS to +VBUS to trigger a module boot.
   - Voltage minimum: 3.6 V, typical: 4.2 V, maximum: 5.25 V, with a current capability of 4 A

3. Required strapping of module pins:
   - The module pin strappings in Table 4-4 must be implemented for boot during the rising edge of PMIC_PWRGOOD (J6, pin 33).
   - Module strap pins can be left unconnected if not used.

Expansion Board Recommendations:

1. Power button (recommended, preferred on all designs):

   Connect an active, low-power button to J6 pin 9 to trigger a reset or to power cycle the board.

2. DnX button (high importance, include if BIOS flashing support is needed. Add a test point for access if the DnX button is not included.):

   Connect an active, high (+VDD1) signal to J6, pin 78, to initiate a download and execute a routine that updates the BIOS through the USB 2.0, port 0. This DnX button signal is the only way to initiate the download and execute the update process.

3. USB 2.0 device connector routed to port 0 to enable DnX BIOS updates

4. UART debugging (critical, preferred on all designs):

   Include a method to access UART port 2 on the module during boot, to collect debug information. This is the only way to access debug messages generated during the power on and boot sequences.

5. External EEPROM for general purpose pin configuration data (high importance, use unless GPIOs are configured in BIOS):

   An external EEPROM (recommend ST Microelectronics M24M02-DR* or equivalent) connected to I2C port 0 holds a specific configuration of the multipurpose pins. During boot, if the BIOS does not find an EEPROM device attached to I2C port 0, the module loads the default configuration that is stored in BIOS.

6. USB 3.0 host connector for general purpose device use; recommend implementing USB host support.

7. Real-Time Clock (RTC) backup power source (optional, implement if RTC support needed):

   A backup power source is required for the RTC to operate robustly; this prevents RTC data losses during unexpected power loss. The most common solution is a non-rechargeable, coin-cell battery connected to +VRTC at module connector J6, pin 11. +VRTC voltage range is from 2.05 V to 3.3 V.

8. HDMI display connector with proper level conditioning appropriate for module