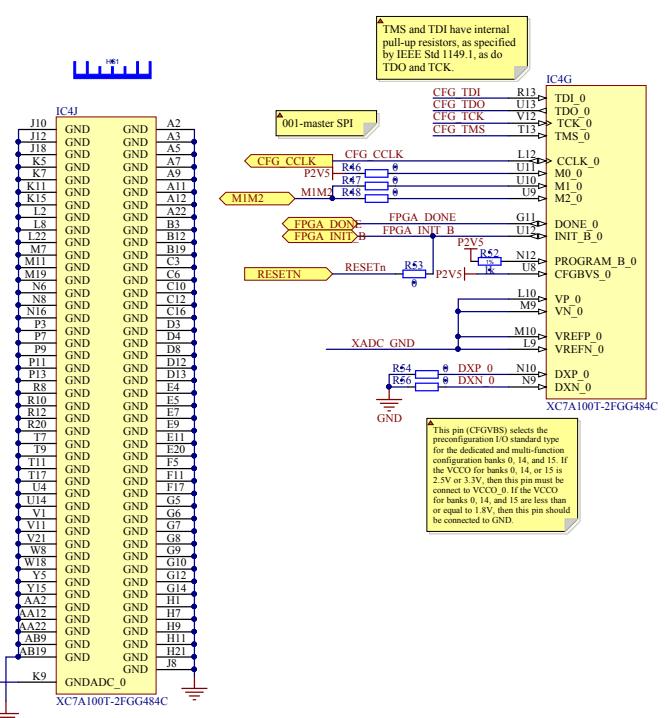


H61

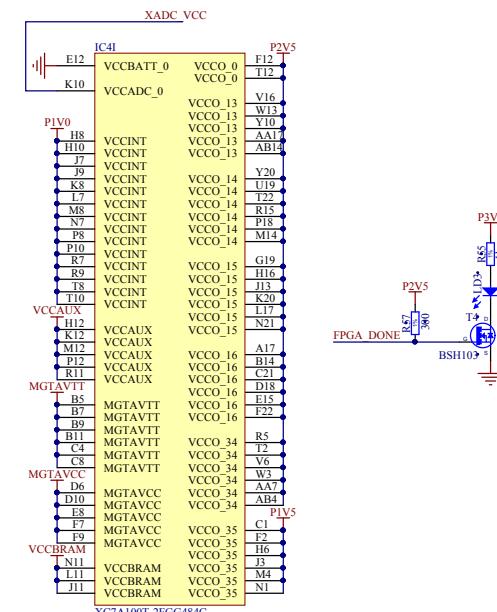


▲ TMS and TDI have internal pull-up resistors, as specified by IEEE Std 1149.1, as do TDO and TCK.

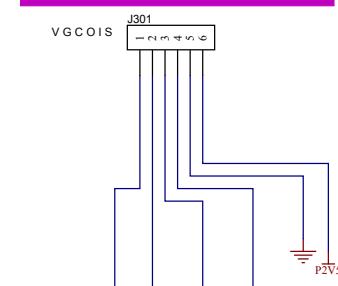
The diagram illustrates the timing sequence for programming and operating a Virtex-5 FPGA. It shows the following signals and their timing:

- Configuration Phase:**
 - CFG TDI: 0.0 - 1.0
 - CFG TDO: 0.0 - 1.0
 - CFG TCK: 0.0 - 1.0
 - CFG TMS: 0.0 - 1.0
- Clock Phase:**
 - L12: 1.0 - 2.0
 - L11: 2.0 - 3.0
 - L10: 3.0 - 4.0
 - L9: 4.0 - 5.0
 - L8: 5.0 - 6.0
 - L7: 6.0 - 7.0
 - L6: 7.0 - 8.0
 - L5: 8.0 - 9.0
 - L4: 9.0 - 10.0
 - L3: 10.0 - 11.0
 - L2: 11.0 - 12.0
 - L1: 12.0 - 13.0
 - L0: 13.0 - 14.0
- Memory Access Phase:**
 - CCLK_L: 1.0 - 14.0
 - M0_0: 1.0 - 14.0
 - M1_0: 1.0 - 14.0
 - M2_0: 1.0 - 14.0
 - DONE_0: 1.0 - 14.0
 - INIT_B_0: 1.0 - 14.0
 - PROGRAM_B: 1.0 - 14.0
 - CFGVBUS_0: 1.0 - 14.0
 - VP_0: 1.0 - 14.0
 - VM_0: 1.0 - 14.0
 - VREFP_0: 1.0 - 14.0
 - VREFN_0: 1.0 - 14.0
 - ND: 1.0 - 14.0
 - M10: 1.0 - 14.0
 - M11: 1.0 - 14.0
 - M12: 1.0 - 14.0
 - M13: 1.0 - 14.0
 - M14: 1.0 - 14.0
 - M15: 1.0 - 14.0
 - M16: 1.0 - 14.0
 - M17: 1.0 - 14.0
 - M18: 1.0 - 14.0
 - M19: 1.0 - 14.0
 - M20: 1.0 - 14.0
 - M21: 1.0 - 14.0
 - M22: 1.0 - 14.0
 - M23: 1.0 - 14.0
 - M24: 1.0 - 14.0
 - M25: 1.0 - 14.0
 - M26: 1.0 - 14.0
 - M27: 1.0 - 14.0
 - M28: 1.0 - 14.0
 - M29: 1.0 - 14.0
 - M30: 1.0 - 14.0
 - M31: 1.0 - 14.0
 - DXP_0: 1.0 - 14.0
 - DXN_0: 1.0 - 14.0
 - N10: 1.0 - 14.0
 - N11: 1.0 - 14.0
 - N12: 1.0 - 14.0
 - N13: 1.0 - 14.0
 - N14: 1.0 - 14.0
 - N15: 1.0 - 14.0
 - N16: 1.0 - 14.0
 - N17: 1.0 - 14.0
 - N18: 1.0 - 14.0
 - N19: 1.0 - 14.0
 - N20: 1.0 - 14.0
 - N21: 1.0 - 14.0
 - N22: 1.0 - 14.0
 - N23: 1.0 - 14.0
 - N24: 1.0 - 14.0
 - N25: 1.0 - 14.0
 - N26: 1.0 - 14.0
 - N27: 1.0 - 14.0
 - N28: 1.0 - 14.0
 - N29: 1.0 - 14.0
 - N30: 1.0 - 14.0
- Address and Data Phase:**
 - 64: 1.0 - 14.0
 - 65: 1.0 - 14.0
 - 66: 1.0 - 14.0
 - 67: 1.0 - 14.0

This pin (CFGVBS) selects the preconfiguration I/O standard type for the dedicated and multi-function configuration banks 0, 14, and 15. If the VCCO for banks 0, 14, or 15 is 2.5V or 3.3V, then this pin must be connected to VCCCO. If the VCCO for banks 0, 14, and 15 are less than or equal to 1.8V, then this pin should be connected to GND.



J301 = used to install bit file with Xilinx USB JTAG
You need a special xilinx Jtag Programmer by loading your _prog.bit
made up with Xilinx ISE tools

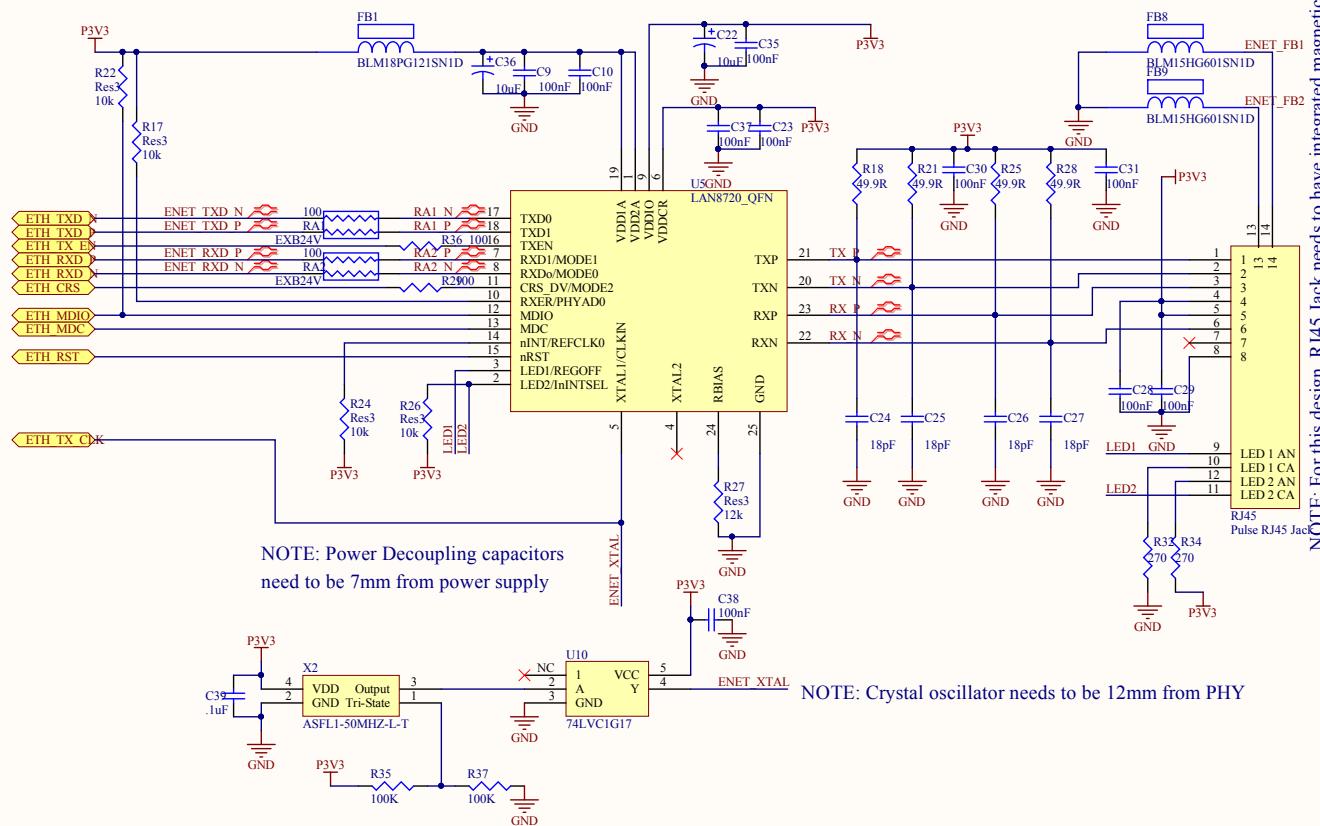


The figure shows the detailed connection between the VCCBRAM, P1V8, and P1V5 blocks. The connections are as follows:

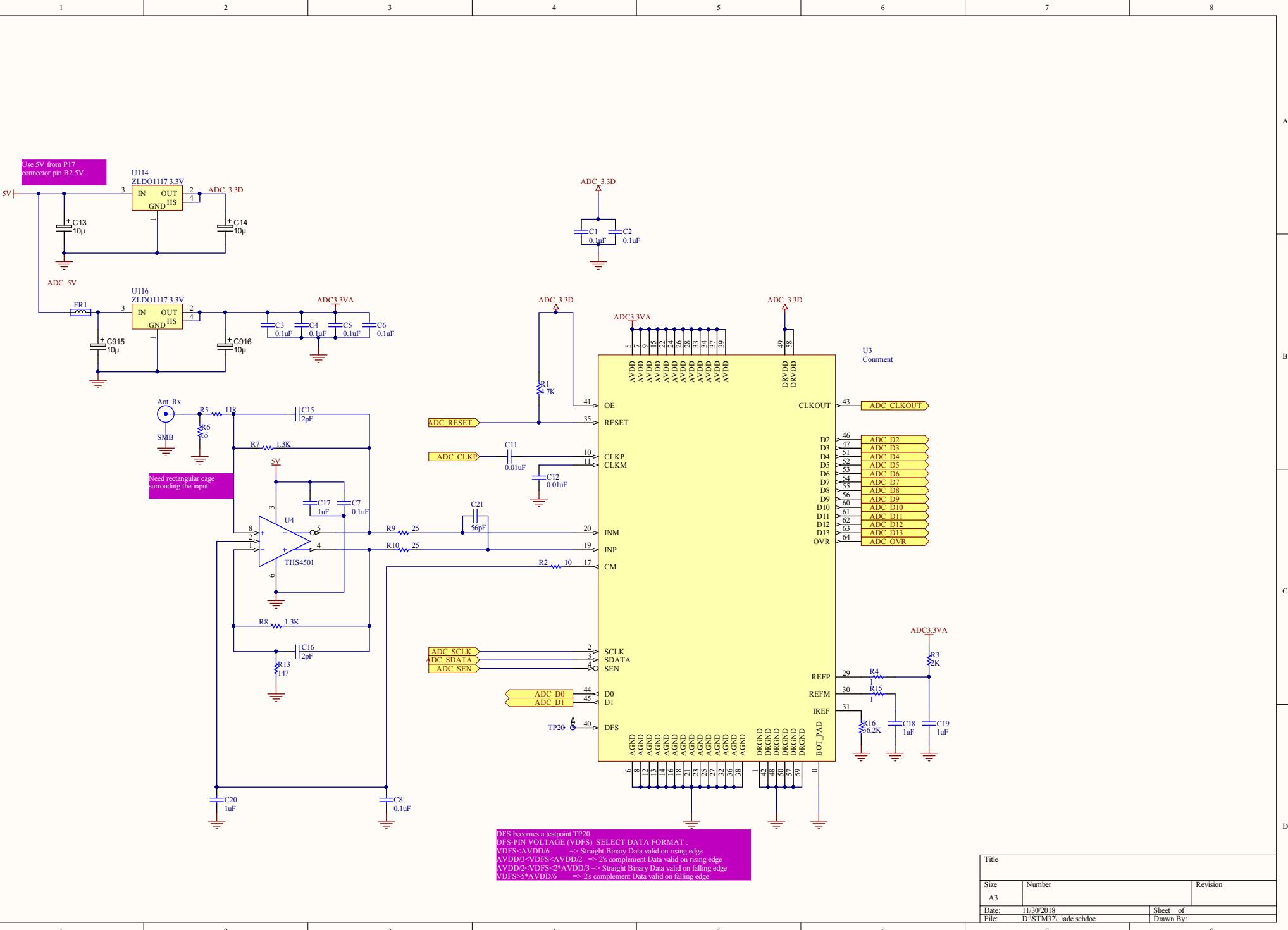
- VCCBRAM:** Connected to ground through a 100nF capacitor C26.
- P1V8:** Connected to ground through a 120R resistor at 400MHz and a 100nF capacitor C50.
- P1V5:** Connected to ground through a 120R resistor at 400MHz and a 100nF capacitor C51.
- Shared Ground Path:** A central ground rail connects the three blocks. It is connected to ground through a 100nF capacitor C270 at the VCCBRAM end and a 100nF capacitor C280 at the P1V5 end. Between P1V8 and P1V5, it is connected to ground through a 4.7nF capacitor C240 and a 2.2nF capacitor C240.
- Power Path:** The P1V8 power rail is connected to the VCCBRAM power rail through a 4.7nF capacitor C240. The P1V5 power rail is connected to the VCCBRAM power rail through a 4.7nF capacitor C240.
- Control Path:** The P1V8 control rail is connected to the VCCBRAM control rail through a 4.7nF capacitor C240. The P1V5 control rail is connected to the VCCBRAM control rail through a 4.7nF capacitor C240.

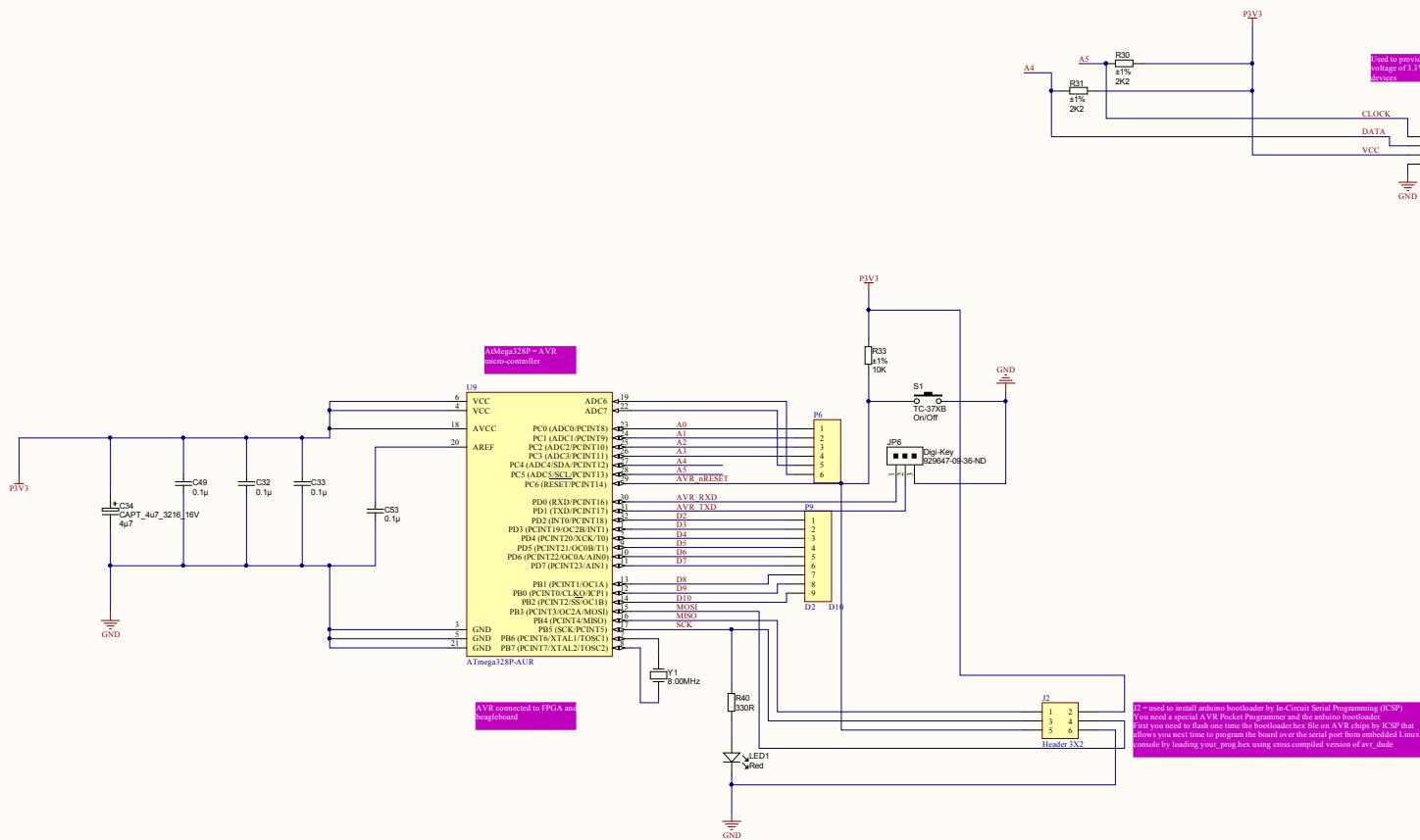
The diagram illustrates the connection between the TMS320C6455 and the C6456 memory chip. The TMS320C6455 is shown at the top, with its pins labeled: GND, V_{DD}, A₁₅, A₁₄, A₁₃, A₁₂, A₁₁, A₁₀, A₉, A₈, A₇, A₆, A₅, A₄, A₃, A₂, A₁, A₀, and P2VS. The C6456 memory chip is shown below, with its pins labeled: GND, V_{DD}, CSB, A₁₅, A₁₄, A₁₃, A₁₂, A₁₁, A₁₀, A₉, A₈, A₇, A₆, A₅, A₄, A₃, A₂, A₁, A₀, and P2VS. A blue horizontal line connects the P2VS pin of the TMS320C6455 to the P2VS pin of the C6456 chip. A red ground symbol is connected to the GND pins of both chips.

Ethernet Physical Layer (SMSC LAN8720)



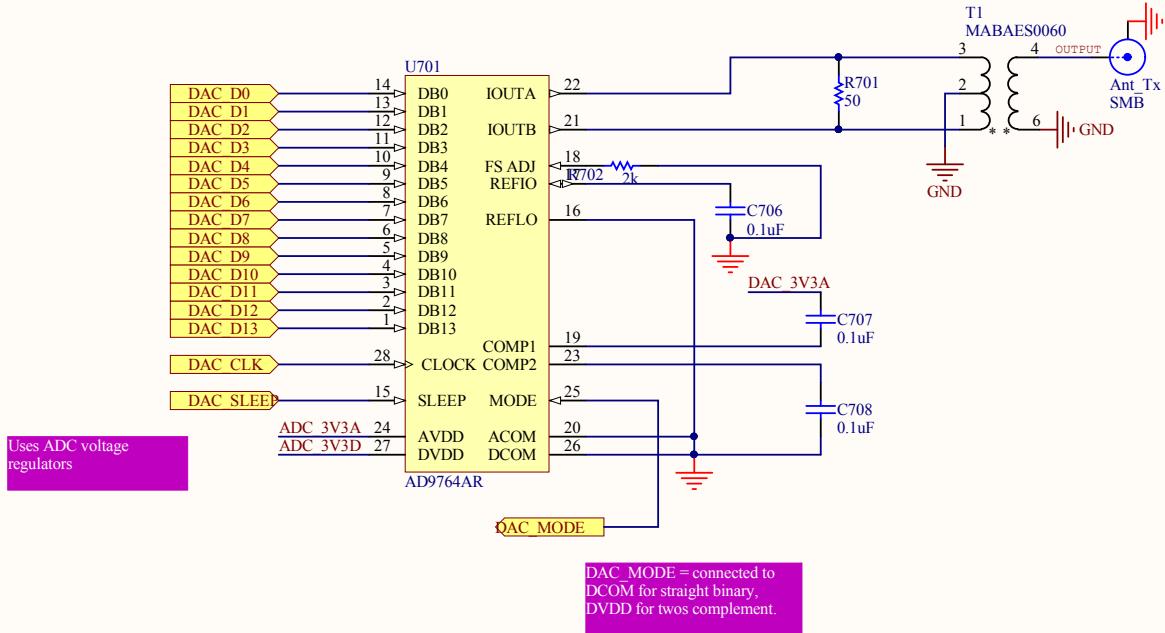
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