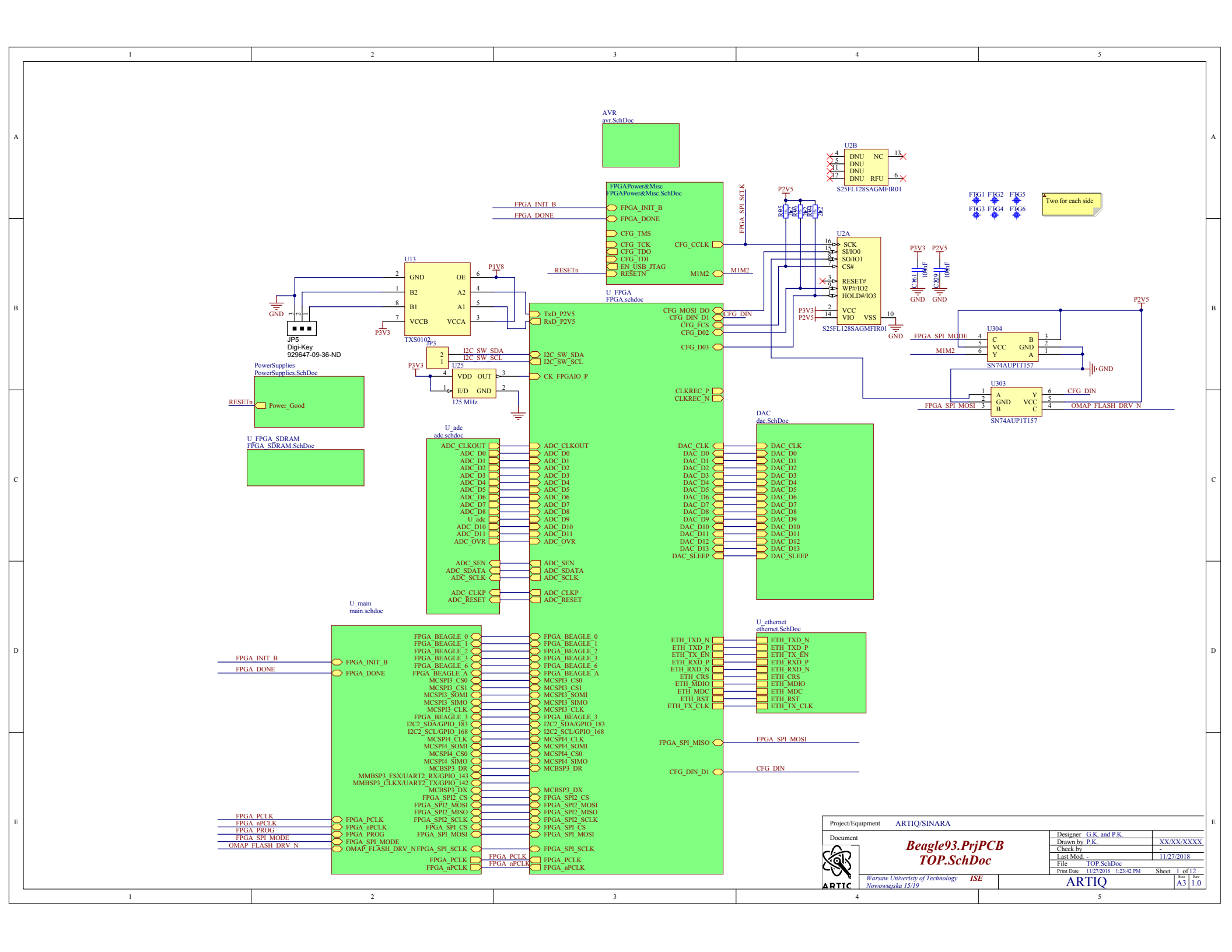
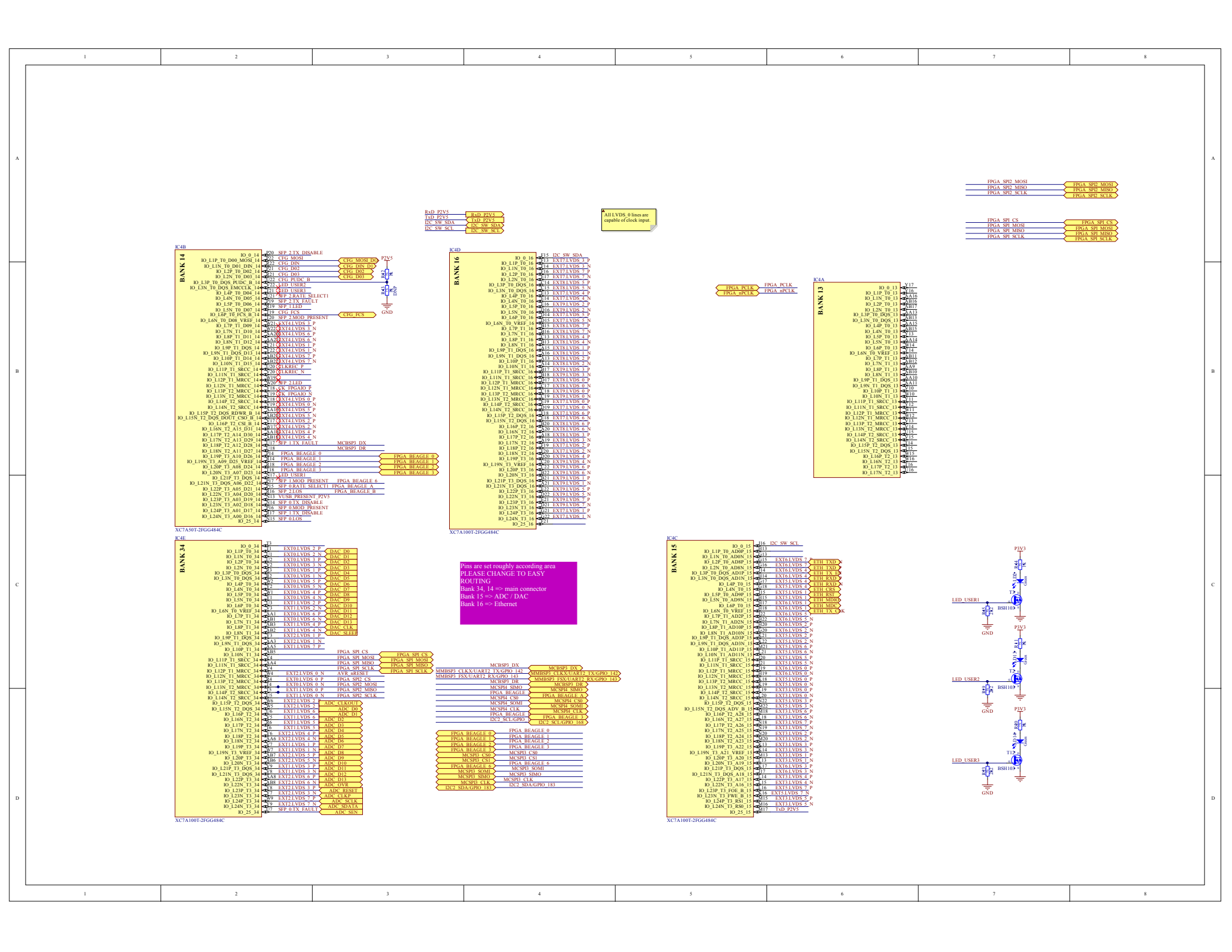

AVR
avr.SchDoc
FPGAPower&Misc
FPGAPower&Misc.SchDoc
U_FPGA
FPGA.schdoc
U2B
S25FL128SAGMFIR01
U2A
S25FL128SAGMFIR01
U13
TXS0102
JP5
Digi-Key
929647-09-36-ND
JP3
U25
125 MHz
PowerSupplies
PowerSupplies.SchDoc
U_FPGA_SDRAM
FPGA_SDRAM.SchDoc
U_adc
adc.schdoc
U_main
main.schdoc
DAC
dac.SchDoc
U_ethernet
ethernet.SchDoc
U304
SN74AUP1T157
U303
SN74AUP1T157
Two for each side
Project/Equipment ARTIQ/SINARA
Document Beagle93.PrjPCB
TOP.SchDoc
Designer G.K. and P.K.
Drawn by P.K.
Check by
Last Mod. -
File TOP.SchDoc
Print Date 11/27/2018 1:23:42 PM
Sheet 1 of 12
Warsaw Univeristy of Technology
Nowowiejska 15/19
ISE
ARTIQ
Size A3
Rev 1.0


IC4B
BANK 14
XC7A50T-2FGG484C
IC4D
BANK 16
XC7A100T-2FGG484C
IC4A
BANK 13
IC4E
BANK 34
XC7A100T-2FGG484C
IC4C
BANK 15
XC7A100T-2FGG484C
All LVDS_0 lines are capable of clock input.
Pins are set roughly according area
PLEASE CHANGE TO EASY
ROUTING
Bank 34, 14 => main connector
Bank 15 => ADC / DAC
Bank 16 => Ethernet
FPGA_SPI2_MOSI
FPGA_SPI2_MISO
FPGA_SPI2_SCLK
FPGA_SPI_CS
FPGA_SPI_MOSI
FPGA_SPI_MISO
FPGA_SPI_SCLK
RxD_P2V5
TxD_P2V5
I2C_SW_SDA
I2C_SW_SCL
FPGA_PCLK
FPGA_nPCLK
LED_USER1
LED_USER2
LED_USER3
BSH103
P3V3
GND

Maximum power calculation

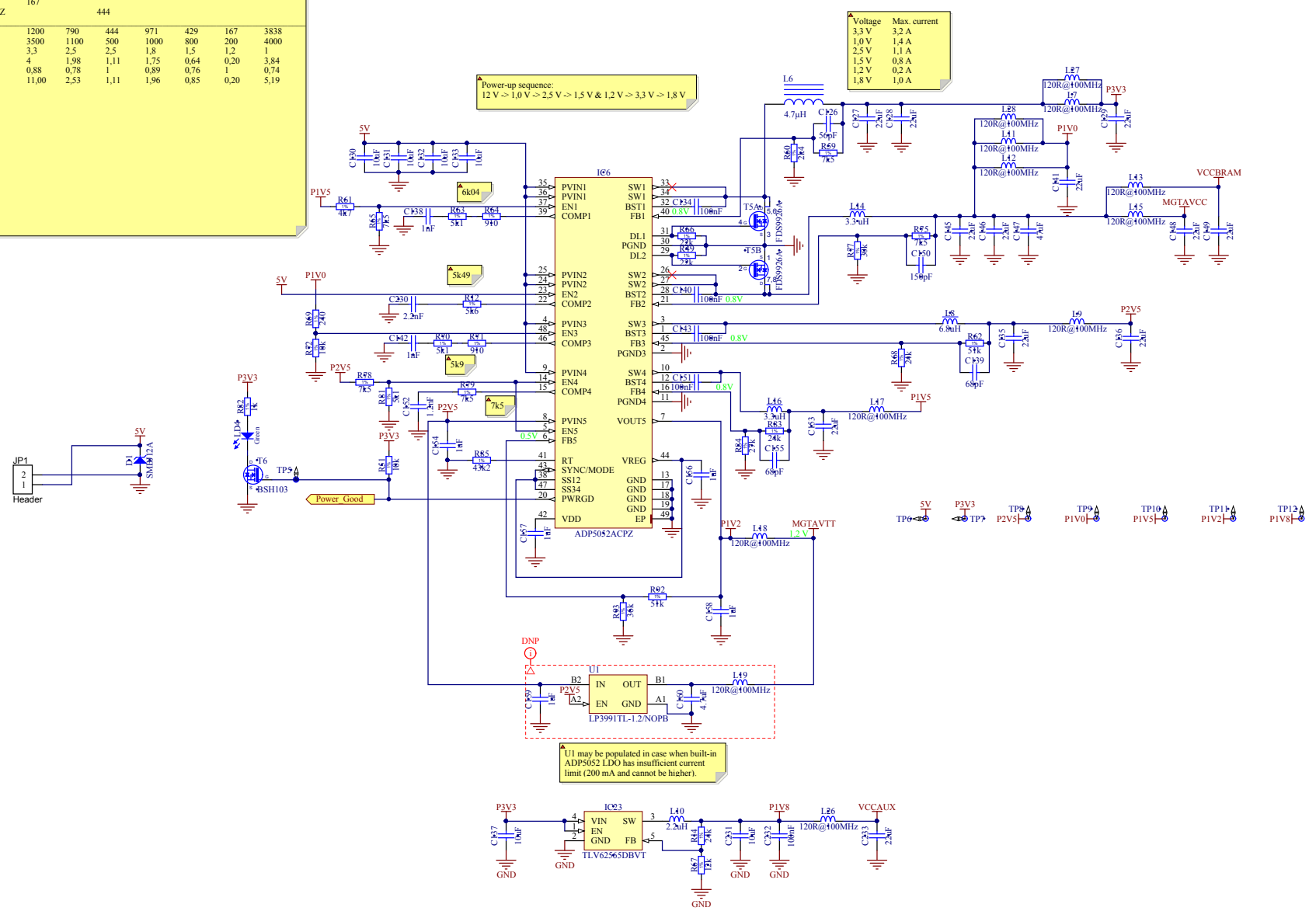
		P3V3	P2V5	LDO P2V5	P1V8	P1V5	LDO P1V2	P1V0
DAC / ADC / Amp. Op THS4501		900						
LED user, power good, fpga done, 3V3 LED12								
1kHz-68Mhz Frequency Clock Multiplier LTC6904		10						
Ethernet Controller	LAN8720	400						
FPGA memory	S25FL128SAGBHIA	100						
125 MHz clock	510FBA125M000	23						
RAM x16, rev E	MT41K256M16					274		
Artix 7 FPGA	XC7A100T		767		971	155	167	3838
LDO 1V2		167						
2V5 LDO	ADP5052ACPZ			444				
SUM [mA]		1200	790	444	971	429	167	3838
Current available [mA]		3500	1100	500	1000	800	200	4000
Voltage [V]		3,3	2,5	2,5	1,8	1,5	1,2	1
POWER [W]		4	1,98	1,11	1,75	0,64	0,20	3,84
Efficiency		0,88	0,78	1	0,89	0,76	1	0,74
POWER [W]		11,00	2,53	1,11	1,96	0,85	0,20	5,19

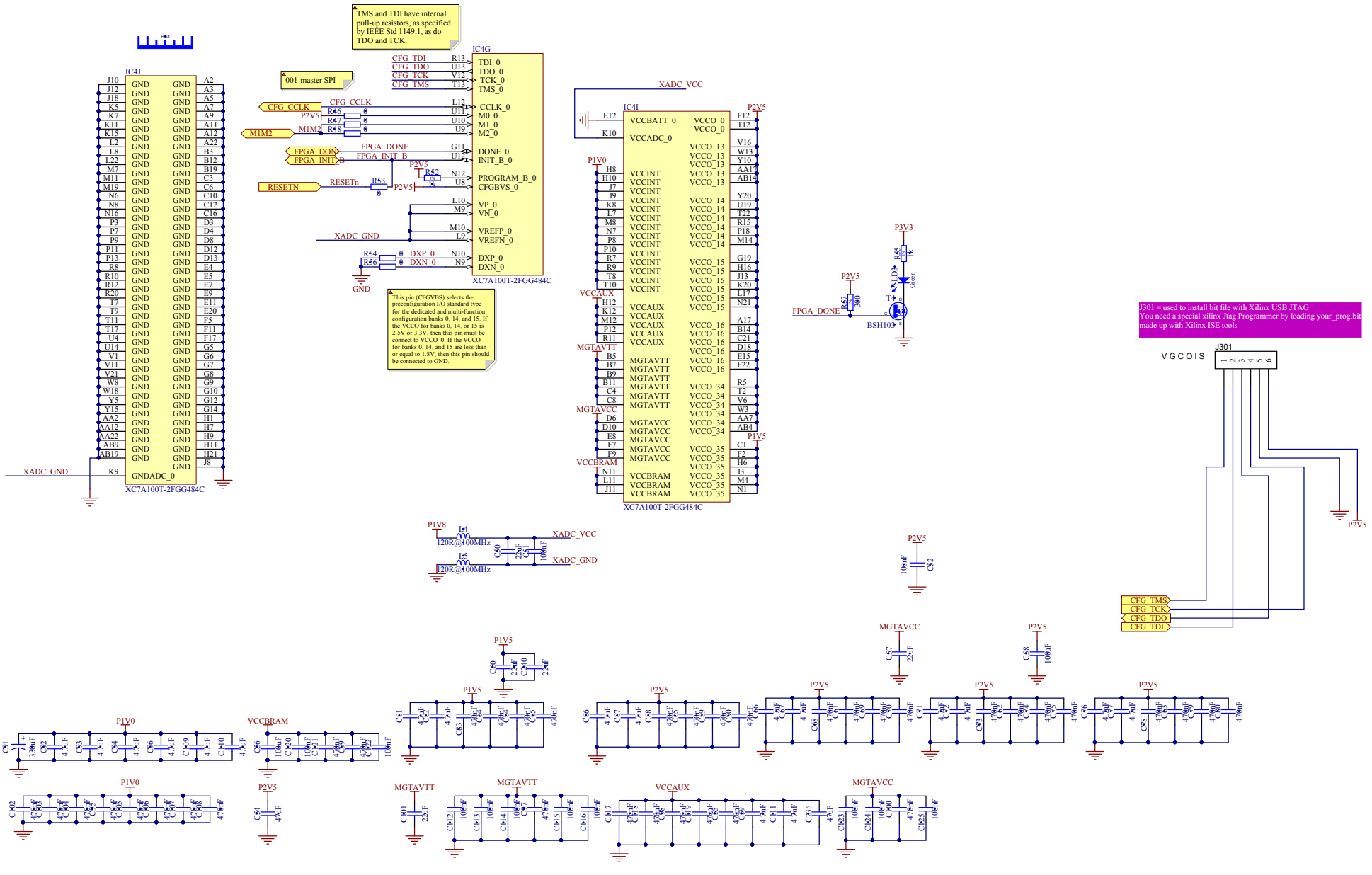
Total power : 14 W
Maximum P5V0 current: 2.8 A

Voltage	Max. current
3,3 V	3,2 A
1,0 V	1,4 A
2,5 V	1,1 A
1,5 V	0,8 A
1,2 V	0,2 A
1,8 V	1,0 A

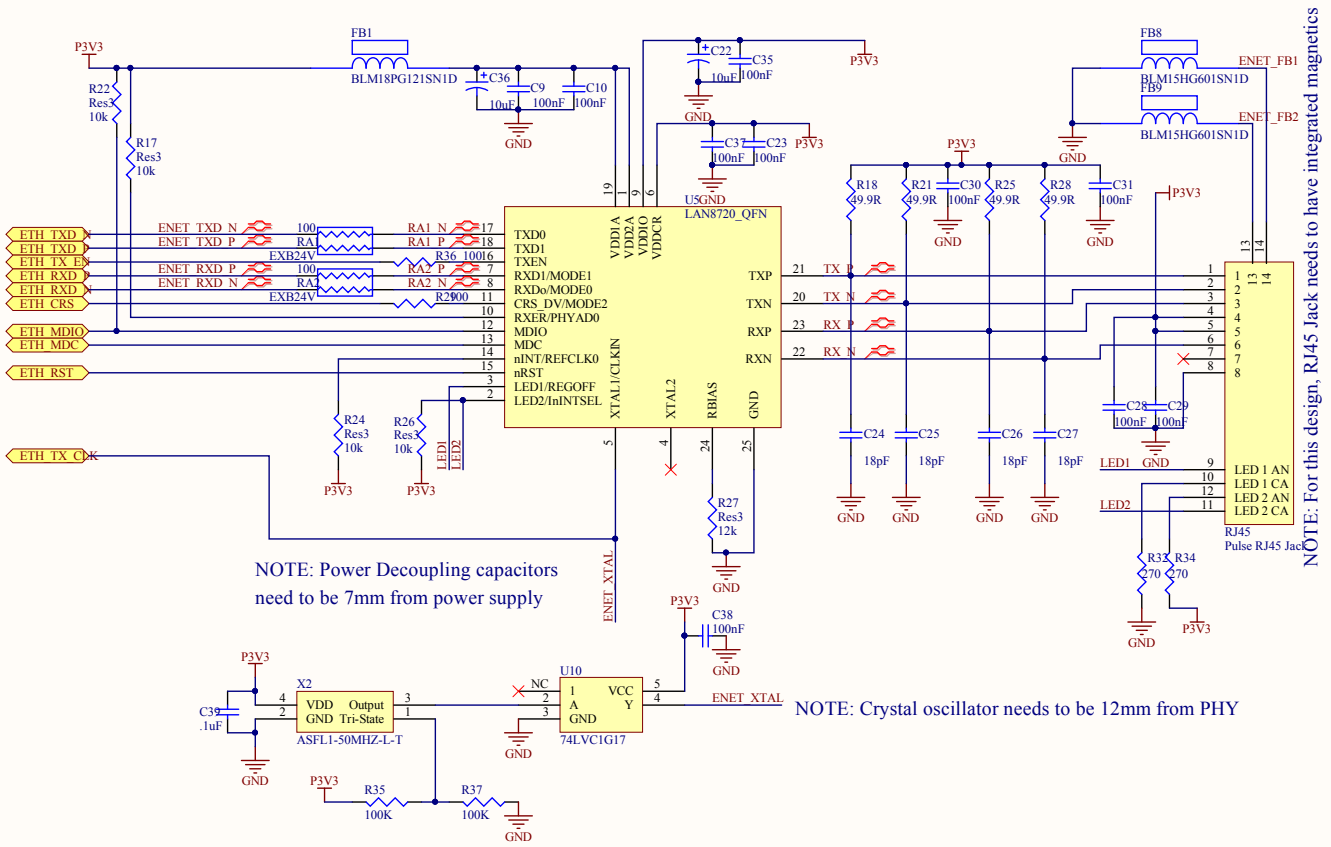
Power-up sequence:
12 V -> 1,0 V -> 2,5 V -> 1,5 V & 1,2 V -> 3,3 V -> 1,8 V

U1 may be populated in case when built-in ADP5052 LDO has insufficient current limit (200 mA and cannot be higher).

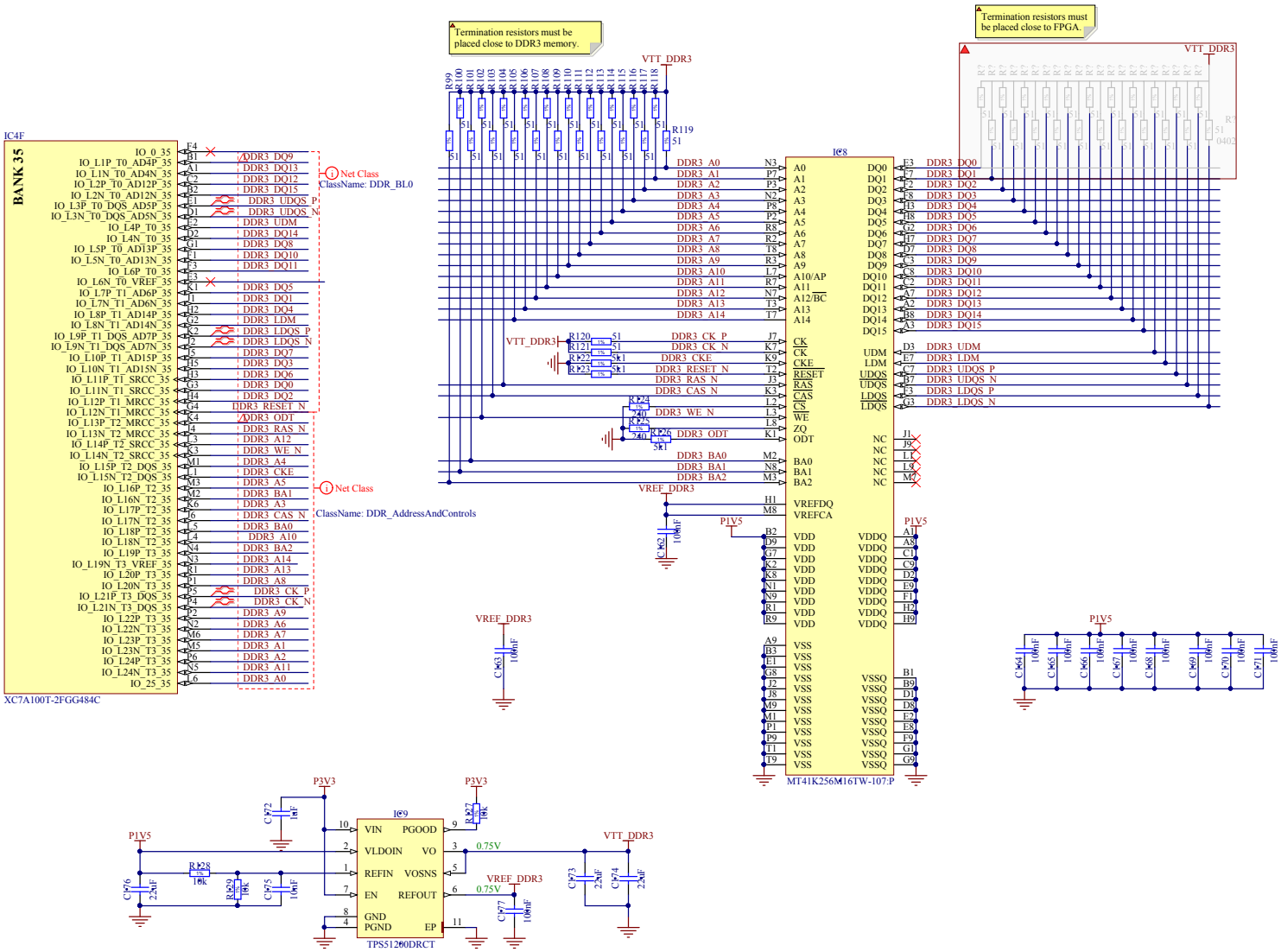


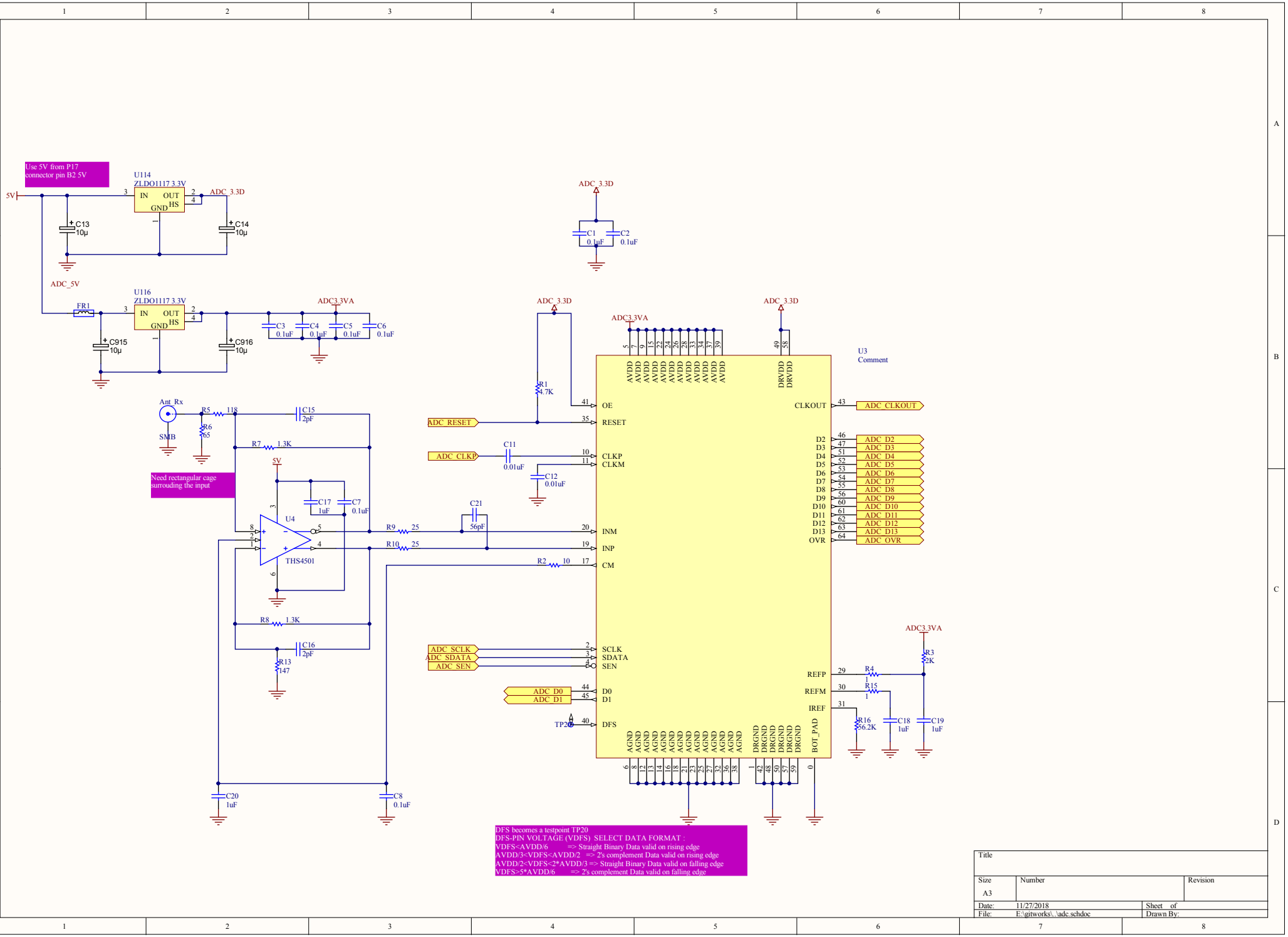

TMS and TDI have internal pull-up resistors, as specified by IEEE Std 1149.1, as do TDO and TCK.
001-master SPI
This pin (CFGVBS) selects the preconfiguration I/O standard type for the dedicated and multi-function configuration banks 0, 14, and 15. If the VCCO for banks 0, 14, or 15 is 2.5V or 3.3V, then this pin must be connect to VCCO_0. If the VCCO for banks 0, 14, and 15 are less than or equal to 1.8V, then this pin should be connected to GND.
J301 = used to install bit file with Xilinx USB JTAG
You need a special xilinx Jtag Programmer by loading your_prog.bit made up with Xilinx ISE tools
IC4J
IC4G
IC4I
XC7A100T-2FGG484C
CFG_TMS
CFG_TCK
CFG_TDO
CFG_TDI
XADC_VCC
XADC_GND
FPGA_DONE
FPGA_INIT_B
RESETn
M1M2
CFG_CCLK
P1V0
P1V5
P2V5
P3V3
VCCBRAM
MGTAVTT
MGTAVCC
VCCAUX
VGCOIS
J301
BSH103
LED Green

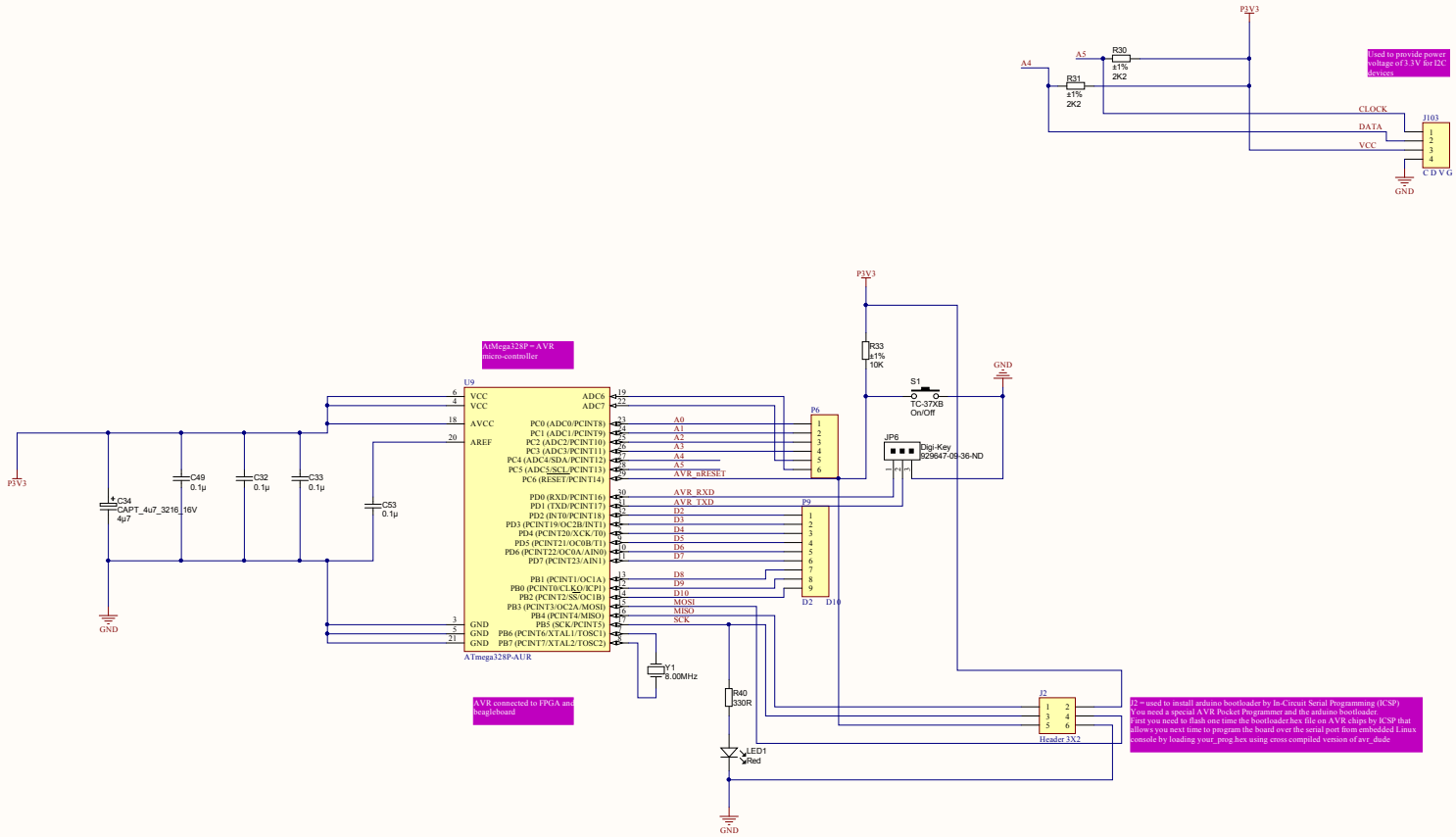
Ethernet Physical Layer (SMSC LAN8720)



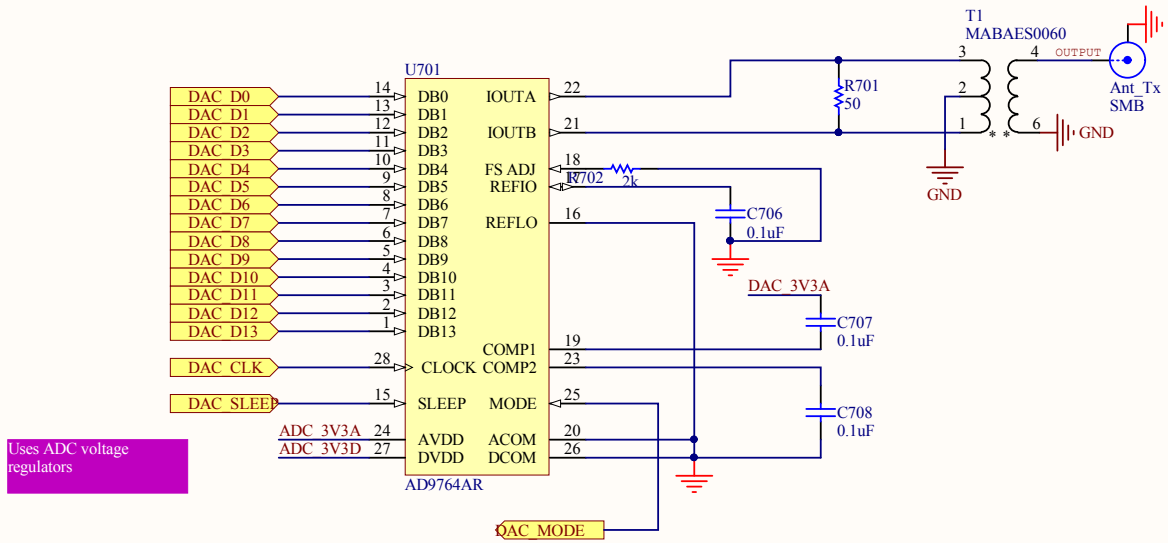
Title	Ethernet Section	
Size: B	Number:	Revision: 2.4b
Date: 11/27/2018		Sheet 5of 9
File: E:\gitworks\..\ethernet.SchDoc		Drawn By: Adam Vadala-Roth


Termination resistors must be placed close to DDR3 memory.
Termination resistors must be placed close to FPGA.
VTT_DDR3
IC4F
BANK 35
XC7A100T-2FGG484C
Net Class
ClassName: DDR_BL0
ClassName: DDR_AddressAndControls
IC8
MT41K256M16TW-107:P
VREF_DDR3
P1V5
P3V3
IC9
TPS51200DRCT
0.75V

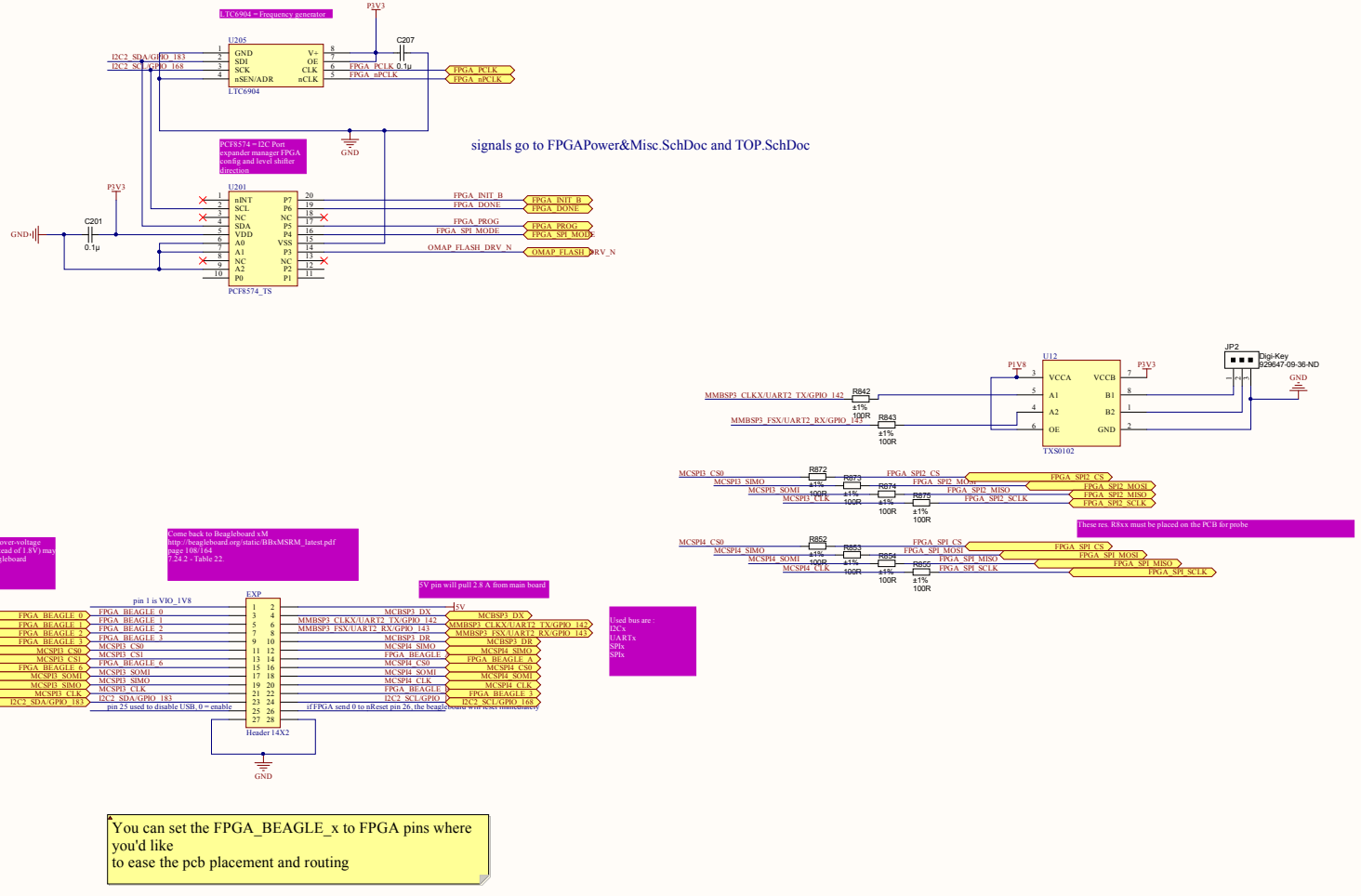

Use 5V from P17 connector pin B2 5V
5V
U114
ZLDO1117 3.3V
IN
OUT
GND
HS
ADC_3.3D
C13 10µ
C14 10µ
ADC_5V
U116
ZLDO1117 3.3V
FR1
C915 10µ
C916 10µ
ADC3.3VA
C3 0.1uF
C4 0.1uF
C5 0.1uF
C6 0.1uF
C1 0.1uF
C2 0.1uF
U3
Comment
AVDD
DRVDD
AGND
DRGND
BOT_PAD
OE
RESET
CLKP
CLKM
INM
INP
CM
SCLK
SDATA
SEN
D0
D1
DFS
CLKOUT
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
OVR
REFP
REFM
IREF
R1 4.7K
ADC_RESET
ADC_CLKP
C11 0.01uF
C12 0.01uF
ADC_CLKOUT
ADC_D2
ADC_D3
ADC_D4
ADC_D5
ADC_D6
ADC_D7
ADC_D8
ADC_D9
ADC_D10
ADC_D11
ADC_D12
ADC_D13
ADC_OVR
Ant_Rx
SMB
R5 118
R6 65
R7 1.3K
C15 2pF
Need rectangular cage surrouding the input
U4
THS4501
C17 1uF
C7 0.1uF
C21 56pF
R9 25
R10 25
R2 10
R8 1.3K
C16 2pF
R13 147
C20 1uF
C8 0.1uF
ADC_SCLK
ADC_SDATA
ADC_SEN
ADC_D0
ADC_D1
TP20
R3 2K
R4 1
R15 1
R16 56.2K
C18 1uF
C19 1uF
DFS becomes a testpoint TP20
DFS-PIN VOLTAGE (VDFS) SELECT DATA FORMAT :
VDFS<AVDD/6 => Straight Binary Data valid on rising edge
AVDD/3<VDFS<AVDD/2 => 2's complement Data valid on rising edge
AVDD/2<VDFS<2*AVDD/3 => Straight Binary Data valid on falling edge
VDFS>5*AVDD/6 => 2's complement Data valid on falling edge
Title
Size
A3
Number
Revision
Date: 11/27/2018
Sheet of
File: E:\gitworks\..\adc.schdoc
Drawn By:



Title		
Size: A2	Number	Revision
Date: 11/27/2018		Sheet of
File: E:\gitworks\...\avr.SchDoc		Drawn By:



Title		
Size: A4	Number	Revision
Date: 11/27/2018		Sheet of
File: E:\gitworks\..\dac.SchDoc		Drawn By:


LTC6904 = Frequency generator
U205
LTC6904
P3V3
C207
0.1µ
I2C2_SDA/GPIO_183
I2C2_SCL/GPIO_168
FPGA_PCLK
FPGA_nPCLK
GND
signals go to FPGAPower&Misc.SchDoc and TOP.SchDoc
PCF8574 = I2C Port expander manager FPGA config and level shifter direction
U201
PCF8574_TS
C201
0.1µ
FPGA_INIT_B
FPGA_DONE
FPGA_PROG
FPGA_SPI_MODE
OMAP_FLASH_DRV_N
U12
TXS0102
P1V8
P3V3
JP2
Digi-Key
929647-09-36-ND
MMBSP3_CLKX/UART2_TX/GPIO_142
MMBSP3_FSX/UART2_RX/GPIO_143
R842
R843
100R
±1%
MCSPI3_CS0
MCSPI3_SIMO
MCSPI3_SOMI
MCSPI3_CLK
FPGA_SPI2_CS
FPGA_SPI2_MOSI
FPGA_SPI2_MISO
FPGA_SPI2_SCLK
R872
R873
R874
R875
These res. R8xx must be placed on the PCB for probe
MCSPI4_CS0
MCSPI4_SIMO
MCSPI4_SOMI
MCSPI4_CLK
FPGA_SPI_CS
FPGA_SPI_MOSI
FPGA_SPI_MISO
FPGA_SPI_SCLK
R852
R853
R854
R855
warning: over-voltage (3.3V instead of 1.8V) may harm beagleboard
Come back to Beagleboard xM http://beagleboard.org/static/BBxMSRM_latest.pdf page 108/164 7.2.4.2 - Table 22.
5V pin will pull 2.8 A from main board
pin 1 is VIO_1V8
EXP
Header 14X2
FPGA_BEAGLE_0
FPGA_BEAGLE_1
FPGA_BEAGLE_2
FPGA_BEAGLE_3
MCSPI3_CS0
MCSPI3_CS1
FPGA_BEAGLE_6
MCSPI3_SOMI
MCSPI3_SIMO
MCSPI3_CLK
I2C2_SDA/GPIO_183
pin 25 used to disable USB, 0 = enable
MCBSP3_DX
MMBSP3_CLKX/UART2_TX/GPIO_142
MMBSP3_FSX/UART2_RX/GPIO_143
MCBSP3_DR
MCSPI4_SIMO
FPGA_BEAGLE_4
MCSPI4_CS0
MCSPI4_SOMI
MCSPI4_CLK
FPGA_BEAGLE_5
I2C2_SCL/GPIO_168
if FPGA send 0 to nReset pin 26, the beagleboard will reset immediately
Used bus are :
I2Cx
UARTx
SPIx
SPIx
You can set the FPGA_BEAGLE_x to FPGA pins where you'd like
to ease the pcb placement and routing