Application Report
SPRABI1A—April 2011

DDR3 Design Requirements for KeyStone Devices

High-Performance and Multicore Processors

Abstract

This document provides implementation instructions for the DDR3 interface incorporated in the Texas Instruments (TI) Keystone series of DSP devices. It supports 1333 MT/s and higher memory speeds in a variety of topologies (see to the Data Manual for supported speeds). This document assumes the user has a familiarization with DRAM implementation concepts and constraints. When searching for a particular configuration see the appendix, which will alleviate the need for searching the entire document which contains all possible variations.

Contents

List of Tables

List of Figures

Scope

The primary scope of this document is to establish a minimum set of requirements necessary to assure functional success in new application designs for Texas Instruments High Performance Multiprocessor DSPs incorporating DDR3 memory interfaces.

Background

Technological advances in memory architecture in both speed and densities require a different mindset when it comes to application implementation and design from the customary and traditional SRAM, DDR, and DDR2 devices.

Related Specifications and Documentation

The following documentation shall be used in conjunction with this design guide to properly design in and implement a successful DDR3 interface to Texas Instruments high performance multiprocessor DSPs.

JESD 79-3C:	JEDEC DDR3 Standard
SPRUGV8:	*DDR3 Memory Controller for KeyStone Devices User Guide*
By Part #	TMS320TCI66xx Data Manual (appropriate data manual to be used)
SPRABI2:	*Hardware Design Guide for KeyStone Devices*
TN-41-04:	DDR3 Dynamic On-Die Termination; Micron, technical Note
TN-41-06:	DDR3 Termination Data Strobe (TDQS); Micron
MO-269D:	JEDEC Document: MO (Module Outline) {for DDR3}
SO-007B:	JEDEC Document: SO (Socket Outline)
TN-42-02:	DDR3 ZQ Calibration; Micron
TN-04-54:	High-Speed DRAM Controller Design; Micron,
TN-41-01:	Calculating Memory System Power for DDR3; Micron,
TN-41-07:	DDR3 Power-Up, Initialization, and Reset; Micron,
TN-41-08:	Design Guide for Two DDR3-1066 UDIMM Systems; Micron
JEDEC 21-C:	Unbuffered DIMM Design Specification
Pub 95 PS-001A:	Connector Performance Standards for Outlines of Solid State Related Products – 240 pin DDR3 UDIMM

1 Migrating Designs from DDR2 to DDR3 (Features & Comparisons)

This section is not intended to present a detailed listing of differences between DDR2 and DDR3 designs, but to provide key insight into specific differences that will have a positive impact as customers migrate from a DDR2 to a DDR3 platform (based on the assumption the DDR3 interface is implemented correctly).

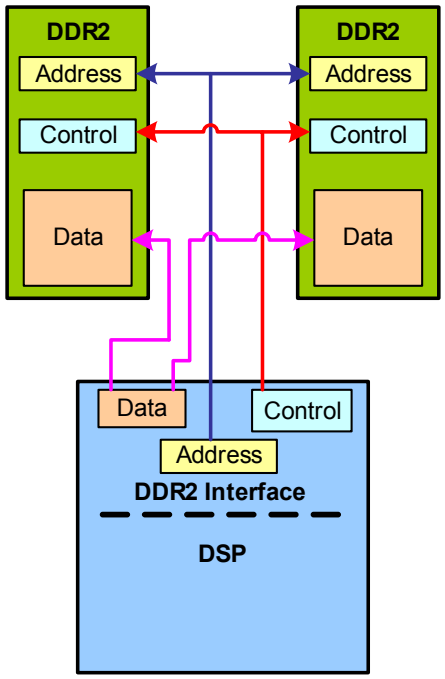
1.1 Topologies

In a DDR2 to DDR3 comparison the single greatest improvement from a topology standpoint is the change from a "Balanced – T" to a "Fly-By" architecture. Each architecture is briefly described below.

1.1.1 Balanced Line Topology

In a traditional DDR2 design a balanced "T" style topology is typically recommended if not required for address and control lines (depending on the number of SDRAMs utilized). This is generally recommended to balance any delays to each SDRAM device. The general concept of a balanced line topology is not used in DDR3 implementations. Figure 1 illustrates the general concept of a "balanced line topology" found in a typical DDR2 design. The balanced line topology in DDR3 has been abandoned for "Fly-By" topology which better accommodates the higher performance SDRAMs.

Figure 1 Typical DDR Balanced Line Topology



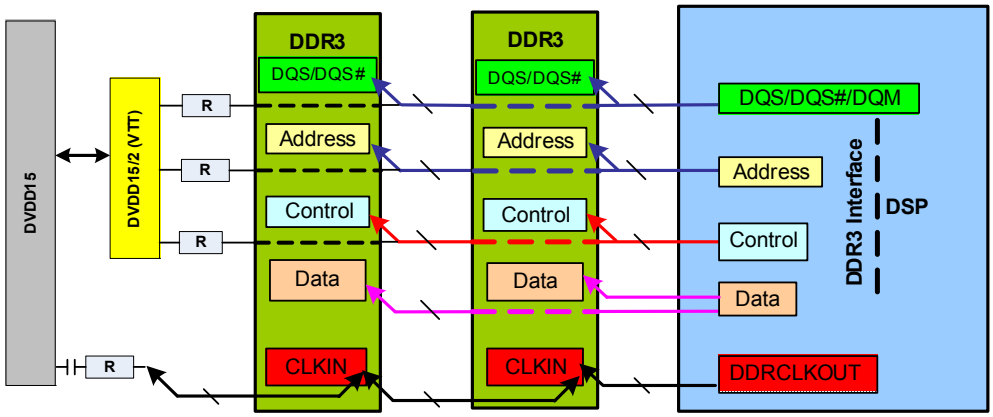
1.1.1.1 Balanced Line Topology Issues

The down side to the use of a balanced T-line topology for DDR2 designs is that it may introduce a varying amount of additional skew because of the inclusion of multiple stubs and stub lengths for each individual net. The addition of multiple loads on respective address and control nets limits bandwidth. Skews normally encountered between the address/control and data nets also induce bandwidth limitations.

1.1.2 Fly By Topology

The DDR3 "fly-by" architecture provides a benefit to layout and routing of control and address signals. In this topology, each respective signal from the DSP DDR3 controller is sequentially routed from one SDRAM to the next thus eliminating reflections associated with any stub or superfluous traces previously seen in DDR2 designs. Figure 2 illustrates a typical DDR3 SDRAM "fly-by" interface topology.

Figure 2 Typical DDR3 "Fly-By" Architecture



Note 1: DVDD15 is a 1.5VDC supply rail common to both the SDRAM and DSP.

Note 2: DVDD15/2 or VTT refers to 750mV DC.

Note 3: Differential ended terminations require dedicated discrete component(s) per complementary net.

1.1.2.1 Balanced Line Topology Issues

The down side to the use of a fly-by topology for DDR3 designs is the induced delay from the DSP DDR3 controller to the SDRAMs. In fact, the delay is different at each SDRAM. Correction or compensation for the different controller to DRAM lengths is handled through Read and Write Leveling. Also keep in mind the following:

- Data nets are point-to-point unless designed as a dual rank implementation.
- Clock nets are point-to-multipoint and end terminated (differently than control, command, or address nets).
- Control nets are point-to-multipoint and end terminated to Vtt.
- Address nets are point-to-multipoint and are end terminated to Vtt.

1.2 ECC (Error Correction)

Error correction has not been supported in previous TI DSPs utilizing JEDEC compliant SDRAM (DDR or DDR2). Error correction is now supported in TI's new Keystone DSP processor family. Supporting ECC allows for the automatic detection and correction of single and double-bit errors. ECC software configuration and control is described in detail in the Keystone DDR3 Controller Guide.

1.3 DDR3 Features & Improvements

In addition to TI's DDR3 controller now supporting ECC, the DSP DDR3 controller and new DDR3 SDRAMs offer five notable features. The additional features include:

- Read Leveling
- Write Leveling
- Change in pre-fetch size
- ZQ calibration
- A reset pin

These features are described briefly below. Detailed configuration is described in the Keystone DDR3 Controller Guide.

1.3.1 Read Leveling

The memory controller also automatically corrects for delay skew between SDRAMs during Read Leveling. Read Leveling takes advantage of values loaded into the SDRAMs multi-purposed register (MPR). The values loaded into this register are used by the DSP DDR3 controller to calibrate each signal path relative to skew. Each respective SDRAM byte is then internally corrected thus improving performance.

1.3.2 Write Leveling

The memory controller automatically corrects for delay skew between SDRAMs during Write Leveling. During Write Leveling, correction for SDRAM skew (the tDQSS, tDSS and tDSH) is handled using a programmable DQS delay to shore up the timing relationship to the clock and strobe signals. During the Write Leveling procedure the DSP controller will delay the DQS until a valid change of state is detected at the SDRAM clock (CK) signal (*see* Section 4.3 *for additional details*).

1.3.3 Pre-fetch

The new DDR3 architecture now supports an 8-bit pre-fetch to improve back-to-back accesses (DDR2 only allowed a 4-bit pre-fetch).

1.3.4 ZQ Calibration

ZQ calibration is intended to control the ODT values and output drivers (R_{TT} and R_{ON} respectively) of the SDRAM. ZQ calibration is not a controllable feature from the DSP. It is controlled using a precision (≤ 1% tolerance) 240Ω resistor.

The DDR3 SDRAM ZQ calibration cycle is made up of an initial long (ZQ_{CL}) calibration cycle requiring 512 clock cycles to complete (which is why it is typically performed during the initial boot or reset conditions) and a shorter ZQ calibration period.

The subsequent short (ZQ_{SC}) calibration requires only 64 clock cycles and used when the SDRAM is idle. The periodic short calibrations cycles accommodate for minor variations in the temperature and voltage. The short calibration cycle (ZQ_{SC}) is designed to correct for a minimum 0.5% impedance error within the allotted 64 clock cycles.

See the selected SDRAM data sheet for the maximum ODT, temperature and voltage sensitivity values. The ZQ calibration is intended to help minimize PCB impedance discontinuities between traces and SDRAM drivers.

Note—IMPORTANT: Texas Instruments requires the use of dedicated ZQ resistor (240Ω) to be connected to each SDRAM ZQ pin (cannot share pins).

1.3.5 Reset Pin Functionality

The new DDR3 architecture also supports a reset pin. This Reset Pin is designed to allow the user to clear all data (information) stored the DDR3 SDRAM. The advanced benefit of this feature is that there is no need to reset each control register separately or restart (power down and up again) each individual DDR3 SDRAM. By initiating a reset the SDRAM will recover in a known good state (if needed).

The reset function of the UDIMM or SDRAM are an active low (RESET#) LVCMOS input and referenced to Vss. The SDRAM /UDIMM input pin functions rail-to-rail with a DC HIGH $\geq 0.8 \times$ Vdd (1.5 V $\times$ 0.8 = 1.2 Vdc) and DC LOW $\leq 0.2 \times$ Vdd (1.5 V x 0.2 V = 0.3 V).

Note—IMPORTANT: The TI DSP DDR3 controller cannot be held in reset for more than 1 hour during the initial power-up. Also, the TI DSP DDR3 controller cannot be held in reset for more than 5% of its total power-on hours.

1.3.6 Additional DDR2 to DDR3 Differences

The change from supporting a both a single ended and differential DQS (DDR2) to only a differential DQS (DDR3) improves noise immunity, and allows for longer signal paths without compromising signal integrity.

2 Prerequisites

2.1 High Speed Designs

The goal of this document is to make the DDR3 system implementation and integration easier while reducing the added risk of designing in a high performance interface. It is still expected that the PCB design work (design, layout, and fabrication) is performed, supervised, or reviewed by a highly knowledgeable high-speed PCB designer. This includes a thorough understanding of all high-speed design rules. Specific areas to avoid include ground plane cuts, incorrect spacing, and signal skew mis-matches as well as timing violations. The total system should be evaluated for such areas including power, filtering, termination, crosstalk, and EMI.

2.2 JEDEC DDR3 Specification – Compatibility & Familiarity

The DDR3 interface on the Keystone devices is designed to be compatible with the JEDEC JESD79-3C DDR3 specification. It is assumed that the reader is familiar with this specification and the basic electrical operation of the interface. In addition, several memory manufacturers provide detailed application reports on DDR3 operation.

2.3 Memory Types

Devices from many manufacturers are available at the time this document was generated. It is recommended that only quality DRAMs be used from known good manufacturers that fully comply with the latest DDR3 JEDEC specification. Incorrect DRAM manufacturer selection can cause performance problems that may not be resolved within the available software or configuration limitations of the DSP.

In addition to supporting the DDR3 SDRAMs, the TI Keystone family of DSPs also supports SDRAMs including ECC (Error correction) or UDIMMs.

2.4 Memory Speeds

The Keystone family of DSPs memory interface currently supports various configurations as specified in the JEDEC DDR3 standard. Keystone devices support data rates of DDR3 1333 MT/s and higher. See the Data Manual for supported data rates.

2.5 Addressable Memory Space

The TI DSP DRAM interface supports up to 8G Bytes of DDR3 DRAM in the configurations and topologies identified in Section 2.6.1 and Section 2.6.2.

2.6 DDR3 SDRAM/UDIMM Memories, Topologies, and Configurations

2.6.1 Topologies

The current DDR3 controller design implementation supports several different DRAM topologies. The following list describes the known available topologies to be used with the TI Keystone DSPs. See the final data manual for a definitive confirmation on available memory topologies for the DSP before proceeding.

- ×8 [×16 is the minimum supported width, two ×8 devices are required]
- ×16
- ×32 [with and without ECC]
- ×64 [with and without ECC]
- UDIMM [×72 & ×36]

2.6.2 Configurations

The current DDR3 controller design implementation allows for multiple DRAM configurations to be used. The following list describes the known useable configurations available when using a TI Keystone family of DSPs. See the final data manual for a definitive confirmation on useable memory configurations and bus widths before proceeding.

The following tables are intended to provide a general overview of the possible DDR3 DRAM topologies useable with the TI DDR3-supported DSP. In all cases only JEDEC compliant (JESD79-3C) SDRAMs are supported:

For all tables below, the notation "*" implies possible support, not plan of record.

Table 1 x8 Width DDR3 SDRAM Possible Configurations Supported

Device Width	Total Memory / Memory Topology	Rank Width	Total Size
x8 SDRAM	1Gb / (16M x 8 x 8) x 2 SDRAMS	x16	256MB
x8 SDRAM	1Gb / (16M x 8 x 8) x 4 SDRAMS	x32	512MB
x8 SDRAM	4Gb / (16M x 8 x 8) x 8 SDRAMS	x64	1024MB
x8 SDRAM	1Gb / (16M x 8 x 8) x 8 SDRAMS x 2 Ranks	x64	2048MB
x8 SDRAM	2Gb / (32M x 8 x 8) x 2 SDRAMS	x16	512MB
x8 SDRAM	2Gb / (32M x 8 x 8) x 4 SDRAMS	x32	1024MB
x8 SDRAM	2Gb / (32M x 8 x 8) x 8 SDRAMS	x64	2048MB
x8 SDRAM	2Gb / (32M x 8 x 8) x 8 SDRAMS x 2 Ranks	x64	4096MB
x8 SDRAM	4Gb / (64M x 8 x 8) x 2 SDRAMS	x16	1024MB
x8 SDRAM	4Gb / (64M x 8 x 8) x 4 SDRAMS	x32	2048MB
x8 SDRAM	4Gb / (64M x 8 x 8) x 8 SDRAMS	x64	4096MB
x8 SDRAM	4Gb / (64M x 8 x 8) x 8 SDRAMS x 2 Ranks	x64	8192MB
x8 SDRAM	8Gb / (64M x 8 x 8) x 2 SDRAMS	x16	2048MB
x8 SDRAM	8Gb / (64M x 8 x 8) x 4 SDRAMS	x32	4096MB
x8 SDRAM	8Gb / (64M x 8 x 8) x 8 SDRAMS	x64	8192MB
End of Table 1			

Table 2 x16 Width DDR3 SDRAM Possible Configurations Supported (Part 1 of 2)

Device Width	Total Memory / Memory Topology	Rank Width	Total Size
x16 SDRAM	1Gb / (8M x 16 x 8) x 1 SDRAMS	x16	128MB
x16 SDRAM	1Gb / (8M x 16 x 8) x 2 SDRAMS	x32	256MB
x16 SDRAM	1Gb / (8M x 16 x 8) x 4 SDRAMS	x64	512MB
x16 SDRAM	1Gb / (8M x 16 x 8) x 4 SDRAMS x 2 Ranks	x64	1024MB
x16 SDRAM	2Gb / (16M x 16 x 8) x 1 SDRAM	x16	256MB
x16 SDRAM	2Gb / (16M x 16 x 8) x 2 SDRAMS	x32	512MB
x16 SDRAM	2Gb / (16M x 16 x 8) x 4 SDRAMS	X64	1024MB
x16 SDRAM	2Gb / (16M x 16 x 8) x 4 SDRAMS x 2 Ranks	x64	2048MB
x16 SDRAM	4Gb / (32M x 16 x 8) x 1 SDRAMS	x16	512MB
x16 SDRAM	4Gb / (32M x 16 x 8) x 2 SDRAMS	x32	1024MB
x16 SDRAM	4Gb / (32M x 16 x 8) x 4 SDRAMS	x64	2048MB
x16 SDRAM	4Gb / (32M x 16 x 8) x 4 SDRAMS x 2 Ranks	x64	4096MB
x16 SDRAM	8Gb / (64M x 16 x 8) x 1 SDRAMS	x16	1024MB

Table 2 x16 Width DDR3 SDRAM Possible Configurations Supported (Part 2 of 2)

Device Width	Total Memory / Memory Topology	Rank Width	Total Size
x16 SDRAM	8Gb / (64M x 16 x 8) x 2 SDRAMS	x32	2048MB
x16 SDRAM	8Gb / (64M x 16 x 8) x 4 SDRAMS	x64	4096MB
x16 SDRAM	8Gb / (64M x 16 x 8) x 4 SDRAMS x 2 Ranks	x64	8192MB
End of Table 2			

Table 3 x32 Width DDR3 SDRAM Possible Configurations Supported

Device Width	Total Memory / Memory Topology	Rank Width	Total Size
x32 SDRAM	2Gb / (8M x 32 x8) x 1 SDRAM	x32	256MB*
x32 SDRAM	4Gb / (8M x 32 x 8) x 2 SDRAMS	x64	512MB*
x32 SDRAM	4Gb / (8M x 32 x 8) x 2 SDRAMS x 2 Ranks	x32	256MB*
x32 SDRAM	8Gb / (8M x 32 x 8) x 4 SDRAMS x 2 Ranks	x64	512MB*
x32 SDRAM	4Gb / (16M x 32 x 8) x 1 SDRAM	x32	512MB*
x32 SDRAM	8Gb / (16M x 32 x 8) x 2 SDRAM	x64	1024MB*
x32 SDRAM	8Gb / (16M x 32 x 8) x 2 SDRAMS x 2 Ranks	x32	1024MB*
x32 SDRAM	16Gb / (16M x 32 x 8) x 4 SDRAMS x 2 Ranks	x64	2048MB*
End of Table 3			

In addition to the discrete SDRAM devices configurations listed above, the following ECC configurations are supported:

Table 4 Discrete SDRAM Configurations with ECC (Part 1 of 2)

Device Width	Memory rank Topology	Rank Width	Total Size
x8 SDRAM	1Gb (16M x 8 x 8) x 5 SDRAMS	x36	512MB
	1Gb (16M x 8 x 8) x 9 SDRAMS	x72	1024MB
	1Gb (16M x 8 x 8) x 9 SDRAMS x 2 Ranks	x72	2048MB
	2Gb (32M x 8 x 8) x 5 SDRAMS	x36	1024MB
	2Gb (32M x 8 x 8) x 9 SDRAMS	x72	2048MB
	2Gb (32M x 8 x 8) x 9 SDRAMS x 2 Ranks	x72	4096MB
	4Gb (64M x 8 x 8) x 5 SDRAMS	x36	2048MB
	4Gb (64M x 8 x 8) x 9 SDRAMS	x72	4096MB
	4Gb (64M x 8 x 8) x 9 SDRAMS x 2 Ranks	x72	8192MB
	8Gb (64M x 8 x 8) x 5 SDRAMS	x36	4096MB
	8Gb (64M x 8 x 8) x 9 SDRAMS	x72	8192MB
Device Width	Memory rank Topology	Rank Width	Total Size
x16 SDRAM [1]	1Gb (8M x 16 x 8) x 3 SDRAMS	x36	256MB
	1Gb (8M x 16 x 8) x 5 SDRAMS	x72	512MB
	1Gb (8M x 16 x 8) x 5 SDRAMS x 2 Ranks	x72	1024MB
	2Gb (16M x 16 x 8) x 3 SDRAMS	x36	512MB
	2Gb (16M x 16 x 8) x 5 SDRAMS	x72	1024MB
	2Gb (16M x 16 x 8) x 5 SDRAMS x 2 Ranks	x72	2048MB
	4Gb (32M x 16 x 8) x 3 SDRAMS	x36	1024MB
	4Gb (32M x 16 x 8) x 5 SDRAMS	x72	2048MB
	4Gb (32M x 16 x 8) x 5 SDRAMS x 2 Ranks	x72	4096MB

Table 4 Discrete SDRAM Configurations with ECC (Part 2 of 2)

Device Width	Memory rank Topology	Rank Width	Total Size
	8Gb (64M x 16 x 8) x 3 SDRAMS	x36	2048MB
	8Gb (64M x 16 x 8) x 5 SDRAMS	x72	4096MB
	8Gb (64M x 16 x 8) x 5 SDRAMS x 2 Ranks	x72	8192MB
End of Table 4			

1. The ECC device can be either x8 or x16 as long as the number of row and column address bits match for all devices in the memory array.

2.6.2.1 Alternate Configurations

Texas Instruments is currently evaluating support for certain DIMMs. In the future this document will be updated to discuss the use and support of DIMMs (TI is currently evaluating the use of single and dual rank DIMMs).

Note—DIMM designs incorporating ×4 devices are not allowed.

2.6.3 Memories – Recommended Devices

Due to the increasing number of JEDEC compliant DDR3 memory devices being developed or obsoleted, only the following criteria will be provided towards the recommendation of recommended DRAM devices to be supported.

Table 5 SDRAM Selection Requirements

Width[1]	Clock Rate (MHz)	Data Rate (MT/s)	CL[2]
x8, x16, x32[3], x36[4], x64[3], x72[4]	400, 533, 667, 800[3]	800, 1066, 1333, 1600[3]	11, 10, 9, 8, 7

1. The minimum acceptable bus with is x16, two x8 DRAM modules are acceptable as long as they are organized in a x16 configuration.
2. See the DRAM data sheet and the DSP memory controller and data sheet for further clarification.
3. See Data Manual for applicability.
4. Provided as ECC support only.

2.6.3.1 Memories – SDRAM Selection Criteria

Table 6 defines the criteria necessary when selecting DDR3 SDRAMs not on the lists above.

Table 6 DDR3 SDRAM Selection Criteria

SDRAM Selection Criteria				
Description	**Min**	**Max**	**Unit**	**Notes**
Width	×8	×64	bit	Minimum supported width is ×16 (2- ×8)
Depth (Density)	512M	8192M	bit	Definition may also include ranked devices (UDIMM)
Data Rate	800	1600	MT/s	
Clock Rate	400	800	Mhz	
Temperature Range	0	95	°C	Depends on end use application
VDD	1.425	1.575	V	
VDDq	1.425	1.575	V	
Latency	5	11		All CAS latencies supported between 5 and 11
JEDEC Compliant DDR3 SDRAM				
End of Table 6				

2.7 DRAM Electrical Interface Requirements

This section briefly defines the electrical interface requirements for using JEDEC compliant DDR3 SDRAM with the TI DSP. Additional information and requirements may exist. Where different or conflicting requirements exist (between applicable standards, SDRAM and DSP data sheets, and this design guide, this design guide should take precedence. Details provided in the following subsection were obtained from TI internal reference material and applicable JEDEC DDR3 SDRAM standards.

2.7.1 Slew

The released JEDEC standard describes in detail skew requirements imposed on the SDRAM, in particular CLK, CLK#, DQS, and DQS#. In order to meet these requirements, loading, SDRAM component selection, and trace routing will have a large impact. See the the modeling and simulation section of this guide for additional information regarding meeting slew rate requirements.

2.7.2 Overshoot & Undershoot Specifications

Overshoot and undershoot limitations are defined in the following tables and figures. A theoretical instantaneous maximum upper and lower amplitude limit of 400mV is allowed for overshoots and undershoots respectively (assuming zero time is involved). Since each overshoot and undershoot have a component of time, each applicable signal must be further independent evaluated. Table 7 defines the limitations as listed in the current released standard for all address and control signals. (Measurements are obtained at the pin of the memory DRAM and not the DSP.)

Table 7 OS & US Requirements for Address & Control Lines

For All Address and Control Pins				
	Max pk OS amplitude (V)	**Max pk US amplitude (V)**	**Max OS area above VDD (V-nS)**	**Max US area below VSS (V-nS)**
DDR3-800	0.4	0.4	0.67	0.67
DDR3-1066	0.4	0.4	0.5	0.5
DDR3-1333	0.4	0.4	0.4	0.4
DDR3-1600	0.4	0.4	0.33	0.33

Figure 3 graphically table defines the limitations as listed in the current released standard for all address and control pins.

Figure 3 Control and Address Overshoot & Undershoot Requirements

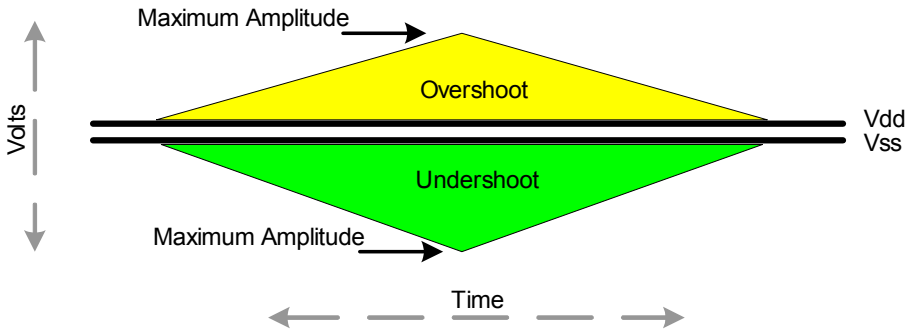


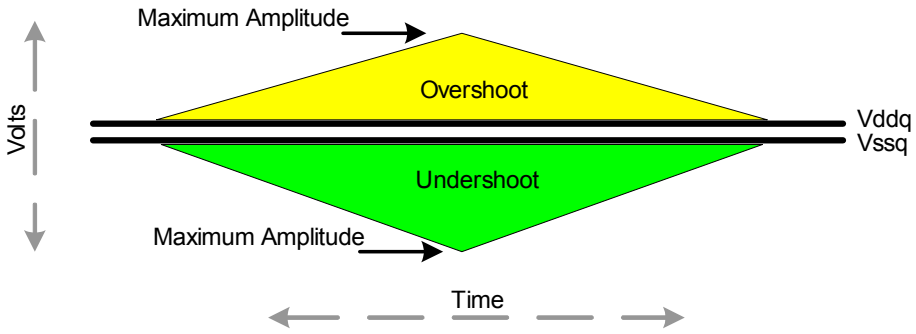
Table 8 defines the limitations as listed in the current released standard for all data, clock, strobe, and mask signals.

Table 8 OS and US Requirements for CK, CK#, DQ, DQS, DQS#, DM lines

For All Data, Clock, Strobe, and Mask Pins				
	Max pk OS amplitude (V)	**Max pk US amplitude (V)**	**Max OS area above VDD (V-nS)**	**Max US area below VSS (V-nS)**
DDR3-800	0.4	0.4	0.25	0.25
DDR3-1066	0.4	0.4	0.19	0.19
DDR3-1333	0.4	0.4	0.15	0.15
DDR3-1600	0.4	0.4	0.13	0.13

Figure 4 graphically defines the limitations as listed in the current released standard for all data, clock, strobe, and mask signals.

Figure 4 Data, Clock, Strobe, & Mask Overshoot & Undershoot Requirements



2.7.2.1 Overshoot & Undershoot Example Calculations

The following provides as an example the steps necessary to calculate the over and undershoots for any waveform.

Assumptions: Vdd = 1.5 Vdc; Vss = 0.00 Vdc; Vref = 0.75 Vdc (Vdd/2)

Overshoot Example (Figure 4)

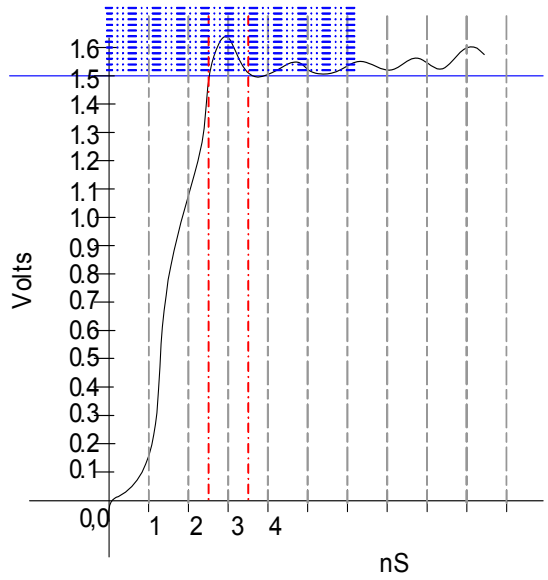
1. Determine amplitude over V_{DD}
2. Determine the duration of the amplitude
3. Calculate the final value

   $OS = Amplitude * Duration$

   $OS = 180mV * 1nS$

   $OS = 0.18VnS$
4. Compare results to the applicable SDRAM row and column (Section 2.7.2) paying attention to speed grade and signal type differences. If the SDRAM speed was DDR3-800 or DDR3-1066 and this were a data, clock, strobe, or mask net the overshoot would be acceptable. In the case of data, clock, strobe, or mask DDR3-1333 and DDR3-1600 speed grades this level of overshoot is not acceptable. Note: this level is acceptable for all speed grades of control and address lines.

Figure 5 Signal Overshoot Calculations



Undershoot Example (Figure 6)

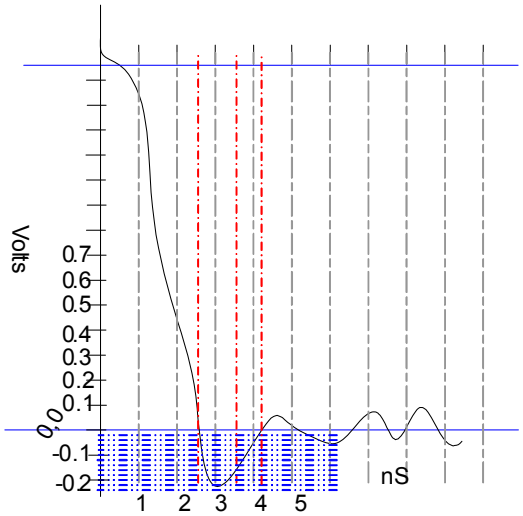
1. Determine amplitude under Vss
2. Determine the duration of the amplitude
3. Calculate the final value

   $US = Amplitude * Duration$

   $US = 215mV * 1.5nS$

   $US = 0.322VnS$
4. Compare results to the applicable SDRAM row and column (Section 2.7.2 paying attention to speed grade and signal type differences). If the SDRAM was DDR3-800 or DDR3-1066 and this were a data net, this overshoot would be acceptable. In the case of DDR3-1333 and DDR3-1600 this level of undershoot is not acceptable. Note: this level is acceptable for control and address lines. Compare results to the applicable SDRAM row and column (notice speed grade differences). This example undershoot is unacceptable for all speed grades for all data, clock, strobe, and mask signals. It is acceptable for all speed grades of address and control signals.

Figure 6 Signal Undershoot Calculations



2.7.3 Typical DDR3 AC & DC Characteristics

Table 9 DDR3 Single-Ended Output Levels

Symbol	Parameter	DDR3-800, 1066, 1333, and 1600	Unit
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.2 x V_{DDQ}	V
$V_{OH(AC)}$	AC output high measurement level (for output SR)	VTT + 0.1 x V_{DDQ}	V
$V_{OL(AC)}$	AC output low measurement level (for output SR)	VTT - 0.1 x V_{DDQ}	V
End of Table 9			

Table 10 DDR3 Differential Output Levels

Symbol	Parameter	DDR3-800, 1066, 1333, and 1600	Unit
V_{OH}diff(AC)	AC differential output high measurement level (for output SR)	+ 0.2 x V_{DDQ}	V
V_{OL}diff(AC)	AC differential output low measurement level (for output SR)	- 0.2 x V_{DDQ}	V
End of Table 10			

2.7.4 DDR3 Tolerances and Noise – Reference Signals

Limitations on DC voltage tolerance and AC noise for all reference voltages is well defined in the applicable JEDEC standard (pg. 129 of JESD79-3C). Strict conformity to these limitations is important to assure proper functionality of the DDR3 SDRAM interface. The Vref tolerance is ±1% or Vdd/2 ±1% which equates to 0.7425 Vdc – 0.7575 Vdc. To achieve this tight tolerance it is recommended (when using a standard resistor divider network) that better then 1% tolerance components be used. The alternative would be an active reference voltage source. Proper component selection and decoupling is critical (see the layout and routing section for additional details).

It is important to properly design the reference supply voltage to track Vdd/Vddq.

3 Package Selection

Individual SDRAMs are available in four different packages that support the various memory device densities, and widths. The following summarizes and describes the primary differences between package and density for common ×8 and ×16 SDRAMs. See Section 8.2 of the Appendix for additional details.

3.1 Summary

The following packaging subsection summarizes at a high level each DDR3 SDRAM configuration and pinout. See the manufacturers data sheets for the latest information.

3.1.1 x4 SDRAM

- Texas Instruments does not support DDR3 SDRAMs in an ×4 configuration.

3.1.2 x8 SDRAM

- 1Gb ×8 devices are compatible in both the 106 and 78 pin packages provided the layout is correct and accounts for the larger package inclusive of the NC (support ball) pin placements. (Note: if designed for the larger package there is no difference in routing required.)
- 1Gb and 2Gb devices are pin compatible in the 106 and 78 pin packages
- The 1Gb, 2Gb, and 4Gb devices are pin compatible in the 78 pin package (Note: other packages not available at the time this document was created)
- 1Gb devices, regardless of package are not compatible between ×16 and ×8 devices, see the respective data sheets for additional details. (Note: It is possible to layout for both ×16 and ×8 devices but this requires additional consideration on switching signals and net attachments which vary between packages. As a general rule, Texas Instruments does not recommend designing the application board for both topologies [×8 & ×16]).
- The twin die version of the 4Gb ×8 SDRAM is not compatible with the monolithic version of the same density.
- The twin die version of the 2Gb ×8 SDRAM is not compatible with the monolithic version of the same density.

3.1.3 x16 SDRAM

- 1Gb and 2Gb ×16 devices are compatible in the 96-pin package. (Note: Some pinouts may change across manufacturers – review data sheets before selecting the DRAMs).
- The twin die version of the 1Gb ×16 SDRAM are not compatible with the monolithic version of the same density.
- The twin die version of the 2Gb ×16 SDRAM are not compatible with the monolithic version of the same density.

3.1.4 x32 SDRAM

- At the time this document was generated no ×32 devices exists. Texas Instruments cannot guarantee functionality or support for ×32 SDRAM devices.

3.1.5 x64 SDRAM

- At the time this document was generated no ×64 devices exists. Texas Instruments cannot guarantee functionality or support for ×64 SDRAM devices.

4 Physical Design and Implementation

4.1 Electrical Connections

This section discusses the proper electrical interface between JEDEC compliant DDR3 SDRAMs and UDIMMs to the Texas Instruments Keystone DSP family DDR3 controller. These sections, in conjunction with Section 8.1 and Section 8.3 of the Appendix provide details for the electrical pin connectivity between the DSP DDR3 interface and DDR3 SDRAM or UDIMM respectively. This is not an all inclusive listing of available parts as DRAM manufacturers are continuously developing higher density parts or obsoleting others. It should also be noted that not all DSPs will have the same width bus – see the data sheet for details. This section assumes both 32- and 64-bit wide buses are used.

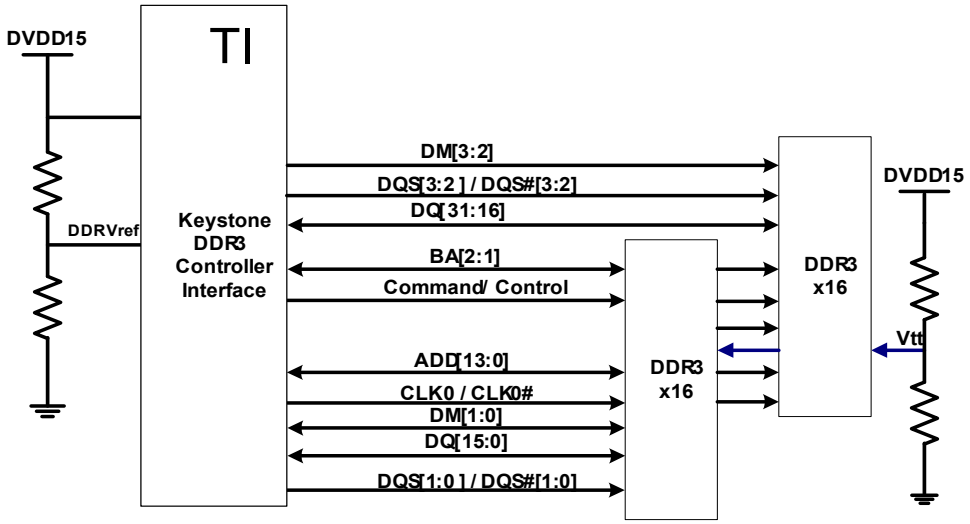
4.1.1 Pin Connectivity & Unused Pins – SDRAM Examples

Correct DDR3 pin connectivity is vital to insure the performance and reliability of the DSP/DRAM system. Tables describing specific pin connectivity for many of the following common SDRAM configurations are included in the appendix to this document.

Note—This is not an all inclusive listing of potential configurations and each should be evaluated based on the guideline provided and good engineering judgement.

This section and the Appendix (Section 8.1) are intended to provide specific details regarding the recommended configuration and connections for used and unused pins on both the SDRAM and DSP DDR3 interfaces. Pin nomenclatures are identified in detail in the respective DSP and SDRAM data sheets and should be confirmed before releasing the design to layout, PCB fabrication, or production. This section does not include specific details for non-JEDEC compliant (JESD79-3C) SDRAM components nor does TI recommend the use of any non-compliant JEDEC SDRAMs.

Figure 7 DSP-to-SDRAM Connection Example



4.1.1.1 Two 16 Meg x 8 x 8 banks (2048Mb total)

The Keystone family of DSPs, unless otherwise specified within the respective data manual, supports two JEDEC compliant DDR3 SDRAMs configured as two 16Meg ×8 ×8 resulting in a total of 2048Mb (256MB) of available memory space. See the data manual and the appendix of this design guide for specific pin connectivity. Where pin designation discrepancies occur, see the individual data manual. It is important also to confirm DRAM pin count and package size. See Section 8.1 Table 26 through Table 29 for connection details. Always verify DSP and SDRAM pinout as well as SDRAM packaging type as pin nomenclature or pin assignment changes.

4.1.1.2 Four 16 Meg x 8 x 8 banks (4096Mb total)

The Keystone family of DSPs, unless otherwise specified within the respective data manual supports four JEDEC compliant DDR3 SDRAMs configured as four 16Meg ×8 ×8 resulting in a total of 4096Mb (512MB) of available memory space. See the data manual and the appendix of this design guide for specific pin connectivity. Where pin designation discrepancies occur, see the individual data manual. It is important also to confirm DRAM pin count and package size. See Section 8.1 Table 30 through Table 33 for connection details. Always verify DSP and SDRAM pinout as well as SDRAM packaging type as pin nomenclature or pin assignment changes.

4.1.1.3 Eight 16 Meg x 8 x 8 banks (8192Mb total)

The Keystone family of DSPs, unless otherwise specified within the respective data manual supports four JEDEC compliant DDR3 SDRAMs configured as eight 16Meg ×8 ×8 resulting in a total of 8192Mb (1024MB) of available memory space. See the data manual and the appendix of this design guide for specific pin connectivity. Where pin designation discrepancies occur, see the individual data manual. It is important also to confirm DRAM pin count and package size. See Section 8.1 Table 34 through Table 37 for connection details. Always verify DSP and SDRAM pinout as well as SDRAM packaging type as pin nomenclature or pin assignment changes.

4.1.1.4 Two 32 Meg x 8 x 8 banks (4096Mb total)

The Keystone family of DSPs, unless otherwise specified within the respective data manual supports two JEDEC compliant DDR3 SDRAMs configured as two 32Meg ×8 ×8 banks resulting in a total of 4096Mb (512MB) of available memory space. See the data manual and the appendix of this design guide for specific pin connectivity. Where pin designation discrepancies occur, see the individual data manual. It is important also to confirm DRAM pin count and package size. See Section 8.1 Table 38 through Table 41 for connection details. Always verify DSP and SDRAM pinout as well as SDRAM packaging type as pin nomenclature or pin assignment changes.

4.1.1.5 Four 16 Meg x 8 x 8 banks x 2 Ranks (4096Mb total)

The Keystone family of DSPs, unless otherwise specified within the respective data manual supports four JEDEC compliant DDR3 SDRAMs configured as four 16Meg ×8 ×8 banks configured as dual rank resulting in a total of 4096Mb (512MB) of available memory space. See the data manual and the appendix of this design guide for specific pin connectivity. Where pin designation discrepancies occur, see the individual data manual. It is important also to confirm DRAM pin count and package size. See Section 8.1 Table 42 through Table 45 for connection details. Always verify DSP and SDRAM pinout as well as SDRAM packaging type as pin nomenclature or pin assignment changes.

4.1.1.6 One 8 Meg x 16 x 8 banks (1024Mb total)

The Keystone family of DSPs, unless otherwise specified within the respective data manual supports one JEDEC compliant DDR3 SDRAM configured as a single 8Meg ×16 ×8 bank and resulting in a total of 1024Mb (128MB) of available memory space. See the data manual and the appendix of this design guide for specific pin connectivity. Where pin designation discrepancies occur, see the individual data manual. It is important also to confirm DRAM pin count and package size. See Section 8.1 Table 46 through Table 49 for connection details. Always verify DSP and SDRAM pinout as well as SDRAM packaging type as pin nomenclature or pin assignment changes.

4.1.1.7 Two 8 Meg x 16 x 8 banks (2048Mb total)

The Keystone family of DSPs, unless otherwise specified within the respective data manual, supports two JEDEC compliant DDR3 SDRAMs configured as a two 8Meg ×16 ×8 banks and resulting in a total of 2048Mb (256MB) of available memory space. See the data manual and the appendix of this design guide for specific pin connectivity. Where pin designation discrepancies occur, see the individual data manual. It is important also to confirm DRAM pin count and package size. See Section 8.1 Table 50 through Table 53 for connection details. Always verify DSP and SDRAM pinout as well as SDRAM packaging type as pin nomenclature or pin assignment changes.

4.1.1.8 Four 8 Meg x 16 x 8 banks (4096Mb total)

The Keystone family of DSPs, unless otherwise specified within the respective data manual, supports four JEDEC compliant DDR3 SDRAMs configured as a four 8Meg ×16 ×8 banks and resulting in a total of 4096Mb (512MB) of available memory space. See the data manual and the appendix of this design guide for specific pin connectivity. Where pin designation discrepancies occur, see the individual data manual. It is important also to confirm DRAM pin count and package size. See Section 8.1 Table 54 through Table 57 for connection details. Always verify DSP and SDRAM pinout as well as SDRAM packaging type as pin nomenclature or pin assignment changes.

4.1.1.9 One 16 Meg x 16 x 8 banks (2048Mb total)

The Keystone family of DSPs, unless otherwise specified within the respective data manual supports one JEDEC compliant DDR3 SDRAM configured as a single 16Meg ×16 ×8 bank and resulting in a total of 2048Mb (256MB) of available memory space. See the data manual and the appendix of this design guide for specific pin connectivity. Where pin designation discrepancies occur, see the individual data manual. It is important also to confirm DRAM pin count and package size. See Section 8.1 Table 58 through Table 61 for connection details. Always verify DSP and SDRAM pinout as well as SDRAM packaging type as pin nomenclature or pin assignment changes.

4.1.1.10 Two 16 Meg x 16 x 8 banks (4096Mb total)

The Keystone family of DSPs, unless otherwise specified within the respective data manual, supports two JEDEC compliant DDR3 SDRAMs configured as two 16Meg ×16 ×8 bank and resulting in a total of 4096Mb (512MB) of available memory space. See the data manual and the appendix of this design guide for specific pin connectivity. Where pin designation discrepancies occur, see the individual data manual. It is important also to confirm DRAM pin count and package size. See Section 8.1 Table 62 through Table 65 for connection details. Always verify DSP and SDRAM pinout as well as SDRAM packaging type as pin nomenclature or pin assignment changes.

4.1.1.11 Four 16 Meg x 16 x 8 banks (8192Mb total)

The Keystone family of DSPs, unless otherwise specified within the respective data manual, supports four JEDEC compliant DDR3 SDRAMs configured as four 16Meg ×16 ×8 bank and resulting in a total of 8192Mb (1024MB) of available memory space. See the data manual and the appendix of this design guide for specific pin connectivity. Where pin designation discrepancies occur, see the individual data manual. It is important also to confirm DRAM pin count and package size. See Section 8.1 Table 66 through Table 69 for connection details. Always verify DSP and SDRAM pinout as well as SDRAM packaging type as pin nomenclature or pin assignment changes.

4.1.2 Pin Connectivity – ECC UDIMM & Non-ECC UDIMM Examples

This section defines the recommended configuration(s) when using a standard DDR3 UDIMM (unbuffered DIMM) with and without EDC (Error Detection & Correction). Additional details pertaining to UDIMM implementation can be found in the JEDEC DDR3 UDIMM standard 21C, the JEDEC UDIMM mechanical standard, MO-269 and the JEDEC socket standard, SO-007B (latest revision). See Section 4.3.2 for additional details pertaining to routing requirements.

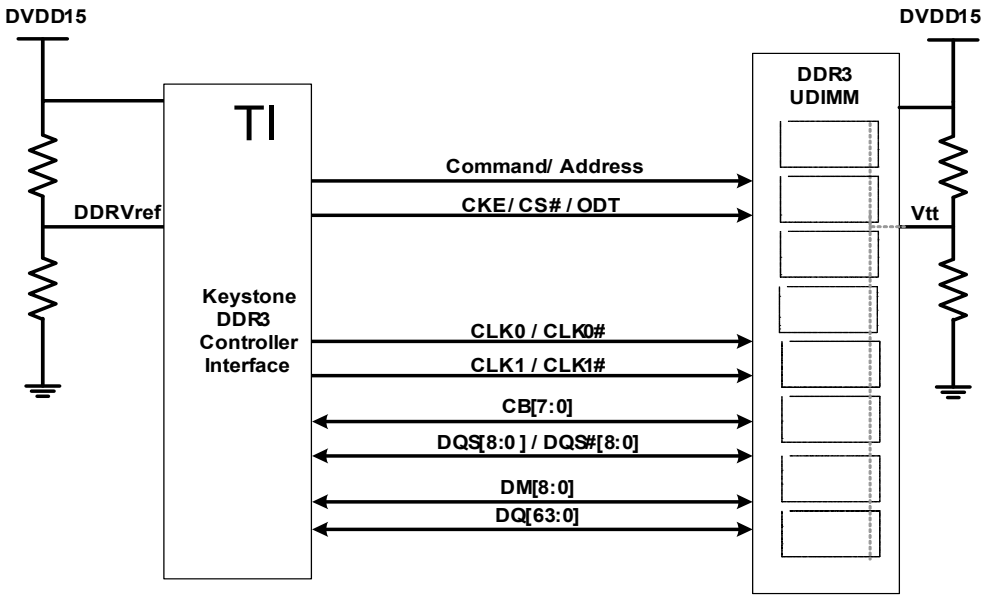
Correct DDR3 pin connectivity is vital to ensure the performance and reliability of the DSP/UDIMM system. Tables describing specific pin connectivity for the following common UDIMM configurations are included in the Appendix to this document.

Note—This is not an all inclusive listing of potential configurations and each should be evaluated based on the guidelines provided and good engineering judgement.

This section and appendix (Section 8.3) are intended to provide specific details regarding the recommended configuration and connections for used and unused pins on both the UDIMM and DSP DDR3 interfaces. Pin nomenclatures are identified in detail in the respective DSP and UDIMM data sheets and should be confirmed before releasing the design to layout, PCB fabrication, or production. This section does not include specific details for non-JEDEC compliant UDIMMs nor does TI recommend the use of any non-compliant JEDEC UDIMMs.

Figure 8 illustrates the basic interconnection between the TI KeyStone DSP and respective UDIMM.

Figure 8 DSP to UDIMM Connection



The following two tables define the pinout for a standard ECC x72 and a non-ECC x64 UDIMM. See the actual data sheet for specific pin nomenclatures and connectivity requirements. The pinouts listed support both a single and dual rank UDIMMs.

Table 11 Standard ECC x 72 UDIMM Pin Assignments (Part 1 of 2)

Pin #	Front	Pin #	Back	Pin #	Front	Pin #	Back	Pin #	Front	Pin #	Back
1	VrefDQ	121	Vss	46	CB3	166	Vss	91	DQ41	211	Vss
2	Vss	122	DQ4	47	Vss	167	NU	92	Vss	212	DM5
3	DQ0	123	DQ5	48	NC	168	RESET#	93	DQS5#	213	NC
4	DQ1	124	Vss	49	NC	169	CKE1	94	2.26	214	Vss
5	Vss	125	DM0	50	CKE0	170	Vdd	95	Vss	215	DQ46
6	DQS0#	126	NC	51	Vdd	171	NF	96	DQ42	216	DQ47
7	DQS0	127	Vss	52	BA2	172	NF/A14	97	DQ43	217	Vss
8	Vss	128	DQ6	53	NC	173	Vdd	98	Vss	218	DQ52
9	DQ2	129	DQ7	54	Vdd	174	A12	99	DQ48	219	DQ53
10	DQ3	130	Vss	55	A11	175	A9	100	DQ49	220	Vss
11	Vss	131	DQ12	56	A7	176	Vdd	101	Vss	221	DM6
12	DQ8	132	DQ13	57	Vdd	177	A8	102	DQS6#	222	NC
13	DQ9	133	Vss	58	A5	178	A6	103	DQS6	223	Vss
14	Vss	134	DM1	59	A4	179	Vdd	104	Vss	224	DQ54
15	DQS1#	135	NC	60	Vdd	180	A3	105	DQ50	225	DQ55
16	DQS1	136	Vss	61	A2	181	A1	106	DQ51	226	Vss
17	Vss	137	DQ14	62	Vdd	182	Vdd	107	Vss	227	DQ60
18	DQ10	138	DQ15	63	CK1	183	Vdd	108	DQ56	228	DQ61
19	DQ11	139	Vss	64	CK1#	184	CK0	109	DQ57	229	Vss
20	Vss	140	DQ20	65	Vdd	185	CK0#	110	Vss	230	DM7
21	DQ16	141	DQ21	66	Vdd	186	Vdd	111	DQS7#	231	NC

Table 11 Standard ECC x 72 UDIMM Pin Assignments (Part 2 of 2)

Pin #	Front	Pin #	Back	Pin #	Front	Pin #	Back	Pin #	Front	Pin #	Back
22	DQ17	142	Vss	67	VrefCA	187	EVENT#	112	DQS7	232	Vss
23	Vss	143	DM2	68	NC	188	A0	113	Vss	233	DQ62
24	DQS2#	144	NC	69	Vdd	189	Vdd	114	DQ58	234	DQ63
25	DQS2	145	Vss	70	A10	190	BA1	115	DQ59	235	Vss
26	Vss	146	DQ22	71	BA0	191	Vdd	116	Vss	236	Vddspd
27	DQ18	147	DQ23	72	Vdd	192	RAS#	117	SA0	237	SA1
28	DQ19	148	Vss	73	WE#	193	S0#	118	SCL	238	SDA
29	Vss	149	DQ28	74	CAS#	194	Vdd	119	SA2	239	Vss
30	DQ24	150	DQ29	75	Vdd	195	ODT0	120	Vtt	240	Vtt
31	DQ25	151	Vss	76	S1#	196	A13				
32	Vss	152	DM3	77	ODT1	197	Vdd				
33	DQS3#	153	NC	78	Vdd	198	NC				
34	DQS3	154	Vss	79	NC	199	Vss				
35	Vss	155	DQ30	80	Vss	200	DQ36				
36	DQ26	156	DQ31	81	DQ32	201	DQ37				
37	DQ27	157	Vss	82	DQ33	202	Vss				
38	Vss	158	CB4	83	Vss	203	DM4				
39	CB0	159	CB5	84	DQS4#	204	NC				
40	CB1	160	Vss	85	DQS4	205	Vss				
41	Vss	161	DM8	86	Vss	206	DQ38				
42	DQS8#	162	NC	87	DQ34	207	DQ39				
43	DQS8	163	Vss	88	DQ35	208	Vss				
44	Vss	164	CB6	89	Vss	209	DQ44				
45	CB2	165	CB7	90	DQ40	210	DQ45				
End of Table 11											

Table 12 Standard Non-ECC x 64 UDIMM Pin Assignments (Part 1 of 2)

Pin #	Front	Pin #	Back	Pin #	Front	Pin #	Back	Pin #	Front	Pin #	Back
1	VREFDQ	121	VSS	46	NC	166	VSS	91	DQ41	211	VSS
2	VSS	122	DQ4	47	VSS	167	NC	92	VSS	212	DM5
3	DQ0	123	DQ5	48	NC	168	RESET#	93	DQS5#	213	NC
4	DQ1	124	VSS	49	NC	169	CKE1	94	DQS5	214	VSS
5	VSS	125	DM0	50	CKE0	170	VDD	95	VSS	215	DQ46
6	DQS0#	126	NC	51	VDD	171	NC	96	DQ42	216	DQ47
7	DQS0	127	VSS	52	BA2	172	NC/A141	97	DQ43	217	VSS
8	VSS	128	DQ6	53	NC	173	VDD	98	VSS	218	DQ52
9	DQ2	129	DQ7	54	VDD	174	A12	99	DQ48	219	DQ53
10	DQ3	130	VSS	55	A11	175	A9	100	DQ49	220	VSS
11	VSS	131	DQ12	56	A7	176	VDD	101	VSS	221	DM6
12	DQ8	132	DQ13	57	VDD	177	A8	102	DQS6#	222	NC
13	DQ9	133	VSS	58	A5	178	A6	103	DQS6	223	VSS
14	VSS	134	DM1	59	A4	179	VDD	104	VSS	224	DQ54
15	DQS1#	135	NC	60	VDD	180	A3	105	DQ50	225	DQ55

Table 12 Standard Non-ECC x 64 UDIMM Pin Assignments (Part 2 of 2)

Pin #	Front	Pin #	Back	Pin #	Front	Pin #	Back	Pin #	Front	Pin #	Back
16	DQS1	136	VSS	61	A2	181	A1	106	DQ51	226	VSS
17	VSS	137	DQ14	62	VDD	182	VDD	107	VSS	227	DQ60
18	DQ10	138	DQ15	63	CK1	183	VDD	108	DQ56	228	DQ61
19	DQ11	139	VSS	64	CK1#	184	CK0	109	DQ57	229	VSS
20	VSS	140	DQ20	65	VDD	185	CK0#	110	VSS	230	DM7
21	DQ16	141	DQ21	66	VDD	186	VDD	111	DQS7#	231	NC
22	DQ17	142	VSS	67	VREFCA	187	NC	112	DQS7	232	VSS
23	VSS	143	DM2	68	NC	188	A0	113	VSS	233	DQ62
24	DQS2#	144	NC	69	VDD	189	VDD	114	DQ58	234	DQ63
25	DQS2	145	VSS	70	A10	190	BA1	115	DQ59	235	VSS
26	VSS	146	DQ22	71	BA0	191	VDD	116	VSS	236	VDDSPD
27	DQ18	147	DQ23	72	VDD	192	RAS#	117	SA0	237	SA1
28	DQ19	148	VSS	73	WE#	193	S0#	118	SCL	238	SDA
29	VSS	149	DQ28	74	CAS#	194	VDD	119	SA2	239	VSS
30	DQ24	150	DQ29	75	VDD	195	ODT0	120	VTT	240	VTT
31	DQ25	151	VSS	76	S1#	196	A13				
32	VSS	152	DM3	77	ODT1	197	VDD				
33	DQS3#	153	NC	78	VDD	198	NC				
34	DQS3	154	VSS	79	NC	199	VSS				
35	VSS	155	DQ30	80	VSS	200	DQ36				
36	DQ26	156	DQ31	81	DQ32	201	DQ37				
37	DQ27	157	VSS	82	DQ33	202	VSS				
38	VSS	158	NC	83	VSS	203	DM4				
39	NC	159	NC	84	DQS4#	204	NC				
40	NC	160	VSS	85	DQS4	205	VSS				
41	VSS	161	NC	86	VSS	206	DQ38				
42	NC	162	NC	87	DQ34	207	DQ39				
43	NC	163	VSS	88	DQ35	208	VSS				
44	VSS	164	NC	89	VSS	209	DQ44				
45	NC	165	NC	90	DQ40	210	DQ45				

End of Table 12

4.1.2.1 ECC UDIMM Connectivity – One 4Gb Module

Details for connectivity between the DDR3 interface on the Keystone DSPs and a standard 240 pin ×72 ECC dual rank UDIMM are provided in greater detail in Appendix Section 8.3. The specific details provided for in the Appendix are for interconnection to a single 4Gb 240-pin ECC UDIMM. Texas Instruments always recommends verifying specific pinouts of both the UDIMM selected and the DSP before proceeding to design layout, fabrication, and production. Configuration as indicated will support one single or dual rank UDIMM.

4.1.2.2 Non-ECC UDIMM Connectivity – One 4Gb Module

Details for connectivity between the DDR3 interface on the Keystone family of DSPs and standard 240 pin ×64 non-ECC UDIMM are provided in defined in greater detail in Appendix Section 8.3. The specific details provided for in the Appendix are for interconnection to a single 4Gb 240-pin non-ECC UDIMM. Texas Instruments always recommends verifying specific pinouts of both the UDIMM selected and the DSP before proceeding to design layout, fabrication, and production. Configuration as indicated will support one single or dual rank UDIMM.

4.2 Signal Terminations (External & Internal)

The following subsection describes the two signal termination methods (Leveling and non-leveling) used for DDR3 interfaces, specific termination placement, and the impact of incorrect termination schemes and component values. Terminations are placed at the end of the signal path. In the current "Fly-by" architecture placing the terminations at the last SDRAM improves the overall signal characteristics which is an improvement over previous DDR2 SDRAM topology.

4.2.1 External Terminations – When Using Read & Write Leveling

As a rule of thumb, terminations should be applied to all clock, address, and control lines. Although all address, control, and command lines should be end terminated when using leveling, clocking nets may require different termination values than that used on the command and address nets. Each respective address and command net should be end terminated using a parallel termination resistor (in the range of 40Ω – 42Ω) and connected to Vtt (preferred value is 39Ω 1%). Vtt is defined as Vddq/2 or 0.75 Vdc. The DDR3 clock nets also must be end terminated. However, instead of end terminating the clock nets (DDRCLKOUTP/Nx where x is DDRCLKOUTP/N0 or DDRCLKOUTP/N1, whichever is used) each net shall be terminated with a series 39 ohm 1% resistor to a 0.1µF capacitor to DVDD15 (VDDq). Figure 2 (and respective notes) illustrate the required clock termination implementation. All components should be 1% tolerance or better. Vtt should be generated using a resistor divider network (1% tolerance or better). For proper operation the Vtt termination must track VDDq/2.

Again, an important point is that the parallel termination should be placed at the last SDRAM in the fly-by or daisy-chained architecture. Each trace to the respective termination should be ≤ within 500 mils and the opposite side of the termination resistor should tie directly to the Vtt rail.

External terminations may not be required – the only way to determine if your topology requires end terminations is to perform complete simulations inclusive of all topology parasitics.

Note—IMPORTANT: All Vtt terminations should be placed at the end of the transmission line (net), incorrect placement will have an impact on performance and functionality.

4.2.2 External Terminations – When Read & Write Leveling is Not Used

Texas Instruments does not recommend the use of DDR3 without leveling. The use of DDR3 SDRAMs without read and write leveling places an undue burden and constraints on the physical design and topology. In essence, any DDR3 design not making use of read and write leveling becomes nothing more than a DDR2 layout with all of the negative implications associated with DDR2 and none of the benefits of DDR3 (except possibly speed).

4.2.3 Internal Termination – On Die Terminations

Prior DSPs supporting DDR2 interfaces did not support ODT, whereas the Keystone family of DSPs now supports ODT (on die terminations). One of the primary advantages to using DDR3 is the fact that the data lines no longer require series terminations to optimize signal overshoots and undershoots. The current DDR3 instantiation allows for a wider range of values, additionally DDR3 now support dynamic ODT which has enormous benefits in a complex application board topology. In DDR3, the DSP controller ODT pins (connected to each SDRAM) serve to turn on or off the SDRAM internal termination. The actual ODT functionality of each SDRAM is controlled using the mode registers (see the respective SDRAM data sheets for additional information).

In most all cases, Texas Instruments recommends the use of dynamic ODT (see the DSP data sheet for final confirmation).

4.2.4 Active Terminations

Active terminations, regardless of configuration are not required. The combination of TI's new DSP controller and the new DDR3 DRAM architecture in the supported configurations eliminates the need for active terminations.

4.2.5 Passive Terminations

Unlike DDR2, the addition of series passive components is no longer necessary when using DDR3 (with leveling). The only passive terminations to be used (when using DDR3 with leveling) are the end termination pull up resistors identified in Section 6.1.2.

4.2.6 Termination Component Selection

All termination components shall be 1% tolerance, component size (form factor) will be dependent upon power requirements and parasitics. Texas Instruments recommends 0402 size discrete (passive) components to improve routing, and reduce parasitic inductance.

4.3 Mechanical Layout and Routing Considerations

This subsection defines the basic requirements regarding mechanical layout and PCB routing. These are general guidelines which when followed in conjunction with the remainder of sections in this design guide (and good engineering practices) will guarantee a functional DDR3 interface. In all cases it is recommended that the DDR3 interface be modeled to verify functionality and performance.

4.3.1 SDRAMs Details

This subsection describes the specific requirements for discrete SDRAM implementations.

4.3.1.1 Mechanical Layout – SDRAMs

This subsection shall provide basic information regarding mechanical DDR3 → DSP layout constraints. Included are such topics as routing, stack up, trace lengths, and the use of net classes. Issues not covered (in any great detail) within this document include thermal considerations, part density, pick and place problems, and different packages / footprints. 'Depending on the number of SDRAM's utilized, they can be placed on opposite sides of the PCB. However, stub lengths are an important factor to consider - excessive stub lengths or misplaced vias will have a significant impact on performance including signal integrity.

This document assumes that the user has an above average level of understanding regarding mechanical layout and design – including the impact of trace width, spacing, via size, bulk and decoupling capacitance selection and placement.

4.3.1.2 Stack Up – SDRAMs

Stack up refers to the mechanical layer assembly of the printed circuit board. In all high speed designs it is good practice to maintain symmetry between the top half of the board and the bottom half. Referencing (sandwiching) high signal layers containing high speed signals between power planes reduces EMI problems and provides for a reduced resistive path to the respective plane. Power and ground planes should be solid planes (without breaks)

Proper stack up must also include the proper characteristic printed circuit board (pcb) impedance. Most DSPs' respective application board systems require a pcb impedance of 50Ω.

Board thicknesses depend on end use application, a typical stack-up to support a DDR3 implementation requires a minimum of four routing layers (less if a reduced subset of DSP peripherals are used).

4.3.1.3 Routing Rules – General Overview – SDRAMs

Several key points to remember when routing any signals on the application board:

- Organize the power, ground, and signal planes so that you eliminate or significantly reduce the number of split / cut planes present in the design (No splits are allowed under any DDR3 routes).
- Do not allow for high-speed signals to cross broken or cut planes.
- Apply net classes, e.g., group key signals together.
- Maintain an acceptable level of skew across the entire DDR3 interface (by net class).
- Utilize proper low-pass filtering on the Vref pins.
- Follow the Fly-By architecture concept for all address and control lines.
- Increase the size of the decoupling capacitor trace width as large as possible, key the stub length as short as possible.
- Add additional spacing for on-clock and strobe nets to eliminate crosstalk.
- Maintain a common ground reference for all bypass/decoupling capacitors, DSP, and SDRAMs.
- Take into account the differences in propagation delays between Microstrip and stripline nets when evaluating timing constraints.

- All numbers provided are based on an equivalent stripline length. An equivalent stripline length is defined as the length of a stripline trace that will have the same delay as your nets. {e.g., 1" microstrip + 1" stripline → 1.8" of equivalent stripline should your trace be routed on different layers. ((140pS + 176pS)/176pS) → 1.8"}. Note: Figures provided are based on a fixed dielectric constant that may change depending on PCB material selected.
- There can not be any mid point vias in the design or vias that are located on the respective net that will impact signal integrity, it is strongly recommended that all nets be simulated to assure proper design, performance, and signal integrity.
- Where possible all vias should be blind or buried. Where blind or buried vias are not possible, back drilling vias is strongly recommended to eliminate any stubs. If stubs must be included in the design, then the stub length must be taken into account with regards to layout, component placement, performance, and signal integrity.
- It is strongly recommended that the routing channels between the DSP to SDRAM be dedicated solely to the SDRAM interface and that no other signals be routed in the area. If other signals are required to be routed on same layers there should be adequate spacing to any SDRAM nets (> ×4 spacing) and that the entire interface be models with respect to signal integrity to assure no problems exist.

Net classes are an important concept when routing high speed signals that incorporate timing constraints or timing relationships. When routing the DDR3 nets, there are four basic groups (net classes) to consider – Table 13 establishes the recommended net classes:

Table 13 SRAM Net Class Routing Rules

Net Class	Signals	Notes
Data	DQS[8:0], DQS#[8:0], DQ[n:0], CB[7:0]	1, 2, 4
Address/Command	BA[2:0], A[n:0], Command lines	2, 3
Control	CSn (DDRCEnz), CKEn, ODTn, RESET#	2
Clock	CK and CK#; DDRCLKOUTP/N	
Note 1: CB[7:0] refer to ECC devices Note 2: "n" refers to some number of lines and is dependent upon device selected Note 3: Command refers to command inputs including RAS#, CAS#, WE# signal lines. Note 4: Observe relationship between DQ,DQS, DQS#, DDRCLKOUT, and DDRCLKOUT#		

4.3.1.4 Routing Rules –Address Lines (SDRAMs)

A general rule when routing address nets is that they should be referenced to either a solid power (i.e., 1.5V DDR3 SDRAM power plane or VDDq) or ground plane – the preferred selection would be a solid ground plane. Referencing the entire address bus to the ground plane provides a low impedance current return path. During the routing of the DSP to DDR3 address lines it is strongly suggested that the entire address bus be routed away from the data bus/nets.

Maximum trace length for any address net should not exceed 4.5 inches (114.3mm), all address nets should be skew matched to within ±20 mils (0.50mm) of the DSP clock out to SDRAM length. (Note: fly-by topologies will be slightly longer.) The recommended trace-to-trace spacing (for address-to-address nets) should be no less then 12 mils (0.300mm). The recommended trace-to-trace spacing (for address to other nets) should be no less then 20 mils (0.50mm).

Note—Fly-by topology skew matching for address and command nets must be skew matched per segment in addition to the entire net.

All address and command net classes shall be skew matched to respective clock lines to within CLK ±20 mils (1.00mm).

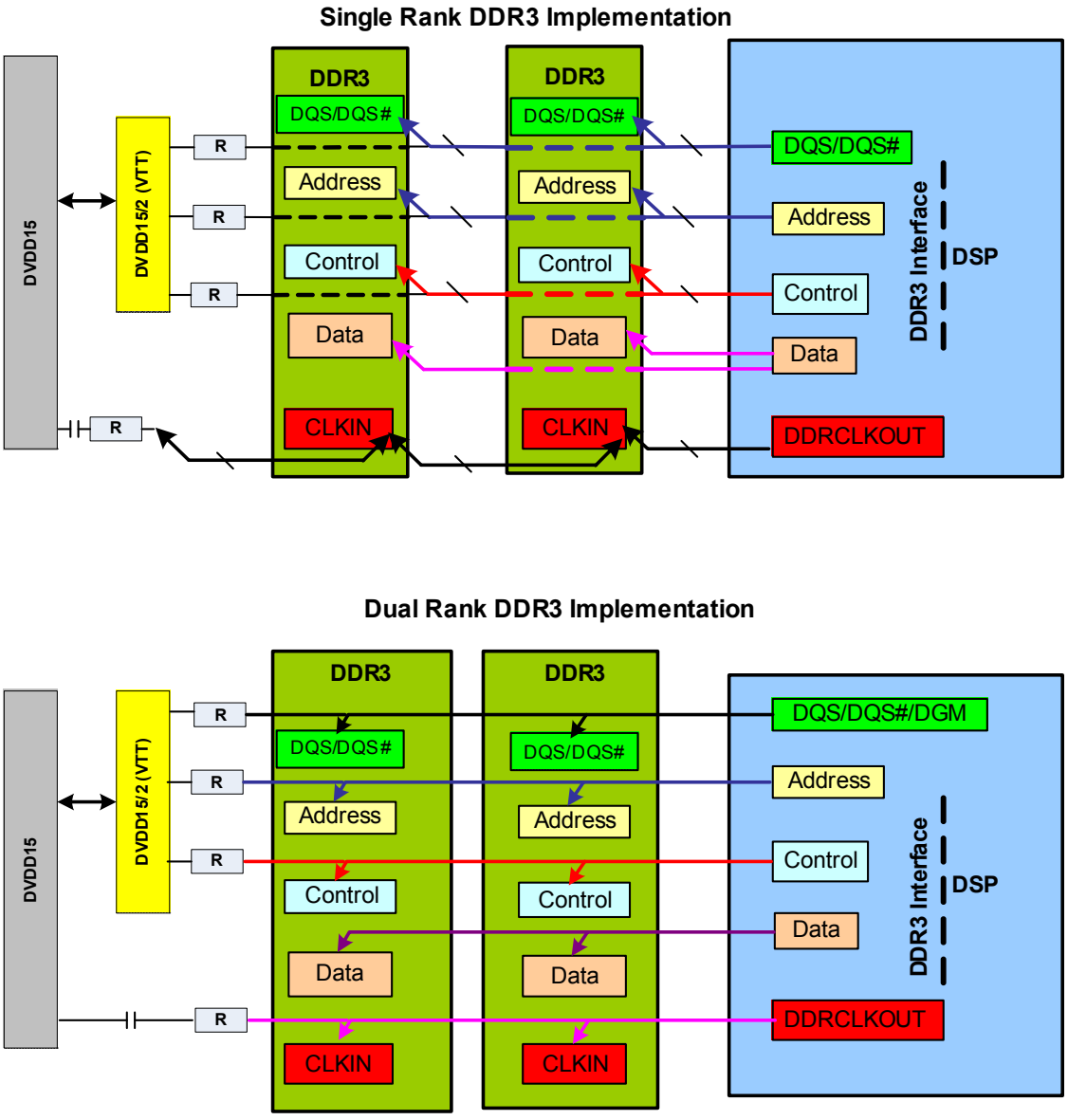
4.3.1.5 Routing Rules – Control Lines – (SDRAMs)

Similar to the address signals, the control signals must be referenced to a solid plane (ground or power - power is preferred). Both control and address lines must be aligned or referenced to the adjacent plane for optimal operation. Maintaining this reference assures a low-z return current path.

The control lines are designed to be routed from the DSP directly to the DRAM (point-to-point). This is different than the address lines which are designed to be routed in a "fly-by" configuration. All control signals must be routed clear of the data signals to prevent cross coupling.

All control group signals (Figure 9) should be skew matched to within ±20 mils (1.00mm).

Figure 9 Control Group Signals



4.3.1.6 Routing Rules – Data Lines – [SDRAMs]

The DDR3 SDRAM architecture differs from the previous DDR2 SDRAMs with regards to collection of data by the SDRAM. In previous DDR2 designs the clock was used to set up and capture the data in memory, in DDR3 SDRAMs the DQS and DQS# (data strobes) are now used (instead of the clock). Both the data strobe (DQS) and its complementary signal (DQS#) must be routed as a differential pair. All data lines must be of matched length to the data strobe lines. As with the address, control, and clock lines the high-speed data lines must have a good return path to assure proper signal integrity and to minimize the effect of the added inductance (found in poor signal return paths). Where the address and control lines are better referenced to a power or ground plane (solid), the data lines must be referenced to a solid ground plane.

The optimal design and layout embodiment for the data lines would be all nets routed on the top layer (adjacent to a solid / full ground plane) and should not contain any vias at all. Should the design or topology dictate the use of vias, the impact of each via and the added delays induced by them must be taken into account with respect to trace length. Vias on an average can add between 8 to >20pS of propagation delays, depending highly on the size, parasitics, and number of layers it connects between. (Simulation and modeling high performance interfaces is strongly recommended).

Total length from DSP to each SDRAM for all respective DQ and DM signals within a byte lane should be skew matched to the DQS line ± 10.00 mils (0.50 mm). DQS to DQS# skew shall be ≤ 10.00 mils (0.254mm).

Table 14 Data and Data Strobe Byte Lane Grouping

DATA	DATA STROBE	DATA $\overline{\text{STROBE}}$	DATA MASK
DQ[7:0]	DQS0	DQS0#	DM0
DQ[15:8]	DQS1	DQS1#	DM1
DQ[23:16]	DQS2	DQS2#	DM2
DQ[31:24]	DQS3	DQS3#	DM3
DQ[39:32]	DQS4	DQS4#	DM4
DQ[47:40]	DQS5	DQS5#	DM5
DQ[55:48]	DQS6	DQS6#	DM6
DQ[63:56]	DQS7	DQS7#	DM7
CB[7:0]	DQS8	DQS8#	DM8

End of Table 14

4.3.1.7 Routing Rules – Clock Lines [SDRAMs]

Data strobe lines are used set up and capture data in the current DDR3 implementation. However it is the respective memory clocks CK & CK# that the SDRAM use to capture both the control and address data. The DDR3 clock lines should not be terminated to Vddg/2 (Vtt) – all DDR3 input clocks are differential by design and should be routed as a differential pair. Clock source and clocking terminations depend highly on the nature of the source – see the Hardware Design Guide for recommended termination schemes.

The differential clock source (unless otherwise specified in the data sheets) must be matched length to within ±10.0 mils (0.254mm) between complementary lines. All differential clocks must be routed in parallel and the spacing between the differential pairs should be a minimum 2 times (2×) the trace width. The maximum clock trace length should not exceed 4 inches (5 depending on topology).

It is recommended that the differential clock signals be slightly longer than the control and address lines – this is due to the fact that differential signals have an inherently faster propagation time than the single-ended address and control pins. The differential clock lines can have up to a 12pS faster propagation time per 1000 mils (25.4mm) over a single ended control or address net assuming the same IO buffer and drive strength are used.

CLK and CLK# nets correspond to the DDRCLKOUTP/N on the DSP.

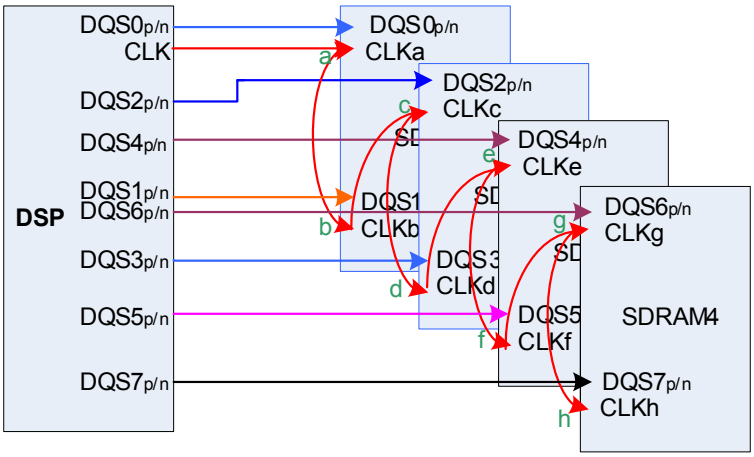
During layout it is imperative that the DSP DQS, DQS#, and DDRCLKOUTP/N lines retain the same relationship between the DSP and respective byte lane.

As an example, the length for each leg of a hop must be a similar ratio. In most cases the DDRCLKOUTP/N nets will be longer due to the point-to-multipoint topology, whereas the DQ and DQS/# nets are a point-to-point topology and therefore typically shorter. Because of this inherent design limitation, the DQ, DQS, DQS# nets should always be shorter then the corresponding DDRCLKOUT hop.

Using the following figure, clock net "a" must be a longer length than DQS0, clock net "b" (total length including clock length "a") must be longer than the total length of DQS1, clock length "c" (total length including clock length "a"+"b") must be close to the length of DQS1 and so on.

Figure 10 illustrates the required DDRCLKOUT and DQ/DQS/# routing from the DSP to SDRAM(s).

Figure 10 DDRCLKOUT and DQ/DQS/# Routing from the DSP to SDRAM(s)



4.3.1.8 Routing Rules – Power (SDRAMs)

When routing the DDR3 SDRAM Vref voltages, it is necessary to decouple them at the SDRAMs and not at the source. The use of 0.01µF and 0.1µF ceramic capacitors (0402 or smaller recommended) should be distributed across the Vref power rail with one 0.01µF and 0.1µF ceramic capacitor located at each Vref pin and one 0.1µF capacitor directly at the source. Traces between the decoupling capacitors and Vref pins should be a minimum of 30 mils (0.762mm) wide and as short as possible. The Vref pins and interconnection to decoupling capacitors should maintain a minimum of 15 mils (0.381mm) spacing from all other nets. All Vref nets should be routed on the top layer. Vref pins should be isolated with or shielded with ground.

When routing the SDRAM Vtt power supply the regulator should be kept as close to the Vtt pin on the respective SDRAMs. In most cases a Vtt voltage island will be used, in most cases it is recommended that the voltage island be placed on the component side signal layer. There should be a minimum of one 0.1µF decoupling capacitor close to each Vtt SDRAM pin and a minimum of one 10 – 22µF bulk ceramic (low ESR) capacitor on the Vtt island. The number of Vtt bulk capacitors is based on the size of island and topology, and loading.

4.3.1.9 Round-Trip Delay Impact on Routing

The leveling processes in the DDR3 interface impose an upper limit on the maximum round-trip delay. If this limit is exceeded, the DDR3 interface fails the leveling process and data corruption occurs. This limit is sufficiently large that well-controlled topologies will never exceed this limit.

The round-trip delay for a given SDRAM is defined as the sum of two delays. The first is the longest delay for the clock, command, control, and address groups to that SDRAM. The second is the delay for the data group to that same SDRAM. This round-trip delay must be calculated for each byte-lane to each SDRAM device implemented in the DDR3 memory topology, including SDRAM devices on DIMM. All of these individual sums must be below the limit to guarantee robust operation.

Internally, the DDR3 controller logic has a theoretical upper limit of 4 clock cycles. There are multiple processes that have variation terms that reduce this time window, as listed below:

- $ddrclkout_{period}$ – period of reference clock the DSP is providing to SDRAM
- *tDQSCK* - DQS to CK skew limit from SDRAM datasheet – this is stated for each standard speed grade in the JEDEC DDR3 SDRAM standard
- Invert Clock Out - delay of half a clock cycle if enabled – option normally only used in very small memory topologies
- *adjustment_sum* - sum which accounts for all of the leveling errors, buffer delays, and jitter terms associated with the circuitry and the leveling adjustment – upper limit defined to be half a clock period plus 225ps

The following equation provides an approximation of the maximum round trip delay:

- Case 1: Invert Clock Out disabled
  - $round\_trip_{delay} < (4 * ddrclkout_{period})$ - tDQSCK - adjustment_sum
  - $round\_trip_{delay} < (4 * ddrclkout_{period})$ - tDQSCK - $0.5 * ddrclkout_{period}$ - 225ps
  - $round\_trip_{delay} < (3.5 * ddrclkout_{period})$ - *tDQSCK - 225ps*
- Case 2: Invert Clock Out enabled (adds an additional half-clock period of delay to the command delay term)
  - $round\_trip_{delay} < (4 * ddrclkout_{period})$ - tDQSCK - $0.5 * ddrclkout_{period}$ - adjustment_sum
  - $round\_trip_{delay} < (4 * ddrclkout_{period})$ - tDQSCK - $0.5 * ddrclkout_{period}$ - 0.5 * drclkoutperiod - 225ps
  - $round\_trip_{delay} < (3 * ddrclkout_{period})$ - tDQSCK - 225ps

Based on the previous equations, the following calculations and summary table show the write leveling skew limitations for both 'Invert Clock Out' enabled and disabled, given the DDR3-1333 and DDR3-1600 JEDEC SDRAM specification. The first column for each speed-grade category lists the maximum write leveling skew in picoseconds. The second column for each lists the maximum write leveling skew into inches assuming a signal propagation rate of 180ps/in.

For DDR3-1333:

- $ddrclkout_{period}$ = 1500ps
- tDQSCK = +/-255ps

- margin = 100ps

  Case 1: Invert Clock Out disabled
  - $round\_trip_{delay} < (3.5 * ddrclkout_{period}) - tDQSCK - 225ps$
  - $round\_trip_{delay} < (3.5 * 1500ps) - 255ps - 225ps$
  - $round\_trip_{delay} < 4770ps$

  Case 2: Invert Clock Out enabled (adds an additional half-clock period of delay to the command delay term)
  - $round\_trip_{delay} < (3 * ddrclkout_{period}) - tDQSCK - 225ps$
  - $round\_trip_{delay} < (3 * 1500ps) - 255ps - 225ps$
  - $round\_trip_{delay} < 4020ps$

For DDR3-1600:

- $ddrclkout_{period}$ = 1250ps
- tDQSCK = +/-225ps
- margin = 100ps

  Case 1: Invert Clock Out disabled
  - $round\_trip_{delay} < (3.5 * ddrclkout_{period}) - tDQSCK - 225ps$
  - $round\_trip_{delay} < (3.5 * 1250ps) - 225ps - 225ps$
  - $round\_trip_{delay} < 3925ps$

  Case 2: Invert Clock Out enabled (adds an additional half-clock period of delay to the command delay term)
  - $round\_trip_{delay} < (3 * ddrclkout_{period}) - tDQSCK - 225ps$
  - $round\_trip_{delay} < (3 * 1250ps) - 225ps - 225ps$
  - $round\_trip_{delay} < 3300ps$

Table 15 shows the round trip delay limitations for both "Invert Clock Out" enabled and disabled. The first column for each lists the maximum round-trip delay in picoseconds. The second column for each lists the maximum routing length in inches assuming a signal propagation rate of 180 ps/in.

Table 15 Maximum Round Trip Delay Example - "Invert Clock Out" Enabled & Disabled

	Invert Clock Out Disabled		Invert Clock Out Enabled	
DDR3-1333	4770 ps	26.50 in	4020 ps	22.33 in
DDR3-1600	3925 ps	21.81in	3300 ps	18.33 in

Because this is preliminary guidance and some small margin should be subtracted from these delays to account for additional terms such as multi-rank delay skew, TI recommends that the maximum routing lengths be reduced by 10%.

4.3.1.10 Write Leveling Limit Impact on Routing

The write leveling process in the DDR3 interface imposes a limit on the maximum and minimum skew between the command delay and the data delay. If these limits are exceeded, the DDR3 interface fails the write leveling process and data corruption occurs. These limits are sufficiently large that well-controlled topologies will never exceed this limit.

The command delay is defined as delay for the clock, command, control, and address group signals from the DSP to a given SDRAM. The data delay is the delay for the data group signals to that same SDRAM. The write leveling result is effectively the difference, or skew, between these two delays.

The maximum write leveling skew is the largest difference between the two delays in the topology to a single SDRAM. Likewise, the minimum write leveling skew is the smallest difference between the two delays in the topology to a single SDRAM.

The write leveling logic has a theoretical upper limit of 2500ps. This limit does not scale with SDRAM data rate. The theoretical upper limit equates to two full clock cycles when the clock frequency is 800 MHz for DDR3-1600. It is reduced by half a clock cycle when 'Invert Clock Out' is enabled as this effectively lengthens the clock by this amount.

The following set of equations provides an approximation of the maximum and minimum write leveling skew allowed:

- $ddrclkout_{period}$ - period of reference clock the DSP is providing to SDRAM
- *tWLS* - from JEDEC DDR3 SDRAM specification, Write Leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing
- *tJIT(per, lck)* - Clock Period Jitter during DLL locking period
- $command_{delay}$ - delay for the clock, command, control and address group signals from the DSP to a given SDRAM
- $data_{delay}$ - delay for the data group signals to that same SDRAM
- $write\_leveling_{skew}$ - defined as the value $command_{delay}$ - $data_{delay}$
- *margin* - additional margin added for preliminary use

Maximum Write Leveling Skew:

- Case 1: Invert Clock disabled
  - $write\_leveling_{skew} < 2500ps - tWLS - tJIT(per, lck) - margin$
- Case 2: Invert Clock enabled (adds an additional half-clock period of delay to the command delay term)
  - $command_{delay} + (0.5 * ddrclkout_{period}) - data_{delay} = write\_leveling_{skew} < 2500ps - tWLS - tJIT(per, lck) - margin$
  - $write\_leveling_{skew} < 2500ps - tWLS - tJIT(per, lck) - (0.5 * ddrclkout_{period}) - margin$

Minimum Write Leveling Skew:

- Case 1: Invert Clock disabled
  - $write\_leveling_{skew} > tWLS + tJIT(per, lck) + margin$
- Case 2: Invert Clock enabled (adds an additional half-clock period of delay to the command delay term)
  - $command_{delay} + (0.5 * ddrclkout_{period}) - data_{delay} = write\_leveling_{skew} > tWLS + tJIT(per, lck) + margin$
  - $write\_leveling_{skew} > tWLS + tJIT(per, lck) - (0.5 * ddrclkout_{period}) + margin$

tWLS and tJIT(per, lck) are standard JEDEC DDR3 SDRAM timing parameters which can be gathered from the specific datasheet of the SDRAM chosen.

Note—Because this is preliminary guidance some small margin should be subtracted from these delays to account for additional terms such as multi-rank delay skew. TI currently recommends setting the extra 'margin' term to 100ps.

Based on the previous equations, the following calculations and summary table shows the write leveling skew limitations for both 'Invert Clock Out' enabled and disabled given the DDR3-1333 and DDR3-1600 JEDEC SDRAM specification. The first column for each speed-grade category lists the maximum write leveling skew in picoseconds. The second column for each lists the maximum write leveling skew in inches assuming a signal propagation rate of 180ps/in.

For DDR3-1333:

- $ddrclkout_{period}$ = 1500ps
- tWLS = 195ps
- tJIT(per, lck) = +/- 70ps
- margin = 100ps

Maximum Write Leveling Skew:

- Case 1: Invert Clock disabled
  - $write\_leveling_{skew} < 2500ps - tWLS - tJIT(per, lck) - margin$
  - $write\_leveling_{skew} < 2500ps - 195ps - 70ps - 100ps$
  - $write\_leveling_{skew} < 2500ps - 195ps - 70ps - 100ps$
  - $write\_leveling_{skew} < 2135ps$
- Case 2: Invert Clock enabled (adds an additional half-clock period of delay to the command delay term)
  - $write\_leveling_{skew} < 2500ps - tWLS - tJIT(per, lck) - (0.5 * ddrclkout_{period}) - margin$
  - $write\_leveling_{skew} < 2500ps - 195ps - 70ps - (0.5 * 1500ps) - 100ps$
  - $write\_leveling_{skew} < 1385ps$

Minimum Write Leveling Skew:

- Case 1: Invert Clock disabled
  - $write\_leveling_{skew} > tWLS + tJIT(per, lck) + margin$
  - $write\_leveling_{skew} > 195ps + 70ps + 100ps$
  - $write\_leveling_{skew} > 365ps$
- Case 2: Invert Clock enabled (adds an additional half-clock period of delay to the command delay term)
  - $write\_leveling_{skew} > tWLS + tJIT(per, lck) - (0.5 * ddrclkout_{period}) + margin$
  - $write\_leveling_{skew} > 195ps + 70ps - (0.5 * 1500ps) + 100ps$
  - $write\_leveling_{skew} > -385ps$

Note—This minimum write leveling skew calculation with Invert Clock enabled shows how the Invert Clock mode can be used to correct a small amount of negative skew between the command and data groups. However, as specified in Section 4.3.1.7, all topologies should be designed for a positive skew between the command delay and data delay to avoid this situation.

For DDR3-1600:

- $ddrclkout_{period}$ = 1250ps
- tWLS = 165ps
- tJIT(per, lck) = +/- 60ps
- margin = 100ps

Maximum Write Leveling Skew:

- Case 1: Invert Clock disabled
  - $write\_leveling_{skew}$ < 2500ps - 165ps - 60ps -100ps
  - $write\_leveling_{skew}$ < 2500ps - 165ps - 60ps -100ps
  - $write\_leveling_{skew}$ < 2175ps
- Case 2: Invert Clock enabled (adds an additional half-clock period of delay to the command delay term)
  - $write\_leveling_{skew}$ < 2500ps - 165ps - 60ps - (0.5 *1250ps) - 100ps
  - $write\_leveling_{skew}$ < 1610ps

Minimum Write Leveling Skew:

- Case 1: Invert Clock disabled
  - $write\_leveling_{skew}$ > 165ps + 60ps + 100ps
  - $write\_leveling_{skew}$ > *325ps*
- Case 2: Invert Clock enabled (adds an additional half-clock period of delay to the command delay term)
  - $write\_leveling_{skew}$ > 165ps + 60ps - (0.5 *1250ps) + 100ps
  - $write\_leveling_{skew}$ > -300ps

Note—This minimum write leveling skew calculation with Invert Clock enabled shows how the Invert Clock mode can be used to correct a small amount of negative skew between the command and data groups. However, as specified in Section 4.3.1.7, all topologies should be designed for a positive skew between the command delay and data delay to avoid this situation.

Table 16 Maximum Write Leveling Skew Example

	Invert Clock Out State			
	Disabled		Enabled	
Speed-Grade	skew in ps	skew in inches	skew in ps	skew in inches
DDR3-1333	2135	11.861	1385	7.694
DDR3-1600	2175	12.083	1610	8.944

Table 17 Maximum Write Leveling Skew Example

	Invert Clock Out State			
	Disabled		Enabled	
Speed-Grade	skew in ps	skew in inches	skew in ps	skew in inches
DDR3-1333	365	2.027	-385	2.138
DDR3-1600	325	1.805	-300	1.666

Note—Because this is preliminary guidance and some small margin should be subtracted or added from these delays to account for additional terms such as multi-rank delay skew, TI recommends that the maximum routing lengths be reduced by 10% and the minimum routing lengths be increased by 10%.

4.3.2 Mechanical Layout and Routing Considerations – UDIMMs

4.3.2.1 Mechanical Layout – UDIMMs

When designing the application hardware to use a UDIMM there are several issues to take into account that may differ when using individual SDRAMs, including power and route lengths. Key issues including stack-up and power / ground plane referencing do not differ between the two topologies (SDRAM versus UDIMM).

4.3.2.2 Stack Up – UDIMMs

The board stack-up should not change regardless of whether you are using a UDIMM or individual SDRAMs. General guidelines for stack up under the SDRAMs section apply. It is worth mentioning that a good quality connector and proper impedance is critical to minimize signal reflections.

4.3.2.3 Routing Rules – General Overview – UDIMMs

General routing rules between the Keystone DSP DDR3 interface and UDIMM are the same as those identified for discrete components (SDRAMs). Return ground paths and power plane decoupling also are critical and should be evaluated properly.

All aspects of this application note and especially those pertaining to the use and implementation of UDIMMs assumes that the user has an above average level of understanding regarding mechanical layout and design – including the impact of trace width, spacing, via size, bulk and decoupling capacitance selection and placement.

Net classes are an important concept when routing high speed signals, they typically identify signals which have a critical timing relationship. When routing between the DSP and UDIMM, you should consider four different routing groups or net classes. Table 18 defines the net classes to consider.

Table 18 UDIMM Net Class Routing Rules (Part 1 of 2)

Net Class	Signals	Notes
Data	DQS[8:0], DQS#[8:0], DQ[n:0], CB[7:0]	1, 2
Address/Command	BA[2:0], A[n:0], Command lines	2, 3
Control	CSn (DDRCEnz), CKEn, ODTn, RESET#	2

Table 18 UDIMM Net Class Routing Rules (Part 2 of 2)

Net Class	Signals	Notes
Clocks	CK and CK#	
Note 1: CB[7:0] refer to ECC devices Note 2: "n" refers to some number of lines and is dependent upon device selected Note 3: Command refers to command inputs including RAS#, CAS#, WE# signal lines.		
End of Table 18		

4.3.2.4 Routing Rules –Address Lines [UDIMMs]

All address nets between the DSP and UDIMM must be referenced to a solid ground or solid power plane - the best option would be a solid power plane. If possible and recommended, the entire address bus should be referenced to the $V_{DD}15$ power/ground plane to establish a low impedance current return path. All nets routing from the DSP to the UDIMM socket must be adjacent to the referenced plane.

The address bus between the DSP and UDIMM should be routed away from the data bus and respective nets.

Maximum trace length for any address net (between DSP pin and UDIMM pin) should not exceed 4.5 inches (114.3mm). All address nets should be skew matched to within ±20 mils (1.00mm) of the DSP clock out at the UDIMM (respective pin). The recommended trace-to-trace spacing (for address-to-address nets) should be no less than 12 mils (0.300mm). The recommended trace-to-trace spacing (for address-to-other nets) should be no less than 20 mils (0.50mm).

All address and command net classes shall be skew matched to respective clock lines to within CLK ± 20 mils (1.00mm).

Note—The maximum length shall never exceed 4.5" (DSP-to-UDIMM pins) due to the additional UDIMM loading when two UDIMMs are used.

4.3.2.5 Routing Rules – Control Lines – UDIMMs

All command nets between the DSP and UDIMM must be referenced to a solid ground or solid power plane - the best option would be a solid power plane. As with the address nets, the command (or control) nets also should be referenced to the $V_{DD}15$ power/ground plane to establish a low impedance current return path. All nets routing from the DSP to the UDIMM socket must be adjacent to the referenced plane.

The command bus between the DSP and UDIMM should be routed away from the data bus and respective nets.

The maximum trace length for any command/control net (between DSP pin and UDIMM) must follow the guidelines established in the previous section. This includes spacing and skew requirements.

All nets having complementary pairs (differential signals) must be routed as a differential pair with a 50Ω single ended impedance and a differential impedance of 100Ω.

To reiterate, all address and command net classes shall be skew matched to respective clock lines to within CLK ± 20 mils (1.00mm).

As with the address nets, the control/command nets shall not increase in total length beyond the 4.5" if two UDIMMs are used. The maximum spacing is calculated between the furthest UDIMM (respective pin) and the DSP (respective) pin.

4.3.2.6 Routing Rules – Data Lines – UDIMMs

Like all other signals (command and address) the data lines must also be referenced to a plane (ground is preferred).

If possible, all nets should be routed on the top layer (adjacent to a plane). If it becomes necessary to route data (or other nets) on an internal layer, then the added delays attributed by vias and landing pads must be taken into account. Signal propagation differences between internally and externally routed nets also must be accounted for.

Note—There should be no vias in the data lines.

Data nets must also be skew matched relative to other signals. The maximum allowable skew between complementary data strobe pins shall be within ±10 mils (0.500mm). Table 19 illustrates the relationship between byte lane and data/data mask.

Table 19 Data and Data Strobe Byte Lane Grouping

DATA	DATA STROBE	DATA $\overline{\text{STROBE}}$	DATA MASK
DQ[7:0]	DQS0	DQS0#	DM0
DQ[15:8]	DQS1	DQS1#	DM1
DQ[23:16]	DQS2	DQS2#	DM2
DQ[31:24]	DQS3	DQS3#	DM3
DQ[39:32]	DQS4	DQS4#	DM4
DQ[47:40]	DQS5	DQS5#	DM5
DQ[55:48]	DQS6	DQS6#	DM6
DQ[63:56]	DQS7	DQS7#	DM7
CB[7:0]	DQS8	DQS8#	DM8
End of Table 19			

As with control (command) and address nets, the maximum trace length between DSP and UDIMM pin shall not exceed 4.5 inches (114.3mm) given the constraints identified previously. All data nets should be skew matched between data/strobe within the respective byte lane. The byte lanes are identified in Table 19.

Each respective data to strobe within a byte lane must be skew matched to be ≤ 10.00 mils (0.254mm).

4.3.2.7 Routing Rules – Clock Lines UDIMMs

All DDR3 clocks between the DSP and respective UDIMM must be routed as differential pair(s). Each differential clock pair (depends on number of UDIMMs used) must maintain a specific relationship in length to the address and control signals.

The relationship between the differential clock lines and address/control nets should be evaluated at the UDIMM socket. As a general rule of thumb, single-ended nets typically have a longer propagation time than differential nets – this phenomena must be taken into account when routing clock signals with respect to address and control signals.

Additionally, and during routing (clock lines between DSP and UDIMM) it is important to remember that clock nets are typically less heavily loaded (than address and control signals) which also adds to faster propagation times (relative to the address, command, and control nets). There are several methods used to normalize the faster clock propagation times, the most common is increasing the clock (and complementary clock net) trace length (accordingly).

It is recommended that the differential clock signals routed to the UDIMM be slightly longer then the control and address lines – this is due to the fact that differential signals have an inherently faster propagation time than the single-ended address, and control pins. The differential clock lines can have up to a 12pS faster propagation time per 1000 mils (25.4mm) over a single-ended control or address net assuming the same IO buffer and drive strength are used.

CLK and CLK# nets correspond to the DDRCLKOUTP/N on the DSP.

4.3.2.8 Routing Rules – Power [UDIMMs]

For the UDIMM there exist three separate power supplies, all derived from a common rail. The first is the 1.5 V supply which provides power to all the DDR3 UDIMM IOs. The second supply is the V_{REF} supply which must track the VDD15 supply and establishes a reference voltage for the UDIMM. The last supply is the bus termination supply (Vtt).

Each of the Vref supplies to the UDIMM (VrefCA and VrefDQ) can originate from a common rail but must be individually decoupled at the UDIMM. V_{REF} must be 50% of the V_{DD}/V_{DDQ} level and meet the tolerances identified in the respective UDIMM data manual. The typical method for establishing each of these reference voltages is through a 1% (or less) resistor divider network. It is important that the V_{REF} (VrefCA and VrefDQ) voltages track the V_{DD}/V_{DDQ} level across all corners (process, temperature, and noise). See the applicable data manual for transient (AC & DC) requirements.

When routing the UDIMM V_{REF} voltages, properly decouple them as close to the socket as possible. The use of 0.01µF and 0.1µF ceramic capacitors (0402 or smaller recommended) should be distributed across the V_{REF} power rail with one 0.01µF and 0.1µF ceramic capacitor located at each V_{REF} pin and one 0.1µF capacitor directly at the source. Traces between the decoupling capacitors and V_{REF} pins should be a minimum of 0.030 inch (0.762mm) wide and as short as possible. The V_{REF} pins and interconnection to decoupling capacitors should maintain a minimum of 0.015 inch (0.381mm) spacing from all other nets. All V_{REF} nets should be routed on the top layer. V_{REF} pins should be isolated with or shielded with ground.

The UDIMM termination voltage (Vtt) must be at a constant level of 0.750 Vdc and must be capable of sinking a reasonable amount of current while maintaining a voltage regulation. Vtt must remain stable at all times for the UDIMM to function properly. Issues including noise and crosstalk must be eliminated or reduced to a negligible amount. Vtt like V_{REF} must track all variations with respect to Vdd/Vddq.

When routing the UDIMM Vtt power supply the regulator should be kept as close to the Vtt pin on the respective SDRAMs. In most cases a Vtt voltage island will be used. In most cases it is recommended that the voltage island be placed on the component-side signal layer. There should be a minimum of one 0.1µF decoupling capacitor close to each Vtt SDRAM pin and a minimum of one 10 – 22µF bulk capacitor one the Vtt island. The number of Vtt bulk capacitors is based on the size of island and topology.

4.3.2.9 Write Leveling Limit Impact on Routing

The write leveling process in the DDR3 interface imposes an upper and lower limit on the maximum and minimum skew between the command delay and the data delay. If this limit is exceeded, the DDR3 interface will fail the write leveling process and data corruption will occur. This limit is sufficiently large so that well controlled topologies will never exceed this limit.

The command delay is defined as the track length for the clock, command, control and address groups from the DSP to a given DRAM. The data delay is the track length for the data group to that same DRAM. The write leveling result is effectively the difference, or skew, between these two lengths. The maximum write leveling skew is the largest difference in the topology to a single DRAM byte lane. This would typically be the last DRAM in a fly-by routing topology.

The write leveling logic has a theoretical upper limit of 2500ps. This limit does not scale with DRAM data rate. The theoretical upper limit equates to 2 full clock cycles when the clock frequency is 800MHz for DDR3-1600. It will be reduced by half a clock cycle when 'Invert Clock Out' is enabled as this effectively lengthens the clock by this amount.

The following equation provides an approximation of the maximum write leveling skew:

```
write_leveling_skew < 2500ps - (invert_clock_out * 0.5 * clock_period) - margin
```

Note—write_leveling_skew is CK_to_DQS skew, where minimum delta is the maximum clock (CK) to DQS skew and maximum delta is the minimum clock (CK) to DQS skew.

Table 20 shows the write leveling skew limitations for both 'Invert Clock Out' enabled and disabled. The first column for each lists the maximum write leveling skew in picoseconds. The second column for each lists the maximum write leveling skew in inches assuming a signal propagation rate of 180ps/in.

Table 20 Write Leveling Skew Limitations - "Invert Clock Out" Enabled & Disabled

	Invert Clock Out Disabled		Invert Clock Out Enabled	
DDR3-1333	2500 ps	13.89 in	1750 ps	9.72 in
DDR3-1600	2500 ps	13.89in	1875 ps	10.42 in

Since this is preliminary guidance and some small margin should be subtracted from these delays to account for additional terms such as multi-rank delay skew, we recommend that the maximum routing lengths be reduced by 10%.

Note—The above table does not include subtraction for any margin.

Note—Margin is defined as tJIT (per,lck) plus tWLS plus a margin of 100ps[1].
ex: 195ps (tWLS) + 70 tJIT(per,lck) + 100ps for DDR3-1333.

[1] - 100ps is an estimate that will be confirmed during DDR characterization.

4.4 Loading

The current instantiation of the Texas Instruments Keystone DSP DDR3 Controller supports point to multi-point loading on most signal lines. The maximum loading allowed (on the DSP DDR3 output per respective pin) is specified in Table 21.

Table 21 Maximum DSP DDR3 Pin Loading

Sign Name	Maximum DDR3 Loading[1]	Total Maximum Loading[2]
CK & CK#	1.6pF	4pF
DQS & DQS#	3pF[3]	15pF
DM (LDM & UDM)	3pF[3]	15pF
ZQ	3pF	25pF
A0:An	1.4pF	15pF
BA0:Ban	1.4pF	6pF
CKE	1.4pF	6pF
CS#	1.4pF	6pF
ODT	1.4pF	6pF
RAS#, CAS#, WE#	1.4pF	15pF
RESET#	1.4pF	15pF
DQ0:7	3pF[3]	15pF
DQ8:15	3pF[3]	15pF
End of Table 21		

1. Depending on number of devices and width utilized. The number provided is absolute maximum load for the SDRAM per respective pin
2. Depending on number of devices and width utilized. The number provided is absolute maximum inclusive of application hardware per pin
3. DQ and DQM loading must be matched

4.5 Timing Considerations

DDR3 requires strict timing relationships between CLK (& CLK#) and the address/control lines, and between data and the DQS (& DQS#) lines. The TI DSP (DDR3 Interface) is designed to comply with the DDR3 JEDEC Standard with regards to timing constraints. See the applicable standard when evaluating timing. Additional timing considerations or constraints may be included in the respective DSP or SDRAM data sheets.

4.6 Switching and Output Considerations

Signal switching and output swings can have a significant if not catastrophic impact on signal integrity and EMI compliance. Routing, SDRAM placement, stack up, and use cases can also attribute to added dynamic switching noise. The concept of dynamic switching noise and induced ground bounce is usually attributed to improper layout, stack up, insufficient decoupling, and routing. To minimize the output and switching problems system modeling is recommended and usually employed.

5 Simulation and Modeling

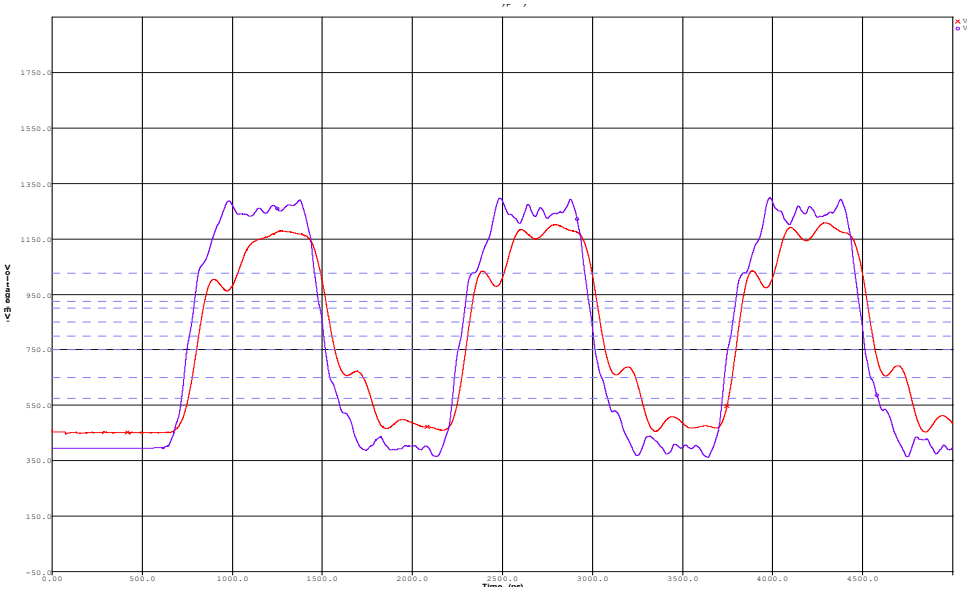
This section provides a quick overview regarding the importance of simulating and modeling the DSP and DDR3 interfaces.

5.1 Simulation and modeling

All high-performance interfaces, especially those operating above 300MHz, should always be modeled. Proper simulation and modeling (which must include a complete application board (PCB) stack up, DSP DDR3 interface and SDRAMs) is important to verify and confirm component placement, selection, and signal integrity. In a high performance interface, signal stubs, perturbations, non-monotonic waveforms, inflections, and reflections become significant. Time spent properly modeling the DDR3 interface regardless of the topology or condition selected will pay off in the long run.

Figure 11 illustrates the impact of proper placement and routing of high speed signals.

Figure 11 DDR3 Simulations



5.2 Tools

A variety of software tools exists allowing customers the ability to model high-performance interfaces. Up until recently, the most common simulation tool was Spice or HSpice. These tools are extremely costly, difficult to use, and vary between types. Other tools including the IBIS standard and protocol were traditionally avoided because of their limitation at high frequencies.

5.3 Models

Different simulation models can be found for the DDR3 SDRAMs and will be available from the SDRAM vendor you have selected. The available models are typically one of the following three formats: Spice, HSpice, and IBIS. Texas Instruments intends to provide IBIS models to our customers.

5.4 TI Commitment

Texas Instruments has taken the initiative to provide IBIS models compliant with the latest 5.0 IBIS standard for the DDR3 interface. The Texas Instruments DSP IBIS model will be correlated to internal Matlab or Spice models, and functionally against timing and performance parameters prior to release (TMS).

6 Power

This section briefly describes the DDR3 relative power, DSP DDR3 interface relative power, power assessment, and power sequencing.

6.1 DDR3 SDRAM Power Requirements

There exists three (3) different power supplies on the SDRAM (1.5V primary IO supply, Vref, and Vtt) and three (3) different power supplies on the on the DSP (1.1V, 1.5V, and Vref).

It is recommended that the Keystone DSP DDR3 interface and SDRAM share a common 1.5V supply rail. A common 1.5V supply rail (±5% maximum AC/DC tolerance) simplifies the overall design, and reduces the differential between the two devices and minimizes the need for additional layers (power) in the end-use application.

6.1.1 Vref Voltage Requirements

There exist two DDR3 SDRAM Vreference pins: VrefCA and VrefDQ. VrefCA is the reference voltage for all command, address, and control pins, whereas VrefDQ is the reference voltage for the data lines. It is not necessary, but typically recommended that both Vreference voltages originate from the same supply source. Both Vreference pins must be derived from Vdd/2 (Vddq/2). The recommended Vreference (Vref) implementation is by using a simple resistor divider with 1% or better accuracy. The distance between the source voltage through the divider network and to the decoupled Vreference pins must be short. Each Vreference pin must properly track the Vdd/2 (Vddq/2) variations over voltage, noise, and temperature differences. The pk-to-pk AC and DC noise on the Vreference pins cannot exceed ±2% or 1.5mV.

6.1.2 Vtt Voltage Requirements

The DDR3 SDRAM termination voltage is referred to as “Vtt” and requires a 750mV DC supply. The recommended Vtt source is a regulator that is capable of sinking a sufficient amount of current while at the same time maintains a tight voltage tolerance. Like the Vref pins, the distance between the Vtt source voltage and SDRAM pin must be short and decoupled properly. The Vtt pin must be kept stable and properly track the Vdd/Vddq variations over voltage, noise, and temperature differences. The pk-to-pk AC and DC noise on the Vtt pin cannot exceed ±2% or 1.5mV.

6.2 DSP DDR3 Power Requirements

On the DSP, the AVDDA2 pins are designed to supply power to the internal DDR3 clock PLL. These pins must be connected to a clean 1.8V supply rail. There exist other DSP 1.8V supplies which can be used provided the voltage tolerance is maintained and a separate filter is used. All VDDS1V5 pins are designed to supply power to the DSP DDR3 IO buffers – as with the 1.5V power pins these must also be connected to a clean 1.5V supply rail. The VREFSSTL pin provides the reference voltage to the DSP DDR3 interface. This supply pin is derived from Vdd/2 using 1% or better resistors. The DSP VDD10MON pin is a voltage rail monitor pin and should be tied through a short connection to the VDDS1V5 rail.

See the respective DSP data sheet and application notes for power supply requirements.

6.3 DDR3 Power Estimation

Actual power for each SDRAM is dependent upon many factors. Most DDR3 SDRAM manufacturers have application notes to aid in estimating the DDR3 power. Power can be broken up into two categories, active and leakage, all SDRAMs containing some element of each. When designing the power supplies it is strongly recommended that you take into account both active and leakage powers as well as peak in rush currents. A suitable margin should always be added to the final calculation.

As a general rule of thumb a single DDR3 SDRAM in a ×16 (256M Byte) configuration running at 1.333MT/s and assuming 50% reads and 50% writes will consume a maximum total power of 864mW or 576mA.

6.4 DSP DDR3 Interface Power Estimation

Excluding the DDR3 SDRAM power discussed above, power estimates for the DSP DDR3 interface can be obtained using the respective Keystone DSP power application note and spreadsheet.

6.5 Sequencing - DDR3 & DSP

Your DSP requires specific power sequencing as well as the DDR3 DRAM(s). In all cases please see the respective data sheet for verification of power up and power down sequencing requirements.

In all cases, the DRAM cannot be allowed to drive into the DSP until the DSP has been fully powered and sequenced properly.

7 Disclaimers

Comments and proposals identified within this document are presented as guidelines. Texas Instruments can not fully anticipate every possible design permutation, topology, and application variation and therefore requires each end user to perform proper due diligence (using good engineering practices and including proper component selection) when designing for a DDR3 interface. This includes proper simulation and modeling to verify the recommendations provided function in an acceptable manner (in the end-use application).

This application guide is not intended to be the sole source or reference design guide. Many factors not encompassed within this document can force a change in component values, selection, placement, or termination type.

The possible permutations available due to component, layout, and assembly can also induce variations not encompassed in the recommendations provided. Voltage rails, manufacturer parts selection, switching levels should all be verified before committing the design to production.

It is the end user's responsibility to always verify the design, and connectivity between any active or passive component and the targeted DSP. This includes verifying against individual data sheets and application notes.

Simulation and modeling play an important role in system verification and validation. This effort and the need to conduct this level of analysis should not be overlooked in any design – regardless of simplicity or complexity.

This is not a primer for high-speed design. Use of the information provided assumes a strong understanding of electrical and mechanical design requirements in a high-performance DSP application environment.

From time to time there exist DSP or application design changes. It is the end user's responsibility to verify that the appropriate data sheets and application notes are followed.

Specifications continuously change and are updated. Verify the specifications have not changed and that the documents used are correct for the version of silicon you are designing with.

Prior to final design release it is recommended that a full engineering assessment be performed by the end user in order to assure functionality.

8 Appendix

The following section is provided as additional support. Information contained within this section is intended as general guidelines only. All information contained within this section was checked for correctness at the time respective data sheets and application notes were available.

8.1 DRAM Configurations

The following sub-section provides connectivity tables for several common SDRAMs. It is a requirement of the end user or designer to verify the pin connectivity between the DSP and SDRAM based on released data manuals. This section contains combinations from two ×8 SDRAM to a single UDIMM configuration. The headers for each listed configuration identify which package was selected and the number of pins within each respective package (in most cases it is a 78-pin package). Alternate DRAM and DSP packages may exist and should be thoroughly evaluated if selected for correct connection between the DSP and SDRAM(s).

Note—Many of the configurations listed below make use of the second DSP DDRCLKOUTP/N1 pins as a clock source in multi-DRAM configurations. Although this is typically reserved for dual rank designs, TI recommends using the second DSP DRAM clock source to ease routing and loading typically encountered in a single-clock source configuration.

8.1.1 Common Configurations

8.1.1.1 Two 16M x8 x8 banks (2.048G bit total)

The following tables illustrate the connectivity between a KeyStone DSP and two 128M Byte ×8 SDRAMs resulting in a total memory capacity of 256M Bytes. The following four tables define in detail the recommended inner-connectivity for a 16-bit wide bus and between two ×8 1G bit SDRAMs and a Keystone class DSP DDR3 controller. This table is also provided and based on a 78-pin SDRAM package.

Table 22 Pin Connectivity →2 - 16M x8 x8 Banks (2G bit total) [1 of 4]

Two 16Meg x 8 x 8 banks (256MB total) [1 of 4] [78 pin MO-207 x8 DT-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRA00	K3	A0	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA01	L7	A1	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA02	L3	A2	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA03	K2	A3	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA04	L8	A4	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA05	L2	A5	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA06	M8	A6	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA07	M2	A7	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA08	N8	A8	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA09	M3	A9	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA10	H7	A10/AP	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA11	M7	A11	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA12	K7	A12/BC#	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA13	N3	A13	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA14			N	Leave unconnected

Table 22 Pin Connectivity →2 - 16M x8 x8 Banks (2G bit total) [1 of 4]

Two 16Meg x 8 x 8 banks (256MB total) [1 of 4] [78 pin MO-207 x8 DT-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRA15			N	Leave unconnected
	DDRD00	B3	DQ0	Y	Connected SDRAM #1 to DSP pin
	DDRD01	C7	DQ1	Y	Connected SDRAM #1 to DSP pin
	DDRD02	C2	DQ2	Y	Connected SDRAM #1 to DSP pin
	DDRD03	C8	DQ3	Y	Connected SDRAM #1 to DSP pin
	DDRD04	E3	NF, DQ4	Y	Connected SDRAM #1 to DSP pin
	DDRD05	E8	NF, DQ5	Y	Connected SDRAM #1 to DSP pin
	DDRD06	D2	NF, DQ6	Y	Connected SDRAM #1 to DSP pin
	DDRD07	E7	NF, DQ7	Y	Connected SDRAM #1 to DSP pin
	DDRD08	B3	DQ0	Y	Connected SDRAM #2 to DSP pin
	DDRD09	C7	DQ1	Y	Connected SDRAM #2 to DSP pin
	DDRD10	C2	DQ2	Y	Connected SDRAM #2 to DSP pin
	DDRD11	C8	DQ3	Y	Connected SDRAM #2 to DSP pin
	DDRD12	E3	NF, DQ4	Y	Connected SDRAM #2 to DSP pin
	DDRD13	E8	NF, DQ5	Y	Connected SDRAM #2 to DSP pin
	DDRD14	D2	NF, DQ6	Y	Connected SDRAM #2 to DSP pin
	DDRD15	E7	NF, DQ7	Y	Connected SDRAM #2 to DSP pin
	DDRD16			N	Leave DSP pin unconnected
	DDRD17			N	Leave DSP pin unconnected
	DDRD18			N	Leave DSP pin unconnected
	DDRD19			N	Leave DSP pin unconnected
	DDRD20			N	Leave DSP pin unconnected
End of Table 22					

Table 23 Pin Connectivity →2 - 16M x8 x8 banks (2G bit total) [2 of 4]

Two 16Meg x 8 x 8 banks (256MB total) [2 of 4] [78 pin MO-207 x8 DT-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD21			N	Leave DSP pin unconnected
	DDRD22			N	Leave DSP pin unconnected
	DDRD23			N	Leave DSP pin unconnected
	DDRD24			N	Leave DSP pin unconnected
	DDRD25			N	Leave DSP pin unconnected
	DDRD26			N	Leave DSP pin unconnected
	DDRD27			N	Leave DSP pin unconnected
	DDRD28			N	Leave DSP pin unconnected
	DDRD29			N	Leave DSP pin unconnected
	DDRD30			N	Leave DSP pin unconnected
	DDRD31			N	Leave DSP pin unconnected
	DDRD32			N	Leave DSP pin unconnected

Table 23 Pin Connectivity →2 - 16M x8 x8 banks (2G bit total) [2 of 4]

Two 16Meg x 8 x 8 banks (256MB total) [2 of 4] [78 pin MO-207 x8 DT-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD33			N	Leave DSP pin unconnected
	DDRD34			N	Leave DSP pin unconnected
	DDRD35			N	Leave DSP pin unconnected
	DDRD36			N	Leave DSP pin unconnected
	DDRD37			N	Leave DSP pin unconnected
	DDRD38			N	Leave DSP pin unconnected
	DDRD39			N	Leave DSP pin unconnected
	DDRD40			N	Leave DSP pin unconnected
	DDRD41			N	Leave DSP pin unconnected
	DDRD42			N	Leave DSP pin unconnected
	DDRD43			N	Leave DSP pin unconnected
	DDRD44			N	Leave DSP pin unconnected
	DDRD45			N	Leave DSP pin unconnected
	DDRD46			N	Leave DSP pin unconnected
	DDRD47			N	Leave DSP pin unconnected
	DDRD48			N	Leave DSP pin unconnected
	DDRD49			N	Leave DSP pin unconnected
	DDRD50			N	Leave DSP pin unconnected
	DDRD51			N	Leave DSP pin unconnected
	DDRD52			N	Leave DSP pin unconnected
	DDRD53			N	Leave DSP pin unconnected
	DDRD54			N	Leave DSP pin unconnected
	DDRD55			N	Leave DSP pin unconnected
	DDRD56			N	Leave DSP pin unconnected
	DDRD57			N	Leave DSP pin unconnected
	DDRD58			N	Leave DSP pin unconnected
	DDRD59			N	Leave DSP pin unconnected
End of Table 23					

Table 24 Pin Connectivity →2 - 16M x8 x8 banks (2G bit total) [3 of 4]

Two 16Meg x 8 x 8 banks (256MB total) [3 of 4] [78pin MO-207 x8 DT-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD60			N	Leave DSP pin unconnected
	DDRD61			N	Leave DSP pin unconnected
	DDRD62			N	Leave DSP pin unconnected
	DDRD63			N	Leave DSP pin unconnected
	$\overline{\text{DDRCE0}}$	H 2	CS#	Y	Connected SDRAM #1 & 2 to DSP pin
	$\overline{\text{DDRCE1}}$	H 2	CS#	N	Leave DSP pin unconnected
	DDRBA0	J2	BA0	Y	Connect to like pin between SDRAM and DSP
	DDRBA1	K8	BA1	Y	Connect to like pin between SDRAM and DSP

Table 24 Pin Connectivity →2 - 16M x8 x8 banks (2G bit total) [3 of 4]

Two 16Meg x 8 x 8 banks (256MB total) [3 of 4] [78pin MO-207 x8 DT-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRBA2	J3	BA2	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRCAS}}$	G3	CAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRRAS}}$	F3	RAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRWE}}$	H 3	WE#	Y	Connect to like pin between SDRAM and DSP
	DDRCKE0	G 9	CKE	Y	Connect to like pin between SDRAM and DSP
	DDRCKE1	G 9	CKE	N	Leave unconnected on DSP
	DDRCLKOUTP0	F 7	CK	Y	Connected SDRAM #1 & #2 to DSP pin
	DDRCLKOUTN0	G 7	CK#	Y	Connected SDRAM #1 & #2 to DSP pin
	DDRCLKOUTP1	F 7	CK	N	Leave unconnected on DSP
	DDRCLKOUTN1	G 7	CK#	N	Leave unconnected on DSP
	DDRODT0	G 1	ODT	Y	Connected SDRAM #1 & #2 to DSP pin
	DDRODT1	G 1	ODT	N	Leave unconnected on DSP
	DDRSLRATE0			Y	See Data Manual For Details
	DDRSLRATE1			Y	See Data Manual For Details
	DDRCB00			N	Leave unconnected on DSP
	DDRCB01			N	Leave unconnected on DSP
	DDRCB02			N	Leave unconnected on DSP
	DDRCB03			N	Leave unconnected on DSP
	DDRCB04			N	Leave unconnected on DSP
	DDRCB05			N	Leave unconnected on DSP
	DDRCB06			N	Leave unconnected on DSP
	DDRCB07			N	Leave unconnected on DSP
	DDRDQM0	B 7	DM	Y	Connected SDRAM #1 to DSP pin
	DDRDQM1	B 7	DM	Y	Connected SDRAM #2 to DSP pin
	DDRDQM2			N	Leave unconnected on DSP
	DDRDQM3			N	Leave unconnected on DSP
	DDRDQM4			N	Leave unconnected on DSP
	DDRDQM5			N	Leave unconnected on DSP
	DDRDQM6			N	Leave unconnected on DSP
	DDRDQM7			N	Leave unconnected on DSP
	DDRDQM8			N	Leave unconnected on DSP
End of Table 24					

Table 25 Pin Connectivity →2 - 16M x8 x8 banks (2G bit total) [4 of 4]

Two 16Meg x 8 x 8 banks (256MB total) [4 of 4] [78-pin MO-207 DT-z x8 Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRDQS0N	D 3	DQS#	Y	Connected SDRAM #1 to DSP pin
	DDRDQS0P	C 3	DQS	Y	Connected SDRAM #1 to DSP pin
	DDRDQS1N	D 3	DQS#	Y	Connected SDRAM #2 to DSP pin
	DDRDQS1P	C 3	DQS	Y	Connected SDRAM #2 to DSP pin
	DDRDQS2N			N	

Table 25 Pin Connectivity →2 - 16M x8 x8 banks (2G bit total) [4 of 4]

Two 16Meg x 8 x 8 banks (256MB total) [4 of 4] [78-pin MO-207 DT-z x8 Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRDQS2P			N	
	DDRDQS3N			N	
	DDRDQS3P			N	
	DDRDQS4N			N	
	DDRDQS4P			N	
	DDRDQS5N			N	
	DDRDQS5P			N	
	DDRDQS6N			N	
	DDRDQS6P			N	
	DDRDQS7N			N	
	DDRDQS7P			N	
	DDRDQS8N			N	
	DDRDQS8P			N	
	DDRCLKP			Y	Differential DDR PLL clock input to DSP (+)
	DDRCLKN			Y	Differential DDR PLL clock input to DSP (-)
		H 8	ZQ	Y	Each DDR3 SDRAM ZQ pin should be tied to a 240Ω resistor to ground
	$\overline{\text{DDRRESET}}$	N 2	RESET#	Y	DDR3 DSP & SDRAM reset pins
		A 7	TDQS#	Y	Unused if DM is implemented, see the data sheet for alternate use
	AVDDA2			Y	DDRCLK PLL Power Supply, connect to dedicated and clean 1.8V (use filter)
$D_{VDD}15$	See device data manual	A2, A9, D7, G2, G8, K9, M9	VDD	Y	Connect 1.5V pins to same source
	See device data manual	B9, C1, E2, E9, K1, M1	VddQ	Y	Connected to respective VDD (1.5V) Supply, pay attention to tolerance and sequencing requirements. Should be same supply for both.
	VREFSSTL	J 8	VrefCA	Y	DDR3 Vref pin, connect to DSP DDR3 Vdd/2 (.1% tol.)
					Connect to VDD/2, pay attention to power sequencing requirements
		E 1	VrefDQ	Y	Connect to VDD/2, pay attention to power sequencing requirements
Vss	See device data manual	A1, A8, B1, D8, F8, J1, J9, L1, L9, N1, N9	Vss	Y	Connected to Ground, must be same ground potential as DSP
		B2, B8, C9,D1, D9, F2	VssQ	Y	Connected to Ground, connection MUST be short
	PTV15A			Y	45.3Ω tied to ground (must be short)
		A 3	NC	N	Leave unconnected on both SDRAM
		F 1	NC	N	Leave unconnected on both SDRAM
		F 9	NC	N	Leave unconnected on both SDRAM
		H 1	NC	N	Leave unconnected on both SDRAM
		H 9	NC	N	Leave unconnected on both SDRAM

End of Table 25

8.1.1.2 Four 16M x8 x8 banks (4.096G bit total)

The following tables illustrate the connectivity for between a KeyStone DSP and four 128M Byte ×8 SDRAMs resulting in a total memory capacity of 512M Bytes. The following four tables define in detail the recommended inner-connectivity for a 32-bit wide bus and between four ×8 1G bit SDRAMs and a Keystone class DSP DDR3 controller. This table is also provided and based on a 78-pin SDRAM package.

Table 26 Pin Connectivity →4 - 16M x8 x8 banks (4G bit total) [1 of 4]

Four 16Meg x 8 x 8 banks (512MB total) [1 of 4] [78-pin MO-207 x8 DT-z Pkg w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRA00	K3	A0	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA01	L7	A1	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA02	L3	A2	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA03	K2	A3	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA04	L8	A4	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA05	L2	A5	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA06	M8	A6	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA07	M2	A7	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA08	N8	A8	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA09	M3	A9	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA10	H7	A10/AP	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA11	M7	A11	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA12	K7	A12/BC#	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA13	N3	A13	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA14			N	Leave unconnected
	DDRA15			N	Leave unconnected
	DDRD00	B3	DQ0	Y	Connected SDRAM #1 to DSP pin
	DDRD01	C7	DQ1	Y	Connected SDRAM #1 to DSP pin
	DDRD02	C2	DQ2	Y	Connected SDRAM #1 to DSP pin
	DDRD03	C8	DQ3	Y	Connected SDRAM #1 to DSP pin
	DDRD04	E3	NF, DQ4	Y	Connected SDRAM #1 to DSP pin
	DDRD05	E8	NF, DQ5	Y	Connected SDRAM #1 to DSP pin
	DDRD06	D2	NF, DQ6	Y	Connected SDRAM #1 to DSP pin
	DDRD07	E7	NF, DQ7	Y	Connected SDRAM #1 to DSP pin
	DDRD08	B3	DQ0	Y	Connected SDRAM #2 to DSP pin
	DDRD09	C7	DQ1	Y	Connected SDRAM #2 to DSP pin
	DDRD10	C2	DQ2	Y	Connected SDRAM #2 to DSP pin
	DDRD11	C8	DQ3	Y	Connected SDRAM #2 to DSP pin
	DDRD12	E3	NF, DQ4	Y	Connected SDRAM #2 to DSP pin
	DDRD13	E8	NF, DQ5	Y	Connected SDRAM #2 to DSP pin
	DDRD14	D2	NF, DQ6	Y	Connected SDRAM #2 to DSP pin
	DDRD15	E7	NF, DQ7	Y	Connected SDRAM #2 to DSP pin
	DDRD16	B3	DQ0	Y	Connected SDRAM #3 to DSP pin
	DDRD17	C7	DQ1	Y	Connected SDRAM #3 to DSP pin
	DDRD18	C2	DQ2	Y	Connected SDRAM #3 to DSP pin
	DDRD19	C8	DQ3	Y	Connected SDRAM #3 to DSP pin

Table 26 Pin Connectivity →4 - 16M x8 x8 banks (4G bit total) [1 of 4]

Four 16Meg x 8 x 8 banks (512MB total) [1 of 4] [78-pin MO-207 x8 DT-z Pkg w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD20	E3	NF, DQ4	Y	Connected SDRAM #3 to DSP pin
	DDRD21	E8	NF, DQ5	Y	Connected SDRAM #3 to DSP pin
	DDRD22	D2	NF, DQ6	Y	Connected SDRAM #3 to DSP pin
	DDRD23	E7	NF, DQ7	Y	Connected SDRAM #3 to DSP pin
	DDRD24	B3	DQ0	Y	Connected SDRAM #4 to DSP pin
	DDRD25	C7	DQ1	Y	Connected SDRAM #4 to DSP pin
End of Table 26					

Table 27 Pin Connectivity →4 - 16M x8 x8 banks (4G bit total) [2 of 4]

Four 16Meg x 8 x 8 banks (512MB total) [2 of 4] [78 pin MO-207 x8 DT-z Pkg w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD26	C2	DQ2	Y	Connected SDRAM #4 to DSP pin
	DDRD27	C8	DQ3	Y	Connected SDRAM #4 to DSP pin
	DDRD28	E3	NF, DQ4	Y	Connected SDRAM #4 to DSP pin
	DDRD29	E8	NF, DQ5	Y	Connected SDRAM #4 to DSP pin
	DDRD30	D2	NF, DQ6	Y	Connected SDRAM #4 to DSP pin
	DDRD31	E7	NF, DQ7	Y	Connected SDRAM #4 to DSP pin
	DDRD32			N	Leave DSP pin unconnected
	DDRD33			N	Leave DSP pin unconnected
	DDRD34			N	Leave DSP pin unconnected
	DDRD35			N	Leave DSP pin unconnected
	DDRD36			N	Leave DSP pin unconnected
	DDRD37			N	Leave DSP pin unconnected
	DDRD38			N	Leave DSP pin unconnected
	DDRD39			N	Leave DSP pin unconnected
	DDRD40			N	Leave DSP pin unconnected
	DDRD41			N	Leave DSP pin unconnected
	DDRD42			N	Leave DSP pin unconnected
	DDRD43			N	Leave DSP pin unconnected
	DDRD44			N	Leave DSP pin unconnected
	DDRD45			N	Leave DSP pin unconnected
	DDRD46			N	Leave DSP pin unconnected
	DDRD47			N	Leave DSP pin unconnected
	DDRD48			N	Leave DSP pin unconnected
	DDRD49			N	Leave DSP pin unconnected
	DDRD50			N	Leave DSP pin unconnected
	DDRD51			N	Leave DSP pin unconnected
	DDRD52			N	Leave DSP pin unconnected
	DDRD53			N	Leave DSP pin unconnected
	DDRD54			N	Leave DSP pin unconnected

Table 27 Pin Connectivity →4 - 16M x8 x8 banks (4G bit total) [2 of 4]

Four 16Meg x 8 x 8 banks (512MB total) [2 of 4] [78 pin MO-207 x8 DT-z Pkg w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD55			N	Leave DSP pin unconnected
	DDRD56			N	Leave DSP pin unconnected
	DDRD57			N	Leave DSP pin unconnected
	DDRD58			N	Leave DSP pin unconnected
	DDRD59			N	Leave DSP pin unconnected
	DDRD60			N	Leave DSP pin unconnected
	DDRD61			N	Leave DSP pin unconnected
	DDRD62			N	Leave DSP pin unconnected
	DDRD63			N	Leave DSP pin unconnected
	$\overline{\text{DDRCE0}}$	H 2	CS#	Y	Connected SDRAM #1, #2, #3 & #4 to DSP pin
End of Table 27					

Table 28 Pin Connectivity →4 - 16M x8 x8 banks (4G bit total) [3 of 4]

Four 16Meg x 8 x 8 banks (512MB total) [3 of 4] [78pin MO-207 x8 DT-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	$\overline{\text{DDRCE1}}$	H 2	CS#	N	Leave DSP pin unconnected
	DDRBA0	J2	BA0	Y	Connect to like pin between SDRAM and DSP
	DDRBA1	K8	BA1	Y	Connect to like pin between SDRAM and DSP
	DDRBA2	J3	BA2	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRCAS}}$	G3	CAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRRAS}}$	F3	RAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRWE}}$	H 3	WE#	Y	Connect to like pin between SDRAM and DSP
	DDRCKE0	G 9	CKE	Y	Connect to like pin between SDRAMs and DSP
	DDRCKE1	G 9	CKE	N	Leave unconnected on SDRAM
	DDRCLKOUTP0	F 7	CK	Y	Connected SDRAM #1, 2, 3, & #4 to DSP pin
	DDRCLKOUTN0	G 7	CK#	Y	Connected SDRAM #1, 2, 3, & #4 to DSP pin
	DDRCLKOUTP1	F 7	CK	N	Leave unconnected on SDRAM
	DDRCLKOUTN1	G 7	CK#	N	Leave unconnected on SDRAM
	DDRODT0	G 1	ODT	Y	Connected SDRAM #1, 2, 3, & #4 to DSP pin
	DDRODT1	G 1	ODT	N	Leave unconnected on SDRAM
	DDRSLRATE0			Y	See Data Manual For Details
	DDRSLRATE1			Y	See Data Manual For Details
	DDRCB00			N	Leave unconnected on DSP
	DDRCB01			N	Leave unconnected on DSP
	DDRCB02			N	Leave unconnected on DSP
	DDRCB03			N	Leave unconnected on DSP
	DDRCB04			N	Leave unconnected on DSP
	DDRCB05			N	Leave unconnected on DSP
	DDRCB06			N	Leave unconnected on DSP
	DDRCB07			N	Leave unconnected on DSP

Table 28 Pin Connectivity →4 - 16M x8 x8 banks (4G bit total) [3 of 4]

Four 16Meg x 8 x 8 banks (512MB total) [3 of 4] [78pin MO-207 x8 DT-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRDQM0	B 7	DM	Y	Connected SDRAM #1 to DSP pin
	DDRDQM1	B 7	DM	Y	Connected SDRAM #2 to DSP pin
	DDRDQM2	B 7	DM	Y	Connected SDRAM #3 to DSP pin
	DDRDQM3	B 7	DM	Y	Connected SDRAM #4 to DSP pin
	DDRDQM4			N	
	DDRDQM5			N	
	DDRDQM6			N	
	DDRDQM7			N	
	DDRDQM8			N	
	DDRDQS0N	D 3	DQS#	Y	Connected SDRAM #1 to DSP pin
	DDRDQS0P	C 3	DQS	Y	Connected SDRAM #1 to DSP pin
	DDRDQS1N	D 3	DQS#	Y	Connected SDRAM #2 to DSP pin
	DDRDQS1P	C 3	DQS	Y	Connected SDRAM #2 to DSP pin
	DDRDQS2N	D 3	DQS#	Y	Connected SDRAM #3 to DSP pin
End of Table 28					

Table 29 Pin Connectivity →4 - 16M x8 x8 banks (4G bit total) [4 of 4]

Four 16Meg x 8 x 8 banks (512MB total) [4 of 4] [78pin MO-207 DT-z x8 Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRDQS2P	C 3	DQS	Y	Connected SDRAM #3 to DSP pin
	DDRDQS3N	D 3	DQS#	Y	Connected SDRAM #4 to DSP pin
	DDRDQS3P	C 3	DQS	Y	Connected SDRAM #4 to DSP pin
	DDRDQS4N			N	
	DDRDQS4P			N	
	DDRDQS5N			N	
	DDRDQS5P			N	
	DDRDQS6N			N	
	DDRDQS6P			N	
	DDRDQS7N			N	
	DDRDQS7P			N	
	DDRDQS8N			N	
	DDRDQS8P			N	
	DDRCLKP			Y	Differential DDR PLL clock input to DSP (+)
	DDRCLKN			Y	Differential DDR PLL clock input to DSP (-)
		H 8	ZQ	Y	Each DDR3 SDRAM ZQ pin should be tied to a 240Ω resistor to ground
	$\overline{\text{DDRRESET}}$	N 2	RESET#	Y	DDR3 DSP & SDRAM reset pins
		A 7	TDQS#	Y	Unused if DM is implemented, see data sheet for alternate use
	AVDDA2			Y	DDRCLK PLL Power Supply, connect to dedicated and clean 1.8V (use filter)

Table 29 Pin Connectivity →4 - 16M x8 x8 banks (4G bit total) [4 of 4]

Four 16Meg x 8 x 8 banks (512MB total) [4 of 4] [78pin MO-207 DT-z x8 Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
$D_{VDD}15$	See device data manual	A2, A9, D7, G2, G8, K9, M9	VDD	Y	Connect 1.5 V pins to same source
	See device data manual	B9, C1, E2, E9, K1, M1	VddQ	Y	Connected to respective VDD (1.5V) Supply, pay attention to tolerance and sequencing requirements. Should be same supply for both.
	VREFSSTL	J 8	VrefCA	Y	DDR3 Vref pin, connect to DSP DDR3 Vdd/2 (.1% tol.)
					Connect to VDD/2, pay attention to power sequencing requirements
		E 1	VrefDQ	Y	Connect to VDD/2, pay attention to power sequencing requirements
Vss	See device data manual	A1, A8, B1, D8, F8, J1, J9, L1, L9, N1, N9	Vss	Y	Connected to Ground, must be same ground potential as DSP
		B2, B8, C9,D1, D9, F2	VssQ	Y	Connected to Ground, connection MUST be short
	PTV15A			Y	45.3Ω tied to ground (must be short)
		A 3	NC	N	Leave unconnected on both SDRAM
		F 1	NC	N	Leave unconnected on both SDRAM
		F 9	NC	N	Leave unconnected on both SDRAM
		H 1	NC	N	Leave unconnected on both SDRAM
		H 9	NC	N	Leave unconnected on both SDRAM
End of Table 29					

8.1.1.3 Eight 16M x8 x8 banks (8.192G bit total)

The following tables illustrate the connectivity for between a KeyStone DSP and eight 128M Byte ×8 SDRAMs resulting in a total memory capacity of 1024M Bytes. The following four tables define in detail the recommended inner-connectivity for a 64 bit wide bus and between eight ×8 1G bit SDRAMs and a Keystone class DSP DDR3 controller. This table is also provided and based on a 78-pin SDRAM package.

Table 30 Pin Connectivity →8 - 16M x8 x8 banks (8G bit total) [1 of 4]

Eight 16 Meg x 8 x 8 banks (8G bit total) [1 of 4] [MO-207 DT-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRA00	K3	A0	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA01	L7	A1	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA02	L3	A2	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA03	K2	A3	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA04	L8	A4	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA05	L2	A5	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA06	M8	A6	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA07	M2	A7	Y	Connect Controller Address pin to both SDRAMs with like name

Table 30 Pin Connectivity →8 - 16M x8 x8 banks (8G bit total) [1 of 4]

Eight 16 Meg x 8 x 8 banks (8G bit total) [1 of 4]			[MO-207 DT-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRA08	N8	A8	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA09	M3	A9	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA10	H7	A10/AP	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA11	M7	A11	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA12	K7	A12/BC#	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA13	N3	A13	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA14			N	Leave unconnected
	DDRA15			N	Leave unconnected
	DDRD00	B3	DQ0	Y	Connected SDRAM #1 to DSP pin
	DDRD01	C7	DQ1	Y	Connected SDRAM #1 to DSP pin
	DDRD02	C2	DQ2	Y	Connected SDRAM #1 to DSP pin
	DDRD03	C8	DQ3	Y	Connected SDRAM #1 to DSP pin
	DDRD04	E3	NF, DQ4	Y	Connected SDRAM #1 to DSP pin
	DDRD05	E8	NF, DQ5	Y	Connected SDRAM #1 to DSP pin
	DDRD06	D2	NF, DQ6	Y	Connected SDRAM #1 to DSP pin
	DDRD07	E7	NF, DQ7	Y	Connected SDRAM #1 to DSP pin
	DDRD08	B3	DQ0	Y	Connected SDRAM #2 to DSP pin
	DDRD09	C7	DQ1	Y	Connected SDRAM #2 to DSP pin
	DDRD10	C2	DQ2	Y	Connected SDRAM #2 to DSP pin
	DDRD11	C8	DQ3	Y	Connected SDRAM #2 to DSP pin
	DDRD12	E3	NF, DQ4	Y	Connected SDRAM #2 to DSP pin
	DDRD13	E8	NF, DQ5	Y	Connected SDRAM #2 to DSP pin
	DDRD14	D2	NF, DQ6	Y	Connected SDRAM #2 to DSP pin
	DDRD15	E7	NF, DQ7	Y	Connected SDRAM #2 to DSP pin
	DDRD16	B3	DQ0	Y	Connected SDRAM #3 to DSP pin
	DDRD17	C7	DQ1	Y	Connected SDRAM #3 to DSP pin
	DDRD18	C2	DQ2	Y	Connected SDRAM #3 to DSP pin
	DDRD19	C8	DQ3	Y	Connected SDRAM #3 to DSP pin
	DDRD20	E3	NF, DQ4	Y	Connected SDRAM #3 to DSP pin
	DDRD21	E8	NF, DQ5	Y	Connected SDRAM #3 to DSP pin
	DDRD22	D2	NF, DQ6	Y	Connected SDRAM #3 to DSP pin
	DDRD23	E7	NF, DQ7	Y	Connected SDRAM #3 to DSP pin
End of Table 30					

Table 31 Pin Connectivity →8 - 16M x8 x8 banks (8G bit total) [2 of 4]

Eight 16 Meg x 8 x 8 banks (8G bit total) [2 of 4]			[MO-207 DT-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD24	B3	DQ0	Y	Connected SDRAM #4 to DSP pin
	DDRD25	C7	DQ1	Y	Connected SDRAM #4 to DSP pin
	DDRD26	C2	DQ2	Y	Connected SDRAM #4 to DSP pin

Table 31 Pin Connectivity →8 - 16M x8 x8 banks (8G bit total) [2 of 4]

Eight 16 Meg x 8 x 8 banks (8G bit total) [2 of 4]			[MO-207 DT-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD27	C8	DQ3	Y	Connected SDRAM #4 to DSP pin
	DDRD28	E3	NF, DQ4	Y	Connected SDRAM #4 to DSP pin
	DDRD29	E8	NF, DQ5	Y	Connected SDRAM #4 to DSP pin
	DDRD30	D2	NF, DQ6	Y	Connected SDRAM #4 to DSP pin
	DDRD31	E7	NF, DQ7	Y	Connected SDRAM #4 to DSP pin
	DDRD32	B3	DQ0	Y	Connected SDRAM #5 to DSP pin
	DDRD33	C7	DQ1	Y	Connected SDRAM #5 to DSP pin
	DDRD34	C2	DQ2	Y	Connected SDRAM #5 to DSP pin
	DDRD35	C8	DQ3	Y	Connected SDRAM #5 to DSP pin
	DDRD36	E3	NF, DQ4	Y	Connected SDRAM #5 to DSP pin
	DDRD37	E8	NF, DQ5	Y	Connected SDRAM #5 to DSP pin
	DDRD38	D2	NF, DQ6	Y	Connected SDRAM #5 to DSP pin
	DDRD39	E7	NF, DQ7	Y	Connected SDRAM #5 to DSP pin
	DDRD40	B3	DQ0	Y	Connected SDRAM #6 to DSP pin
	DDRD41	C7	DQ1	Y	Connected SDRAM #6 to DSP pin
	DDRD42	C2	DQ2	Y	Connected SDRAM #6 to DSP pin
	DDRD43	C8	DQ3	Y	Connected SDRAM #6 to DSP pin
	DDRD44	E3	NF, DQ4	Y	Connected SDRAM #6 to DSP pin
	DDRD45	E8	NF, DQ5	Y	Connected SDRAM #6 to DSP pin
	DDRD46	D2	NF, DQ6	Y	Connected SDRAM #6 to DSP pin
	DDRD47	E7	NF, DQ7	Y	Connected SDRAM #6 to DSP pin
	DDRD48	B3	DQ0	Y	Connected SDRAM #7 to DSP pin
	DDRD49	C7	DQ1	Y	Connected SDRAM #7 to DSP pin
	DDRD50	C2	DQ2	Y	Connected SDRAM #7 to DSP pin
	DDRD51	C8	DQ3	Y	Connected SDRAM #7 to DSP pin
	DDRD52	E3	NF, DQ4	Y	Connected SDRAM #7 to DSP pin
	DDRD53	E8	NF, DQ5	Y	Connected SDRAM #7 to DSP pin
	DDRD54	D2	NF, DQ6	Y	Connected SDRAM #7 to DSP pin
	DDRD55	E7	NF, DQ7	Y	Connected SDRAM #7 to DSP pin
	DDRD56	B3	DQ0	Y	Connected SDRAM #8 to DSP pin
	DDRD57	C7	DQ1	Y	Connected SDRAM #8 to DSP pin
	DDRD58	C2	DQ2	Y	Connected SDRAM #8 to DSP pin
	DDRD59	C8	DQ3	Y	Connected SDRAM #8 to DSP pin
	DDRD60	E3	NF, DQ4	Y	Connected SDRAM #8 to DSP pin
	DDRD61	E8	NF, DQ5	Y	Connected SDRAM #8 to DSP pin
	DDRD62	D2	NF, DQ6	Y	Connected SDRAM #8 to DSP pin
	DDRD63	E7	NF, DQ7	Y	Connected SDRAM #8 to DSP pin
End of Table 31					

Table 32 Pin Connectivity →8 - 16M x8 x8 banks (8G bit total) [3 of 4]

Eight 16 Meg x 8 x 8 banks (8G bit total) [3 of 4]			[MO-207 DT-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	$\overline{\text{DDRCE0}}$	H 2	CS#	Y	Connected SDRAM #1, #2, #3, & #4 to DSP pin
	$\overline{\text{DDRCE1}}$	H 2	CS#	Y	Connected SDRAM #5, #6, #7, & #8 to DSP pin Use only CE1 for dual-rank designs
	DDRBA0	J2	BA0	Y	Connect to like pin between SDRAM and DSP
	DDRBA1	K8	BA1	Y	Connect to like pin between SDRAM and DSP
	DDRBA2	J3	BA2	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRCAS}}$	G3	CAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRRAS}}$	F3	RAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRWE}}$	H 3	WE#	Y	Connect to like pin between SDRAM and DSP
	DDRCKE0	G 9	CKE	Y	Connect to like pin between SDRAM 1-4 and DSP
	DDRCKE1	G 9	CKE	Y	Connect to like pin between SDRAM 5-8 and DSP
	DDRCLKOUTP0	F 7	CK	Y	Connected SDRAM #1, #2, #3, & #4 to DSP pin
	DDRCLKOUTN0	G 7	CK#	Y	Leave unconnected, only for use with dual-rank designs
	DDRCLKOUTP1	F 7	CK	Y	Leave unconnected, only for use with dual-rank designs
	DDRCLKOUTN1	G 7	CK#	Y	Connected SDRAM #5, #6, #7, & #8 to DSP pin^^^
	DDRODT0	G 1	ODT	Y	Connected SDRAM #1–#8 to DSP pin
	DDRODT1	G 1	ODT	Y	Leave unconnected, only for use with dual-rank designs
	DDRSLRATE0			Y	External configuration pin
	DDRSLRATE1			Y	External configuration pin
	DDRCB00			N	
	DDRCB01			N	
	DDRCB02			N	
	DDRCB03			N	
	DDRCB04			N	
	DDRCB05			N	
	DDRCB06			N	
	DDRCB07			N	
	DDRDQM0	C7	DM	Y	Connected SDRAM #1 to DSP pin
	DDRDQM1	C7	DM	Y	Connected SDRAM #2 to DSP pin
	DDRDQM2	C7	DM	Y	Connected SDRAM #3 to DSP pin
	DDRDQM3	C7	DM	Y	Connected SDRAM #4 to DSP pin
	DDRDQM4	C7	DM	Y	Connected SDRAM #5 to DSP pin
	DDRDQM5	C7	DM	Y	Connected SDRAM #6 to DSP pin
	DDRDQM6	C7	DM	Y	Connected SDRAM #7 to DSP pin
	DDRDQM7	C7	DM	Y	Connected SDRAM #8 to DSP pin
	DDRDQM8			N	For ECC connectivity, do not use
	DDRDQS0N	D 3	DQS#	Y	Connected SDRAM #1 to DSP pin
	DDRDQS0P	C 3	DQS	Y	Connected SDRAM #1 to DSP pin
	DDRDQS1N	D 3	DQS#	Y	Connected SDRAM #2 to DSP pin

Table 32 Pin Connectivity →8 - 16M x8 x8 banks (8G bit total) [3 of 4]

Eight 16 Meg x 8 x 8 banks (8G bit total) [3 of 4] [MO-207 DT-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRDQS1P	C 3	DQS	Y	Connected SDRAM #2 to DSP pin
	DDRDQS2N	D 3	DQS#	Y	Connected SDRAM #3 to DSP pin
End of Table 32					

Table 33 Pin Connectivity →8 - 16M x8 x8 banks (8G bit total) [4 of 4]

Eight 16 Meg x 8 x 8 banks (8G bit total) [4 of 4] [MO-207 DT-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRDQS2P	C 3	DQS	Y	Connected SDRAM #3 to DSP pin
	DDRDQS3N	D 3	DQS#	Y	Connected SDRAM #4 to DSP pin
	DDRDQS3P	C 3	DQS	Y	Connected SDRAM #4 to DSP pin
	DDRDQS4N	D 3	DQS#	Y	Connected SDRAM #5 to DSP pin
	DDRDQS4P	C 3	DQS	Y	Connected SDRAM #5 to DSP pin
	DDRDQS5N	D 3	DQS#	Y	Connected SDRAM #6 to DSP pin
	DDRDQS5P	C 3	DQS	Y	Connected SDRAM #6 to DSP pin
	DDRDQS6N	D 3	DQS#	Y	Connected SDRAM #7 to DSP pin
	DDRDQS6P	C 3	DQS	Y	Connected SDRAM #7 to DSP pin
	DDRDQS7N	D 3	DQS#	Y	Connected SDRAM #8 to DSP pin
	DDRDQS7P	C 3	DQS	Y	Connected SDRAM #8 to DSP pin
	DDRDQS8N			N	
	DDRDQS8P			N	
	DDRCLKP			Y	Differential DDR PLL clock input to DSP (+)
	DDRCLKN			Y	Differential DDR PLL clock input to DSP (-)
		H 8	ZQ	Y	Each DDR3 SDRAM ZQ pin should be tied to a 240Ω resistor to ground
	$\overline{\text{DDRREST}}$	N 2	RESET#	Y	DDR3 DSP & SDRAM reset pins
		A 7	TDQS#	Y	Unused if DM is implemented, see data sheet for alternate use
	AVDDA2			Y	DDRCLK PLL Power Supply, connect to dedicated and clean 1.8V (use filter) (DSP pin name may change)
$D_{VDD}15$	See device data manual	A2, A9, D7, G2, G8, K9, M9	VDD	Y	Connect 1.5 V pins to same source
	See device data manual	B9, C1, E2, E9, K1, M1	VddQ	Y	Connected to respective VDD (1.5V) Supply, pay attention to tolerance and sequencing requirements. Should be same supply for both.
	VREFSSTL	J 8	VrefCA	Y	DDR3 Vref pin, connect to DSP DDR3 Vdd/2 (.1% tol.).
					Connect to VDD/2, pay attention to power sequencing requirements
		E 1	VrefDQ	Y	Connect to VDD/2, pay attention to power sequencing requirements
Vss	See device data manual	A1, A8, B1, D8, F8, J1, J9, L1, L9, N1, N9	Vss	Y	Connected to Ground, must be same ground potential as DSP
		B2, B8, C9,D1, D9, F2	VssQ	Y	Connected to Ground, connection MUST be short

Table 33 Pin Connectivity →8 - 16M x8 x8 banks (8G bit total) [4 of 4]

Eight 16 Meg x 8 x 8 banks (8G bit total) [4 of 4]			[MO-207 DT-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	PTV15A			Y	45.3Ω tied to ground (must be short)
		A 3	NC	N	Leave unconnected on both SDRAM
		F 1	NC	N	Leave unconnected on both SDRAM
		F 9	NC	N	Leave unconnected on both SDRAM
		H 1	NC	N	Leave unconnected on both SDRAM
		H 9	NC	N	Leave unconnected on both SDRAM
End of Table 33					

8.1.1.4 Two 32 Meg x 8 x 8 banks (4.096 G bit total)

The following tables illustrate the connectivity for between a KeyStone DSP and two 256M Byte ×8 SDRAMs resulting in a total memory capacity of 512M Bytes. The following four tables define in detail the recommended inner-connectivity for a 16-bit wide bus and between two ×8 2G bit SDRAMs and a Keystone class DSP DDR3 controller. This table is also provided and based on a 78-pin SDRAM package.

Table 34 Pin Connectivity →2 - 32M x8 x8 banks (4G bit total) [1 of 4]

Two 32 Meg x 8 x 8 banks (4G bit total) [1 of 4]			[MO-207 DT-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRA00	K3	A0	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA01	L7	A1	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA02	L3	A2	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA03	K2	A3	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA04	L8	A4	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA05	L2	A5	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA06	M8	A6	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA07	M2	A7	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA08	N8	A8	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA09	M3	A9	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA10	H7	A10/AP	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA11	M7	A11	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA12	K7	A12/BC#	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA13	N3	A13	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA14	N7	A14	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA15			N	Leave unconnected
	DDRD00	B3	DQ0	Y	Connected SDRAM #1 to DSP pin
	DDRD01	C7	DQ1	Y	Connected SDRAM #1 to DSP pin
	DDRD02	C2	DQ2	Y	Connected SDRAM #1 to DSP pin
	DDRD03	C8	DQ3	Y	Connected SDRAM #1 to DSP pin
	DDRD04	E3	DQ4	Y	Connected SDRAM #1 to DSP pin
	DDRD05	E8	DQ5	Y	Connected SDRAM #1 to DSP pin
	DDRD06	D2	DQ6	Y	Connected SDRAM #1 to DSP pin
	DDRD07	E7	DQ7	Y	Connected SDRAM #1 to DSP pin
	DDRD08	B3	DQ0	Y	Connected SDRAM #2 to DSP pin
	DDRD09	C7	DQ1	Y	Connected SDRAM #2 to DSP pin

Table 34 Pin Connectivity →2 - 32M x8 x8 banks (4G bit total) [1 of 4]

Two 32 Meg x 8 x 8 banks (4G bit total) [1 of 4]			[MO-207 DT-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD10	C2	DQ2	Y	Connected SDRAM #2 to DSP pin
	DDRD11	C8	DQ3	Y	Connected SDRAM #2 to DSP pin
	DDRD12	E3	DQ4	Y	Connected SDRAM #2 to DSP pin
	DDRD13	E8	DQ5	Y	Connected SDRAM #2 to DSP pin
	DDRD14	D2	DQ6	Y	Connected SDRAM #2 to DSP pin
	DDRD15	E7	DQ7	Y	Connected SDRAM #2 to DSP pin
	DDRD16			N	Leave unconnected on DSP
	DDRD17			N	Leave unconnected on DSP
	DDRD18			N	Leave unconnected on DSP
	DDRD19			N	Leave unconnected on DSP
	DDRD20			N	Leave unconnected on DSP
	DDRD21			N	Leave unconnected on DSP
	DDRD22			N	Leave unconnected on DSP
End of Table 34					

Table 35 Pin Connectivity →2 - 32M x8 x8 banks (4G bit total) [2 of 4]

Two 32 Meg x 8 x 8 banks (4G bit total) [2 of 4]			[MO-207 DT-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD23			N	Leave unconnected on DSP
	DDRD24			N	Leave unconnected on DSP
	DDRD25			N	Leave unconnected on DSP
	DDRD26			N	Leave unconnected on DSP
	DDRD27			N	Leave unconnected on DSP
	DDRD28			N	Leave unconnected on DSP
	DDRD29			N	Leave unconnected on DSP
	DDRD30			N	Leave unconnected on DSP
	DDRD31			N	Leave unconnected on DSP
	DDRD32			N	Leave unconnected on DSP
	DDRD33			N	Leave unconnected on DSP
	DDRD34			N	Leave unconnected on DSP
	DDRD35			N	Leave unconnected on DSP
	DDRD36			N	Leave unconnected on DSP
	DDRD37			N	Leave unconnected on DSP
	DDRD38			N	Leave unconnected on DSP
	DDRD39			N	Leave unconnected on DSP
	DDRD40			N	Leave unconnected on DSP
	DDRD41			N	Leave unconnected on DSP
	DDRD42			N	Leave unconnected on DSP
	DDRD43			N	Leave unconnected on DSP
	DDRD44			N	Leave unconnected on DSP
	DDRD45			N	Leave unconnected on DSP
	DDRD46			N	Leave unconnected on DSP
	DDRD47			N	Leave unconnected on DSP

Table 35 Pin Connectivity →2 - 32M x8 x8 banks (4G bit total) [2 of 4]

Two 32 Meg x 8 x 8 banks (4G bit total) [2 of 4]			[MO-207 DT-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD48			N	Leave unconnected on DSP
	DDRD49			N	Leave unconnected on DSP
	DDRD50			N	Leave unconnected on DSP
	DDRD51			N	Leave unconnected on DSP
	DDRD52			N	Leave unconnected on DSP
	DDRD53			N	Leave unconnected on DSP
	DDRD54			N	Leave unconnected on DSP
	DDRD55			N	Leave unconnected on DSP
	DDRD56			N	Leave unconnected on DSP
	DDRD57			N	Leave unconnected on DSP
	DDRD58			N	Leave unconnected on DSP
	DDRD59			N	Leave unconnected on DSP
	DDRD60			N	Leave unconnected on DSP
	DDRD61			N	Leave unconnected on DSP
End of Table 35					

Table 36 Pin Connectivity →2 - 32M x8 x8 banks (4G bit total) [3 of 4]

Two 32 Meg x 8 x 8 banks (4G bit total) [3 of 4]			[MO-207 DT-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD62			N	Leave unconnected on DSP
	DDRD63			N	Leave unconnected on DSP
	$\overline{\text{DDRCE0}}$	H 2	CS#	Y	Connected SDRAM #1 & 2 to DSP pin
	$\overline{\text{DDRCE1}}$	H 2	CS#	N	Leave DSP pin unconnected, only for use with dual-rank designs.
	DDRBA0	J2	BA0	Y	Connect to like pin between SDRAM and DSP
	DDRBA1	K8	BA1	Y	Connect to like pin between SDRAM and DSP
	DDRBA2	J3	BA2	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRCAS}}$	G3	CAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRRAS}}$	F3	RAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRWE}}$	H 3	WE#	Y	Connect to like pin between SDRAM and DSP
	DDRCKE0	G 9	CKE	Y	Connect to like pin between SDRAM and DSP
	DDRCKE1	G 9	CKE	N	Leave unconnected at DSP, only for use with dual-rank designs.
	DDRCLKOUTP0	F 7	CK	Y	Connected SDRAM #1 & #2 to DSP pin
	DDRCLKOUTN0	G 7	CK#	Y	Connected SDRAM #1 & #2 to DSP pin
	DDRCLKOUTP1	F 7	CK	N	Leave unconnected at DSP
	DDRCLKOUTN1	G 7	CK#	N	Leave unconnected at DSP
	DDRODT0	G 1	ODT	Y	Connected SDRAM #1 & #2 to DSP pin
	DDRODT1	G 1	ODT	N	Leave unconnected at DSP, only for use with dual-rank designs.
	DDRSLRATE0			Y	External configuration pin
	DDRSLRATE1			Y	External configuration pin
	DDRCB00			N	
	DDRCB01			N	
	DDRCB02			N	
	DDRCB03			N	

Table 36 Pin Connectivity →2 - 32M x8 x8 banks (4G bit total) [3 of 4]

Two 32 Meg x 8 x 8 banks (4G bit total) [3 of 4]			[MO-207 DT-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRCB04			N	
	DDRCB05			N	
	DDRCB06			N	
	DDRCB07			N	
	DDRDQM0	B 7	DM	Y	Connected SDRAM #1 to DSP pin
	DDRDQM1	B 7	DM	Y	Connected SDRAM #2 to DSP pin
	DDRDQM2			N	
	DDRDQM3			N	
	DDRDQM4			N	
	DDRDQM5			N	
	DDRDQM6			N	
	DDRDQM7			N	
	DDRDQM8			N	
	DDRDQS0N	D 3	DQS#	Y	Connected SDRAM #1 to DSP pin
	DDRDQS0P	C 3	DQS	Y	Connected SDRAM #1 to DSP pin
End of Table 36					

Table 37 Pin Connectivity →2 - 32M x8 x8 banks (4G bit total) [4 of 4]

Two 32 Meg x 8 x 8 banks (4G bit total) [4 of 4]			[MO-207 DT-z Package w/o support pins]		
DSP Name	**DSP Pin**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRDQS1N	D 3	DQS#	Y	Connected SDRAM #2 to DSP pin
	DDRDQS1P	C 3	DQS	Y	Connected SDRAM #2 to DSP pin
	DDRDQS2N			N	
	DDRDQS2P			N	
	DDRDQS3N			N	
	DDRDQS3P			N	
	DDRDQS4N			N	
	DDRDQS4P			N	
	DDRDQS5N			N	
	DDRDQS5P			N	
	DDRDQS6N			N	
	DDRDQS6P			N	
	DDRDQS7N			N	
	DDRDQS7P			N	
	DDRDQS8N			N	
	DDRDQS8P			N	
	DDRCLKP			Y	Differential DDR PLL clock input to DSP (+)
	DDRCLKN			Y	Differential DDR PLL clock input to DSP (-)
		H 8	ZQ	Y	Each DDR3 SDRAM ZQ pin should be tied to a 240Ω resistor to ground
	$\overline{\text{DDRREST}}$	N 2	RESET#	Y	DDR3 DSP & SDRAM reset pins
		A 7	TDQS#	Y	Unused if DM is implemented, see data sheet for alternate use

Table 37 Pin Connectivity →2 - 32M x8 x8 banks (4G bit total) [4 of 4]

Two 32 Meg x 8 x 8 banks (4G bit total) [4 of 4]			[MO-207 DT-z Package w/o support pins]		
DSP Name	**DSP Pin**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	AVDDA2			Y	DDRCLK PLL Power Supply, connect to dedicated and clean 1.8V (use filter)
$D_{VDD}15$	See device data manual	A2, A9, D7, G2, G8, K9, M9	VDD	Y	Connect 1.5 V pins to same source
	See device data manual	B9, C1, E2, E9, K1, M1	VddQ	Y	Connected to respective VDD (1.5V) Supply, pay attention to tolerance and sequencing requirements. Should be same supply for both.
	VREFSSTL	J 8	VrefCA	Y	DDR3 Vref pin, connect to DSP DDR3 Vdd/2 (.1% tol.).
					Connect to VDD/2, pay attention to power sequencing requirements
		E 1	VrefDQ	Y	Connect to VDD/2, pay attention to power sequencing requirements
Vss	See device data manual	A1, A8, B1, D8, F8, J1, J9, L1, L9, N1, N9	Vss	Y	Connected to Ground, must be same ground potential as DSP
		B2, B8, C9,D1, D9, F2	VssQ	Y	Connected to Ground, connection MUST be short
	PTV15A			Y	45.3Ω tied to ground (must be short)
		A 3	NC	N	Leave unconnected on both SDRAM
		F 1	NC	N	Leave unconnected on both SDRAM
		F 9	NC	N	Leave unconnected on both SDRAM
		H 1	NC	N	Leave unconnected on both SDRAM
		H 9	NC	N	Leave unconnected on both SDRAM
End of Table 37					

8.1.1.5 Four 16 Meg x 8 x 8 banks x 2 Ranks (4.096 G bit total)

The following tables illustrate the connectivity for between a KeyStone DSP and four 128M Byte ×8 SDRAMs configured as a dual rank design which results in a total memory capacity of 512M Bytes. The following four tables define in detail the recommended inner-connectivity for a 16-bit wide bus and between four ×8 1G bit SDRAMs and a Keystone class DSP DDR3 controller. This table is also provided and based on a 78-pin SDRAM package.

Table 38 Pin Connectivity →4 - 16M x8 x8 banks x 2 Ranks (4G bit total) [1 of 4]

Four 16 Meg x 8 x 8 banks x 2 Ranks (4G bit total) [1 of 4]			[MO-207 DT-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRA00	K3	A0	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA01	L7	A1	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA02	L3	A2	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA03	K2	A3	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA04	L8	A4	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA05	L2	A5	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA06	M8	A6	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA07	M2	A7	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA08	N8	A8	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA09	M3	A9	Y	Connect Controller Address pin to all SDRAMs with like name

Table 38 Pin Connectivity →4 - 16M x8 x8 banks x 2 Ranks (4G bit total) [1 of 4]

Four 16 Meg x 8 x 8 banks x 2 Ranks (4G bit total) [1 of 4] [MO-207 DT-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRA10	H7	A10/AP	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA11	M7	A11	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA12	K7	A12/BC#	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA13	N3	A13	Y	Connect Controller Address pin to all SDRAMs with like name
	DDRA14			N	Leave unconnected
	DDRA15			N	Leave unconnected
	DDRD00	B3	DQ0	Y	Connect between SDRAM #1 & #3 to DSP pin
	DDRD01	C7	DQ1	Y	Connect between SDRAM #1 & #3 to DSP pin
	DDRD02	C2	DQ2	Y	Connect between SDRAM #1 & #3 to DSP pin
	DDRD03	C8	DQ3	Y	Connect between SDRAM #1 & #3 to DSP pin
	DDRD04	E3	DQ4	Y	Connect between SDRAM #1 & #3 to DSP pin
	DDRD05	E8	DQ5	Y	Connect between SDRAM #1 & #3 to DSP pin
	DDRD06	D2	DQ6	Y	Connect between SDRAM #1 & #3 to DSP pin
	DDRD07	E7	DQ7	Y	Connect between SDRAM #1 & #3 to DSP pin
	DDRD08	B3	DQ0	Y	Connect between SDRAM #2 & #4 to DSP pin
	DDRD09	C7	DQ1	Y	Connect between SDRAM #2 & #4 to DSP pin
	DDRD10	C2	DQ2	Y	Connect between SDRAM #2 & #4 to DSP pin
	DDRD11	C8	DQ3	Y	Connect between SDRAM #2 & #4 to DSP pin
	DDRD12	E3	DQ4	Y	Connect between SDRAM #2 & #4 to DSP pin
	DDRD13	E8	DQ5	Y	Connect between SDRAM #2 & #4 to DSP pin
	DDRD14	D2	DQ6	Y	Connect between SDRAM #2 & #4 to DSP pin
	DDRD15	E7	DQ7	Y	Connect between SDRAM #2 & #4 to DSP pin
	DDRD16			N	Leave unconnected
	DDRD17			N	Leave unconnected
	DDRD18			N	Leave unconnected
	DDRD19			N	Leave unconnected
	DDRD20			N	Leave unconnected
	DDRD21			N	Leave unconnected
	DDRD22			N	Leave unconnected
	DDRD23			N	Leave unconnected
End of Table 38					

Table 39 Pin Connectivity →4 - 16M x8 x8 banks x 2 Ranks (4G bit total) [2 of 4]

Four 16 Meg x 8 x 8 banks x 2 Ranks (4G bit total) [2 of 4] [MO-207 DT-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD24			N	Leave unconnected
	DDRD25			N	Leave unconnected
	DDRD26			N	Leave unconnected
	DDRD27			N	Leave unconnected
	DDRD28			N	Leave unconnected

Table 39 Pin Connectivity →4 - 16M x8 x8 banks x 2 Ranks (4G bit total) [2 of 4]

Four 16 Meg x 8 x 8 banks x 2 Ranks (4G bit total) [2 of 4] [MO-207 DT-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD29			N	Leave unconnected
	DDRD30			N	Leave unconnected
	DDRD31			N	Leave unconnected
	DDRD32			N	Leave unconnected
	DDRD33			N	Leave unconnected
	DDRD34			N	Leave unconnected
	DDRD35			N	Leave unconnected
	DDRD36			N	Leave unconnected
	DDRD37			N	Leave unconnected
	DDRD38			N	Leave unconnected
	DDRD39			N	Leave unconnected
	DDRD40			N	Leave unconnected
	DDRD41			N	Leave unconnected
	DDRD42			N	Leave unconnected
	DDRD43			N	Leave unconnected
	DDRD44			N	Leave unconnected
	DDRD45			N	Leave unconnected
	DDRD46			N	Leave unconnected
	DDRD47			N	Leave unconnected
	DDRD48			N	Leave unconnected
	DDRD49			N	Leave unconnected
	DDRD50			N	Leave unconnected
	DDRD51			N	Leave unconnected
	DDRD52			N	Leave unconnected
	DDRD53			N	Leave unconnected
	DDRD54			N	Leave unconnected
	DDRD55			N	Leave unconnected
	DDRD56			N	Leave unconnected
	DDRD57			N	Leave unconnected
	DDRD58			N	Leave unconnected
	DDRD59			N	Leave unconnected
	DDRD60			N	Leave unconnected
	DDRD61			N	Leave unconnected
	DDRD62			N	Leave unconnected
	DDRD63			N	Leave unconnected
End of Table 39					

Table 40 Pin Connectivity →4 - 16M x8 x8 banks x 2 Ranks (4G bit total) [3 of 4]

Four 16 Meg x 8 x 8 banks x 2 Ranks (4G bit total) [3 of 4] [MO-207 DT-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	$\overline{\text{DDRCE0}}$	H 2	CS0#	Y	Connect between SDRAM #1 & #2 to DSP pin
	$\overline{\text{DDRCE1}}$	H 1	CS1#	Y	Leave unconnected, only for use with dual-rank designs
	DDRBA0	J2	BA0	Y	Connect to like pins between SDRAMs and DSP
	DDRBA1	K8	BA1	Y	Connect to like pins between SDRAMs and DSP
	DDRBA2	J3	BA2	Y	Connect to like pins between SDRAMs and DSP
	$\overline{\text{DDRCAS}}$	G3	CAS#	Y	Connect to like pins between SDRAMs and DSP
	$\overline{\text{DDRRAS}}$	F3	RAS#	Y	Connect to like pins between SDRAMs and DSP
	$\overline{\text{DDRWE}}$	H3	WE#	Y	Connect to like pins between SDRAMs and DSP
	DDRCKE0	G 9	CKE0	Y	Connect between SDRAM #1–#4 like pin to DSP pin
	DDRCKE1	F 9	CKE1	Y	Leave unconnected, only for use with dual-rank designs
	DDRCLKOUTP0	F7	CK	Y	Connect between SDRAM #1–#4 to DSP pin
	DDRCLKOUTN0	G7	CK#	Y	Connect between SDRAM #1–#4 to DSP pin
	DDRCLKOUTP1	F 7	CK	Y	Leave unconnected, only for use with dual-rank designs
	DDRCLKOUTN1	G 7	CK#	Y	Leave unconnected, only for use with dual-rank designs
	DDRODT0	G1	ODT0	Y	Connect between SDRAM #1–#4 to DSP pin
	DDRODT1	F1	ODT1	Y	Leave unconnected, only for use with dual-rank designs
	DDRSLRATE0			Y	External configuration pin
	DDRSLRATE1			Y	External configuration pin
	DDRCB00			N	Leave unconnected on DSP
	DDRCB01			N	Leave unconnected on DSP
	DDRCB02			N	Leave unconnected on DSP
	DDRCB03			N	Leave unconnected on DSP
	DDRCB04			N	Leave unconnected on DSP
	DDRCB05			N	Leave unconnected on DSP
	DDRCB06			N	Leave unconnected on DSP
	DDRCB07			N	Leave unconnected on DSP
	DDRDQM0	A7	DM	Y	Connect between SDRAM #1 & #3 to DSP pin
	DDRDQM1	A7	DM	Y	Connect between SDRAM #2 & #4 to DSP pin
	DDRDQM2			N	Leave unconnected on DSP
	DDRDQM3			N	Leave unconnected on DSP
	DDRDQM4			N	Leave unconnected on DSP
	DDRDQM5			N	Leave unconnected on DSP
	DDRDQM6			N	Leave unconnected on DSP
	DDRDQM7			N	Leave unconnected on DSP
	DDRDQM8			N	Leave unconnected on DSP
	DDRDQS0N	D 3	DQS#	Y	Connected SDRAM #1 & #3 to DSP pin
	DDRDQS0P	C 3	DQS	Y	Connected SDRAM #1 & #3 to DSP pin
	DDRDQS1N	D 3	DQS#	Y	Connected SDRAM #2 & #4 to DSP pin
	DDRDQS1P	C 3	DQS	Y	Connected SDRAM #2 & #4 to DSP pin
End of Table 40					

Table 41 Pin Connectivity →4 - 16M x8 x8 banks x 2 Ranks (4G bit total) [4 of 4]

Four 16 Meg x 8 x 8 banks x 2 Ranks (4G bit total) [4 of 4] [MO-207 DT-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRDQS2N			N	Leave unconnected on DSP
	DDRDQS2P			N	Leave unconnected on DSP
	DDRDQS3N			N	Leave unconnected on DSP
	DDRDQS3P			N	Leave unconnected on DSP
	DDRDQS4N			N	Leave unconnected on DSP
	DDRDQS4P			N	Leave unconnected on DSP
	DDRDQS5N			N	Leave unconnected on DSP
	DDRDQS5P			N	Leave unconnected on DSP
	DDRDQS6N			N	Leave unconnected on DSP
	DDRDQS6P			N	Leave unconnected on DSP
	DDRDQS7N			N	Leave unconnected on DSP
	DDRDQS7P			N	Leave unconnected on DSP
	DDRDQS8N			N	Leave unconnected on DSP
	DDRDQS8P			N	Leave unconnected on DSP
	DDRCLKP			Y	Differential DDR PLL clock input to DSP (+)
	DDRCLKN			Y	Differential DDR PLL clock input to DSP (-)
		H 8	ZQ0	Y	DDR3 SDRAM ZQ0 pin should be tied to a 240Ω resistor to ground
		H 9	ZQ1	Y	DDR3 SDRAM ZQ1 pin should be tied to a 240Ω resistor to ground
	$\overline{\text{DDRREST}}$	N 2	RESET#	Y	DDR3 DSP & SDRAM reset pins
		B 7	TDQS	Y	Unused if DM is implemented, see data sheet for alternate use
		A 7	TDQS#	Y	Unused if DM is implemented, see data sheet for alternate use
	AVDDA2			Y	DDRCLK PLL Power Supply, connect to dedicated and clean 1.8V (use filter)
	$D_{VDD}15$	A2, A9, D7, G2, G8 K9 M9	VDD	Y	Connect 1.5 V pins to same source
		B9, C1, E2 E9, K1, M1	VddQ	Y	Connected to respective VDD (1.5V) Supply, pay attention to tolerance and sequencing requirements. Should be same supply for both.
	VREFSSTL	J 8	VrefCA	Y	DDR3 Vref pin, connect to DSP DDR3 Vdd/2 (.1% tol.).
					Connect to VDD/2, pay attention to power sequencing requirements
		E 1	VrefDQ	Y	Connect to VDD/2, pay attention to power sequencing requirements
	Vss	A1, A8 B1, D8, F8, J1 J9 L1, L9, N1, N9	Vss	Y	Connected to Ground, must be same ground potential as DSP
		B2, B8 C9, D1, D9, F2	VssQ	Y	Connected to Ground, connection MUST be short
	PTV15A			Y	45.3Ω tied to ground (must be short)
		A 3	NC	N	Leave unconnected on all SDRAMs
		N 3	NC	N	Leave unconnected on all SDRAMs
End of Table 41					

8.1.1.6 One 8 Meg x 16 x 8 banks x 2 Ranks (4.096G bit total)

The following tables illustrate the connectivity between a KeyStone DSP and one 128M Byte ×8 SDRAM which results in a total memory capacity of 128M Bytes. The following four tables define in detail the recommended inner-connectivity for a 16 bit wide bus and between one ×16 1G bit SDRAM and a Keystone class DSP DDR3 controller. This table is also provided and based on a 96-pin SDRAM package.

Table 42 Pin Connectivity →1 - 8M x16 x8 banks (1G bit total) [1 of 4]

One 8 Meg x 16 x 8 banks (1G bit total) [1 of 4]			[MO-207 DU-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRA00	N3	A0	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA01	P7	A1	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA02	P3	A2	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA03	N2	A3	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA04	P8	A4	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA05	P2	A5	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA06	R8	A6	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA07	R2	A7	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA08	T8	A8	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA09	R3	A9	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA10	L7	A10/AP	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA11	R7	A11	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA12	N7	A12/BC#	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA13	T3	A13	N	Leave unconnected
	DDRA14	T7	A14	N	Leave unconnected
	DDRA15	M7	A15	N	Leave unconnected
	DDRD00	E3	DQL0	Y	Connected SDRAM #1 to DSP pin
	DDRD01	F7	DQL1	Y	Connected SDRAM #1 to DSP pin
	DDRD02	F2	DQL2	Y	Connected SDRAM #1 to DSP pin
	DDRD03	F8	DQL3	Y	Connected SDRAM #1 to DSP pin
	DDRD04	H3	DQL4	Y	Connected SDRAM #1 to DSP pin
	DDRD05	H8	DQL5	Y	Connected SDRAM #1 to DSP pin
	DDRD06	G2	DQL6	Y	Connected SDRAM #1 to DSP pin
	DDRD07	H7	DQL7	Y	Connected SDRAM #1 to DSP pin
	DDRD08	D7	DQU0	Y	Connected SDRAM #1 to DSP pin
	DDRD09	C3	DQU1	Y	Connected SDRAM #1 to DSP pin
	DDRD10	C8	DQU2	Y	Connected SDRAM #1 to DSP pin
	DDRD11	C2	DQU3	Y	Connected SDRAM #1 to DSP pin
	DDRD12	A7	DQU4	Y	Connected SDRAM #1 to DSP pin
	DDRD13	A2	DQU5	Y	Connected SDRAM #1 to DSP pin
	DDRD14	B8	DQU6	Y	Connected SDRAM #1 to DSP pin
	DDRD15	A3	DQU7	Y	Connected SDRAM #1 to DSP pin
	DDRD16			N	Leave DSP pin unconnected
	DDRD17			N	Leave DSP pin unconnected
	DDRD18			N	Leave DSP pin unconnected
	DDRD19			N	Leave DSP pin unconnected
	DDRD20			N	Leave DSP pin unconnected

Table 42 Pin Connectivity →1 - 8M x16 x8 banks (1G bit total) [1 of 4]

One 8 Meg x 16 x 8 banks (1G bit total) [1 of 4]		[MO-207 DU-z Package w/o support pins]			
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD21			N	Leave DSP pin unconnected
	DDRD22			N	Leave DSP pin unconnected
	DDRD23			N	Leave DSP pin unconnected
End of Table 42					

Table 43 Pin Connectivity →1 - 8M x16 x8 banks (1G bit total) [2 of 4]

One 8 Meg x 16 x 8 banks (1G bit total) [2 of 4]		[MO-207 DU-z Package w/o support pins]			
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD24			N	Leave DSP pin unconnected
	DDRD25			N	Leave DSP pin unconnected
	DDRD26			N	Leave DSP pin unconnected
	DDRD27			N	Leave DSP pin unconnected
	DDRD28			N	Leave DSP pin unconnected
	DDRD29			N	Leave DSP pin unconnected
	DDRD30			N	Leave DSP pin unconnected
	DDRD31			N	Leave DSP pin unconnected
	DDRD32			N	Leave DSP pin unconnected
	DDRD33			N	Leave DSP pin unconnected
	DDRD34			N	Leave DSP pin unconnected
	DDRD35			N	Leave DSP pin unconnected
	DDRD36			N	Leave DSP pin unconnected
	DDRD37			N	Leave DSP pin unconnected
	DDRD38			N	Leave DSP pin unconnected
	DDRD39			N	Leave DSP pin unconnected
	DDRD40			N	Leave DSP pin unconnected
	DDRD41			N	Leave DSP pin unconnected
	DDRD42			N	Leave DSP pin unconnected
	DDRD43			N	Leave DSP pin unconnected
	DDRD44			N	Leave DSP pin unconnected
	DDRD45			N	Leave DSP pin unconnected
	DDRD46			N	Leave DSP pin unconnected
	DDRD47			N	Leave DSP pin unconnected
	DDRD48			N	Leave DSP pin unconnected
	DDRD49			N	Leave DSP pin unconnected
	DDRD50			N	Leave DSP pin unconnected
	DDRD51			N	Leave DSP pin unconnected
	DDRD52			N	Leave DSP pin unconnected
	DDRD53			N	Leave DSP pin unconnected
	DDRD54			N	Leave DSP pin unconnected
	DDRD55			N	Leave DSP pin unconnected
	DDRD56			N	Leave DSP pin unconnected
	DDRD57			N	Leave DSP pin unconnected
	DDRD58			N	Leave DSP pin unconnected
	DDRD59			N	Leave DSP pin unconnected

Table 43 Pin Connectivity →1 - 8M x16 x8 banks (1G bit total) [2 of 4]

One 8 Meg x 16 x 8 banks (1G bit total) [2 of 4] [MO-207 DU-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD60			N	Leave DSP pin unconnected
	DDRD61			N	Leave DSP pin unconnected
	DDRD62			N	Leave DSP pin unconnected
	DDRD63			N	Leave DSP pin unconnected
End of Table 43					

Table 44 Pin Connectivity →1 - 8M x16 x8 banks (1G bit total) [3 of 4]

One 8 Meg x 16 x 8 banks (1G bit total) [3 of 4] [MO-207 DU-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	$\overline{\text{DDRCE0}}$	L2	CS#	Y	Connected SDRAM #1 to DSP pin
	$\overline{\text{DDRCE1}}$			N	Leave unconnected, only for use with dual-rank designs
	DDRBA0	M2	BA0	Y	Connect to like pin between SDRAM and DSP
	DDRBA1	N8	BA1	Y	Connect to like pin between SDRAM and DSP
	DDRBA2	M3	BA2	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRCAS}}$	K3	CAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRRAS}}$	J3	RAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRWE}}$	L3	WE#	Y	Connect to like pin between SDRAM and DSP
	DDRCKE0	K9	CKE	Y	Connect to like pin between SDRAM and DSP
	DDRCKE1	K9	CKE	N	Leave unconnected, only for use with dual-rank designs
	DDRCLKOUTP0	J7	CK	Y	Connected SDRAM #1 to DSP pin
	DDRCLKOUTN0	K7	CK#	Y	Connected SDRAM #1 to DSP pin
	DDRCLKOUTP1			N	Leave unconnected, only for use with dual-rank designs
	DDRCLKOUTN1			N	Leave unconnected, only for use with dual-rank designs
	DDRODT0	K 1	ODT	Y	Connected SDRAM #1 to DSP pin
	DDRODT1			N	Leave unconnected, only for use with dual-rank designs
	DDRSLRATE0			N	Under software or hardware control
	DDRSLRATE1			N	Under software or hardware control
	DDRCB00			N	
	DDRCB01			N	
	DDRCB02			N	
	DDRCB03			N	
	DDRCB04			N	
	DDRCB05			N	
	DDRCB06			N	
	DDRCB07			N	
	DDRDQM0	LDM	E7	Y	Connected SDRAM #1 to DSP pin
	DDRDQM1	UDM	D3	Y	Connected SDRAM #1 to DSP pin
	DDRDQM2			N	
	DDRDQM3			N	
	DDRDQM4			N	
	DDRDQM5			N	
	DDRDQM6			N	
	DDRDQM7			N	

Table 44 Pin Connectivity →1 - 8M x16 x8 banks (1G bit total) [3 of 4]

One 8 Meg x 16 x 8 banks (1G bit total) [3 of 4]			[MO-207 DU-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRDQM8			N	
	DDRDQS0N	G 3	LDQS#	Y	Connected SDRAM #1 to DSP pin
	DDRDQS0P	F 3	LDQS	Y	Connected SDRAM #1 to DSP pin
	DDRDQS1N	B7	UDQS#	Y	Connected SDRAM #1 to DSP pin
	DDRDQS1P	C7	UDQS	Y	Connected SDRAM #1 to DSP pin
	DDRDQS2N			N	
End of Table 44					

Table 45 Pin Connectivity →1 - 8M x16 x8 banks (1G bit total) [4 of 4]

One 8 Meg x 16 x 8 banks (1G bit total) [4 of 4]			[MO-207 DU-z Package w/o support pins]		
DSP Name	**DSP Pin**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRDQS2P			N	
	DDRDQS3N			N	
	DDRDQS3P			N	
	DDRDQS4N			N	
	DDRDQS4P			N	
	DDRDQS5N			N	
	DDRDQS5P			N	
	DDRDQS6N			N	
	DDRDQS6P			N	
	DDRDQS7N			N	
	DDRDQS7P			N	
	DDRDQS8N			N	
	DDRDQS8P			N	
	DDRCLKP			Y	Differential DDR PLL clock input to DSP (+)
	DDRCLKN			Y	Differential DDR PLL clock input to DSP (-)
		L 8	ZQ	Y	Each DDR3 SDRAM ZQ pin should be tied to a 240Ω resistor to ground
	$\overline{\text{DDRREST}}$	T 2	RESET#	Y	DDR3 DSP & SDRAM reset pins
	AVDDA2			Y	DDRCLK PLL Power Supply, connect to dedicated and clean 1.8V (use filter)
$D_{VDD}15$	See device data manual	B2, D9, G7, K2, K8, N1, N9, R1, R9	Vdd	Y	Connected to respective VDD (1.5V) Supply, pay attention to tolerance and sequencing requirements
	See device data manual	A1, A8, C1, C9, D2, E9, F1, H2, H9	VddQ	Y	Connected to respective VDD (1.5V) Supply, pay attention to tolerance and sequencing requirements
		H 1	VrefDQ	Y	Connect to VDD/2, pay attention to power sequencing requirements
Vss	See device data manual	A9, B3, E1, G8, J2, J8, M1, M9, P1, P9, T1, T9	Vss	Y	Connected to Ground
	See device data manual	B1, B9, D1, D8, E2, E8, F9, G1, G9	VssQ	Y	Connected to Ground, connection MUST be short
	VREFSSTL	M 8	VrefCA	Y	DDR3 Vref pin, connect to DSP DDR3 Vdd/2 (.1% tol.).
					Connect to VDD/2, pay attention to power sequencing requirements

Table 45 Pin Connectivity →1 - 8M x16 x8 banks (1G bit total) [4 of 4]

One 8 Meg x 16 x 8 banks (1G bit total) [4 of 4] [MO-207 DU-z Package w/o support pins]					
DSP Name	**DSP Pin**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	PTV15A			Y	45.3Ω tied to ground (must be short)
		J1	NC	N	Leave unconnected on all SDRAMs
		J9	NC	N	Leave unconnected on all SDRAMs
		L1	NC	N	Leave unconnected on all SDRAMs
		L9	NC	N	Leave unconnected on all SDRAMs
End of Table 45					

8.1.1.7 Two 8 Meg x 16 x 8 banks (2.048G bit total)

The following tables illustrate the connectivity for between a KeyStone DSP and two 128M Byte ×8 SDRAMs which results in a total memory capacity of 256M Bytes. The following four tables define in detail the recommended inner-connectivity for a 32 bit wide bus and between two ×16 1G bit SDRAMs and a Keystone class DSP DDR3 controller. This table is also provided and based on a 96-pin SDRAM package.

Table 46 Pin Connectivity →2 - 8M x16 x8 banks (2G bit total) [1 of 4]

Two 8 Meg x 16 x 8 banks (2G bit total) [1 of 4] [MO-207 DU-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRA00	N3	A0	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA01	P7	A1	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA02	P3	A2	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA03	N2	A3	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA04	P8	A4	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA05	P2	A5	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA06	R8	A6	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA07	R2	A7	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA08	T8	A8	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA09	R3	A9	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA10	L7	A10/AP	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA11	R7	A11	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA12	N7	A12/BC#	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA13	T3	A13	N	Leave unconnected
	DDRA14	T7	A14	N	Leave unconnected
	DDRA15	M7	A15	N	Leave unconnected
	DDRD00	E3	DQL0	Y	Connected SDRAM #1 to DSP pin
	DDRD01	F7	DQL1	Y	Connected SDRAM #1 to DSP pin
	DDRD02	F2	DQL2	Y	Connected SDRAM #1 to DSP pin
	DDRD03	F8	DQL3	Y	Connected SDRAM #1 to DSP pin
	DDRD04	H3	DQL4	Y	Connected SDRAM #1 to DSP pin
	DDRD05	H8	DQL5	Y	Connected SDRAM #1 to DSP pin
	DDRD06	G2	DQL6	Y	Connected SDRAM #1 to DSP pin
	DDRD07	H7	DQL7	Y	Connected SDRAM #1 to DSP pin
	DDRD08	D7	DQU0	Y	Connected SDRAM #1 to DSP pin
	DDRD09	C3	DQU1	Y	Connected SDRAM #1 to DSP pin

Table 46 Pin Connectivity →2 - 8M x16 x8 banks (2G bit total) [1 of 4]

Two 8 Meg x 16 x 8 banks (2G bit total) [1 of 4] [MO-207 DU-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD10	C8	DQU2	Y	Connected SDRAM #1 to DSP pin
	DDRD11	C2	DQU3	Y	Connected SDRAM #1 to DSP pin
	DDRD12	A7	DQU4	Y	Connected SDRAM #1 to DSP pin
	DDRD13	A2	DQU5	Y	Connected SDRAM #1 to DSP pin
	DDRD14	B8	DQU6	Y	Connected SDRAM #1 to DSP pin
	DDRD15	A3	DQU7	Y	Connected SDRAM #1 to DSP pin
	DDRD16	E3	DQL0	Y	Connected SDRAM #2 to DSP pin
	DDRD17	F7	DQL1	Y	Connected SDRAM #2 to DSP pin
	DDRD18	F2	DQL2	Y	Connected SDRAM #2 to DSP pin
	DDRD19	F8	DQL3	Y	Connected SDRAM #2 to DSP pin
	DDRD20	H3	DQL4	Y	Connected SDRAM #2 to DSP pin
	DDRD21	H8	DQL5	Y	Connected SDRAM #2 to DSP pin
	DDRD22	G2	DQL6	Y	Connected SDRAM #2 to DSP pin
	DDRD23	H7	DQL7	Y	Connected SDRAM #2 to DSP pin
End of Table 46					

Table 47 Pin Connectivity →2 - 8M x16 x8 banks (2G bit total) [2 of 4]

Two 8 Meg x 16 x 8 banks (2G bit total) [2 of 4] [MO-207 DU-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD24	D7	DQU0	Y	Connected SDRAM #2 to DSP pin
	DDRD25	C3	DQU1	Y	Connected SDRAM #2 to DSP pin
	DDRD26	C8	DQU2	Y	Connected SDRAM #2 to DSP pin
	DDRD27	C2	DQU3	Y	Connected SDRAM #2 to DSP pin
	DDRD28	A7	DQU4	Y	Connected SDRAM #2 to DSP pin
	DDRD29	A2	DQU5	Y	Connected SDRAM #2 to DSP pin
	DDRD30	B8	DQU6	Y	Connected SDRAM #2 to DSP pin
	DDRD31	A3	DQU7	Y	Connected SDRAM #2 to DSP pin
	DDRD32			N	Leave DSP pin unconnected
	DDRD33			N	Leave DSP pin unconnected
	DDRD34			N	Leave DSP pin unconnected
	DDRD35			N	Leave DSP pin unconnected
	DDRD36			N	Leave DSP pin unconnected
	DDRD37			N	Leave DSP pin unconnected
	DDRD38			N	Leave DSP pin unconnected
	DDRD39			N	Leave DSP pin unconnected
	DDRD40			N	Leave DSP pin unconnected
	DDRD41			N	Leave DSP pin unconnected
	DDRD42			N	Leave DSP pin unconnected
	DDRD43			N	Leave DSP pin unconnected
	DDRD44			N	Leave DSP pin unconnected
	DDRD45			N	Leave DSP pin unconnected
	DDRD46			N	Leave DSP pin unconnected

Table 47 Pin Connectivity →2 - 8M x16 x8 banks (2G bit total) [2 of 4]

Two 8 Meg x 16 x 8 banks (2G bit total) [2 of 4] [MO-207 DU-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD47			N	Leave DSP pin unconnected
	DDRD48			N	Leave DSP pin unconnected
	DDRD49			N	Leave DSP pin unconnected
	DDRD50			N	Leave DSP pin unconnected
	DDRD51			N	Leave DSP pin unconnected
	DDRD52			N	Leave DSP pin unconnected
	DDRD53			N	Leave DSP pin unconnected
	DDRD54			N	Leave DSP pin unconnected
	DDRD55			N	Leave DSP pin unconnected
	DDRD56			N	Leave DSP pin unconnected
	DDRD57			N	Leave DSP pin unconnected
	DDRD58			N	Leave DSP pin unconnected
	DDRD59			N	Leave DSP pin unconnected
	DDRD60			N	Leave DSP pin unconnected
	DDRD61			N	Leave DSP pin unconnected
	DDRD62			N	Leave DSP pin unconnected
End of Table 47					

Table 48 Pin Connectivity →2 - 8M x16 x8 banks (2G bit total) [3 of 4]

Two 8 Meg x 16 x 8 banks (2G bit total) [3 of 4] [MO-207 DU-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD63			N	Leave DSP pin unconnected
	$\overline{\text{DDRCE0}}$	L 2	CS#	Y	Connected SDRAM #1 & #2 to DSP pin
	$\overline{\text{DDRCE1}}$	L 2	CS#	N	Leave unconnected, only for use with dual-rank designs
	DDRBA0	M2	BA0	Y	Connect to like pin between SDRAM and DSP
	DDRBA1	N8	BA1	Y	Connect to like pin between SDRAM and DSP
	DDRBA2	M3	BA2	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRCAS}}$	K 3	CAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRRAS}}$	J 3	RAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRWE}}$	L 3	WE#	Y	Connect to like pin between SDRAM and DSP
	DDRCKE0	K 9	CKE	Y	Connect to like pin between SDRAM and DSP
	DDRCKE1	K 9	CKE	N	Leave unconnected, only for use with dual-rank designs
	DDRCLKOUTP0	J 7	CK	Y	Connected SDRAM #1 & #2 to DSP pin
	DDRCLKOUTN0	K 7	CK#	Y	Connected SDRAM #1 & #2 to DSP pin
	DDRCLKOUTP1	J 7	CK	N	Leave unconnected, only for use with dual-rank designs
	DDRCLKOUTN1	K 7	CK#	N	Leave unconnected, only for use with dual-rank designs
	DDRODT0	K 1	ODT	Y	Connected SDRAM #1& #2 to DSP pin
	DDRODT1	K 1	ODT	N	Leave unconnected, only for use with dual-rank designs
	DDRSLRATE0			N	Under software or hardware control
	DDRSLRATE1			N	
	DDRCB00			N	
	DDRCB01			N	

Table 48 Pin Connectivity →2 - 8M x16 x8 banks (2G bit total) [3 of 4]

Two 8 Meg x 16 x 8 banks (2G bit total) [3 of 4] [MO-207 DU-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRCB02			N	
	DDRCB03			N	
	DDRCB04			N	
	DDRCB05			N	
	DDRCB06			N	
	DDRCB07			N	
	DDRDQM0	LDM	E7	Y	Connected SDRAM #1 to DSP pin
	DDRDQM1	UDM	D3	Y	Connected SDRAM #1 to DSP pin
	DDRDQM2	LDM	E7	Y	Connected SDRAM #2 to DSP pin
	DDRDQM3	UDM	D3	Y	Connected SDRAM #2 to DSP pin
	DDRDQM4			N	
	DDRDQM5			N	
	DDRDQM6			N	
	DDRDQM7			N	
	DDRDQM8			N	
	DDRDQS0N	G 3	LDQS#	Y	Connected SDRAM #1 to DSP pin
	DDRDQS0P	F 3	LDQS	Y	Connected SDRAM #1 to DSP pin
	DDRDQS1N	B7	UDQS#	Y	Connected SDRAM #1 to DSP pin
	DDRDQS1P	C7	UDQS	Y	Connected SDRAM #1 to DSP pin
End of Table 48					

Table 49 Pin Connectivity →2 - 8M x16 x8 banks (2G bit total) [4 of 4]

Two 8 Meg x 16 x 8 banks (2G bit total) [4 of 4] [MO-207 DU-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRDQS2N	G 3	LDQS#	Y	Connected SDRAM #1 to DSP pin
	DDRDQS2P	F 3	LDQS	Y	Connected SDRAM #1 to DSP pin
	DDRDQS3N	B7	UDQS#	Y	Connected SDRAM #1 to DSP pin
	DDRDQS3P	C7	UDQS	Y	Connected SDRAM #1 to DSP pin
	DDRDQS4N			N	
	DDRDQS4P			N	
	DDRDQS5N			N	
	DDRDQS5P			N	
	DDRDQS6N			N	
	DDRDQS6P			N	
	DDRDQS7N			N	
	DDRDQS7P			N	
	DDRDQS8N			N	
	DDRDQS8P			N	
	DDRCLKP			Y	Differential DDR PLL clock input to DSP (+)
	DDRCLKN			Y	Differential DDR PLL clock input to DSP (-)
		L 8	ZQ	Y	Each DDR3 SDRAM ZQ pin should be tied to a 240Ω resistor to ground

Table 49 Pin Connectivity →2 - 8M x16 x8 banks (2G bit total) [4 of 4]

Two 8 Meg x 16 x 8 banks (2G bit total) [4 of 4] [MO-207 DU-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	$\overline{\text{DDRREST}}$	T 2	RESET#	Y	DDR3 DSP & SDRAM reset pins
	AVDDA2			Y	DDRCLK PLL Power Supply, connect to dedicated and clean 1.8V (use filter)
$D_{VDD}15$	See device data manual	B2, D9, G7, K2, K8, N1, N9, R1, R9	Vdd	Y	Connected to respective VDD (1.5 V) Supply, pay attention to tolerance and sequencing requirements. The DVDD15 supply rail should be a common 1.5 Vdc rail that the DRAM utilize
	See device data manual	A1, A8, C1, C9, D2, E9, F1, H2, H9	VddQ	Y	Connected to respective VDD (1.5 V) Supply, pay attention to tolerance and sequencing requirements. The DVDD15 supply rail should be a common 1.5 Vdc rail that the DRAM utilize
		H 1	VrefDQ	Y	Connect to VDD/2, pay attention to power sequencing requirements
Vss	See device data manual	A9, B3, E1, G8, J2, J8, M1, M9, P1, P9, T1, T9	Vss	Y	Connected to Ground
		B1, B9, D1, D8, E2, E8, F9, G1, G9	VssQ	Y	Connected to Ground, connection MUST be short
	VREFSSTL	M 8	VrefCA	Y	DDR3 Vref pin, connect to DSP DDR3 Vdd/2 (.1% tol.).
					Connect to VDD/2, pay attention to power sequencing requirements
	PTV15A			Y	45.3Ω tied to ground (must be short)
		J1	NC	N	Leave unconnected on all SDRAMs
		J9	NC	N	Leave unconnected on all SDRAMs
		L1	NC	N	Leave unconnected on all SDRAMs
		L9	NC	N	Leave unconnected on all SDRAMs
End of Table 49					

8.1.1.8 Four 8 Meg x 16 x 8 banks (4.096G bit total)

The following tables illustrate the connectivity for between a KeyStone DSP and four 128M Byte ×8 SDRAMs which results in a total memory capacity of 512M Bytes. The following four tables define in detail the recommended inner-connectivity for a 64 bit wide bus and between four ×16 1G bit SDRAMs and a Keystone class DSP DDR3 controller. This table is also provided and based on a 96-pin SDRAM package.

Table 50 Pin Connectivity →4 - 8M x16 x8 banks (4G bit total) [1 of 4]

Four 8 Meg x 16 x 8 banks (4G bit total) [1 of 4] [MO-207 DU-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRA00	N3	A0	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA01	P7	A1	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA02	P3	A2	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA03	N2	A3	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA04	P8	A4	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA05	P2	A5	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA06	R8	A6	Y	Connect Controller Address pin to both SDRAMs with like name

Table 50 Pin Connectivity →4 - 8M x16 x8 banks (4G bit total) [1 of 4]

Four 8 Meg x 16 x 8 banks (4G bit total) [1 of 4] [MO-207 DU-z Package w/o support pins]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRA07	R2	A7	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA08	T8	A8	Y	Connect Controller Address pin to both SDRAM's with like name
	DDRA09	R3	A9	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA10	L7	A10/AP	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA11	R7	A11	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA12	N7	A12/BC#	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA13	T3	A13	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA14	T7	A14	N	Leave unconnected
	DDRA15	M7	A15	N	Leave unconnected
	DDRD00	E3	DQL0	Y	Connected SDRAM #1 to DSP pin
	DDRD01	F7	DQL1	Y	Connected SDRAM #1 to DSP pin
	DDRD02	F2	DQL2	Y	Connected SDRAM #1 to DSP pin
	DDRD03	F8	DQL3	Y	Connected SDRAM #1 to DSP pin
	DDRD04	H3	DQL4	Y	Connected SDRAM #1 to DSP pin
	DDRD05	H8	DQL5	Y	Connected SDRAM #1 to DSP pin
	DDRD06	G2	DQL6	Y	Connected SDRAM #1 to DSP pin
	DDRD07	H7	DQL7	Y	Connected SDRAM #1 to DSP pin
	DDRD08	D7	DQU0	Y	Connected SDRAM #1 to DSP pin
	DDRD09	C3	DQU1	Y	Connected SDRAM #1 to DSP pin
	DDRD10	C8	DQU2	Y	Connected SDRAM #1 to DSP pin
	DDRD11	C2	DQU3	Y	Connected SDRAM #1 to DSP pin
	DDRD12	A7	DQU4	Y	Connected SDRAM #1 to DSP pin
	DDRD13	A2	DQU5	Y	Connected SDRAM #1 to DSP pin
	DDRD14	B8	DQU6	Y	Connected SDRAM #1 to DSP pin
	DDRD15	A3	DQU7	Y	Connected SDRAM #1 to DSP pin
	DDRD16	E3	DQL0	Y	Connected SDRAM #2 to DSP pin
	DDRD17	F7	DQL1	Y	Connected SDRAM #2 to DSP pin
	DDRD18	F2	DQL2	Y	Connected SDRAM #2 to DSP pin
	DDRD19	F8	DQL3	Y	Connected SDRAM #2 to DSP pin
	DDRD20	H3	DQL4	Y	Connected SDRAM #2 to DSP pin
	DDRD21	H8	DQL5	Y	Connected SDRAM #2 to DSP pin
	DDRD22	G2	DQL6	Y	Connected SDRAM #2 to DSP pin
	DDRD23	H7	DQL7	Y	Connected SDRAM #2 to DSP pin
End of Table 50					

Table 51 Pin Connectivity →4 - 8M x16 x8 banks (4G bit total) [2 of 4]

Four 8 Meg x 16 x 8 banks (4G bit total) [2 of 4] [MO-207 DT-z Package w/o support pins]					
DSP Name	**DSP Pin**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD24	D7	DQU0	Y	Connected SDRAM #2 to DSP pin
	DDRD25	C3	DQU1	Y	Connected SDRAM #2 to DSP pin
	DDRD26	C8	DQU2	Y	Connected SDRAM #2 to DSP pin
	DDRD27	C2	DQU3	Y	Connected SDRAM #2 to DSP pin
	DDRD28	A7	DQU4	Y	Connected SDRAM #2 to DSP pin

Table 51 Pin Connectivity →4 - 8M x16 x8 banks (4G bit total) [2 of 4]

Four 8 Meg x 16 x 8 banks (4G bit total) [2 of 4]			[MO-207 DT-z Package w/o support pins]		
DSP Name	**DSP Pin**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD29	A2	DQU5	Y	Connected SDRAM #2 to DSP pin
	DDRD30	B8	DQU6	Y	Connected SDRAM #2 to DSP pin
	DDRD31	A3	DQU7	Y	Connected SDRAM #2 to DSP pin
	DDRD32	E3	DQL0	Y	Connected SDRAM #3 to DSP pin
	DDRD33	F7	DQL1	Y	Connected SDRAM #3 to DSP pin
	DDRD34	F2	DQL2	Y	Connected SDRAM #3 to DSP pin
	DDRD35	F8	DQL3	Y	Connected SDRAM #3 to DSP pin
	DDRD36	H3	DQL4	Y	Connected SDRAM #3 to DSP pin
	DDRD37	H8	DQL5	Y	Connected SDRAM #3 to DSP pin
	DDRD38	G2	DQL6	Y	Connected SDRAM #3 to DSP pin
	DDRD39	H7	DQL7	Y	Connected SDRAM #3 to DSP pin
	DDRD40	D7	DQU0	Y	Connected SDRAM #3 to DSP pin
	DDRD41	C3	DQU1	Y	Connected SDRAM #3 to DSP pin
	DDRD42	C8	DQU2	Y	Connected SDRAM #3 to DSP pin
	DDRD43	C2	DQU3	Y	Connected SDRAM #3 to DSP pin
	DDRD44	A7	DQU4	Y	Connected SDRAM #3 to DSP pin
	DDRD45	A2	DQU5	Y	Connected SDRAM #3 to DSP pin
	DDRD46	B8	DQU6	Y	Connected SDRAM #3 to DSP pin
	DDRD47	A3	DQU7	Y	Connected SDRAM #3 to DSP pin
	DDRD48	E3	DQL0	Y	Connected SDRAM #4 to DSP pin
	DDRD49	F7	DQL1	Y	Connected SDRAM #4 to DSP pin
	DDRD50	F2	DQL2	Y	Connected SDRAM #4 to DSP pin
	DDRD51	F8	DQL3	Y	Connected SDRAM #4 to DSP pin
	DDRD52	H3	DQL4	Y	Connected SDRAM #4 to DSP pin
	DDRD53	H8	DQL5	Y	Connected SDRAM #4 to DSP pin
	DDRD54	G2	DQL6	Y	Connected SDRAM #4 to DSP pin
	DDRD55	H7	DQL7	Y	Connected SDRAM #4 to DSP pin
	DDRD56	D7	DQU0	Y	Connected SDRAM #4 to DSP pin
	DDRD57	C3	DQU1	Y	Connected SDRAM #4 to DSP pin
	DDRD58	C8	DQU2	Y	Connected SDRAM #4 to DSP pin
	DDRD59	C2	DQU3	Y	Connected SDRAM #4 to DSP pin
	DDRD60	A7	DQU4	Y	Connected SDRAM #4 to DSP pin
	DDRD61	A2	DQU5	Y	Connected SDRAM #4 to DSP pin
	DDRD62	B8	DQU6	Y	Connected SDRAM #4 to DSP pin
	DDRD63	A3	DQU7	Y	Connected SDRAM #4 to DSP pin
End of Table 51					

Table 52 Pin Connectivity →4 - 8M x16 x8 banks (4G bit total) [3 of 4]

Four 8 Meg x 16 x 8 banks (4G bit total) [3 of 4]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	$\overline{\text{DDRCE0}}$	L2	CS#	Y	Connected SDRAM #1, 2, 3, & #4 to DSP pin
	$\overline{\text{DDRCE1}}$	L2	CS#	N	Leave unconnected, only for use with dual-rank designs
	DDRBA0	M2	BA0	Y	Connect to like pin between SDRAM and DSP

Table 52 Pin Connectivity →4 - 8M x16 x8 banks (4G bit total) [3 of 4]

Four 8 Meg x 16 x 8 banks (4G bit total) [3 of 4]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRBA1	N8	BA1	Y	Connect to like pin between SDRAM and DSP
	DDRBA2	M3	BA2	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRCAS}}$	K 3	CAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRRAS}}$	J 3	RAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRWE}}$	L 3	WE#	Y	Connect to like pin between SDRAM and DSP
	DDRCKE0	K 9	CKE	Y	Connect to like pin between SDRAM and DSP
	DDRCKE1	K 9	CKE	N	Leave unconnected at DSP
	DDRCLKOUTP0	J 7	CK	Y	Connected SDRAM #1, 2, 3, & #4 to DSP pin
	DDRCLKOUTN0	K 7	CK#	Y	Connected SDRAM #1, 2, 3, & #4 to DSP pin
	DDRCLKOUTP1	J 7	CK	N	Leave unconnected at DSP, only for use with dual-rank designs
	DDRCLKOUTN1	K 7	CK#	N	Leave unconnected at DSP, only for use with dual-rank designs
	DDRODT0	K 1	ODT	Y	Connected SDRAM #1–#4 to DSP pin
	DDRODT1	K 1	ODT	N	Leave unconnected at DSP, only for use with dual-rank designs
	DDRSLRATE0			N	Under software or hardware control
	DDRSLRATE1			N	
	DDRCB00			N	
	DDRCB01			N	
	DDRCB02			N	
	DDRCB03			N	
	DDRCB04			N	
	DDRCB05			N	
	DDRCB06			N	
	DDRCB07			N	
	DDRDQM0	LDM	E7	Y	Connected SDRAM #1 & #3 to DSP pin
	DDRDQM1	UDM	D3	Y	Connected SDRAM #1 & #3 to DSP pin
	DDRDQM2	LDM	E7	Y	Connected SDRAM #1 & #3 to DSP pin
	DDRDQM3	UDM	D3	Y	Connected SDRAM #1 & #3 to DSP pin
	DDRDQM4	LDM	E7	Y	Connected SDRAM #2 & #4 to DSP pin
	DDRDQM5	UDM	D3	Y	Connected SDRAM #2 & #4 to DSP pin
	DDRDQM6	LDM	E7	Y	Connected SDRAM #2 & #4 to DSP pin
	DDRDQM7	UDM	D3	Y	Connected SDRAM #2 & #4 to DSP pin
	DDRDQM8			N	Leave unconnected
	DDRDQS0N	G 3	LDQS#	Y	Connected SDRAM #1 to DSP pin
	DDRDQS0P	F 3	LDQS	Y	Connected SDRAM #1 to DSP pin
	DDRDQS1N	B7	UDQS#	Y	Connected SDRAM #1 to DSP pin
	DDRDQS1P	C7	UDQS	Y	Connected SDRAM #1 to DSP pin
	DDRDQS2N	G 3	LDQS#	Y	Connected SDRAM #2 to DSP pin
End of Table 52					

Table 53 Pin Connectivity →4 - 8M x16 x8 banks (4G bit total) [4 of 4]

Four 8 Meg x 16 x 8 banks (4G bit total) [4 of 4]					[MO-207 DU-z Package w/o support pins]
DSP Name	**DSP Pin**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRDQS2P	F 3	LDQS	Y	Connected SDRAM #2 to DSP pin
	DDRDQS3N	B7	UDQS#	Y	Connected SDRAM #2 to DSP pin
	DDRDQS3P	C7	UDQS	Y	Connected SDRAM #2 to DSP pin
	DDRDQS4N	G 3	LDQS#	Y	Connected SDRAM #3 to DSP pin
	DDRDQS4P	F 3	LDQS	Y	Connected SDRAM #3 to DSP pin
	DDRDQS5N	B7	UDQS#	Y	Connected SDRAM #3 to DSP pin
	DDRDQS5P	C7	UDQS	Y	Connected SDRAM #3 to DSP pin
	DDRDQS6N	G 3	LDQS#	Y	Connected SDRAM #4 to DSP pin
	DDRDQS6P	F 3	LDQS	Y	Connected SDRAM #4 to DSP pin
	DDRDQS7N	B7	UDQS#	Y	Connected SDRAM #4 to DSP pin
	DDRDQS7P	C7	UDQS	Y	Connected SDRAM #4 to DSP pin
	DDRDQS8N			N	
	DDRDQS8P			N	
	DDRCLKP			Y	Differential DDR PLL clock input to DSP (+)
	DDRCLKN			Y	Differential DDR PLL clock input to DSP (-)
		L 8	ZQ	Y	Each DDR3 SDRAM ZQ pin should be tied to a 240Ω resistor to ground
	$\overline{\text{DDRREST}}$	T 2	RESET#	Y	DDR3 DSP & SDRAM reset pins
	AVDDA2			Y	DDRCLK PLL Power Supply, connect to dedicated and clean 1.8V (use
$D_{VDD}15$	See device data manual	B2, D9, G7, K2, K8, N1, N9, R1, R9	Vdd	Y	Connected to respective VDD (1.5V) Supply, pay attention to tolerance and sequencing requirements
	See device data manual	A1, A8, C1, C9, D2, E9, F1, H2, H9	VddQ	Y	Connected to respective VDD (1.5V) Supply, pay attention to tolerance and sequencing requirements
		H 1	VrefDQ	Y	Connect to VDD/2, pay attention to power sequencing requirements
Vss	See device data manual	A9, B3, E1, G8, J2, J8, M1, M9, P1, P9, T1, T9	Vss	Y	Connected to Ground
		B1, B9, D1, D8, E2, E8, F9, G1, G9	VssQ	Y	Connected to Ground, connection MUST be short
	VREFSSTL	M 8	VrefCA	Y	DDR3 Vref pin, connect to DSP DDR3 Vdd/2 (.1% tol.).
					Connect to VDD/2, pay attention to power sequencing requirements
	PTV15A			Y	45.3Ω tied to ground (must be short)
		J1	NC	N	Leave unconnected on all SDRAMs
		J9	NC	N	Leave unconnected on all SDRAMs
		L1	NC	N	Leave unconnected on all SDRAMs
		L9	NC	N	Leave unconnected on all SDRAMs

End of Table 53

8.1.1.9 One 16 Meg x 16 x 8 banks (2.048G bit total)

The following tables illustrate the connectivity for between a KeyStone DSP and one 256M Byte ×8 banks SDRAM which results in a total memory capacity of 256M Bytes. The following four tables define in detail the recommended inner-connectivity for a 16 bit wide bus and between one ×16 2G bit SDRAM and a Keystone class DSP DDR3 controller. This table is also provided and based on a 96-pin SDRAM package.

Table 54 Pin Connectivity →1 - 16M x16 x8 banks (2G bit total) [1 of 4]

One 16 Meg x 16 x 8 banks (2G bit total) [1 of 4]			[MO-207 DU-z Package w/o support pins]		
DSP Pin	DSP Name	DDR3 Pin	DDR3 Name	Used (Y/N)	Note
	DDRA00	N3	A0	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA01	P7	A1	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA02	P3	A2	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA03	N2	A3	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA04	P8	A4	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA05	P2	A5	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA06	R8	A6	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA07	R2	A7	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA08	T8	A8	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA09	R3	A9	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA10	L7	A10/AP	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA11	R7	A11	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA12	N7	A12/BC#	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA13	T3	A13	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA14	T7	A14	N	Leave unconnected
	DDRA15	M7	A15	N	Leave unconnected
	DDRD00	E3	DQ00	Y	Connected SDRAM #1 to DSP pin
	DDRD01	F7	DQ01	Y	Connected SDRAM #1 to DSP pin
	DDRD02	F2	DQ02	Y	Connected SDRAM #1 to DSP pin
	DDRD03	F8	DQ03	Y	Connected SDRAM #1 to DSP pin
	DDRD04	H3	DQ04	Y	Connected SDRAM #1 to DSP pin
	DDRD05	H8	DQ05	Y	Connected SDRAM #1 to DSP pin
	DDRD06	G2	DQ06	Y	Connected SDRAM #1 to DSP pin
	DDRD07	H7	DQ07	Y	Connected SDRAM #1 to DSP pin
	DDRD08	D7	DQ08	Y	Connected SDRAM #1 to DSP pin
	DDRD09	C3	DQ09	Y	Connected SDRAM #1 to DSP pin
	DDRD10	C8	DQ10	Y	Connected SDRAM #1 to DSP pin
	DDRD11	C2	DQ11	Y	Connected SDRAM #1 to DSP pin
	DDRD12	A7	DQ12	Y	Connected SDRAM #1 to DSP pin
	DDRD13	A2	DQ13	Y	Connected SDRAM #1 to DSP pin
	DDRD14	B8	DQ14	Y	Connected SDRAM #1 to DSP pin
	DDRD15	A3	DQ15	Y	Connected SDRAM #1 to DSP pin
	DDRD16			N	Leave unconnected
	DDRD17			N	Leave unconnected
	DDRD18			N	Leave unconnected
	DDRD19			N	Leave unconnected
	DDRD20			N	Leave unconnected
	DDRD21			N	Leave unconnected

Table 54 Pin Connectivity →1 - 16M x16 x8 banks (2G bit total) [1 of 4]

One 16 Meg x 16 x 8 banks (2G bit total) [1 of 4]					[MO-207 DU-z Package w/o support pins]
DSP Pin	DSP Name	DDR3 Pin	DDR3 Name	Used (Y/N)	Note
	DDRD22			N	Leave unconnected
	DDRD23			N	Leave unconnected
End of Table 54					

Table 55 Pin Connectivity →1 - 16M x16 x8 banks (2G bit total) [2 of 4]

One 16 Meg x 16 x 8 banks (2G bit total) [2 of 4]				[MO-207 DU-z Package w/o support pins]	
DSP Pin	DSP Name	DDR3 Pin	DDR3 Name	Used (Y/N)	Note
	DDRD24			N	Leave unconnected
	DDRD25			N	Leave unconnected
	DDRD26			N	Leave unconnected
	DDRD27			N	Leave unconnected
	DDRD28			N	Leave unconnected
	DDRD29			N	Leave unconnected
	DDRD30			N	Leave unconnected
	DDRD31			N	Leave unconnected
	DDRD32			N	Leave unconnected
	DDRD33			N	Leave unconnected
	DDRD34			N	Leave unconnected
	DDRD35			N	Leave unconnected
	DDRD36			N	Leave unconnected
	DDRD37			N	Leave unconnected
	DDRD38			N	Leave unconnected
	DDRD39			N	Leave unconnected
	DDRD40			N	Leave unconnected
	DDRD41			N	Leave unconnected
	DDRD42			N	Leave unconnected
	DDRD43			N	Leave unconnected
	DDRD44			N	Leave unconnected
	DDRD45			N	Leave unconnected
	DDRD46			N	Leave unconnected
	DDRD47			N	Leave unconnected
	DDRD48			N	Leave unconnected
	DDRD49			N	Leave unconnected
	DDRD50			N	Leave unconnected
	DDRD51			N	Leave unconnected
	DDRD52			N	Leave unconnected
	DDRD53			N	Leave unconnected
	DDRD54			N	Leave unconnected
	DDRD55			N	Leave unconnected
	DDRD56			N	Leave unconnected

Table 55 Pin Connectivity →1 - 16M x16 x8 banks (2G bit total) [2 of 4]

One 16 Meg x 16 x 8 banks (2G bit total) [2 of 4]			[MO-207 DU-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD57			N	Leave unconnected
	DDRD58			N	Leave unconnected
	DDRD59			N	Leave unconnected
	DDRD60			N	Leave unconnected
	DDRD61			N	Leave unconnected
	DDRD62			N	Leave unconnected
End of Table 55					

Table 56 Pin Connectivity →1 - 16M x16 x8 banks (2G bit total) [3 of 4]

One 16 Meg x 16 x 8 banks (2G bit total) [3 of 4]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	$\overline{\text{DDRCE0}}$	L 2	CS#	N	Connected SDRAM #1 to DSP pin
	$\overline{\text{DDRCE1}}$			N	Leave unconnected, only for use with dual-rank designs
	DDRBA0	M2	BA0	Y	Connect to like pin between SDRAM and DSP
	DDRBA1	N8	BA1	Y	Connect to like pin between SDRAM and DSP
	DDRBA2	M3	BA2	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRCAS}}$	K 3	CAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRRAS}}$	J 3	RAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRWE}}$	L 3	WE#	Y	Connect to like pin between SDRAM and DSP
	DDRCKE0	K 9	CKE	Y	Connect to like pin between SDRAM and DSP
	DDRCKE1	K 9	CKE	N	Leave unconnected at DSP, only for use with dual-rank designs
	DDRCLKOUTP0	J 7	CK	Y	Connected SDRAM #1 to DSP pin
	DDRCLKOUTN0	K 7	CK#	Y	Connected SDRAM #1 to DSP pin
	DDRCLKOUTP1			N	Leave unconnected at DSP, only for use with dual-rank designs
	DDRCLKOUTN1			N	Leave unconnected at DSP, only for use with dual-rank designs
	DDRODT0	K 1	ODT	Y	Connected SDRAM #1 to DSP pin
	DDRODT1			N	Leave unconnected at DSP, only for use with dual-rank designs
	DDRSLRATE0			N	Under software or hardware control
	DDRSLRATE1				Leave unconnected
	DDRCB00			N	Leave unconnected
	DDRCB01			N	Leave unconnected
	DDRCB02			N	Leave unconnected
	DDRCB03			N	Leave unconnected
	DDRCB04			N	Leave unconnected
	DDRCB05			N	Leave unconnected
	DDRCB06			N	Leave unconnected
	DDRCB07			N	Leave unconnected
	DDRDQM0	E7	DML	Y	Connected SDRAM #1 to DSP pin
	DDRDQM1	D3	DMU	Y	Connected SDRAM #1 to DSP pin
	DDRDQM2			N	Leave unconnected
	DDRDQM3			N	Leave unconnected
	DDRDQM4			N	Leave unconnected

Table 56 Pin Connectivity →1 - 16M x16 x8 banks (2G bit total) [3 of 4]

One 16 Meg x 16 x 8 banks (2G bit total) [3 of 4]					
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRDQM5			N	Leave unconnected
	DDRDQM6			N	Leave unconnected
	DDRDQM7			N	Leave unconnected
	DDRDQM8			N	Leave unconnected
	DDRDQS0N	G3	DQSL#	Y	Connected SDRAM #1 to DSP pin
	DDRDQS0P	F3	DQSL	Y	Connected SDRAM #1 to DSP pin
	DDRDQS1N	B7	DQSU#	Y	Connected SDRAM #1 to DSP pin
	DDRDQS1P	C7	DQSU	Y	Connected SDRAM #1 to DSP pin
	DDRDQS2N			N	Leave unconnected
End of Table 56					

Table 57 Pin Connectivity →1 - 16M x16 x8 banks (2G bit total) [4 of 4]

One 16 Meg x 16 x 8 banks (2G bit total) [4 of 4]				[MO-207 DU-z Package w/o support pins]	
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRDQS2P			N	Leave unconnected
	DDRDQS3N			N	Leave unconnected
	DDRDQS3P			N	Leave unconnected
	DDRDQS4N			N	Leave unconnected
	DDRDQS4P			N	Leave unconnected
	DDRDQS5N			N	Leave unconnected
	DDRDQS5P			N	Leave unconnected
	DDRDQS6N			N	Leave unconnected
	DDRDQS6P			N	Leave unconnected
	DDRDQS7N			N	Leave unconnected
	DDRDQS7P			N	Leave unconnected
	DDRDQS8N			N	Leave unconnected
	DDRDQS8P			N	Leave unconnected
	DDRCLKP			Y	Differential DDR PLL clock input to DSP (+)
	DDRCLKN			Y	Differential DDR PLL clock input to DSP (-)
		L 8	ZQ	Y	Each DDR3 SDRAM ZQ pin should be tied to a 240Ω resistor to ground
	$\overline{\text{DDRREST}}$	T 2	RESET#	Y	DDR3 DSP & SDRAM reset pins
	AVDDA2			Y	DDRCLK PLL Power Supply, connect to dedicated and clean 1.8V (use filter)
$D_{VDD}15$	See device data manual	B2, D9, G7, K2, K8, N1, N9, R1, R9	Vdd	Y	Connected to respective VDD (1.5V) Supply, pay attention to tolerance and sequencing requirements
	See device data manual	A1, A8, C1, C9, D2, E9, F1, H2, H9	VddQ	Y	Connected to respective VDD (1.5V) Supply, pay attention to tolerance and sequencing requirements
		H 1	VrefDQ	Y	Connect to VDD/2, pay attention to power sequencing requirements

Table 57 Pin Connectivity →1 - 16M x16 x8 banks (2G bit total) [4 of 4]

One 16 Meg x 16 x 8 banks (2G bit total) [4 of 4]				[MO-207 DU-z Package w/o support pins]	
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
Vss	See device data manual	A9, B3, E1, G8, J2, J8, M1, M9, P1, P9, T1, T9	Vss	Y	Connected to Ground
		B1, B9, D1, D8, E2, E8, F9, G1, G9	VssQ	Y	Connected to Ground, connection MUST be short
	VREFSSTL	M 8	VrefCA	Y	DDR3 Vref pin, connect to DSP DDR3 Vdd/2 (.1% tol.).
					Connect to VDD/2, pay attention to power sequencing requirements
	PTV15A			Y	45.3Ω tied to ground (must be short)
		J1	NC	N	Leave unconnected on all SDRAMs
		J9	NC	N	Leave unconnected on all SDRAMs
		L1	NC	N	Leave unconnected on all SDRAMs
		L9	NC	N	Leave unconnected on all SDRAMs
End of Table 57					

8.1.1.10 Two 16 Meg x 16 x 8 banks (4.096G bit total)

The following tables illustrate the connectivity for between a KeyStone DSP and two 256M Byte ×8 banks SDRAMs which results in a total memory capacity of 512M Bytes. The following four tables define in detail the recommended inner-connectivity for a 32bit wide bus and between two ×16 2G bit SDRAM and a Keystone class DSP DDR3 controller. This table is also provided and based on a 96-pin SDRAM package.

Table 58 Pin Connectivity →2 - 16M x16 x8 banks (4G bit total) [1 of 4]

Two 16 Meg x 16 x 8 banks (4G bit total) [1 of 4]				[MO-207 DU-z Package w/o support pins]	
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRA00	N3	A0	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA01	P7	A1	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA02	P3	A2	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA03	N2	A3	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA04	P8	A4	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA05	P2	A5	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA06	R8	A6	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA07	R2	A7	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA08	T8	A8	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA09	R3	A9	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA10	L7	A10/AP	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA11	R7	A11	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA12	N7	A12/BC#	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA13	T3	A13	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA14	T7	A14	N	Leave unconnected
	DDRA15	M7	A15	N	Leave unconnected
	DDRD00	E3	DQ00	Y	Connected SDRAM #1 to DSP pin
	DDRD01	F7	DQ01	Y	Connected SDRAM #1 to DSP pin
	DDRD02	F2	DQ02	Y	Connected SDRAM #1 to DSP pin
	DDRD03	F8	DQ03	Y	Connected SDRAM #1 to DSP pin

Table 58 Pin Connectivity →2 - 16M x16 x8 banks (4G bit total) [1 of 4]

Two 16 Meg x 16 x 8 banks (4G bit total) [1 of 4]			[MO-207 DU-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD04	H3	DQ04	Y	Connected SDRAM #1 to DSP pin
	DDRD05	H8	DQ05	Y	Connected SDRAM #1 to DSP pin
	DDRD06	G2	DQ06	Y	Connected SDRAM #1 to DSP pin
	DDRD07	H7	DQ07	Y	Connected SDRAM #1 to DSP pin
	DDRD08	D7	DQ08	Y	Connected SDRAM #1 to DSP pin
	DDRD09	C3	DQ09	Y	Connected SDRAM #1 to DSP pin
	DDRD10	C8	DQ10	Y	Connected SDRAM #1 to DSP pin
	DDRD11	C2	DQ11	Y	Connected SDRAM #1 to DSP pin
	DDRD12	A7	DQ12	Y	Connected SDRAM #1 to DSP pin
	DDRD13	A2	DQ13	Y	Connected SDRAM #1 to DSP pin
	DDRD14	B8	DQ14	Y	Connected SDRAM #1 to DSP pin
	DDRD15	A3	DQ15	Y	Connected SDRAM #1 to DSP pin
	DDRD16	E3	DQ00	Y	Connected SDRAM #2 to DSP pin
	DDRD17	F7	DQ01	Y	Connected SDRAM #2 to DSP pin
	DDRD18	F2	DQ02	Y	Connected SDRAM #2 to DSP pin
	DDRD19	F8	DQ03	Y	Connected SDRAM #2 to DSP pin
	DDRD20	H3	DQ04	Y	Connected SDRAM #2 to DSP pin
	DDRD21	H8	DQ05	Y	Connected SDRAM #2 to DSP pin
	DDRD22	G2	DQ06	Y	Connected SDRAM #2 to DSP pin
	DDRD23	H7	DQ07	Y	Connected SDRAM #2 to DSP pin
End of Table 58					

Table 59 Pin Connectivity →2 - 16M x16 x8 banks (4G bit total) [2 of 4]

Two 16 Meg x 16 x 8 banks (4G bit total) [2 of 4]			[MO-207 DU-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD24	D7	DQ08	Y	Connected SDRAM #2 to DSP pin
	DDRD25	C3	DQ09	Y	Connected SDRAM #2 to DSP pin
	DDRD26	C8	DQ10	Y	Connected SDRAM #2 to DSP pin
	DDRD27	C2	DQ11	Y	Connected SDRAM #2 to DSP pin
	DDRD28	A7	DQ12	Y	Connected SDRAM #2 to DSP pin
	DDRD29	A2	DQ13	Y	Connected SDRAM #2 to DSP pin
	DDRD30	B8	DQ14	Y	Connected SDRAM #2 to DSP pin
	DDRD31	A3	DQ15	Y	Connected SDRAM #2 to DSP pin
	DDRD32			N	Leave unconnected on DSP
	DDRD33			N	Leave unconnected on DSP
	DDRD34			N	Leave unconnected on DSP
	DDRD35			N	Leave unconnected on DSP
	DDRD36			N	Leave unconnected on DSP
	DDRD37			N	Leave unconnected on DSP
	DDRD38			N	Leave unconnected on DSP
	DDRD39			N	Leave unconnected on DSP
	DDRD40			N	Leave unconnected on DSP
	DDRD41			N	Leave unconnected on DSP

Table 59 Pin Connectivity →2 - 16M x16 x8 banks (4G bit total) [2 of 4]

Two 16 Meg x 16 x 8 banks (4G bit total) [2 of 4]				[MO-207 DU-z Package w/o support pins]	
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD42			N	Leave unconnected on DSP
	DDRD43			N	Leave unconnected on DSP
	DDRD44			N	Leave unconnected on DSP
	DDRD45			N	Leave unconnected on DSP
	DDRD46			N	Leave unconnected on DSP
	DDRD47			N	Leave unconnected on DSP
	DDRD48			N	Leave unconnected on DSP
	DDRD49			N	Leave unconnected on DSP
	DDRD50			N	Leave unconnected on DSP
	DDRD51			N	Leave unconnected on DSP
	DDRD52			N	Leave unconnected on DSP
	DDRD53			N	Leave unconnected on DSP
	DDRD54			N	Leave unconnected on DSP
	DDRD55			N	Leave unconnected on DSP
	DDRD56			N	Leave unconnected on DSP
	DDRD57			N	Leave unconnected on DSP
	DDRD58			N	Leave unconnected on DSP
	DDRD59			N	Leave unconnected on DSP
	DDRD60			N	Leave unconnected on DSP
	DDRD61			N	Leave unconnected on DSP
	DDRD62			N	Leave unconnected on DSP
	DDRD63			N	Leave unconnected on DSP
End of Table 59					

Table 60 Pin Connectivity →2 - 16M x16 x8 banks (4G bit total) [3 of 4]

Two 16 Meg x 16 x 8 banks (4G bit total) [3 of 4]				[MO-207 DU-z Package w/o support pins]	
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	$\overline{\text{DDRCE0}}$	L 2	CS#	Y	Connected SDRAM #1& SDRAM #2 to DSP pin
	$\overline{\text{DDRCE1}}$	L 2	CS#	N	Leave unconnected on DSP, only for use with dual-rank designs
	DDRBA0	M 2	BA0	Y	Connect to like pin between SDRAM and DSP
	DDRBA1	M 3	BA1	Y	Connect to like pin between SDRAM and DSP
	DDRBA2	N 8	BA2	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRCAS}}$	K 3	CAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRRAS}}$	J 3	RAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRWE}}$	L 3	WE#	Y	Connect to like pin between SDRAM and DSP
	DDRCKE0	K 9	CKE	Y	Connect to like pin between SDRAM and DSP
	DDRCKE1	K 9	CKE	N	Leave unconnected at DSP, only for use with dual-rank designs
	DDRCLKOUTP0	J 7	CK	Y	Connected SDRAM #1, 2, 3, & 4 to DSP pin
	DDRCLKOUTN0	K 7	CK#	Y	Connected SDRAM #1, 2, 3, & 4 to DSP pin
	DDRCLKOUTP1	J 7	CK	N	Leave unconnected at DSP, only for use with dual-rank designs
	DDRCLKOUTN1	K 7	CK#	N	Leave unconnected at DSP, only for use with dual-rank designs
	DDRODT0	K 1	ODT	Y	Connected SDRAM #1 to DSP pin
	DDRODT1	K 1	ODT	N	Leave unconnected at DSP, only for use with dual-rank designs

Table 60 Pin Connectivity →2 - 16M x16 x8 banks (4G bit total) [3 of 4]

Two 16 Meg x 16 x 8 banks (4G bit total) [3 of 4]				[MO-207 DU-z Package w/o support pins]	
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRSLRATE0			Y	Under software or hardware control
	DDRSLRATE1			Y	Under software or hardware control
	DDRCB00			N	Leave unconnected at DSP
	DDRCB01			N	Leave unconnected at DSP
	DDRCB02			N	Leave unconnected at DSP
	DDRCB03			N	Leave unconnected at DSP
	DDRCB04			N	Leave unconnected at DSP
	DDRCB05			N	Leave unconnected at DSP
	DDRCB06			N	Leave unconnected at DSP
	DDRCB07			N	Leave unconnected at DSP
	DDRDQM0	E7	DML	Y	Connected SDRAM #1 to DSP pin
	DDRDQM1	D3	DMU	Y	Connected SDRAM #1 to DSP pin
	DDRDQM2	E7	DML	Y	Connected SDRAM #2 to DSP pin
	DDRDQM3	D3	DMU	Y	Connected SDRAM #2 to DSP pin
	DDRDQM4			N	Leave unconnected at DSP & SDRAM
	DDRDQM5			N	Leave unconnected at DSP & SDRAM
	DDRDQM6			N	Leave unconnected at DSP & SDRAM
	DDRDQM7			N	Leave unconnected at DSP & SDRAM
	DDRDQM8			N	Leave unconnected at DSP
	DDRDQS0N	G3	DQSL#	Y	Connected SDRAM #1 to DSP pin
	DDRDQS0P	F3	DQSL	Y	Connected SDRAM #1 to DSP pin
	DDRDQS1N	B7	DQSU#	Y	Connected SDRAM #1 to DSP pin
	DDRDQS1P	C7	DQSU	Y	Connected SDRAM #1 to DSP pin
	DDRDQS2N	G3	DQSL#	Y	Connected SDRAM #2 to DSP pin
End of Table 60					

Table 61 Pin Connectivity →2 - 16M x16 x8 banks (4G bit total) [4 of 4]

Two 16 Meg x 16 x 8 banks (4G bit total) [4 of 4]				[MO-207 DU-z Package w/o support pins]	
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRDQS2P	F3	DQSL	Y	Connected SDRAM #2 to DSP pin
	DDRDQS3N	B7	DQSU#	Y	Connected SDRAM #2 to DSP pin
	DDRDQS3P	C7	UDQS	Y	Connected SDRAM #2 to DSP pin
	DDRDQS4N			Y	Unconnected on DSP
	DDRDQS4P			Y	Unconnected on DSP
	DDRDQS5N			Y	Unconnected on DSP
	DDRDQS5P			Y	Unconnected on DSP
	DDRDQS6N			Y	Unconnected on DSP
	DDRDQS6P			Y	Unconnected on DSP
	DDRDQS7N			Y	Unconnected on DSP
	DDRDQS7P			Y	Unconnected on DSP
	DDRDQS8N			N	
	DDRDQS8P			N	
	DDRCLKP			Y	Differential DDR PLL clock input to DSP (+)

Table 61 Pin Connectivity →2 - 16M x16 x8 banks (4G bit total) [4 of 4]

Two 16 Meg x 16 x 8 banks (4G bit total) [4 of 4]				[MO-207 DU-z Package w/o support pins]	
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRCLKN			Y	Differential DDR PLL clock input to DSP (-)
		L 8	ZQ	Y	Each DDR3 SDRAM ZQ pin should be tied to a 240Ω resistor to ground
	$\overline{\text{DDRREST}}$	T 2	RESET#	Y	DDR3 DSP & SDRAM reset pins
	AVDDA2			Y	DDRCLK PLL Power Supply, connect to dedicated and clean 1.8V (use filter)
$D_{VDD}15$	See device data manual	B2, D9, G7, K2, K8, N1, N9, R1, R9	Vdd	Y	Connected to respective VDD (1.5V) Supply, pay attention to tolerance and sequencing requirements
	See device data manual	A1, A8, C1, C9, D2, E9, F1, H2, H9	VddQ	Y	Connected to respective VDD (1.5V) Supply, pay attention to tolerance and sequencing requirements
		H 1	VrefDQ	Y	Connect to VDD/2, pay attention to power sequencing requirements
	VREFSSTL	M 8	VrefCA	Y	DDR3 Vref pin, connect to DSP DDR3 Vdd/2 (.1% tol.).
					Connect to VDD/2, pay attention to power sequencing requirements
Vss	See device data manual	A9, B3, E1, G8, J2, J8, M1, M9, P1, P9, T1, T9	Vss	Y	Connected to Ground
		B1, B9, D1, D8, E2, E8, F9, G1, G9	VssQ	Y	Connected to Ground, connection MUST be short
	PTV15A			Y	45.3Ω tied to ground (must be short)
		J1	NC	N	Leave unconnected on all SDRAMs
		J9	NC	N	Leave unconnected on all SDRAMs
		L1	NC	N	Leave unconnected on all SDRAMs
		L9	NC	N	Leave unconnected on all SDRAMs
End of Table 61					

8.1.1.11 Four 16 Meg x 16 x 8 banks (8.192G bit total)

The following tables illustrate the connectivity for between a KeyStone DSP and four 256M Byte ×8 banks SDRAMs resulting in a total memory capacity of 1024M Bytes. The following four tables define in detail the recommended inner-connectivity for a 64 bit wide bus and between four ×16 2G bit SDRAM and a Keystone class DSP DDR3 controller. This table is also provided and based on a 96-pin SDRAM package.

Table 62 Pin Connectivity →4 - 16M x16 x8 banks (8G bit total) [1 of 4]

Four 16 Meg x 16 x 8 banks (8G bit total) [1 of 4]				[MO-207 DU-z Package w/o support pins]	
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRA00	N3	A0	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA01	P7	A1	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA02	P3	A2	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA03	N2	A3	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA04	P8	A4	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA05	P2	A5	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA06	R8	A6	Y	Connect Controller Address pin to both SDRAMs with like name

Table 62 Pin Connectivity →4 - 16M x16 x8 banks (8G bit total) [1 of 4]

Four 16 Meg x 16 x 8 banks (8G bit total) [1 of 4]			[MO-207 DU-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRA07	R2	A7	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA08	T8	A8	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA09	R3	A9	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA10	L7	A10/AP	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA11	R7	A11	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA12	N7	A12/BC#	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA13	T3	A13	Y	Connect Controller Address pin to both SDRAMs with like name
	DDRA14	T7	A14	N	Leave unconnected
	DDRA15	M7	A15	N	Leave unconnected
	DDRD00	E3	DQ00	Y	Connected SDRAM #1 to DSP pin
	DDRD01	F7	DQ01	Y	Connected SDRAM #1 to DSP pin
	DDRD02	F2	DQ02	Y	Connected SDRAM #1 to DSP pin
	DDRD03	F8	DQ03	Y	Connected SDRAM #1 to DSP pin
	DDRD04	H3	DQ04	Y	Connected SDRAM #1 to DSP pin
	DDRD05	H8	DQ05	Y	Connected SDRAM #1 to DSP pin
	DDRD06	G2	DQ06	Y	Connected SDRAM #1 to DSP pin
	DDRD07	H7	DQ07	Y	Connected SDRAM #1 to DSP pin
	DDRD08	D7	DQ08	Y	Connected SDRAM #1 to DSP pin
	DDRD09	C3	DQ09	Y	Connected SDRAM #1 to DSP pin
	DDRD10	C8	DQ10	Y	Connected SDRAM #1 to DSP pin
	DDRD11	C2	DQ11	Y	Connected SDRAM #1 to DSP pin
	DDRD12	A7	DQ12	Y	Connected SDRAM #1 to DSP pin
	DDRD13	A2	DQ13	Y	Connected SDRAM #1 to DSP pin
	DDRD14	B8	DQ14	Y	Connected SDRAM #1 to DSP pin
	DDRD15	A3	DQ15	Y	Connected SDRAM #1 to DSP pin
	DDRD16	E3	DQ00	Y	Connected SDRAM #2 to DSP pin
	DDRD17	F7	DQ01	Y	Connected SDRAM #2 to DSP pin
	DDRD18	F2	DQ02	Y	Connected SDRAM #2 to DSP pin
	DDRD19	F8	DQ03	Y	Connected SDRAM #2 to DSP pin
	DDRD20	H3	DQ04	Y	Connected SDRAM #2 to DSP pin
	DDRD21	H8	DQ05	Y	Connected SDRAM #2 to DSP pin
	DDRD22	G2	DQ06	Y	Connected SDRAM #2 to DSP pin
	DDRD23	H7	DQ07	Y	Connected SDRAM #2 to DSP pin
End of Table 62					

Table 63 Pin Connectivity →4 - 16M x16 x8 banks (8G bit total) [2 of 4]

Four 16 Meg x 16 x 8 banks (8G bit total) [2 of 4]			[MO-207 DU-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD24	D7	DQ08	Y	Connected SDRAM #2 to DSP pin
	DDRD25	C3	DQ09	Y	Connected SDRAM #2 to DSP pin
	DDRD26	C8	DQ10	Y	Connected SDRAM #2 to DSP pin
	DDRD27	C2	DQ11	Y	Connected SDRAM #2 to DSP pin
	DDRD28	A7	DQ12	Y	Connected SDRAM #2 to DSP pin

Table 63 Pin Connectivity →4 - 16M x16 x8 banks (8G bit total) [2 of 4]

Four 16 Meg x 16 x 8 banks (8G bit total) [2 of 4]			[MO-207 DU-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRD29	A2	DQ13	Y	Connected SDRAM #2 to DSP pin
	DDRD30	B8	DQ14	Y	Connected SDRAM #2 to DSP pin
	DDRD31	A3	DQ15	Y	Connected SDRAM #2 to DSP pin
	DDRD32	E3	DQ00	Y	Connected SDRAM #3 to DSP pin
	DDRD33	F7	DQ01	Y	Connected SDRAM #3 to DSP pin
	DDRD34	F2	DQ02	Y	Connected SDRAM #3 to DSP pin
	DDRD35	F8	DQ03	Y	Connected SDRAM #3 to DSP pin
	DDRD36	H3	DQ04	Y	Connected SDRAM #3 to DSP pin
	DDRD37	H8	DQ05	Y	Connected SDRAM #3 to DSP pin
	DDRD38	G2	DQ06	Y	Connected SDRAM #3 to DSP pin
	DDRD39	H7	DQ07	Y	Connected SDRAM #3 to DSP pin
	DDRD40	D7	DQ08	Y	Connected SDRAM #3 to DSP pin
	DDRD41	C3	DQ09	Y	Connected SDRAM #3 to DSP pin
	DDRD42	C8	DQ10	Y	Connected SDRAM #3 to DSP pin
	DDRD43	C2	DQ11	Y	Connected SDRAM #3 to DSP pin
	DDRD44	A7	DQ12	Y	Connected SDRAM #3 to DSP pin
	DDRD45	A2	DQ13	Y	Connected SDRAM #3 to DSP pin
	DDRD46	B8	DQ14	Y	Connected SDRAM #3 to DSP pin
	DDRD47	A3	DQ15	Y	Connected SDRAM #3 to DSP pin
	DDRD48	E3	DQ00	Y	Connected SDRAM #4 to DSP pin
	DDRD49	F7	DQ01	Y	Connected SDRAM #4 to DSP pin
	DDRD50	F2	DQ02	Y	Connected SDRAM #4 to DSP pin
	DDRD51	F8	DQ03	Y	Connected SDRAM #4 to DSP pin
	DDRD52	H3	DQ04	Y	Connected SDRAM #4 to DSP pin
	DDRD53	H8	DQ05	Y	Connected SDRAM #4 to DSP pin
	DDRD54	G2	DQ06	Y	Connected SDRAM #4 to DSP pin
	DDRD55	H7	DQ07	Y	Connected SDRAM #4 to DSP pin
	DDRD56	D7	DQ08	Y	Connected SDRAM #4 to DSP pin
	DDRD57	C3	DQ09	Y	Connected SDRAM #4 to DSP pin
	DDRD58	C8	DQ10	Y	Connected SDRAM #4 to DSP pin
	DDRD59	C2	DQ11	Y	Connected SDRAM #4 to DSP pin
	DDRD60	A7	DQ12	Y	Connected SDRAM #4 to DSP pin
	DDRD61	A2	DQ13	Y	Connected SDRAM #4 to DSP pin
	DDRD62	B8	DQ14	Y	Connected SDRAM #4 to DSP pin
	DDRD63	A3	DQ15	Y	Connected SDRAM #4 to DSP pin
End of Table 63					

Table 64 Pin Connectivity →4 - 16M x16 x8 banks (8G bit total) [3 of 4]

Four 16 Meg x 16 x 8 banks (8G bit total) [3 of 4]			[MO-207 DU-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	$\overline{\text{DDRCE0}}$	L 2	CS#	Y	Connected SDRAM #1, 2, 3, & #4 to DSP pin
	$\overline{\text{DDRCE1}}$	L 2	CS#	N	Leave unconnected on DSP, only for use with dual-rank designs
	DDRBA0	M 2	BA0	Y	Connect to like pin between SDRAM and DSP
	DDRBA1	M 3	BA1	Y	Connect to like pin between SDRAM and DSP

Table 64 Pin Connectivity →4 - 16M x16 x8 banks (8G bit total) [3 of 4]

Four 16 Meg x 16 x 8 banks (8G bit total) [3 of 4]			[MO-207 DU-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRBA2	N 8	BA2	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRCAS}}$	K 3	CAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRRAS}}$	J 3	RAS#	Y	Connect to like pin between SDRAM and DSP
	$\overline{\text{DDRWE}}$	L 3	WE#	Y	Connect to like pin between SDRAM and DSP
	DDRCKE0	K 9	CKE	Y	Connect to like pin between SDRAM 1, 2, 3, & 4 and DSP
	DDRCKE1	K 9	CKE	N	Leave unconnected on DSP, only for use with dual-rank designs
	DDRCLKOUTP0	J 7	CK	Y	Connected SDRAM #1, 2, 3, & #4 to DSP pin
	DDRCLKOUTN0	K 7	CK#	Y	Connected SDRAM #1, 2, 3, & #4 to DSP pin
	DDRCLKOUTP1	J 7	CK	N	Leave unconnected on DSP, only for use with dual-rank designs
	DDRCLKOUTN1	K 7	CK#	N	Leave unconnected on DSP, only for use with dual-rank designs
	DDRODT0	K 1	ODT	Y	Connected SDRAM #1, 2, 3, & #4 to DSP pin
	DDRODT1	K 1	ODT	N	Leave unconnected on DSP, only for use with dual-rank designs
	DDRSLRATE0			Y	Under software or hardware control
	DDRSLRATE1			Y	Under software or hardware control
	DDRCB00			N	Leave unconnected
	DDRCB01			N	Leave unconnected
	DDRCB02			N	Leave unconnected
	DDRCB03			N	Leave unconnected
	DDRCB04			N	Leave unconnected
	DDRCB05			N	Leave unconnected
	DDRCB06			N	Leave unconnected
	DDRCB07			N	Leave unconnected
	DDRDQM0	E7	DML	Y	Connected SDRAM #1 to DSP pin
	DDRDQM1	D3	DMU	Y	Connected SDRAM #1 to DSP pin
	DDRDQM2	E7	DML	Y	Connected SDRAM #2 to DSP pin
	DDRDQM3	D3	DMU	Y	Connected SDRAM #2 to DSP pin
	DDRDQM4	E7	DML	Y	Connected SDRAM #3 to DSP pin
	DDRDQM5	D3	DMU	Y	Connected SDRAM #3 to DSP pin
	DDRDQM6	E7	DML	Y	Connected SDRAM #4 to DSP pin
	DDRDQM7	D3	DMU	Y	Connected SDRAM #4 to DSP pin
	DDRDQM8			N	Leave unconnected at DSP
	DDRDQS0N	G 3	LDQS#	Y	Connected SDRAM #1 to DSP pin
	DDRDQS0P	F 3	LDQS	Y	Connected SDRAM #1 to DSP pin
	DDRDQS1N	B7	UDQS#	Y	Connected SDRAM #1 to DSP pin
	DDRDQS1P	C7	UDQS	Y	Connected SDRAM #1 to DSP pin
	DDRDQS2N	G 3	LDQS#	Y	Connected SDRAM #2 to DSP pin
End of Table 64					

Table 65 Pin Connectivity →4 - 16M x16 x8 banks (8G bit total) [4 of 4]

Two 16 Meg x 16 x 8 banks (4G bit total) [4 of 4]			[MO-207 DU-z Package w/o support pins]		
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRDQS2P	F 3	LDQS	Y	Connected SDRAM #2 to DSP pin
	DDRDQS3N	B7	UDQS#	Y	Connected SDRAM #2 to DSP pin
	DDRDQS3P	C7	UDQS	Y	Connected SDRAM #2 to DSP pin

Table 65 Pin Connectivity →4 - 16M x16 x8 banks (8G bit total) [4 of 4]

Two 16 Meg x 16 x 8 banks (4G bit total) [4 of 4]					[MO-207 DU-z Package w/o support pins]
DSP Pin	**DSP Name**	**DDR3 Pin**	**DDR3 Name**	**Used (Y/N)**	**Note**
	DDRDQS4N	G 3	LDQS#	Y	Connected SDRAM #3 to DSP pin
	DDRDQS4P	F 3	LDQS	Y	Connected SDRAM #3 to DSP pin
	DDRDQS5N	B7	UDQS#	Y	Connected SDRAM #3 to DSP pin
	DDRDQS5P	C7	UDQS	Y	Connected SDRAM #3 to DSP pin
	DDRDQS6N	G 3	LDQS#	Y	Connected SDRAM #4 to DSP pin
	DDRDQS6P	F 3	LDQS	Y	Connected SDRAM #4 to DSP pin
	DDRDQS7N	B7	UDQS#	Y	Connected SDRAM #4 to DSP pin
	DDRDQS7P	C7	UDQS	Y	Connected SDRAM #4 to DSP pin
	DDRDQS8N			N	Leave unconnected at DSP
	DDRDQS8P			N	Leave unconnected at DSP
	DDRCLKP			Y	Differential DDR PLL clock input to DSP (+)
	DDRCLKN			Y	Differential DDR PLL clock input to DSP (-)
		L 8	ZQ	Y	Each DDR3 SDRAM ZQ pin should be tied to a 240Ω resistor to ground
	$\overline{\text{DDRREST}}$	T 2	RESET#	Y	DDR3 DSP & SDRAM reset pins
	AVDDA2			Y	DDRCLK PLL Power Supply, connect to dedicated and clean 1.8V (use filter)
$D_{VDD}15$	See device data manual	B2, D9, G7, K2, K8, N1, N9, R1, R9	Vdd	Y	Connected to respective VDD (1.5V) Supply, pay attention to tolerance and sequencing requirements
	See device data manual	A1, A8, C1, C9, D2, E9, F1, H2, H9	VddQ	Y	Connected to respective VDD (1.5V) Supply, pay attention to tolerance and sequencing requirements
		H 1	VrefDQ	Y	Connect to VDD/2, pay attention to power sequencing requirements
Vss	See device data manual	A9, B3, E1, G8, J2, J8, M1, M9, P1, P9, T1, T9	Vss	Y	Connected to Ground
		B1, B9, D1, D8, E2, E8, F9, G1, G9	VssQ	Y	Connected to Ground, connection MUST be short
	VREFSSTL	M 8	VrefCA	Y	DDR3 Vref pin, connect to DSP DDR3 Vdd/2 (.1% tol.).
					Connect to VDD/2, pay attention to power sequencing requirements
	PTV15A			Y	45.3Ω tied to ground (must be short)
		J1	NC	N	Leave unconnected on all SDRAMs
		J9	NC	N	Leave unconnected on all SDRAMs
		L1	NC	N	Leave unconnected on all SDRAMs
		L9	NC	N	Leave unconnected on all SDRAMs

End of Table 65

8.2 Package Pin Count & Pinout

Four different package pin counts exist within the JEDEC approved DDR3 SDRAM standard; 112, 106, 96, and 78 for all 1Gb, 2Gb, and 4Gb devices. Texas Instruments requires the use of JEDEC-compliant SDRAM and packages. Many companies offer subsets of these standard JEDEC packages including 82 and 86 pin versions which include only a partial subset of the added "support balls" – see the appropriate SDRAM data sheet for connectivity.

Per the JEDEC DDR3 standard, the recommended packaging type is MO-207. To allow for greater flexibility between packaging types it is recommended that all designs (where the added size of the different packages does not impact the final application form factor) be designed to include the support balls.

There exist two different packaging types for ×8 SDRAMs and two different packaging types for ×16 SDRAMs. Note that ×8 and ×16 SDRAMs are not compatible. Designs supporting ×16 SDRAMs will not allow ×8 SDRAMs to be used at a later date. Conversely, designs supporting ×8 SDRAMs will not allow ×16 SDRAMs to be used at a later date.

Packaging for ×8 SDRAM devices are defined as follows:

MO-207 ×8 (DW-z)	106 pin	With Support Pins	[Fig. 12] Figure 12
MO-207 ×8 (DW-z**)	106 pin	With Support Pins	[Fig. 13] Figure 13
MO-207 ×8 (DT-z)	78 pin	Without Support Pins	[Fig. 14] Figure 14
MO-207 8 (DT-z**)	78 pin	Without Support Pins	[Fig. 15] Figure 15

Note—Both ×8 parts are pin-compatible if board layout is performed for the package with support pins.

Note—**: Refers to "Stacked Die" Configurations.

Packaging for ×16 SDRAM devices are defined as follows:

MO-207 ×16 (DY-z)	112 pin	With Support Pins	[Fig. 16] Figure 16
MO-207 ×16 (DY-z**)	112 pin	With Support Pins	[Fig. 17] Figure 17
MO-207 ×16 (DU-z)	96 pin	Without Support Pins	[Fig. 18] Figure 18
MO-207 ×16 (DU-z**)	96 pin	Without Support Pins	[Fig. 19] Figure 19

Packaging for a ×72 UDIMM is defined as follows:

MO-269D	240 pin

Note—Both ×16 parts are pin-compatible if board layout is performed for the package with support pins.

Note—**: Refers to "Stacked Die" Configurations.

The following four figures define the JEDEC-compliant MO-207 packaging options and pinout for the ×8 and ×16 1Gb, 2Gb, and 4Gb DDR3 SDRAMs. The views provided are "through package" or top view.

Table 66 is provided as a quick legend for the JEDEC MO-207 packaging options. It should be noted that the pin numbers between ×8 devices and between ×16 devices are different, however this is attributed to the different packaging – actual pin placement within the same width devices is identical. For the purpose of comparison only, Figures 14 & 15, 18 & 19 also denote the extended pin (ball) placement for the larger packages.

Table 66 MO-207 Package Legend

	Address Pins
	Data Pins
	Ground
	Clock and Reference Pins (some NC)
	No Connect or Support Pins
	Control
	Power
SB	Support Pins (shown for comparison only)

Figure 12 DDR3 x8 SDRAM pinout in DW-z Package

MO-207 X8 pinout (DW-z)				106 Pin								
	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC		NC				NC		NC	NC	A
B												B
C	NC	NC		NC				NC		NC	NC	C
D												D
E												E
F	NC	VSS	VDD	NC				NU/TDQS#	VSS	VDD	NC	F
G		VSS	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ		G
H		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ		H
J		VSSQ	DQ6	DQS#				VDD	VSS	VSSQ		J
K		VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ		K
L		NC	VSSQ	RAS#				CK	VSS	NC		L
M		ODT	VDD	CAS#				CK#	VDD	CKE		M
N		NC	CS#	WE#				A10/AP	ZQ	NC		N
P		VSS	BA0	BA2				A15	VREFCA	VSS		P
R		VDDQ	A3	A0				A12/BC#	BA1	VDD		R
T		VSS	A5	A2				A1	A4	VSS		T
U		VDDQ	A7	A9				A11	A6	VDD		U
V	NC	VSS	RESET#	A13				A14	A8	VSS	NC	V
W												W
Y												Y
AA	NC	NC		NC				NC		NC	NC	AA
AB												AB
AC	NC	NC		NC				NC		NC	NC	AC

Figure 13 DDR3 x8 SDRAM pinout in DW-z Package (Stacked Die)

MO-207 X8 pinout (DW-z)				106 Pin								
Stack Die												
	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC		NC				NC		NC	NC	A
B												B
C	NC	NC		NC				NC		NC	NC	C
D												D
E												E
F	NC	VSS	VDD	NC				NU/TDQS#	VSS	VDD	NC	F
G		VSS	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ		G
H		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ		H
J		VSSQ	DQ6	DQS#				VDD	VSS	VSSQ		J
K		VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ		K
L		ODT1	VSSQ	RAS#				CK	VSS	CKE1		L
M		ODT0	VDD	CAS#				CK#	VDD	CKE0		M
N		CS1#	CS0#	WE#				A10/AP	ZQ0	ZQ1		N
P		VSS	BA0	BA2				A15	VREFCA	VSS		P
R		VDDQ	A3	A0				A12/BC#	BA1	VDD		R
T		VSS	A5	A2				A1	A4	VSS		T
U		VDDQ	A7	A9				A11	A6	VDD		U
V	NC	VSS	RESET#	A13				A14	A8	VSS	NC	V
W												W
Y												Y
AA	NC	NC		NC				NC		NC	NC	AA
AB												AB
AC	NC	NC		NC				NC		NC	NC	AC

Figure 14 DDR3 x8 SDRAM pinout in DT-z Package (Part 1 of 2)

MO-207 X8 pinout (DT-z)				78 Pin								
		1	2	3	4	5	6	7	8	9		
	SB	SB		SB				SB		SB	SB	A
												B
	SB	SB		SB				SB		SB	SB	C
												D
												E
A	SB	VSS	VDD	NC				NU/TDQS#	VSS	VDD	SB	F
B		VSS	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ		G
C		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ		H
D		VSSQ	DQ6	DQS#				VDD	VSS	VSSQ		J
E		VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ		K
F		NC	VSSQ	RAS#				CK	VSS	NC		L
G		ODT	VDD	CAS#				CK#	VDD	CKE		M

Figure 14 DDR3 x8 SDRAM pinout in DT-z Package (Part 2 of 2)

H		NC	CS#	WE#				A10/AP	ZQ	NC		N
J		VSS	BA0	BA2				A15	VREFCA	VSS		P
K		VDDQ	A3	A0				A12/BC#	BA1	VDD		R
L		VSS	A5	A2				A1	A4	VSS		T
M		VDDQ	A7	A9				A11	A6	VDD		U
N	SB	VSS	RESET#	A13				A14	A8	VSS	SB	V
												W
												Y
	SB	SB		SB				SB		SB	SB	AA
												AB
	SB	SB		SB				SB		SB	SB	AC
	1	2	3	4	5	6	7	8	9	10	11	

Figure 15 DDR3 x8 SDRAM pinout in DT-z Package (Stacked Die)

MO-207 X8 pinout (DT-z)				**78 Pin**								
Stacked Die												
		1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**		
	SB	SB		SB				SB		SB	SB	A
												B
	SB	SB		SB				SB		SB	SB	C
												D
												E
A	SB	VSS	VDD	NC				NU/TDQS#	VSS	VDD	SB	F
B		VSS	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ		G
C		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ		H
D		VSSQ	DQ6	DQS#				VDD	VSS	VSSQ		J
E		VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ		K
F		ODT1	VSSQ	RAS#				CK	VSS	CKE1		L
G		ODT0	VDD	CAS#				CK#	VDD	CKE0		M
H		CS1#	CS0#	WE#				A10/AP	ZQ0	ZQ1		N
J		VSS	BA0	BA2				A15	VREFCA	VSS		P
K		VDDQ	A3	A0				A12/BC#	BA1	VDD		R
L		VSS	A5	A2				A1	A4	VSS		T
M		VDDQ	A7	A9				A11	A6	VDD		U
N	SB	VSS	RESET#	A13				A14	A8	VSS	SB	V
												W
												Y
	SB	SB		SB				SB		SB	SB	AA
												AB
	SB	SB		SB				SB		SB	SB	AC

Figure 16 DDR3 x16 SDRAM pinout in DY-z Package

MO-207 x16 pinout (DY-z)				112 Pin								
	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC		NC				NC		NC	NC	
B												
C												
D	NC	VDDQ	DQU5 (DQ13)	DQU7 (DQ15)				DQU4 (DQ12)	VDDQ	VSS	NC	A
E		VSSQ	VDD	VSS				DQSU#	DQU6 (DQ14)	VSSQ		B
F		VDDQ	DQU3 (DQ11)	DQU1 (DQ09)				DQSU	DQU2 (DQ10)	VDDQ		C
G		VSSQ	VDDQ	DMU				DQU0 (DQ08)	VSSQ	VDD		D
H		VSS	VSSQ	DQL0 (DQ00)				DML	VSSQ	VDDQ		E
J		VDDQ	DQL2 (DQ02)	DQSL				DQL1 (DQ01)	DQL3 (DQ03)	VSSQ		F
K		VSSQ	DQL6 (DQ06)	DQSL#				VDD	VSS	VSSQ		G
L		VREFDQ	VDDQ	DQL4 (DQ04)				DQL7 (DQ07)	DQL5 (DQ05)	VDDQ		H
M		NC	VSS	RAS#				CK	VSS	NC		J
N		ODT	VDD	CAS#				CK#	VDD	CKE		K
P		NC	CS#	WE#				A10/AP	ZQ	NC		L
R		VSS	BA0	BA2				A15	VREFCA	VSS		M
T		VDD	A3	A0				A12/BC#	BA1	VDD		N
U		VSS	A5	A2				A1	A4	VSS		P
V		VDD	A7	A9				A11	A6	VDD		R
W	NC	VSS	RESET#	A13				A14	A8	VSS	NC	
Y												
AA												
AB	NC	NC		NC				NC		NC	NC	

Figure 17 DDR3 x16 SDRAM pinout in DY-z Package (Stacked Die) (Part 1 of 2)

MO-207 x16 pinout (DY-z)				112 Pin								
Stacked Die												
	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC		NC				NC		NC	NC	
B												
C												
D	NC	VDDQ	DQU5 (DQ13)	DQU7 (DQ15)				DQU4 (DQ12)	VDDQ	VSS	NC	A

Figure 17 DDR3 x16 SDRAM pinout in DY-z Package (Stacked Die) (Part 2 of 2)

E		VSSQ	VDD	VSS				DQSU#	DQU6 (DQ14)	VSSQ		B
F		VDDQ	DQU3 (DQ11)	DQU1 (DQ09)				DQSU	DQU2 (DQ10)	VDDQ		C
G		VSSQ	VDDQ	DMU				DQU0 (DQ08)	VSSQ	VDD		D
H		VSS	VSSQ	DQL0 (DQ00)				DML	VSSQ	VDDQ		E
J		VDDQ	DQL2 (DQ02)	DQSL				DQL1 (DQ01)	DQL3 (DQ03)	VSSQ		F
K		VSSQ	DQL6 (DQ06)	DQSL#				VDD	VSS	VSSQ		G
L		VREFDQ	VDDQ	DQL4 (DQ04)				DQL7 (DQ07)	DQL5 (DQ05)	VDDQ		H
M		ODT1	VSS	RAS#				CK	VSS	CKE1		J
N		ODT0	VDD	CAS#				CK#	VDD	CKE0		K
P		CS1#	CS0#	WE#				A10/AP	ZQ0	ZQ1		L
R		VSS	BA0	BA2				A15	VREFCA	VSS		M
T		VDD	A3	A0				A12/BC#	BA1	VDD		N
U		VSS	A5	A2				A1	A4	VSS		P
V		VDD	A7	A9				A11	A6	VDD		R
W	NC	VSS	RESET#	A13				A14	A8	VSS	NC	
Y												
AA												
AB	NC	NC		NC				NC		NC	NC	

Figure 18 DDR3 x16 SDRAM pinout in DU-z Package (Part 1 of 2)

MO-207 x16 pinout (DU-z)				**96 Pin**								
		1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**		
	SB	SB		SB				SB		SB	SB	A
												B
												C
A	SB	VDDQ	DQU5 (DQ13)	DQU7 (DQ15)				DQU4 (DQ12)	VDDQ	VSS	SB	D
B		VSSQ	VDD	VSS				DQSU#	DQU6 (DQ14)	VSSQ		E
C		VDDQ	DQU3 (DQ11)	DQU1 (DQ09)				DQSU	DQU2 (DQ10)	VDDQ		F
D		VSSQ	VDDQ	DMU				DQU0 (DQ08)	VSSQ	VDD		G
E		VSS	VSSQ	DQL0 (DQ00)				DML	VSSQ	VDDQ		H
F		VDDQ	DQL2 (DQ02)	DQSL				DQL1 (DQ01)	DQL3 (DQ03)	VSSQ		J

Figure 18 DDR3 x16 SDRAM pinout in DU-z Package (Part 2 of 2)

G		VSSQ	DQL6 (DQ06)	DQSL#				VDD	VSS	VSSQ		K
H		VREFDQ	VDDQ	DQL4 (DQ04)				DQL7 (DQ07)	DQL5 (DQ05)	VDDQ		L
J		NC	VSS	RAS#				CK	VSS	NC		M
K		ODT	VDD	CAS#				CK#	VDD	CKE		N
L		NC	CS#	WE#				A10/AP	ZQ	NC		P
M		VSS	BA0	BA2				A15	VREFCA	VSS		R
N		VDD	A3	A0				A12/BC#	BA1	VDD		T
P		VSS	A5	A2				A1	A4	VSS		U
R		VDD	A7	A9				A11	A6	VDD		V
T	SB	VSS	RESET#	A13				A14	A8	VSS	SB	W
Y												Y
AA												AA
AB	SB	SB		SB				SB		SB	SB	AB

Figure 19 DDR3 x16 SDRAM pinout in DU-z Package (Stacked Die) (Part 1 of 2)

MO-207 x16 pinout (DU-z)				**96 Pin**								
Stacked Die												
		1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**		
	SB	SB		SB				SB		SB	SB	A
												B
												C
A	SB	VDDQ	DQU5	DQU7				DQU4 (DQ12)	VDDQ	VSS	SB	D
B		VSSQ	VDD	VSS				DQSU#	DQU6 (DQ14)	VSSQ		E
C		VDDQ	DQU3	DQU1				DQSU	DQU2 (DQ10)	VDDQ		F
D		VSSQ	VDDQ	DMU				DQU0 (DQ08)	VSSQ	VDD		G
E		VSS	VSSQ	DQL0				DML	VSSQ	VDDQ		H
F		VDDQ	DQL2	DQSL				DQL1 (DQ01)	DQL3 (DQ03)	VSSQ		J
G		VSSQ	DQL6	DQSL#				VDD	VSS	VSSQ		K
H		VREFDQ	VDDQ	DQL4				DQL7 (DQ07)	DQL5 (DQ05)	VDDQ		L
J		ODT1	VSS	RAS#				CK	VSS	CKE1		M
K		ODT0	VDD	CAS#				CK#	VDD	CKE0		N
L		CS1#	CS0#	WE#				A10/AP	ZQ0	ZQ1		P
M		VSS	BA0	BA2				A15	VREFCA	VSS		R
N		VDD	A3	A0				A12/BC#	BA1	VDD		T
P		VSS	A5	A2				A1	A4	VSS		U
R		VDD	A7	A9				A11	A6	VDD		V
T	SB	VSS	RESET#	A13				A14	A8	VSS	SB	W

Figure 19 DDR3 x16 SDRAM pinout in DU-z Package (Stacked Die) (Part 2 of 2)

												Y
												AA
	SB	SB		SB				SB		SB	SB	AB

It should be noted that most manufacturers refer to DDR3 SDRAM packaging by the JEDEC defined number of pins (balls) on the package, i.e., 78 or 96. Still, many manufacturers incorporate additional pins (balls) into the number count (i.e., 82 and 100). These typically are comprised of a limited subset of the support pins (balls). See each respective manufacturers data sheet as well as the JEDEC standard for verification of package type and specific pinout before releasing the design.

See the layout and routing section of this DDR3 Design Guide for additional information.

8.3 UDIMM Configurations

The following section and subsections are provided as general guidelines for connection between the Keystone family of DSP DDR3 Controller to both a 240-pin ECC and NON-ECC UDIMMs. See the specific DSP and UDIMM data manuals for final pin nomenclature and pin assignment before finalizing designs.

8.3.1 Common UDIMM Configurations

The following two tables define the pinout between the Keystone family of DSP DDR3 controller interface and a single 240-pin ECC UDIMM module. Confirm all DDR3 pin numbers before finalizing designs.

8.3.1.1 One 4Gb ECC UDIMM Module

The ECC UDIMM pinout table provided in Section 4.1.2 and tables in this subsection describe the recommended configuration for a single 4Gb 240-pin ECC UDIMM. The following two tables define in detail the expected pin connectivity between the Keystone family of DSPs and UDIMM module (for front and back side of DIMM respectfully). Other configurations and densities exist and should be connected in a similar manner. See the DSP data manual and UDIMM data sheet for connectivity requirements. Connectivity between the DSP and UDIMM as indicated will support one single or one dual rank UDIMM. The pin connectivity definition identified in the following tables is based on a 240-pin UDIMM module specification – always confirm the pin locations for the UDIMM and DSP before proceeding as specifications may have changed.

Additionally, this section will provide guidelines for interfacing the DSP to a UDIMM. (Specific details pertaining to UDIMMs can be found in the JEDEC DDR3 UDIMM standard 21C and JEDEC PS-001 latest revisions.)

The following example is offered as an example for connecting the Keystone DSP DDR3 SDRAM interface to a 4Gb UDIMM module. Other manufacturers and UDIMM models may be available and should be connected accordingly. See the SDRAM manufacturer's data sheet for confirmation or pin nomenclature and connectivity.

Note—Texas Instruments does not support a dual UDIMM dual rank configuration.

Table 67 ECC 4Gb x72 UDIMM to DSP pinout - Front Side (Part 1 of 3)

		FRONT SIDE - DSP to SOCKET CONNECTIONS		
DSP Name	**DSP Pin**		**UDIMM Pin #**	**UDIMM Pin Name**
		Tie to Dvdd15 rail, pay attention to tolerance and sequencing	1	VrefDQ
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	2	Vss
DDRD00	See data sheet	Connect between corresponding DSP and UDIMM socket pins	3	DQ0
DDRD01	See data sheet	Connect between corresponding DSP and UDIMM socket pins	4	DQ1
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	5	Vss
DDRDQS0N	See data sheet	Connect between corresponding DSP and UDIMM socket pins	6	DQS0#
DDRDQS0P	See data sheet	Connect between corresponding DSP and UDIMM socket pins	7	DQS0
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	8	Vss
DDRD02	See data sheet	Connect between corresponding DSP and UDIMM socket pins	9	DQ2
DDRD03	See data sheet	Connect between corresponding DSP and UDIMM socket pins	10	DQ3
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	11	Vss
DDRD08	See data sheet	Connect between corresponding DSP and UDIMM socket pins	12	DQ8
DDRD09	See data sheet	Connect between corresponding DSP and UDIMM socket pins	13	DQ9
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	14	Vss
DDRDQS1N	See data sheet	Connect between corresponding DSP and UDIMM socket pins	15	DQS1#
DDRDQS1P	See data sheet	Connect between corresponding DSP and UDIMM socket pins	16	DQS1
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	17	Vss
DDRD10	See data sheet	Connect between corresponding DSP and UDIMM socket pins	18	DQ10
DDRD11	See data sheet	Connect between corresponding DSP and UDIMM socket pins	19	DQ11
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	20	Vss
DDRD16	See data sheet	Connect between corresponding DSP and UDIMM socket pins	21	DQ16
DDRD17	See data sheet	Connect between corresponding DSP and UDIMM socket pins	22	DQ17
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	23	Vss
DDRDQS2N	See data sheet	Connect between corresponding DSP and UDIMM socket pins	24	DQS2#
DDRDQS2P	See data sheet	Connect between corresponding DSP and UDIMM socket pins	25	DQS2
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	26	Vss
DDRD18	See data sheet	Connect between corresponding DSP and UDIMM socket pins	27	DQ18
DDRD19	See data sheet	Connect between corresponding DSP and UDIMM socket pins	28	DQ19
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	29	Vss
DDRD24	See data sheet	Connect between corresponding DSP and UDIMM socket pins	30	DQ24
DDRD25	See data sheet	Connect between corresponding DSP and UDIMM socket pins	31	DQ25
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	32	Vss
DDRDQS3N	See data sheet	Connect between corresponding DSP and UDIMM socket pins	33	DQS3#
DDRDQS3P	See data sheet	Connect between corresponding DSP and UDIMM socket pins	34	DQS3
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	35	Vss
DDRD26	See data sheet	Connect between corresponding DSP and UDIMM socket pins	36	DQ26
DDRD27	See data sheet	Connect between corresponding DSP and UDIMM socket pins	37	DQ27
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	38	Vss
DDRCB00	See data sheet	Connect between corresponding DSP and UDIMM socket pins	39	CB0
DDRCB01	See data sheet	Connect between corresponding DSP and UDIMM socket pins	40	CB1
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	41	Vss
DDRDQS8N	See data sheet	Connect between corresponding DSP and UDIMM socket pins	42	DQS8#

Table 67 ECC 4Gb x72 UDIMM to DSP pinout - Front Side (Part 2 of 3)

		FRONT SIDE - DSP to SOCKET CONNECTIONS		
DSP Name	**DSP Pin**		**UDIMM Pin #**	**UDIMM Pin Name**
DDRDQS8P	See data sheet	Connect between corresponding DSP and UDIMM socket pins	43	DQS8
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	44	Vss
DDRCB02	See data sheet	Connect between corresponding DSP and UDIMM socket pins	45	CB2
DDRCB03	See data sheet	Connect between corresponding DSP and UDIMM socket pins	46	CB3
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	47	Vss
		Termination voltage, VDD/2, must track 1.5 V supply	48	Vtt, NC
		Termination voltage, VDD/2, must track 1.5 V supply	49	Vtt, NC
DDRCKE0	See data sheet	Connect between corresponding DSP and UDIMM socket pins	50	CKE0
DVDD15	See data sheet	Tie to Common DVDD15 Rail	51	Vdd
DDRBA2	See data sheet	Connect between corresponding DSP and UDIMM socket pins	52	BA2
		Error Out - unused	53	NC
DVDD15	See data sheet	Tie to Common DVDD15 Rail	54	Vdd
DDRA11	See data sheet	Connect between corresponding DSP and UDIMM socket pins	55	A11
DDRA07	See data sheet	Connect between corresponding DSP and UDIMM socket pins	56	A7
DVDD15	See data sheet	Tie to Common DVDD15 Rail	57	Vdd
DDRA05	See data sheet	Connect between corresponding DSP and UDIMM socket pins	58	A5
DDRA04	See data sheet	Connect between corresponding DSP and UDIMM socket pins	59	A4
DVDD15	See data sheet	Tie to Common DVDD15 Rail	60	Vdd
DDRA02	See data sheet	Connect between corresponding DSP and UDIMM socket pins	61	A2
DVDD15	See data sheet	Tie to Common DVDD15 Rail	62	Vdd
DDRCLKOUTP0	See data sheet	Connect between corresponding DSP and UDIMM socket pins	63	CK1
DDRCLKOUTN0	See data sheet	Connect between corresponding DSP and UDIMM socket pins	64	CK1#
DVDD15	See data sheet	Tie to Common DVDD15 Rail	65	Vdd
DVDD15	See data sheet	Tie to Common DVDD15 Rail	66	Vdd
VrefSSTL	See data sheet	Connect between corresponding DSP and UDIMM socket pins	67	VrefCA
		Par_IN, unused	68	NC
DVDD15	See data sheet	Tie to Common DVDD15 Rail	69	Vdd
DDRA10	See data sheet	Connect between corresponding DSP and UDIMM socket pins	70	A10
DDRBA0	See data sheet	Connect between corresponding DSP and UDIMM socket pins	71	BA0
DVDD15	See data sheet	Tie to Common DVDD15 Rail	72	Vdd
$\overline{\text{DDRWE}}$	See data sheet	Connect between corresponding DSP and UDIMM socket pins	73	WE#
$\overline{\text{DDRCAS}}$	See data sheet	Connect between corresponding DSP and UDIMM socket pins	74	CAS#
DVDD15	See data sheet	Tie to Common DVDD15 Rail	75	Vdd
DDRCKE1	See data sheet	Connect between corresponding DSP and UDIMM socket pins	76	S1#
DDRODT1	See data sheet	Connect between corresponding DSP and UDIMM socket pins	77	ODT1
DVDD15	See data sheet	Tie to Common DVDD15 Rail	78	Vdd
		Select, unused	79	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	80	Vss
DDRD32	See data sheet	Connect between corresponding DSP and UDIMM socket pins	81	DQ32
DDRD33	See data sheet	Connect between corresponding DSP and UDIMM socket pins	82	DQ33
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	83	Vss
DDRDQS4N	See data sheet	Connect between corresponding DSP and UDIMM socket pins	84	DQS4#

Table 67 ECC 4Gb x72 UDIMM to DSP pinout - Front Side (Part 3 of 3)

		FRONT SIDE - DSP to SOCKET CONNECTIONS		
DSP Name	DSP Pin		UDIMM Pin #	UDIMM Pin Name
DDRDQS4P	See data sheet	Connect between corresponding DSP and UDIMM socket pins	85	DQS4
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	86	Vss
DDRD34	See data sheet	Connect between corresponding DSP and UDIMM socket pins	87	DQ34
DDRD35	See data sheet	Connect between corresponding DSP and UDIMM socket pins	88	DQ35
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	89	Vss
DDRD40	See data sheet	Connect between corresponding DSP and UDIMM socket pins	90	DQ40
DDRD41	See data sheet	Connect between corresponding DSP and UDIMM socket pins	91	DQ41
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	92	Vss
DDRDQS5N	See data sheet	Connect between corresponding DSP and UDIMM socket pins	93	DQS5#
DDRDQS5P	See data sheet	Connect between corresponding DSP and UDIMM socket pins	94	DQS5
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	95	Vss
DDRD42	See data sheet	Connect between corresponding DSP and UDIMM socket pins	96	DQ42
DDRD43	See data sheet	Connect between corresponding DSP and UDIMM socket pins	97	DQ43
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	98	Vss
DDRD48	See data sheet	Connect between corresponding DSP and UDIMM socket pins	99	DQ48
DDRD49	See data sheet	Connect between corresponding DSP and UDIMM socket pins	100	DQ49
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	101	Vss
DDRDQS6N	See data sheet	Connect between corresponding DSP and UDIMM socket pins	102	DQS6#
DDRDQS6P	See data sheet	Connect between corresponding DSP and UDIMM socket pins	103	DQS6
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	104	Vss
DDRD50	See data sheet	Connect between corresponding DSP and UDIMM socket pins	105	DQ50
DDRD51	See data sheet	Connect between corresponding DSP and UDIMM socket pins	106	DQ51
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	107	Vss
DDRD56	See data sheet	Connect between corresponding DSP and UDIMM socket pins	108	DQ56
DDRD57	See data sheet	Connect between corresponding DSP and UDIMM socket pins	109	DQ57
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	110	Vss
DDRDQS7N	See data sheet	Connect between corresponding DSP and UDIMM socket pins	111	DQS7#
DDRDQS7P	See data sheet	Connect between corresponding DSP and UDIMM socket pins	112	DQS7
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	113	Vss
DDRD58	See data sheet	Connect between corresponding DSP and UDIMM socket pins	114	DQ58
DDRD59	See data sheet	Connect between corresponding DSP and UDIMM socket pins	115	DQ59
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	116	Vss
		N/C used for programming UDIMM thermal sensor	117	SA0
			118	SCL
		N/C used for programming UDIMM thermal sensor	119	SA2
Vss	See data sheet	Termination voltage, VDD/2, must track 1.5 V supply	120	Vtt

Table 68 ECC 4Gb x72 UDIMM to DSP pinout - Back Side (Part 1 of 3)

		BACK SIDE DSP to SOCKET CONNECTIONS		
DSP Name	DSP Pin		UDIMM Pin #	UDIMM Pin Name
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	121	Vss
DDRD04	See data sheet	Connect between corresponding DSP and UDIMM socket pins	122	DQ4
DDRD05	See data sheet	Connect between corresponding DSP and UDIMM socket pins	123	DQ5
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	124	Vss
DDRDQM0	See data sheet	Connect between corresponding DSP and UDIMM socket pins	125	DM0
	See data sheet	Unused	126	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	127	Vss
DDRD06	See data sheet	Connect between corresponding DSP and UDIMM socket pins	128	DQ6
DDRD07	See data sheet	Connect between corresponding DSP and UDIMM socket pins	129	DQ7
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	130	Vss
DDRD12	See data sheet	Connect between corresponding DSP and UDIMM socket pins	131	DQ12
DDRD13	See data sheet	Connect between corresponding DSP and UDIMM socket pins	132	DQ13
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	133	Vss
DDRDQM1	See data sheet	Connect between corresponding DSP and UDIMM socket pins	134	DM1
		Unused	135	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	136	Vss
DDRD14	See data sheet	Connect between corresponding DSP and UDIMM socket pins	137	DQ14
DDRD15	See data sheet	Connect between corresponding DSP and UDIMM socket pins	138	DQ15
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	139	Vss
DDRD20	See data sheet	Connect between corresponding DSP and UDIMM socket pins	140	DQ20
DDRD21	See data sheet	Connect between corresponding DSP and UDIMM socket pins	141	DQ21
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	142	Vss
DDRDQM2	See data sheet	Connect between corresponding DSP and UDIMM socket pins	143	DM2
		Unused	144	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	145	Vss
DDRD22	See data sheet	Connect between corresponding DSP and UDIMM socket pins	146	DQ22
DDRD23	See data sheet	Connect between corresponding DSP and UDIMM socket pins	147	DQ23
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	148	Vss
DDRD28	See data sheet	Connect between corresponding DSP and UDIMM socket pins	149	DQ28
DDRD29	See data sheet	Connect between corresponding DSP and UDIMM socket pins	150	DQ29
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	151	Vss
DDRDQM3	See data sheet	Connect between corresponding DSP and UDIMM socket pins	152	DM3
	See data sheet	Unused	153	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	154	Vss
DDRD30	See data sheet	Connect between corresponding DSP and UDIMM socket pins	155	DQ30
DDRD31	See data sheet	Connect between corresponding DSP and UDIMM socket pins	156	DQ31
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	157	Vss
DDRCB04	See data sheet	Connect between corresponding DSP and UDIMM socket pins	158	CB4
DDRCB05	See data sheet	Connect between corresponding DSP and UDIMM socket pins	159	CB5
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	160	Vss
DDRDQM8	See data sheet	Connect between corresponding DSP and UDIMM socket pins	161	DM8
	See data sheet	Unused	162	NC

Table 68 ECC 4Gb x72 UDIMM to DSP pinout - Back Side (Part 2 of 3)

		BACK SIDE DSP to SOCKET CONNECTIONS		
DSP Name	**DSP Pin**		**UDIMM Pin #**	**UDIMM Pin Name**
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	163	Vss
DDRCB06	See data sheet	Connect between corresponding DSP and UDIMM socket pins	164	CB6
DDRCB07	See data sheet	Connect between corresponding DSP and UDIMM socket pins	165	CB7
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	166	Vss
	See data sheet	Test Pin - unused	167	NU
$\overline{\text{DDRRESET}}$	See data sheet	Connect between corresponding DSP and UDIMM socket pins	168	RESET#
DDRCKE1	See data sheet	Connect between corresponding DSP and UDIMM socket pins	169	CKE1
DVDD15	See data sheet	Tie to Common DVDD15 Rail	170	Vdd
DDRA15	See data sheet	Connect between corresponding DSP and UDIMM socket pins	171	NF/A15
DDRA14	See data sheet	Connect between corresponding DSP and UDIMM socket pins	172	NF/A14
DVDD15	See data sheet	Tie to Common DVDD15 Rail	173	Vdd
DDRA12	See data sheet	Connect between corresponding DSP and UDIMM socket pins	174	A12
DDRA09	See data sheet	Connect between corresponding DSP and UDIMM socket pins	175	A9
DVDD15	See data sheet	Tie to Common DVDD15 Rail	176	Vdd
DDRA08	See data sheet	Connect between corresponding DSP and UDIMM socket pins	177	A8
DDRA06	See data sheet	Connect between corresponding DSP and UDIMM socket pins	178	A6
DVDD15	See data sheet	Tie to Common DVDD15 Rail	179	Vdd
DDRA03	See data sheet	Connect between corresponding DSP and UDIMM socket pins	180	A3
DDRA01	See data sheet	Connect between corresponding DSP and UDIMM socket pins	181	A1
DVDD15	See data sheet	Tie to Common DVDD15 Rail	182	Vdd
DVDD15	See data sheet	Tie to Common DVDD15 Rail	183	Vdd
DDRCLKOUTP0	See data sheet	Connect between corresponding DSP and UDIMM socket pins	184	CK0
DDRCLKOUTN0	See data sheet	Connect between corresponding DSP and UDIMM socket pins	185	CK0#
DVDD15	See data sheet	Tie to Common DVDD15 Rail	186	Vdd
	See data sheet	Not required, used for temperature alert	187	EVENT#
DDRA00	See data sheet	Connect between corresponding DSP and UDIMM socket pins	188	A0
DVDD15	See data sheet	Tie to Common DVDD15 Rail	189	Vdd
DDRBA1	See data sheet	Connect between corresponding DSP and UDIMM socket pins	190	BA1
DVDD15	See data sheet	Tie to Common DVDD15 Rail	191	Vdd
$\overline{\text{DDRRAS}}$	See data sheet	Connect between corresponding DSP and UDIMM socket pins	192	RAS#
$\overline{\text{DDRCE0}}$	See data sheet	Connect between corresponding DSP and UDIMM socket pins	193	S0#
DVDD15	See data sheet	Tie to Common DVDD15 Rail	194	Vdd
DDRODT0	See data sheet	Connect between corresponding DSP and UDIMM socket pins	195	ODT0
DDRA13	See data sheet	Connect between corresponding DSP and UDIMM socket pins	196	A13
DVDD15	See data sheet	Tie to Common DVDD15 Rail	197	Vdd
		Unused	198	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	199	Vss
DDRD36	See data sheet	Connect between corresponding DSP and UDIMM socket pins	200	DQ36
DDRD37	See data sheet	Connect between corresponding DSP and UDIMM socket pins	201	DQ37
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	202	Vss
DDRDQM4	See data sheet	Connect between corresponding DSP and UDIMM socket pins	203	DM4
		Unused	204	NC

Table 68 ECC 4Gb x72 UDIMM to DSP pinout - Back Side (Part 3 of 3)

		BACK SIDE DSP to SOCKET CONNECTIONS		
DSP Name	**DSP Pin**		**UDIMM Pin #**	**UDIMM Pin Name**
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	205	Vss
DDRD38	See data sheet	Connect between corresponding DSP and UDIMM socket pins	206	DQ38
DDRD39	See data sheet	Connect between corresponding DSP and UDIMM socket pins	207	DQ39
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	208	Vss
DDRD44	See data sheet	Connect between corresponding DSP and UDIMM socket pins	209	DQ44
DDRD45	See data sheet	Connect between corresponding DSP and UDIMM socket pins	210	DQ45
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	211	Vss
DDRDQM5	See data sheet	Connect between corresponding DSP and UDIMM socket pins	212	DM5
	See data sheet	Unused	213	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	214	Vss
DDRD46	See data sheet	Connect between corresponding DSP and UDIMM socket pins	215	DQ46
DDRD47	See data sheet	Connect between corresponding DSP and UDIMM socket pins	216	DQ47
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	217	Vss
DDRD52	See data sheet	Connect between corresponding DSP and UDIMM socket pins	218	DQ52
DDRD53	See data sheet	Connect between corresponding DSP and UDIMM socket pins	219	DQ53
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	220	Vss
DDRDQM6	See data sheet	Connect between corresponding DSP and UDIMM socket pins	221	DM6
		Unused	222	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	223	Vss
DDRD54	See data sheet	Connect between corresponding DSP and UDIMM socket pins	224	DQ54
DDRD55	See data sheet	Connect between corresponding DSP and UDIMM socket pins	225	DQ55
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	226	Vss
DDRD60	See data sheet	Connect between corresponding DSP and UDIMM socket pins	227	DQ60
DDRD61	See data sheet	Connect between corresponding DSP and UDIMM socket pins	228	DQ61
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	229	Vss
DDRDQM7	See data sheet	Connect between corresponding DSP and UDIMM socket pins	230	DM7
		Unused	231	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	232	Vss
DDRD62	See data sheet	Connect between corresponding DSP and UDIMM socket pins	233	DQ62
DDRD63	See data sheet	Connect between corresponding DSP and UDIMM socket pins	234	DQ63
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	235	Vss
		Connect to clean 3.3 V ±1% tolerance	236	Vddspd
		N/C, used for programming udimm thermal sensor	237	SA1
		N/C, used for programming udimm thermal sensor	238	SDA
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	239	Vss
		Termination voltage, VDD/2, must track 1.5 V supply	240	Vtt

8.3.1.2 One 4Gb non-ECC UDIMM Module

The non-ECC UDIMM pinout table provided in Section 4.1.2 and tables in this subsection describe the recommended configuration for a single 4Gb 240-pin non-ECC UDIMM. The following two tables define in detail the expected pin connectivity between the Keystone family DSP and a non-ECC UDIMM module (front and back side of DIMM respectfully). Other configurations and densities exist and should be connected in a similar manner. See the DSP data manual and UDIMM data sheet for connectivity requirements. Connectivity between the DSP and UDIMM as indicated will support one single or one dual rank UDIMM. The pin connectivity definition identified in the following tables is based on a 240-pin UDIMM module specification – always confirm the pin locations for the UDIMM and DSP before proceeding as specifications may have changed.

Additionally, this section will provide guidelines for interfacing the DSP to a UDIMM. (Specific details pertaining to UDIMMs can be found in the JEDEC DDR3 UDIMM standard 21C and JEDEC PS-001 latest revisions.)

The following example is offered as an example for connecting the Keystone DSP DDR3 SDRAM interface to a 4Gb UDIMM module. Other manufacturers and UDIMM models may be available and should be connected accordingly. See the SDRAM manufacturer's data sheet for confirmation or pin nomenclature and connectivity.

The following two tables define the pinout between the Keystone DSP DDR3 controller interface and a single 240-pin non-ECC UDIMM module. Confirm all DDR3 pin numbers and DSP interface before finalizing designs.

Note—Texas Instruments does not support a dual UDIMM dual rank configuration.

Table 69 Non-ECC 4Gb x64 UDIMM to DSP Pinout - Front Side (Part 1 of 4)

		FRONT SIDE - DSP to SOCKET CONNECTIONS		
DSP Name	**DSP Pin**		**UDIMM Pin #**	**UDIMM Pin Name**
		Tie to DVDD15 rail, pay attention to tolerance and sequencing	1	VrefDQ
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	2	Vss
DDRD00	See data sheet	Connect between corresponding DSP and UDIMM socket pins	3	DQ0
DDRD01	See data sheet	Connect between corresponding DSP and UDIMM socket pins	4	DQ1
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	5	Vss
DDRDQS0N	See data sheet	Connect between corresponding DSP and UDIMM socket pins	6	DQS0#
DDRDQS0P	See data sheet	Connect between corresponding DSP and UDIMM socket pins	7	DQS0
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	8	Vss
DDRD02	See data sheet	Connect between corresponding DSP and UDIMM socket pins	9	DQ2
DDRD03	See data sheet	Connect between corresponding DSP and UDIMM socket pins	10	DQ3
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	11	Vss
DDRD08	See data sheet	Connect between corresponding DSP and UDIMM socket pins	12	DQ8
DDRD09	See data sheet	Connect between corresponding DSP and UDIMM socket pins	13	DQ9
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	14	Vss
DDRDQS1N	See data sheet	Connect between corresponding DSP and UDIMM socket pins	15	DQS1#
DDRDQS1P	See data sheet	Connect between corresponding DSP and UDIMM socket pins	16	DQS1

Table 69 Non-ECC 4Gb x64 UDIMM to DSP Pinout - Front Side (Part 2 of 4)

		FRONT SIDE - DSP to SOCKET CONNECTIONS		
DSP Name	**DSP Pin**		**UDIMM Pin #**	**UDIMM Pin Name**
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	17	Vss
DDRD10	See data sheet	Connect between corresponding DSP and UDIMM socket pins	18	DQ10
DDRD11	See data sheet	Connect between corresponding DSP and UDIMM socket pins	19	DQ11
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	20	Vss
DDRD16	See data sheet	Connect between corresponding DSP and UDIMM socket pins	21	DQ16
DDRD17	See data sheet	Connect between corresponding DSP and UDIMM socket pins	22	DQ17
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	23	Vss
DDRDQS2N	See data sheet	Connect between corresponding DSP and UDIMM socket pins	24	DQS2#
DDRDQS2P	See data sheet	Connect between corresponding DSP and UDIMM socket pins	25	DQS2
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	26	Vss
DDRD18	See data sheet	Connect between corresponding DSP and UDIMM socket pins	27	DQ18
DDRD19	See data sheet	Connect between corresponding DSP and UDIMM socket pins	28	DQ19
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	29	Vss
DDRD24	See data sheet	Connect between corresponding DSP and UDIMM socket pins	30	DQ24
DDRD25	See data sheet	Connect between corresponding DSP and UDIMM socket pins	31	DQ25
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	32	Vss
DDRDQS3N	See data sheet	Connect between corresponding DSP and UDIMM socket pins	33	DQS3#
DDRDQS3P	See data sheet	Connect between corresponding DSP and UDIMM socket pins	34	DQS3
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	35	Vss
DDRD26	See data sheet	Connect between corresponding DSP and UDIMM socket pins	36	DQ26
DDRD27	See data sheet	Connect between corresponding DSP and UDIMM socket pins	37	DQ27
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	38	Vss
DDRCB00	See data sheet	Unused – leave unconnected	39	NC
DDRCB01	See data sheet	Unused – leave unconnected	40	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	41	Vss
DDRDQS8N	See data sheet	Unused – leave unconnected	42	NC
DDRDQS8P	See data sheet	Unused – leave unconnected	43	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	44	Vss
DDRCB02	See data sheet	Unused – leave unconnected	45	NC
DDRCB03	See data sheet	Unused – leave unconnected	46	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	47	Vss
		Termination voltage, VDD/2, must track 1.5 V supply	48	Vtt, NC
		Termination voltage, VDD/2, must track 1.5 V supply	49	Vtt, NC
DDRCKE0	See data sheet	Connect between corresponding DSP and UDIMM socket pins	50	CKE0
DVDD15	See data sheet	Tie to Common DVDD15 Rail	51	Vdd
DDRBA2	See data sheet	Connect between corresponding DSP and UDIMM socket pins	52	BA2
		Error Out - unused	53	NC
DVDD15	See data sheet	Tie to Common DVDD15 Rail	54	Vdd
DDRA11	See data sheet	Connect between corresponding DSP and UDIMM socket pins	55	A11
DDRA07	See data sheet	Connect between corresponding DSP and UDIMM socket pins	56	A7
DVDD15	See data sheet	Tie to Common DVDD15 Rail	57	Vdd

Table 69 Non-ECC 4Gb x64 UDIMM to DSP Pinout - Front Side (Part 3 of 4)

		FRONT SIDE - DSP to SOCKET CONNECTIONS		
DSP Name	**DSP Pin**		**UDIMM Pin #**	**UDIMM Pin Name**
DDRA05	See data sheet	Connect between corresponding DSP and UDIMM socket pins	58	A5
DDRA04	See data sheet	Connect between corresponding DSP and UDIMM socket pins	59	A4
DVDD15	See data sheet	Tie to Common DVDD15 Rail	60	Vdd
DDRA02	See data sheet	Connect between corresponding DSP and UDIMM socket pins	61	A2
DVDD15	See data sheet	Tie to Common DVDD15 Rail	62	Vdd
DDRCLKOUTP0	See data sheet	Connect between corresponding DSP and UDIMM socket pins	63	CK1
DDRCLKOUTN0	See data sheet	Connect between corresponding DSP and UDIMM socket pins	64	CK1#
DVDD15	See data sheet	Tie to Common DVDD15 Rail	65	Vdd
DVDD15	See data sheet	Tie to Common DVDD15 Rail	66	Vdd
VrefSSTL	See data sheet	Connect between corresponding DSP and UDIMM socket pins	67	VrefCA
		Par_IN, unused	68	NC
DVDD15	See data sheet	Tie to Common DVDD15 Rail	69	Vdd
DDRA10	See data sheet	Connect between corresponding DSP and UDIMM socket pins	70	A10
DDRBA0	See data sheet	Connect between corresponding DSP and UDIMM socket pins	71	BA0
DVDD15	See data sheet	Tie to Common DVDD15 Rail	72	Vdd
$\overline{\text{DDRWE}}$	See data sheet	Connect between corresponding DSP and UDIMM socket pins	73	WE#
$\overline{\text{DDRCAS}}$	See data sheet	Connect between corresponding DSP and UDIMM socket pins	74	CAS#
DVDD15	See data sheet	Tie to Common DVDD15 Rail	75	Vdd
DDRCKE1	See data sheet	Connect between corresponding DSP and UDIMM socket pins	76	S1#
DDRODT1	See data sheet	Connect between corresponding DSP and UDIMM socket pins	77	ODT1
DVDD15	See data sheet	Tie to Common DVDD15 Rail	78	Vdd
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	80	Vss
DDRD32	See data sheet	Connect between corresponding DSP and UDIMM socket pins	81	DQ32
DDRD33	See data sheet	Connect between corresponding DSP and UDIMM socket pins	82	DQ33
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	83	Vss
DDRDQS4N	See data sheet	Connect between corresponding DSP and UDIMM socket pins	84	DQS4#
DDRDQS4P	See data sheet	Connect between corresponding DSP and UDIMM socket pins	85	DQS4
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	86	Vss
DDRD34	See data sheet	Connect between corresponding DSP and UDIMM socket pins	87	DQ34
DDRD35	See data sheet	Connect between corresponding DSP and UDIMM socket pins	88	DQ35
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	89	Vss
DDRD40	See data sheet	Connect between corresponding DSP and UDIMM socket pins	90	DQ40
DDRD41	See data sheet	Connect between corresponding DSP and UDIMM socket pins	91	DQ41
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	92	Vss
DDRDQS5N	See data sheet	Connect between corresponding DSP and UDIMM socket pins	93	DQS5#
DDRDQS5P	See data sheet	Connect between corresponding DSP and UDIMM socket pins	94	DQS5
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	95	Vss
DDRD42	See data sheet	Connect between corresponding DSP and UDIMM socket pins	96	DQ42
DDRD43	See data sheet	Connect between corresponding DSP and UDIMM socket pins	97	DQ43
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	98	Vss
DDRD48	See data sheet	Connect between corresponding DSP and UDIMM socket pins	99	DQ48
DDRD49	See data sheet	Connect between corresponding DSP and UDIMM socket pins	100	DQ49

Table 69 Non-ECC 4Gb x64 UDIMM to DSP Pinout - Front Side (Part 4 of 4)

		FRONT SIDE - DSP to SOCKET CONNECTIONS		
DSP Name	**DSP Pin**		**UDIMM Pin #**	**UDIMM Pin Name**
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	101	Vss
DDRDQS6N	See data sheet	Connect between corresponding DSP and UDIMM socket pins	102	DQS6#
DDRDQS6P	See data sheet	Connect between corresponding DSP and UDIMM socket pins	103	DQS6
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	104	Vss
DDRD50	See data sheet	Connect between corresponding DSP and UDIMM socket pins	105	DQ50
DDRD51	See data sheet	Connect between corresponding DSP and UDIMM socket pins	106	DQ51
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	107	Vss
DDRD56	See data sheet	Connect between corresponding DSP and UDIMM socket pins	108	DQ56
DDRD57	See data sheet	Connect between corresponding DSP and UDIMM socket pins	109	DQ57
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	110	Vss
DDRDQS7N	See data sheet	Connect between corresponding DSP and UDIMM socket pins	111	DQS7#
DDRDQS7P	See data sheet	Connect between corresponding DSP and UDIMM socket pins	112	DQS7
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	113	Vss
DDRD58	See data sheet	Connect between corresponding DSP and UDIMM socket pins	114	DQ58
DDRD59	See data sheet	Connect between corresponding DSP and UDIMM socket pins	115	DQ59
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	116	Vss
		N/C used for programming UDIMM thermal sensor	117	SA0
			118	SCL
		N/C used for programming UDIMM thermal sensor	119	SA2
Vss	See data sheet	Termination voltage, VDD/2, must track 1.5 V supply	120	Vtt

Table 70 Non-ECC 4Gb x64 UDIMM to DSP pinout - Back Side (Part 1 of 4)

		BACK SIDE DSP to SOCKET CONNECTIONS		
DSP Name	**DSP Pin**		**UDIMM Pin #**	**UDIMM Pin Name**
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	121	Vss
DDRD04	See data sheet	Connect between corresponding DSP and UDIMM socket pins	122	DQ4
DDRD05	See data sheet	Connect between corresponding DSP and UDIMM socket pins	123	DQ5
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	124	Vss
DDRDQM0	See data sheet	Connect between corresponding DSP and UDIMM socket pins	125	DM0
	See data sheet	Unused	126	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	127	Vss
DDRD06	See data sheet	Connect between corresponding DSP and UDIMM socket pins	128	DQ6
DDRD07	See data sheet	Connect between corresponding DSP and UDIMM socket pins	129	DQ7
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	130	Vss
DDRD12	See data sheet	Connect between corresponding DSP and UDIMM socket pins	131	DQ12
DDRD13	See data sheet	Connect between corresponding DSP and UDIMM socket pins	132	DQ13
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	133	Vss
DDRDQM1	See data sheet	Connect between corresponding DSP and UDIMM socket pins	134	DM1
		Unused	135	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	136	Vss

Table 70 Non-ECC 4Gb x64 UDIMM to DSP pinout - Back Side (Part 2 of 4)

		BACK SIDE DSP to SOCKET CONNECTIONS		
DSP Name	**DSP Pin**		**UDIMM Pin #**	**UDIMM Pin Name**
DDRD14	See data sheet	Connect between corresponding DSP and UDIMM socket pins	137	DQ14
DDRD15	See data sheet	Connect between corresponding DSP and UDIMM socket pins	138	DQ15
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	139	Vss
DDRD20	See data sheet	Connect between corresponding DSP and UDIMM socket pins	140	DQ20
DDRD21	See data sheet	Connect between corresponding DSP and UDIMM socket pins	141	DQ21
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	142	Vss
DDRDQM2	See data sheet	Connect between corresponding DSP and UDIMM socket pins	143	DM2
		Unused	144	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	145	Vss
DDRD22	See data sheet	Connect between corresponding DSP and UDIMM socket pins	146	DQ22
DDRD23	See data sheet	Connect between corresponding DSP and UDIMM socket pins	147	DQ23
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	148	Vss
DDRD28	See data sheet	Connect between corresponding DSP and UDIMM socket pins	149	DQ28
DDRD29	See data sheet	Connect between corresponding DSP and UDIMM socket pins	150	DQ29
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	151	Vss
DDRDQM3	See data sheet	Connect between corresponding DSP and UDIMM socket pins	152	DM3
	See data sheet	Unused	153	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	154	Vss
DDRD30	See data sheet	Connect between corresponding DSP and UDIMM socket pins	155	DQ30
DDRD31	See data sheet	Connect between corresponding DSP and UDIMM socket pins	156	DQ31
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	157	Vss
DDRCB04	See data sheet	Unused – leave unconnected	158	NC
DDRCB05	See data sheet	Unused – leave unconnected	159	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	160	Vss
DDRDQM8	See data sheet	Unused – leave unconnected	161	NC
		Unused	162	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	163	Vss
DDRCB06	See data sheet	Unused – leave unconnected	164	NC
DDRCB07	See data sheet	Unused – leave unconnected	165	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	166	Vss
		Test Pin - unused	167	NU
$\overline{\text{DDRRESET}}$	See data sheet	Connect between corresponding DSP and UDIMM socket pins	168	RESET#
DDRCKE1	See data sheet	Connect between corresponding DSP and UDIMM socket pins	169	CKE1
DVDD15	See data sheet	Tie to Common DVDD15 Rail	170	Vdd
DDRA15	See data sheet	Connect between corresponding DSP and UDIMM socket pins	171	NF/A15
DDRA14	See data sheet	Connect between corresponding DSP and UDIMM socket pins	172	NF/A14
DVDD15	See data sheet	Tie to Common DVDD15 Rail	173	Vdd
DDRA12	See data sheet	Connect between corresponding DSP and UDIMM socket pins	174	A12
DDRA09	See data sheet	Connect between corresponding DSP and UDIMM socket pins	175	A9
DVDD15	See data sheet	Tie to Common DVDD15 Rail	176	Vdd
DDRA08	See data sheet	Connect between corresponding DSP and UDIMM socket pins	177	A8
DDRA06	See data sheet	Connect between corresponding DSP and UDIMM socket pins	178	A6

Table 70 Non-ECC 4Gb x64 UDIMM to DSP pinout - Back Side (Part 3 of 4)

		BACK SIDE DSP to SOCKET CONNECTIONS		
DSP Name	**DSP Pin**		**UDIMM Pin #**	**UDIMM Pin Name**
DVDD15	See data sheet	Tie to Common DVDD15 Rail	179	Vdd
DDRA03	See data sheet	Connect between corresponding DSP and UDIMM socket pins	180	A3
DDRA01	See data sheet	Connect between corresponding DSP and UDIMM socket pins	181	A1
DVDD15	See data sheet	Tie to Common DVDD15 Rail	182	Vdd
DVDD15	See data sheet	Tie to Common DVDD15 Rail	183	Vdd
DDRCLKOUTP0	See data sheet	Connect between corresponding DSP and UDIMM socket pins	184	CK0
DDRCLKOUTN0	See data sheet	Connect between corresponding DSP and UDIMM socket pins	185	CK0#
DVDD15	See data sheet	Tie to Common DVDD15 Rail	186	Vdd
		Not required, used for temperature alert	187	EVENT#
DDRA00	See data sheet	Connect between corresponding DSP and UDIMM socket pins	188	A0
DVDD15	See data sheet	Tie to Common DVDD15 Rail	189	Vdd
DDRBA1	See data sheet	Connect between corresponding DSP and UDIMM socket pins	190	BA1
DVDD15	See data sheet	Tie to Common DVDD15 Rail	191	Vdd
$\overline{\text{DDRRAS}}$	See data sheet	Connect between corresponding DSP and UDIMM socket pins	192	RAS#
$\overline{\text{DDRCE0}}$	See data sheet	Connect between corresponding DSP and UDIMM socket pins	193	S0#
DVDD15	See data sheet	Tie to Common DVDD15 Rail	194	Vdd
DDRODT0	See data sheet	Connect between corresponding DSP and UDIMM socket pins	195	ODT0
DDRA13	See data sheet	Connect between corresponding DSP and UDIMM socket pins	196	A13
DVDD15	See data sheet	Tie to Common DVDD15 Rail	197	Vdd
		Unused	198	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	199	Vss
DDRD36	See data sheet	Connect between corresponding DSP and UDIMM socket pins	200	DQ36
DDRD37	See data sheet	Connect between corresponding DSP and UDIMM socket pins	201	DQ37
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	202	Vss
DDRDQM4	See data sheet	Connect between corresponding DSP and UDIMM socket pins	203	DM4
		Unused	204	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	205	Vss
DDRD38	See data sheet	Connect between corresponding DSP and UDIMM socket pins	206	DQ38
DDRD39	See data sheet	Connect between corresponding DSP and UDIMM socket pins	207	DQ39
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	208	Vss
DDRD44	See data sheet	Connect between corresponding DSP and UDIMM socket pins	209	DQ44
DDRD45	See data sheet	Connect between corresponding DSP and UDIMM socket pins	210	DQ45
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	211	Vss
DDRDQM5	See data sheet	Connect between corresponding DSP and UDIMM socket pins	212	DM5
	See data sheet	Unused	213	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	214	Vss
DDRD46	See data sheet	Connect between corresponding DSP and UDIMM socket pins	215	DQ46
DDRD47	See data sheet	Connect between corresponding DSP and UDIMM socket pins	216	DQ47
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	217	Vss
DDRD52	See data sheet	Connect between corresponding DSP and UDIMM socket pins	218	DQ52
DDRD53	See data sheet	Connect between corresponding DSP and UDIMM socket pins	219	DQ53
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	220	Vss

Table 70 Non-ECC 4Gb x64 UDIMM to DSP pinout - Back Side (Part 4 of 4)

		BACK SIDE DSP to SOCKET CONNECTIONS		
DSP Name	**DSP Pin**		**UDIMM Pin #**	**UDIMM Pin Name**
DDRDQM6	See data sheet	Connect between corresponding DSP and UDIMM socket pins	221	DM6
		Unused	222	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	223	Vss
DDRD54	See data sheet	Connect between corresponding DSP and UDIMM socket pins	224	DQ54
DDRD55	See data sheet	Connect between corresponding DSP and UDIMM socket pins	225	DQ55
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	226	Vss
DDRD60	See data sheet	Connect between corresponding DSP and UDIMM socket pins	227	DQ60
DDRD61	See data sheet	Connect between corresponding DSP and UDIMM socket pins	228	DQ61
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	229	Vss
DDRDQM7	See data sheet	Connect between corresponding DSP and UDIMM socket pins	230	DM7
		Unused	231	NC
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	232	Vss
DDRD62	See data sheet	Connect between corresponding DSP and UDIMM socket pins	233	DQ62
DDRD63	See data sheet	Connect between corresponding DSP and UDIMM socket pins	234	DQ63
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	235	Vss
		Connect to clean 3.3 V ±1% tolerance	236	Vddspd
		N/C, used for programming udimm thermal sensor	237	SA1
		N/C, used for programming udimm thermal sensor	238	SDA
Vss	See data sheet	Connect to common rail, leads to be short with no voltage sag	239	Vss
		Termination voltage, VDD/2, must track 1.5 V supply	240	Vtt

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265