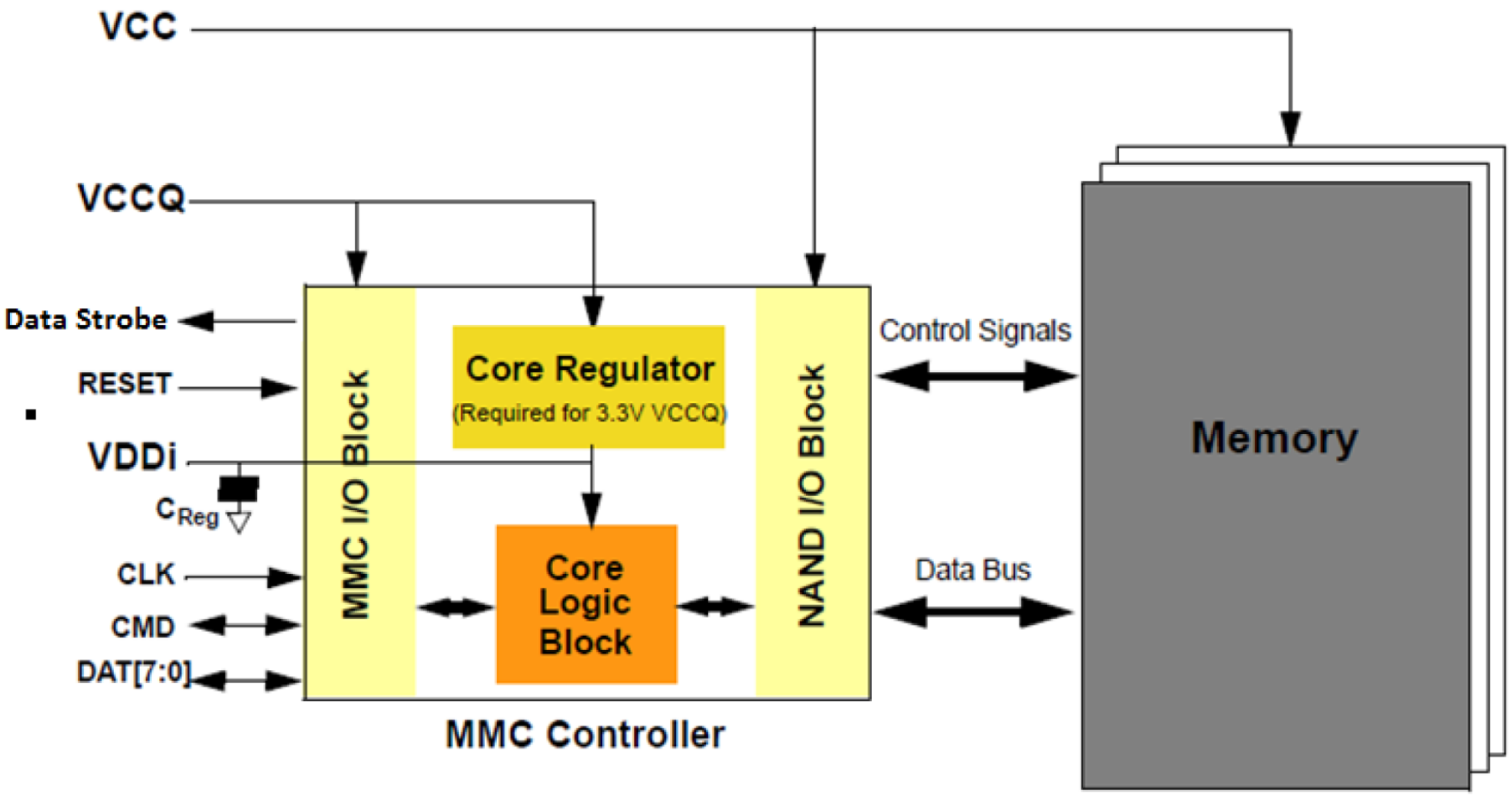
eMMC5.0 vs eMMC5.1

02/26/2020

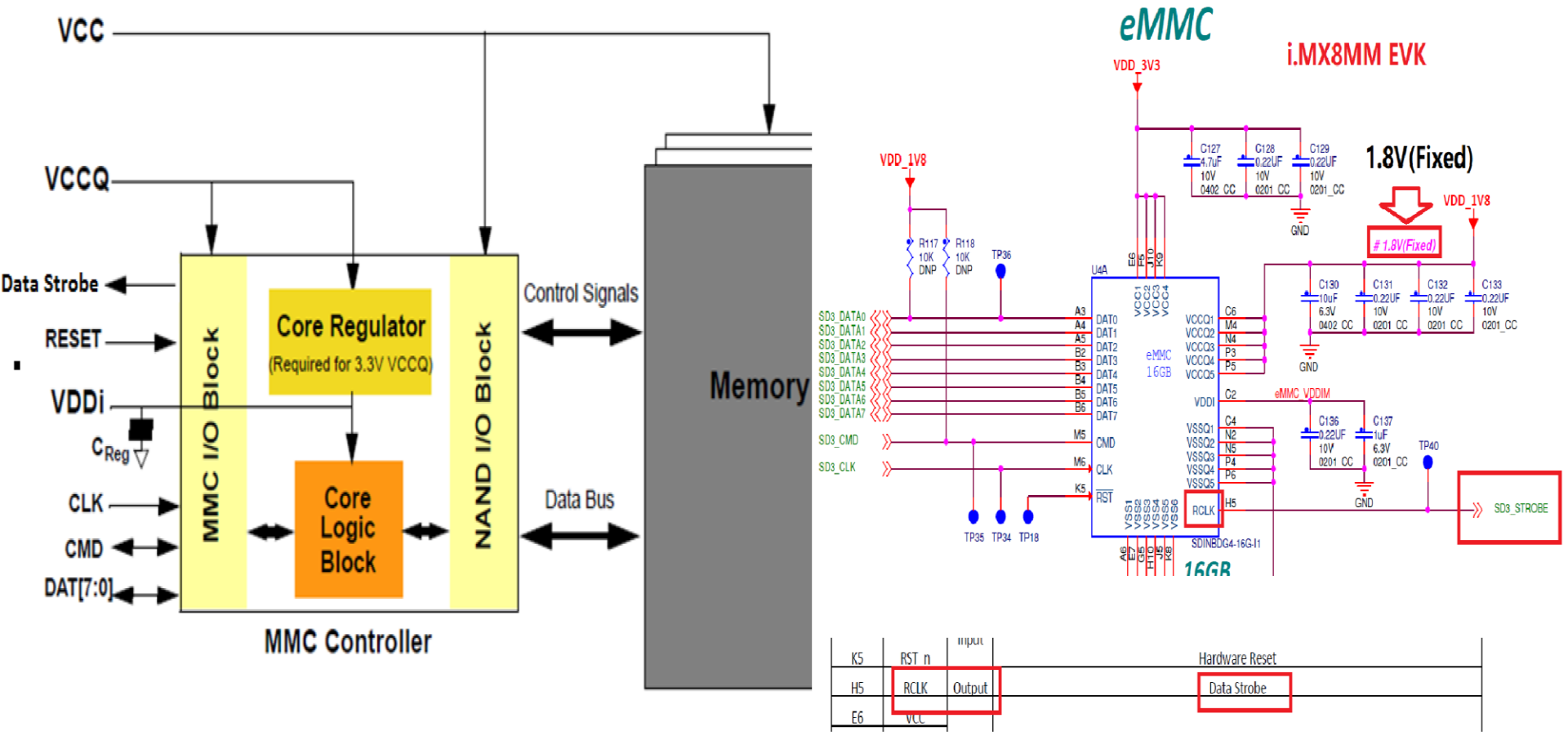
Biyong Sun

Power supply: e • MMC



Note: JESD84-A441, JESD84-B451
JESD84-B50, JESD84-B50-1,JESD84-B51

Power supply: e•MMC to schematic(i.MX8MM EVK)



Note: JESD84-A441, JESD84-B451 JESD84-B50, JESD84-B50-1,JESD84-B51

Most of cases using 1.8v VccQ fixed I/O for eMMC 5.x hardware design

Power supply Voltages

Parameter	Symbol	Min	Max	Unit	Remarks
Supply voltage (NAND)	VCC	2.7	3.6	V	
		1.7	1.95	V	
Supply voltage (I/O)	VCCQ	2.7	3.6	V	
		1.70	1.95	V	
		1.1	1.3	V	
Supply voltage (cache) (e^2•MMC)	D-V_{DD}	1.7	1,9	V	
Supply voltage (cache IO) (e^2•MMC)	D-V_{DDQ}	1.7	1.9	V	
		1.14	1.3	V	
Supply power-up for 3.3V	tPRUH		35	ms	
Supply power-up for 1.8V	tPRUL		25	ms	
Supply power-up for 1.2V	tPRUV		20	ms	

Note: JESD84-A441(No D-Vdd, D-Vddq)

JESD84-B451， JESD84-B50, JESD84-B50-1,JESD84-B51

Most of cases using 1.8v VccQ fixed I/O for eMMC 5.x hardware design

e•MMC voltage combinations

		V_{CCQ}		
		1.1 V-1.3 V	**1.70 V–1.95 V**	**2.7 V–3.6 V**
V_{CC}	**2.7 V–3.6 V**	Valid	Valid	Valid (1)
	1.7 V–1.95 V	Valid	Valid	NOT VALID
NOTE 1 V_{CCQ} (I/O) 3.3 V range is not supported in either HS200 or HS400 devices				

Note: **JESD84-A441, JESD84-B451**

JESD84-B50, JESD84-B50-1(HS200)

JESD84-B51(HS400)

Changes between system specification versions(5.0 vs 5.1)(JESD84-B51)

C.9. Changes from version 5.0 to 5.01

- Added HS400 selection flow diagram
- Clarified clock stopping during read and write operations in HS400 mode
- Editorial Clarifications
- Fixed typos, cross references and formatting
- Generated new figures to improve images quality and correct errors

C.10. Changes from version 5.01 to 5.1

- Added Command Queuing
- Added Enhanced Strobe in HS400 Mode
- Added Cache Barrier
- Added Cache Flushing report
- Added RPMB Throughput Improve. Support write data size 8KB (thirty two 512B frames)
- Added Background Operation Control
- Added Secure Write Protection
- Added Host Controller Interface for Command Queuing as normative reference
- Clarification on HS200/HS400 V_T
- Edit to support v5.1 in EXT_CSD_REV[192]
- Fixed typos, cross references and formatting
- Generated new figures to improve images quality and correct errors

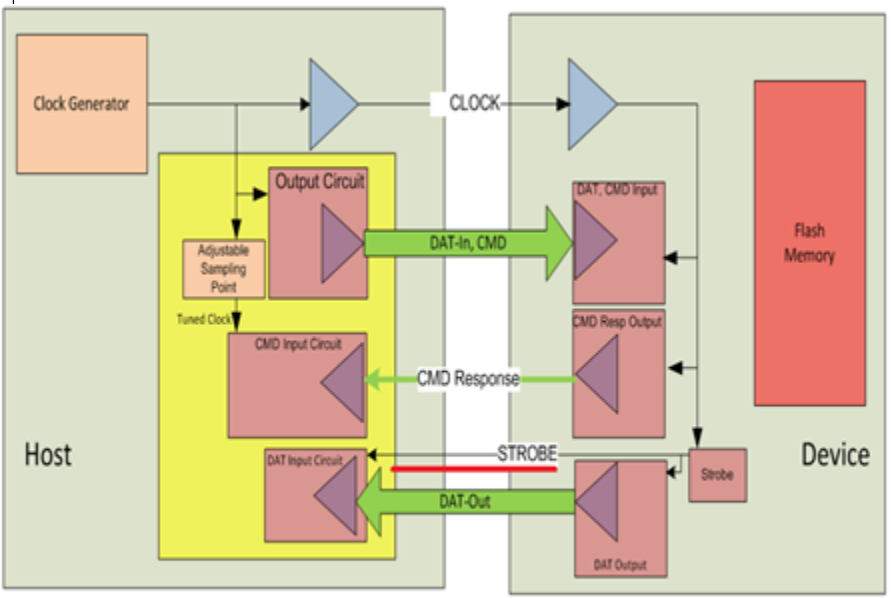
HS400 & HS400ES

JESD84-B50, JESD84-B50-1

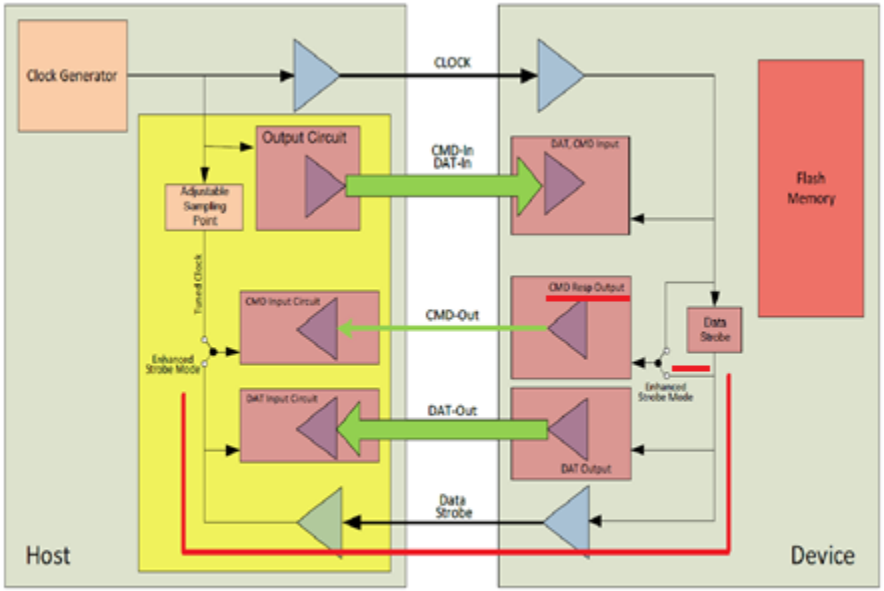
data strobe path in HS400 System Block Diagram

JESD84-B51

data strobe path through CMD Resp Output in HS400 System Block Diagram



JESD84-B50,JESD84-B50-1



JESD84-B51

HS400 & HS400ES(Cont.)

JESD84-B50, JESD84-B50-1

No Enhanced Strobe without the need for tuning procedure.

JESD84-B51

defines the Enhanced Strobe without the need for tuning procedure.

“HS400” timing mode selection(HS200 tuning)

The valid IO Voltage for HS400 is 1.8 V or 1.2 V for VCCQ.

The bus width is set to only DDR 8bit in HS400 mode.

HS400 supports the same commands as DDR52.

After the host initializes the device, host check whether the device supports the HS400 mode by reading the DEVICE_TYPE field in the Extended CSD register. Then it enables the HS400 mode in the device before changing the clock frequency to a frequency higher than 52 MHz.

After power-on or software reset (CMD0), the interface timing of the device is set as the default “Backward Compatible Timing”.

In order to switch to HS400 mode, host should perform the following steps:

1) Initialize device with “Backward Compatible Timings”,

2) Select the device with CMD7,

3) Read the DEVICE_TYPE [196] field of the Extended CSD register to validate whether the device supports HS400,

4) Read the DRIVER_STRENGTH [197] field of the Extended CSD register to find the supported device Driver Strengths,

NOTE This step may be skipped if changes of driver strength is not needed.

5) Set the “Selected Driver Strength” parameter in the HS_TIMING [185] field of the Extended CSD register to the appropriate driver strength for HS400 operation and set the “Timing Interface” parameter to 0x2 to switch to HS200 mode,

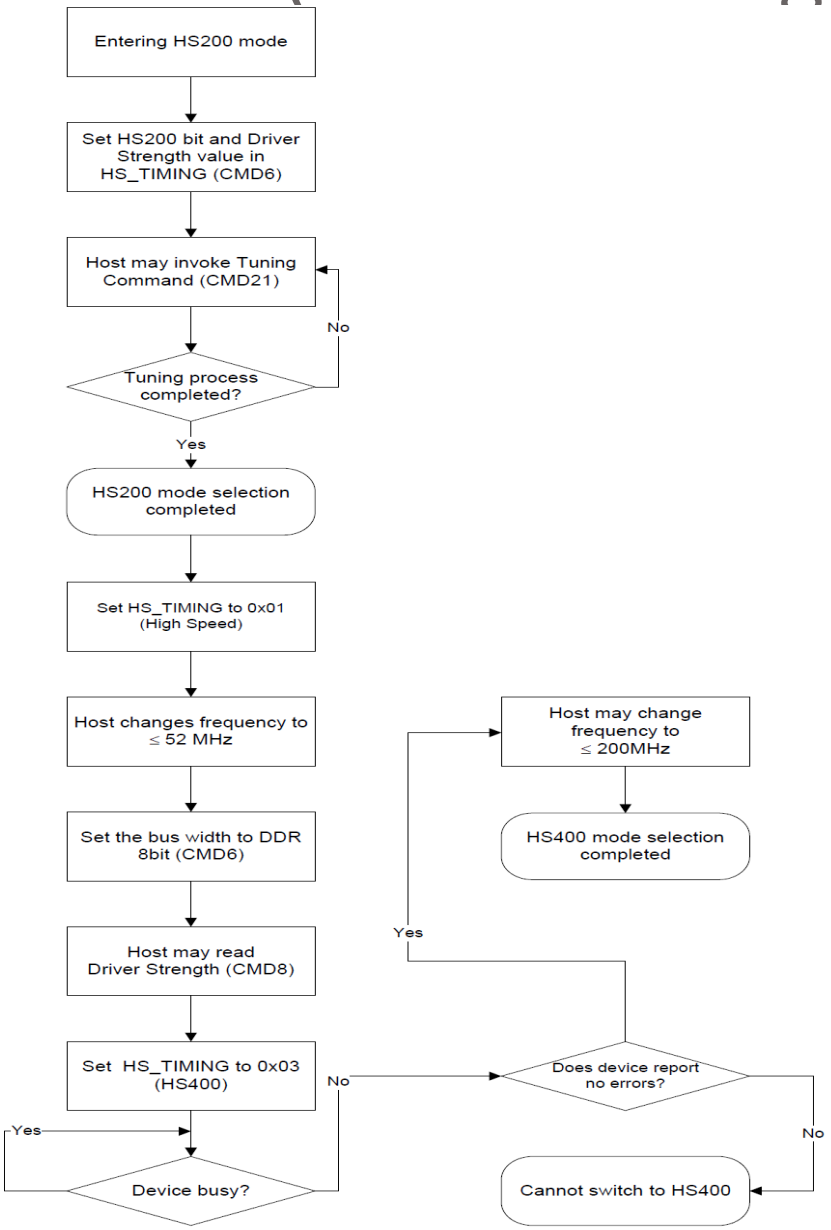
6) Perform the Tuning Process at the HS400 target operating frequency,

NOTE Tuning process in HS200 mode is required to synchronize the command response on the CMD line to CLK for HS400 operation.

7) Set the “Timing Interface” parameter in the HS_TIMING [185] field of the Extended CSD register to 0x1 to switch to High Speed mode and then set the clock frequency to a value not greater than 52 MHz,

8) Set BUS_WIDTH[183] to 0x06 to select the dual data rate x8 bus mode,

9) Set the “Timing Interface” parameter in the HS_TIMING [185] field of the Extended CSD register to 0x3 to switch to HS400 mode.

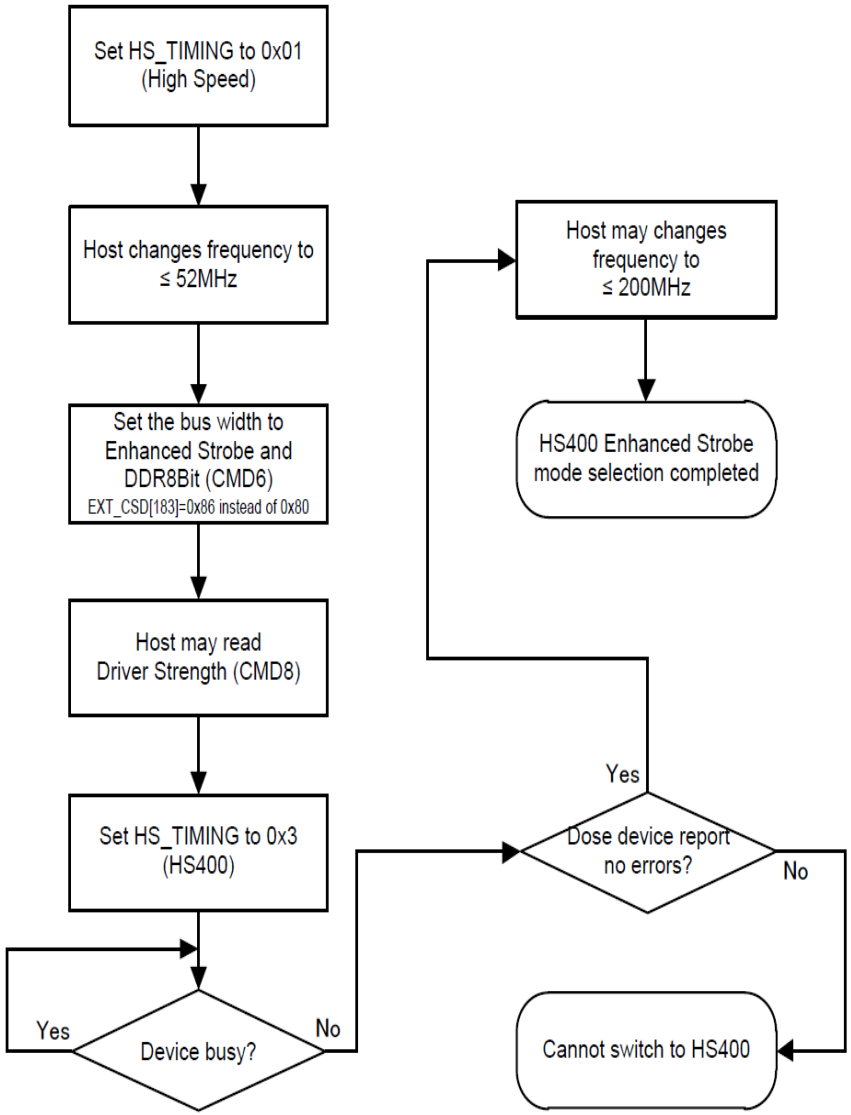


JESD84-B50, JESD84-B50-1, JESD84-B51

“HS400” timing mode selection(HS400ES Enhanced Strobe)

This selection flow describes how to initialize the *e*•MMC device in HS400 mode while enabling Enhanced Strobe without the need for tuning procedure.
After the host initializes the device, host check whether the device supports the HS400 mode and Enhanced Strobe by reading the DEVICE_TYPE and STROBE_SUPPORT fields in the Extended CSD register.
After power-on or software reset (CMD0), the interface timing of the device is set as the default “Backward Compatible Timing”.
In order to switch to HS400 mode with Enhanced Strobe, host should perform the following steps:
1) Initialize device with “Backward Compatible Timings”,
2) Select the device with CMD7,
3) Read the DEVICE_TYPE [196] field of the Extended CSD register to validate whether the device supports HS400,
4) Read the STROBE_SUPPORT[184] field of the Extended CSD register to validate whether the device supports Enhanced Strobe,
5) Set the “Timing Interface” parameter in the HS_TIMING [185] field of the Extended CSD register to 0x1 to switch to High Speed mode and then set the clock frequency to a value not greater than 52 MHz,
6) Set BUS_WIDTH[183] to 0x86 to select the dual data rate x8 bus mode and enable Enhanced Strobe (this will be active only after HS400 mode is selected),
7) Read the DRIVER_STRENGTH [197] field of the Extended CSD register to find the supported device Driver Strengths, NOTE This step may be skipped if changes of driver strength is not needed, if needed host may change the device Driver Strength.
8) Set the “Timing Interface” parameter in the HS_TIMING [185] field of the Extended CSD register to 0x3 to switch to HS400 mode,
9) Host may set the clock frequency to a value not greater than 200 MHz".

JESD84-B51



HS400ES timing mode selection **STROBE_SUPPORT** in Linux Source Code

In order to switch to HS400 mode with Enhanced Strobe, host should perform the following steps:

1) Initialize device with “Backward Compatible Timings”,
2) Select the device with CMD7,
3) Read the DEVICE_TYPE [196] field of the Extended CSD register to validate whether the device supports HS400,
4) **Read the STROBE_SUPPORT[184] field of the Extended CSD register to validate whether the device supports Enhanced Strobe,**
5) Set the “Timing Interface” parameter in the HS_TIMING [185] field of the Extended CSD register to 0x1 to switch to High Speed mode and then set the clock frequency to a value not greater than 52 MHz,
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8) Set the “Timing Interface” parameter in the HS_TIMING [185] field of the Extended CSD register to 0x3 to switch to HS400 mode,
9) Host may set the clock frequency to a value not greater than 200 MHz".

```
linux/include/linux/mmc/mmc.h
#define EXT_CSD_STROBE_SUPPORT          184     /* RO */

linux/drivers/mmc/core/mmc.c
static int mmc_decode_ext_csd(struct mmc_card *card, u8 *ext_csd)

card->ext_csd.strobe_support = ext_csd[EXT_CSD_STROBE_SUPPORT];

static void mmc_select_card_type(struct mmc_card *card)

        if ((caps2 & MMC_CAP2_HS400_ES) &&
            card->ext_csd.strobe_support &&
            (avail_type & EXT_CSD_CARD_TYPE_HS400))
                avail_type |= EXT_CSD_CARD_TYPE_HS400ES;
```

Table 93 — Extended CSD

Name	Field	Size (Bytes)	Cell Type	CSD-slice
Properties Segment				
Reserved[1]		1	TBD	[186]
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]
Strobe Support	STROBE_SUPPORT	1	R	[184]
Bus width mode	BUS_WIDTH	1	W/E_P	[183]
Reserved[1]		1	TBD	[182]
Erased memory content	ERASED_MEM_CONT	1	R	[181]

HS400ES timing mode selection **STROBE_SUPPORT** in Linux Source Code

In order to switch to HS400 mode with Enhanced Strobe, host should perform the following steps:

1) Initialize device with “Backward Compatible Timings”,
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5) Set the “Timing Interface” parameter in the HS_TIMING [185] field of the Extended CSD register to 0x1 to switch to High Speed mode and then set the clock frequency to a value not greater than 52 MHz,
6) Set BUS_WIDTH[183] to 0x86 to select the dual data rate x8 bus mode and enable Enhanced Strobe (this will be active only after HS400 mode is selected),
7) Read the DRIVER_STRENGTH [197] field of the Extended CSD register to find the supported device Driver Strengths, NOTE This step may be skipped if changes of driver strength is not needed, if needed host may change the device Driver Strength.
8) Set the “Timing Interface” parameter in the HS_TIMING [185] field of the Extended CSD register to 0x3 to switch to HS400 mode,
9) Host may set the clock frequency to a value not greater than 200 MHz".

```
linux/include/linux/mmc/mmc.h
#define EXT_CSD_STROBE_SUPPORT          184     /* RO */

linux/drivers/mmc/core/mmc.c
static int mmc_decode_ext_csd(struct mmc_card *card, u8 *ext_csd)

card->ext_csd.strobe_support = ext_csd[EXT_CSD_STROBE_SUPPORT];

static void mmc_select_card_type(struct mmc_card *card)

        if ((caps2 & MMC_CAP2_HS400_ES) &&
            card->ext_csd.strobe_support &&
            (avail_type & EXT_CSD_CARD_TYPE_HS400))
                avail_type |= EXT_CSD_CARD_TYPE_HS400ES;
```

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Properties Segment				
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Strobe Support	STROBE_SUPPORT	1	R	[184]
Bus width mode	BUS_WIDTH	1	W/E_P	[183]
Reserved[1]		1	TBD	[182]
Erased memory content	ERASED_MEM_CONT	1	R	[181]