256K (32K x 8) Static RAM

Features

- **High speed: 55 ns and 70 ns**
- **Voltage range: 4.5V–5.5V operation**
- **Low active power (70 ns, LL version)**
  - **275 mW (max.)**
- **Low standby power (70 ns, LL version)**
  - **28 μW (max.)**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Package available in a standard 450-mil-wide (300-mil body width) 28-lead narrow SOIC, 28-lead TSOP-1, 28-lead reverse TSOP-1, and 600-mil 28-lead PDIP packages**

Functional Description[1]

The CY62256 is a high-performance CMOS static RAM organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 99.9% when deselected.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.
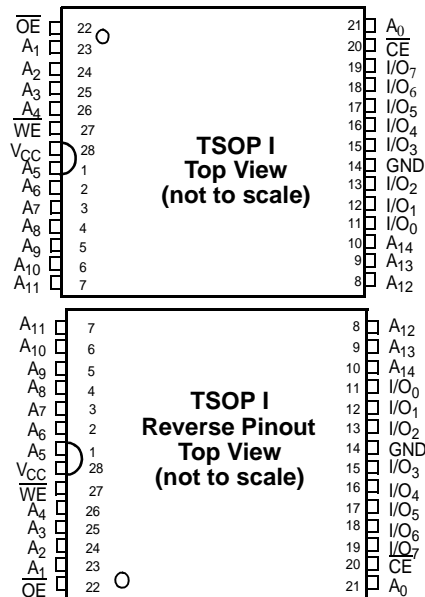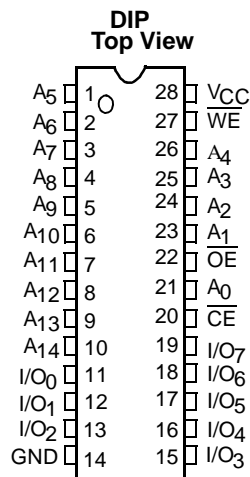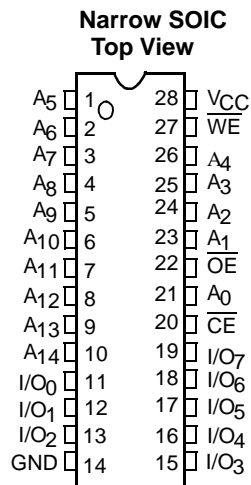
Logic Block Diagram
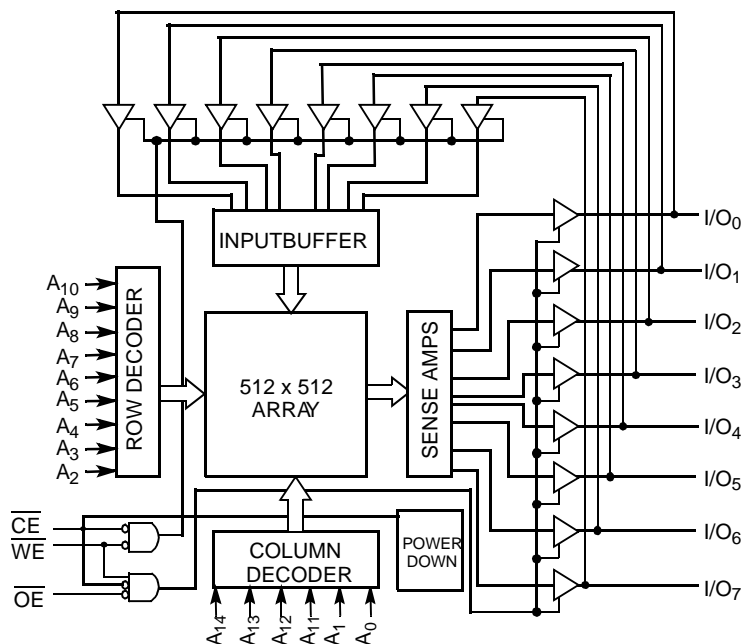
Note:
1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on http://www.cypress.com.

Pin Configurations

Narrow SOIC Top View

A_5	1	28	V_{CC}
A_6	2	27	$\overline{WE}$
A_7	3	26	A_4
A_8	4	25	A_3
A_9	5	24	A_2
A_{10}	6	23	A_1
A_{11}	7	22	$\overline{OE}$
A_{12}	8	21	A_0
A_{13}	9	20	$\overline{CE}$
A_{14}	10	19	I/O_7
I/O_0	11	18	I/O_6
I/O_1	12	17	I/O_5
I/O_2	13	16	I/O_4
GND	14	15	I/O_3

DIP Top View

A_5	1	28	V_{CC}
A_6	2	27	$\overline{WE}$
A_7	3	26	A_4
A_8	4	25	A_3
A_9	5	24	A_2
A_{10}	6	23	A_1
A_{11}	7	22	$\overline{OE}$
A_{12}	8	21	A_0
A_{13}	9	20	$\overline{CE}$
A_{14}	10	19	I/O_7
I/O_0	11	18	I/O_6
I/O_1	12	17	I/O_5
I/O_2	13	16	I/O_4
GND	14	15	I/O_3

TSOP I Top View (not to scale)

$\overline{OE}$	22	21	A_0
A_1	23	20	$\overline{CE}$
A_2	24	19	I/O_7
A_3	25	18	I/O_6
A_4	26	17	I/O_5
$\overline{WE}$	27	16	I/O_4
V_{CC}	28	15	I/O_3
A_5	1	14	GND
A_6	2	13	I/O_2
A_7	3	12	I/O_1
A_8	4	11	I/O_0
A_9	5	10	A_{14}
A_{10}	6	9	A_{13}
A_{11}	7	8	A_{12}

TSOP I Reverse Pinout Top View (not to scale)

A_{11}	7	8	A_{12}
A_{10}	6	9	A_{13}
A_9	5	10	A_{14}
A_8	4	11	I/O_0
A_7	3	12	I/O_1
A_6	2	13	I/O_2
A_5	1	14	GND
V_{CC}	28	15	I/O_3
$\overline{WE}$	27	16	I/O_4
A_4	26	17	I/O_5
A_3	25	18	I/O_6
A_2	24	19	I/O_7
A_1	23	20	$\overline{CE}$
$\overline{OE}$	22	21	A_0

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied... 0°C to +70°C

Supply Voltage to Ground Potential
(Pin 28 to Pin 14) .... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High-Z State[2] .... −0.5V to V_{CC} + 0.5V

DC Input Voltage[2] .... −0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)............................ 20 mA

Static Discharge Voltage... > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current.. > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62256–55			CY62256–70			Unit
				Min.	Typ.[3]	Max.	Min.	Typ.[3]	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −1.0 mA		2.4			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA				0.4			0.4	V
V_{IH}	Input HIGH Voltage			2.2		V_{CC} +0.5V	2.2		V_{CC} +0.5V	V
V_{IL}	Input LOW Voltage			−0.5		0.8	−0.5		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−0.5		+0.5	−0.5		+0.5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−0.5		+0.5	−0.5		+0.5	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$			28	55		28	55	mA
			L		25	50		25	50	mA
			LL		25	50		25	50	mA
I_{SB1}	Automatic $\overline{CE}$ Power-down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			0.5	2		0.5	2	mA
			L		0.4	0.6		0.4	0.6	mA
			LL		0.3	0.5		0.3	0.5	mA

Notes:
2. V_{IL} (min.) = −2.0V for pulse durations of less than 20 ns.
3. Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions (T_A = 25°C, V_{CC}). Parameters are guaranteed by design and characterization, and not 100% tested.

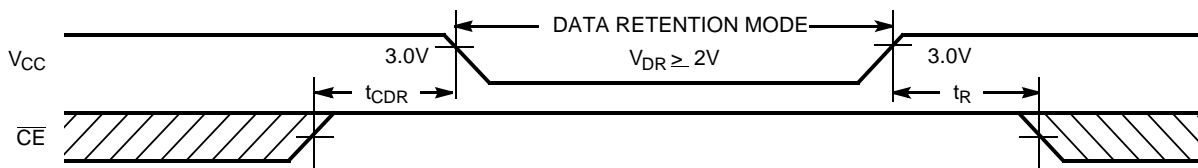**Electrical Characteristics** Over the Operating Range (continued)

Parameter	Description	Test Conditions		CY62256−55			CY62256−70			Unit
				Min.	Typ.[3]	Max.	Min.	Typ.[3]	Max.	
I_{SB2}	Automatic CE Power-down Current— CMOS Inputs	Max. V_{CC}, $\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, f = 0			1	5		1	5	mA
			L		2	50		2	50	µA
			LL		0.1	5		0.1	5	µA
		Indust'l Temp Range	LL		0.1	10		0.1	10	µA

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = 5.0V$	6	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms
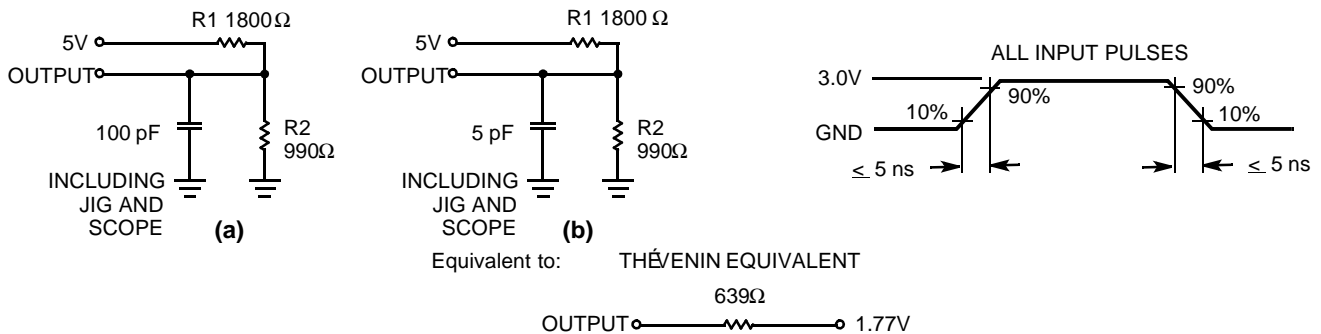
Data Retention Characteristics

Parameter	Description		Conditions[5]	Min.	Typ.[3]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0			V
I_{CCDR}	Data Retention Current	L	$V_{CC} = 3.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$		2	50	µA
		LL			0.1	5	µA
		LL Ind'l			0.1	10	µA
t_{CDR}[4]	Chip Deselect to Data Retention Time			0			ns
t_R[4]	Operation Recovery Time			t_{RC}			ns

## Data Retention Waveform

Notes:
4. Tested initially and after any design or process changes that may affect these parameters.
5. No input may exceed $V_{CC} + 0.5V$.

Switching Characteristics Over the Operating Range[6]

| Parameter	Description	CY62256−55 Min.	CY62256−55 Max.	CY62256−70 Min.	CY62256−70 Max.	Unit
Read Cycle						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[7]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[7, 8]		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[7]	5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[7, 8]		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-down		55		70	ns
Write Cycle[9, 10]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	45		60		ns
t_{AW}	Address Set-up to Write End	45		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	40		50		ns
t_{SD}	Data Set-up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[7, 8]		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[7]	5		5		ns

Switching Waveforms

Read Cycle No. 1[11, 12]
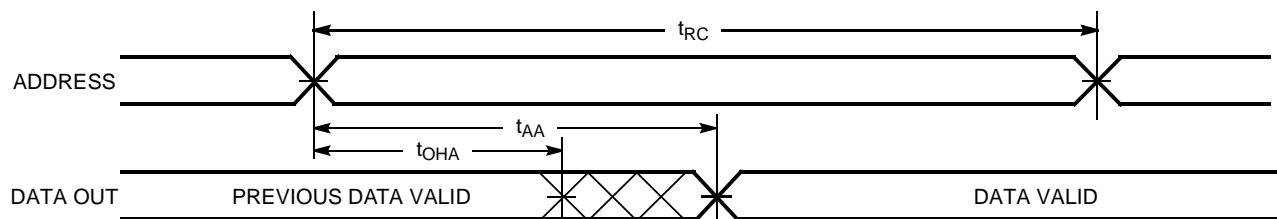
Notes:
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a Write and either signal can terminate a Write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the Write.
10. The minimum Write cycle time for Write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. $\overline{WE}$ is HIGH for Read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 [12, 13]
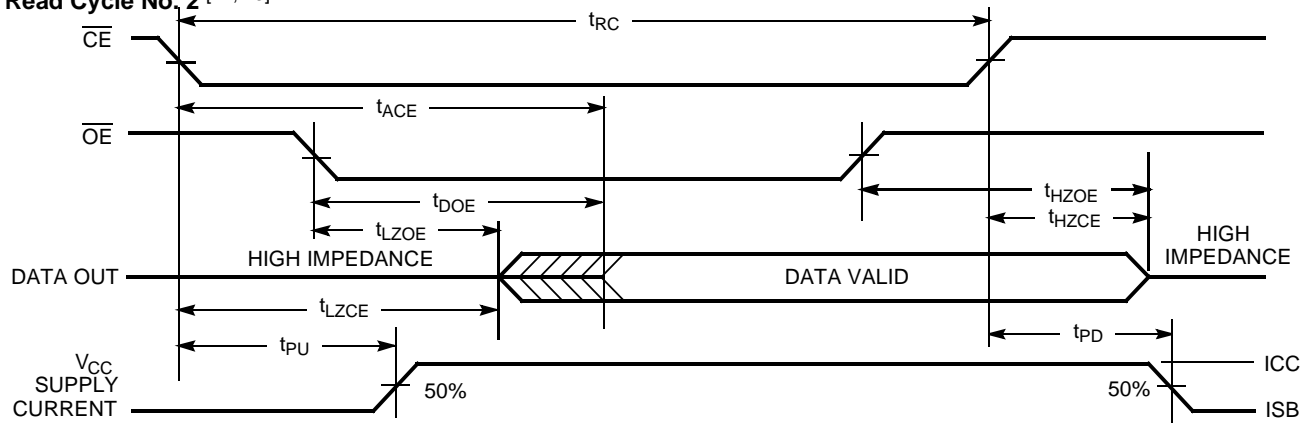
Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled) [9, 14, 15]
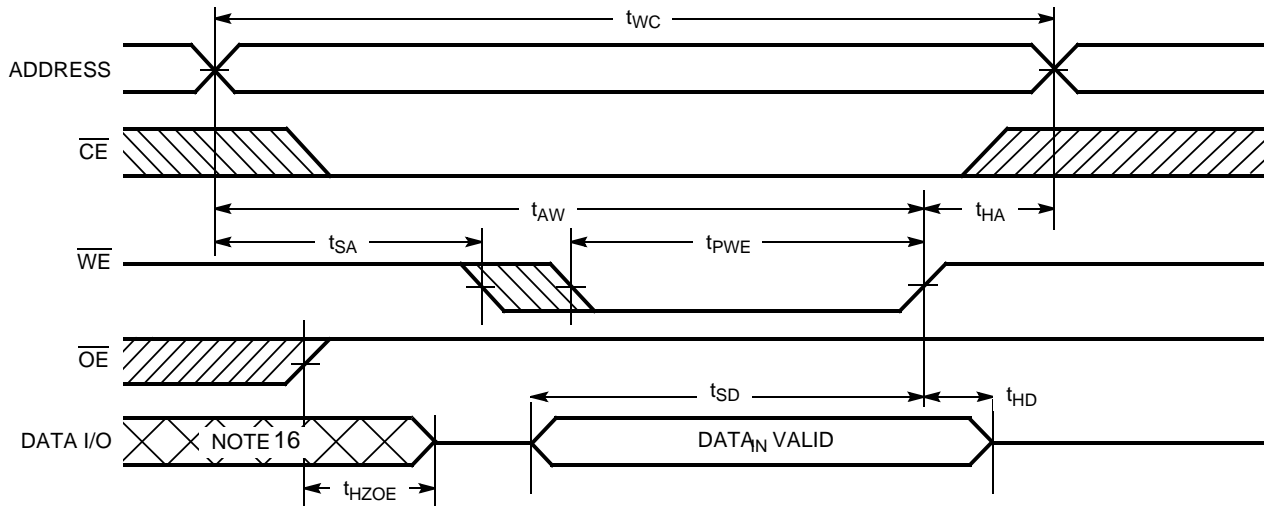
Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) [9, 14, 15]
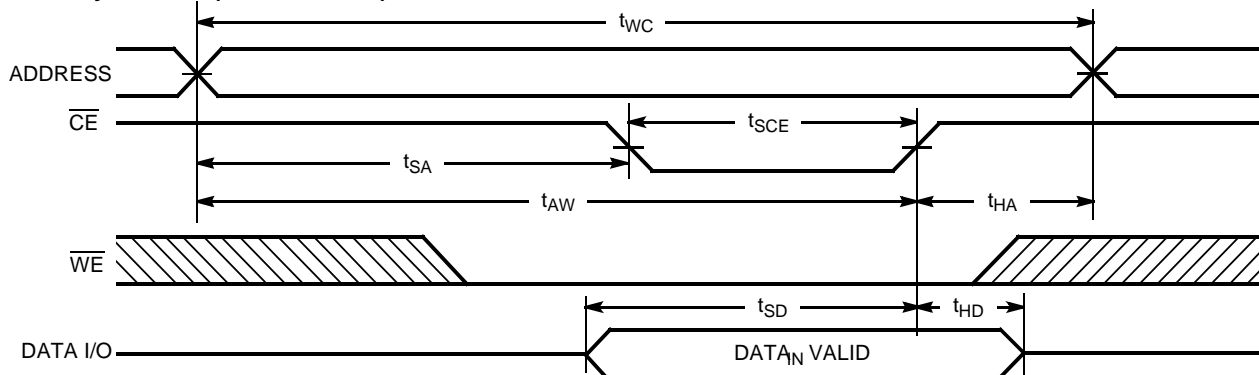
Notes:
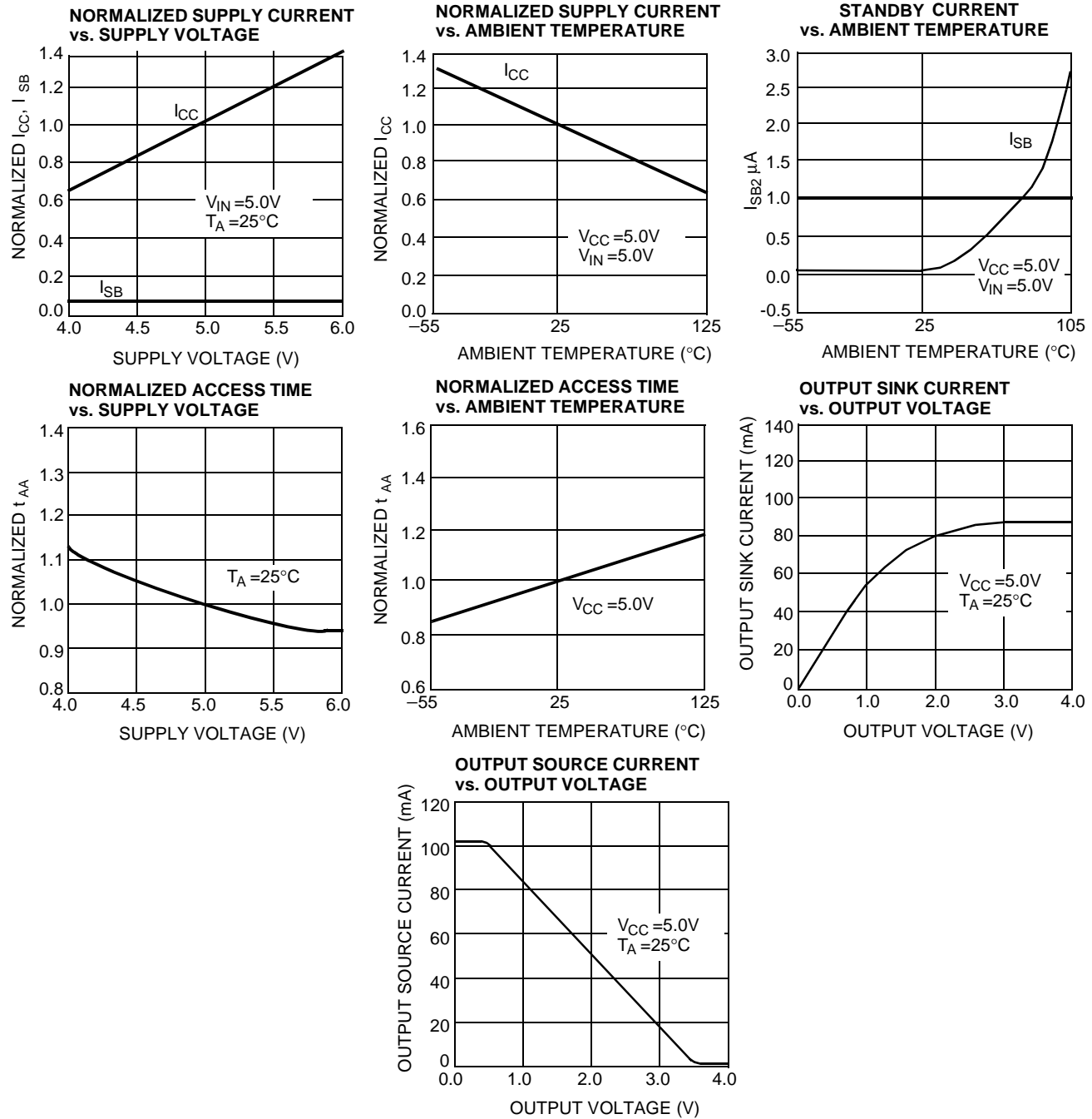13. Address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.
14. Data I/O is high impedance if $\overline{\text{OE}} = V_{IH}$.
15. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.
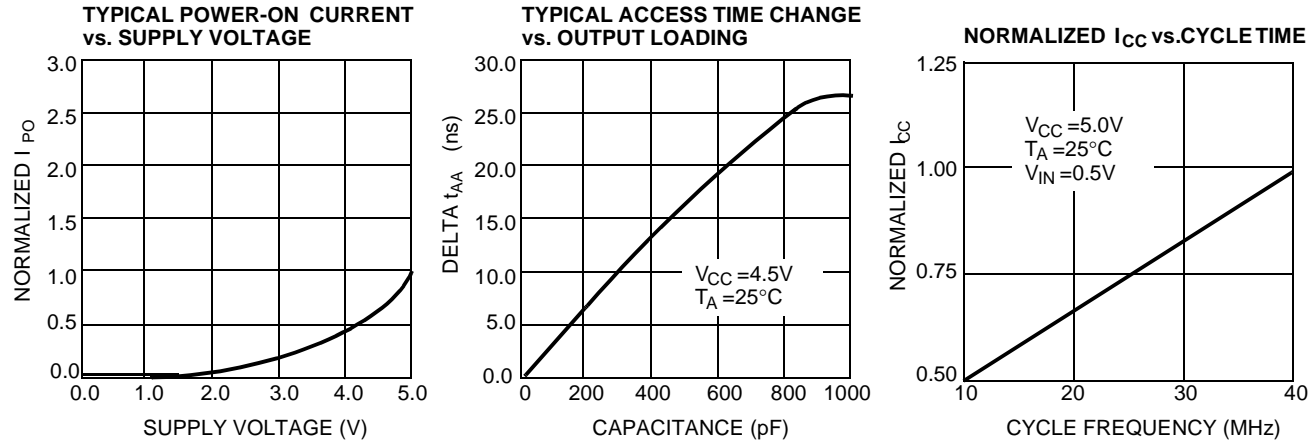
Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [10, 15]
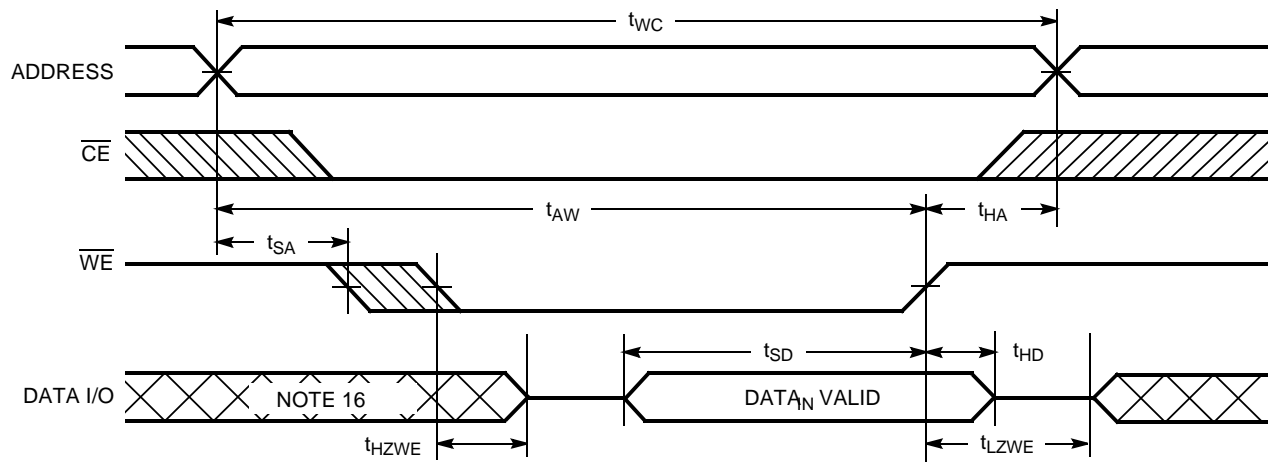
Note:
16. During this period, the I/Os are in output state and input signals should not be applied.

Typical DC and AC Characteristics

NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

$V_{IN} = 5.0V$
$T_A = 25°C$

NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE

$V_{CC} = 5.0V$
$V_{IN} = 5.0V$

STANDBY CURRENT vs. AMBIENT TEMPERATURE

$V_{CC} = 5.0V$
$V_{IN} = 5.0V$

NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

$T_A = 25°C$

NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

$V_{CC} = 5.0V$

OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

$V_{CC} = 5.0V$
$T_A = 25°C$

OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

$V_{CC} = 5.0V$
$T_A = 25°C$

Typical DC and AC Characteristics (continued)

TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE

TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING

NORMALIZED I_{CC} vs. CYCLE TIME

Truth Table

CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High-Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62256LL–55SNI	SN28	28-lead (300-Mil Narrow Body) Narrow SOIC	Industrial
	CY62256LL–55ZI	Z28	28-lead Thin Small Outline Package	
70	CY62256–70SNC	SN28	28-lead (300-Mil Narrow Body) Narrow SOIC	Commercial
	CY62256L–70SNC			
	CY62256LL–70SNC			
	CY62256L–70SNI			Industrial
	CY62256LL–70SNI			
	CY62256LL–70ZC	Z28	28-lead Thin Small Outline Package	Commercial
	CY62256LL–70ZI	Z28		Industrial
	CY62256–70PC	P15	28-lead (600-Mil) Molded DIP	Commercial
	CY62256L–70PC	P15		
	CY62256LL–70PC	P15		
	CY62256LL–70ZRI	ZR28	28-lead Reverse Thin Small Outline Package	Industrial

Package Diagrams

28-lead (600-mil) Molded DIP P15
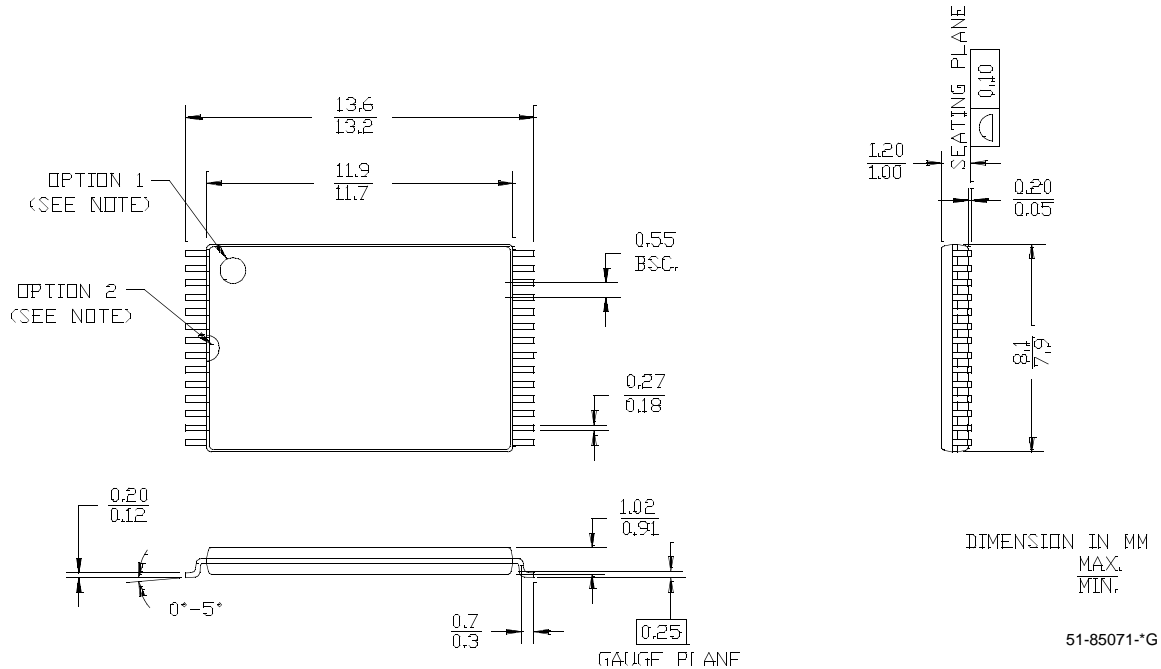

DIMENSIONS IN INCHES MIN.
MAX.

51-85017-A
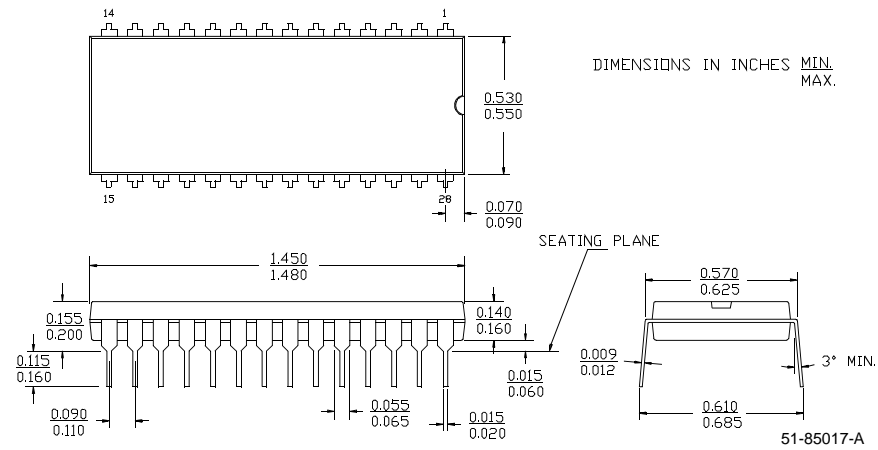
**28-lead (300-mil) SNC (Narrow Body) SN28**

51-85092-*B
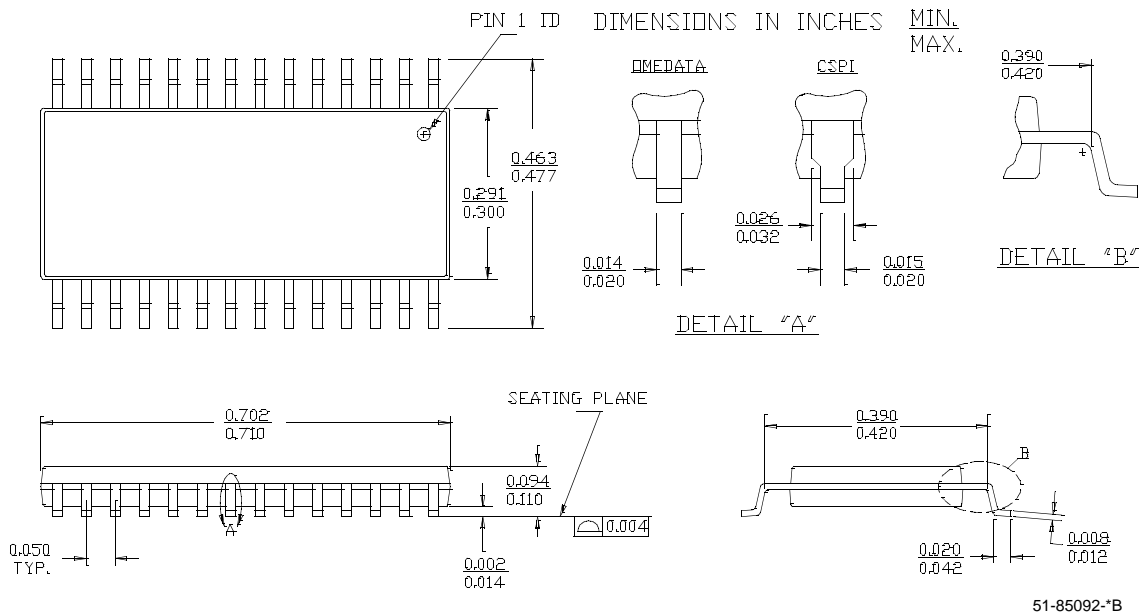
Package Diagrams (continued)

28-lead Thin Small Outline Package Type 1 (8 x 13.4 mm) Z28

NOTE: ORIENTATION I.D MAY BE LOCATED EITHER
AS SHOWN IN OPTION 1 OR OPTION 2

DIMENSION IN MM
MAX.
MIN.

51-85071-*G

28-lead Reverse Type 1 Thin Small Outline Package (8 x 13.4 mm) ZR28

NOTE: ORIENTATION I.D MAY BE LOCATED EITHER
AS SHOWN IN OPTION 1 OR OPTION 2

DIMENSION IN MM
MAX.
MIN.

51-85074-*F
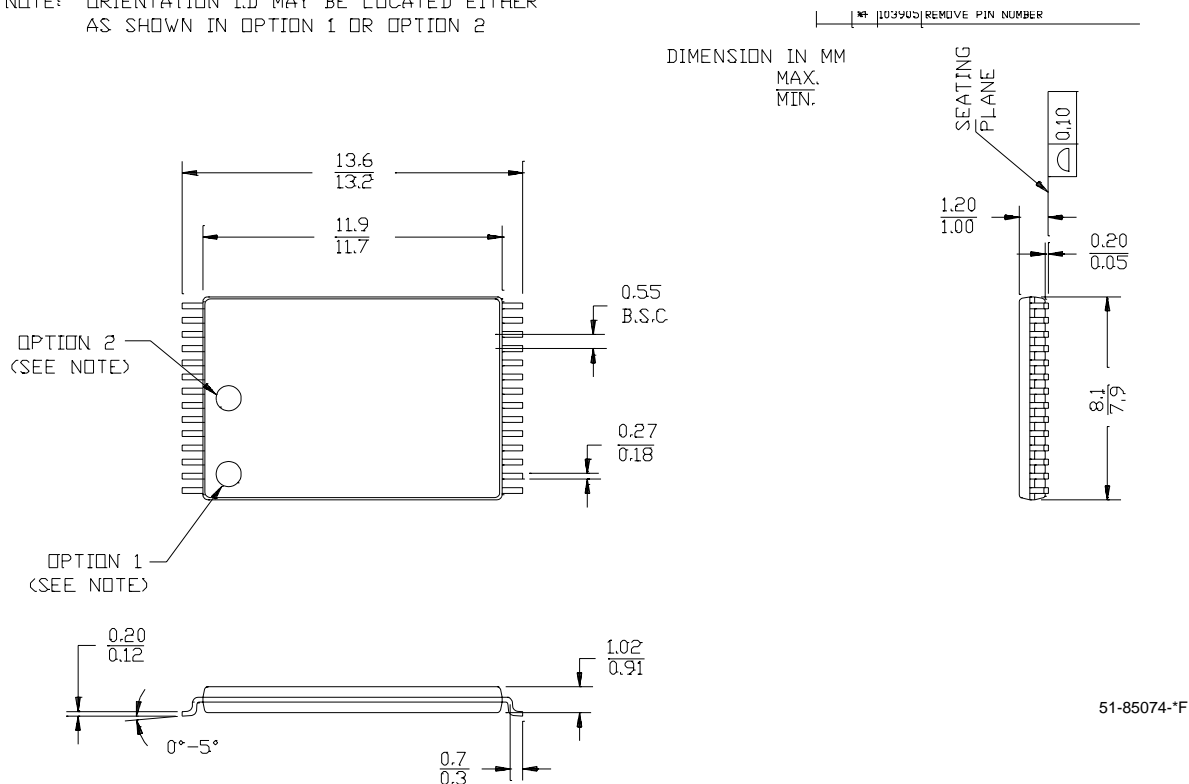
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Document Title: CY62256 256K (32K x 8) Static RAM
Document Number: 38-05248

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	113454	03/06/02	MGN	Change from Spec number: 38-00455 to 38-05248 Remove obsolete parts from ordering info, standardize format
*A	115227	05/23/02	GBI	Changed SN Package Diagram
*B	116506	09/04/02	GBI	Added footnote 1. Corrected package description in Ordering Information table