

Open-Source EDA and Benchmarking Summit

DAC-2022 Birds-of-a-Feather Meeting
Tuesday, July 12, 2022 7:00pm

Organizers: Andrew Kahng and Tom Spyrou

<https://open-source-eda-birds-of-a-feather.github.io/>

About This Meeting

- Third in a series of DAC Birds-of-a-Feather meetings: 2018, 2019 ... **2022**
- **See:** <https://open-source-eda-birds-of-a-feather.github.io/>
- **Informal meeting point to share ideas and latest news**
- **Topics:**
 - **Ecosystem of open-source EDA tools**
 - **Use of relevant and principled benchmarking methodologies**
 - **Overarching goal: clarify and accelerate the leading edge of EDA research**
- **Today:**
 - **Current landscape and key updates**
 - **Goals for the community**
 - **Potential next steps / action items**

Planning Form - 48 responses, thank you !

Questions

Responses

46

Settings

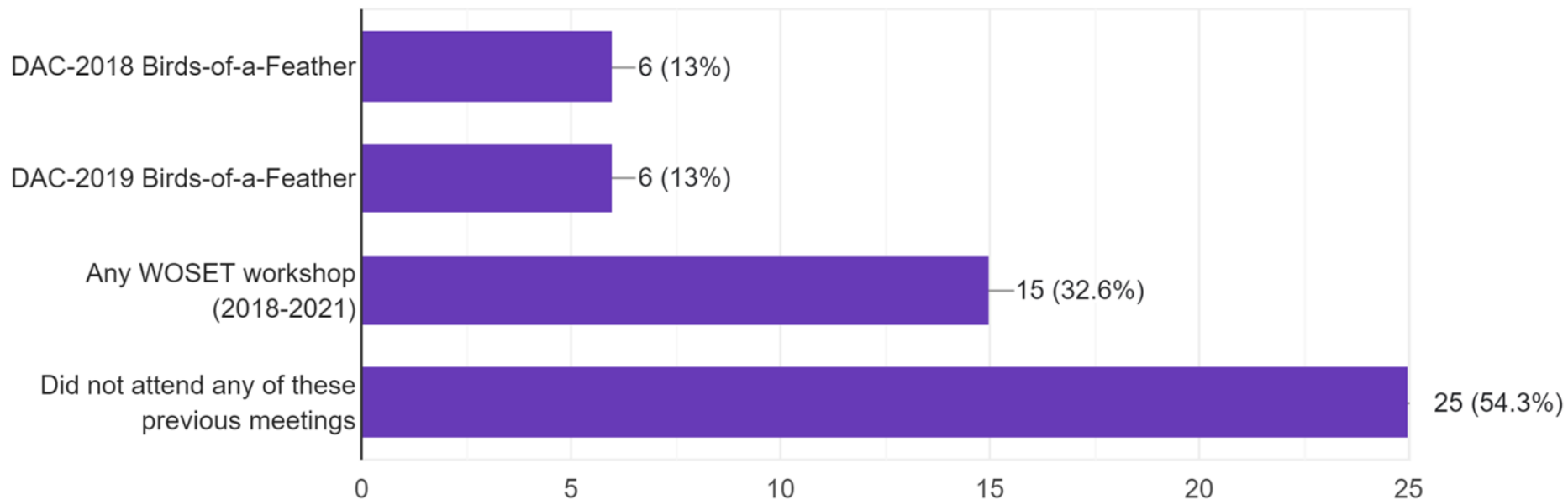
DAC-2022 Birds-of-a-Feather: Open-Source EDA and Benchmarking Summit

The purpose of this form is to gauge interest in a Tuesday evening (July 12, 7:00pm - 10:00pm -- Room 3000 in Moscone West) discussion of open-source EDA (tools, flows, gaps ...) and benchmarking (data/benchmarks, benchmarking methodology)

This meeting follows on to the DAC 2018-2019 Open-Source Academic EDA Software meetings, and the WOSET 2018-2021 workshops. It is an informal meeting point for anyone interested in meeting up and sharing ideas or latest news on: (1) the ecosystem of open-source EDA tools, and/or (2) the use of relevant and principled benchmarking methodologies to clarify and advance the leading edge of EDA research. Goals for the community, along with current landscape, key updates, and potential next steps / actions for the worldwide academic/CAD community are topics for discussion. Potential contributors, developers, advisors, users ... Everyone is WELCOME !!! (Please send email to abk@eng.ucsd.edu with any questions.)

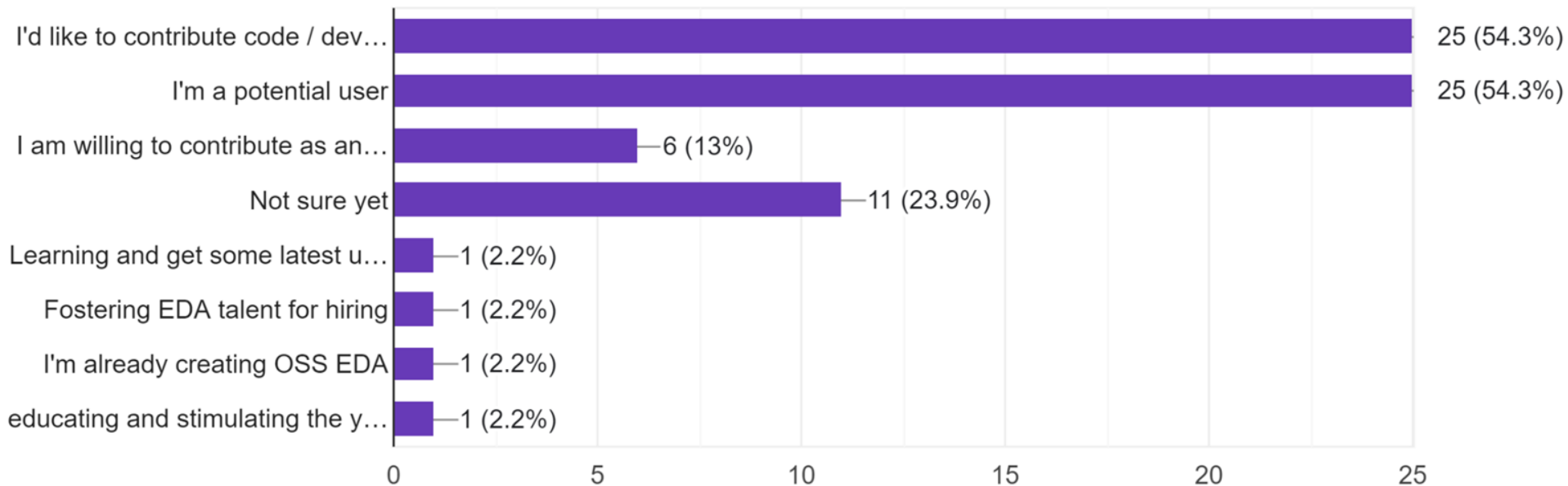
Which of these previous meetings did you attend, if any?

46 responses



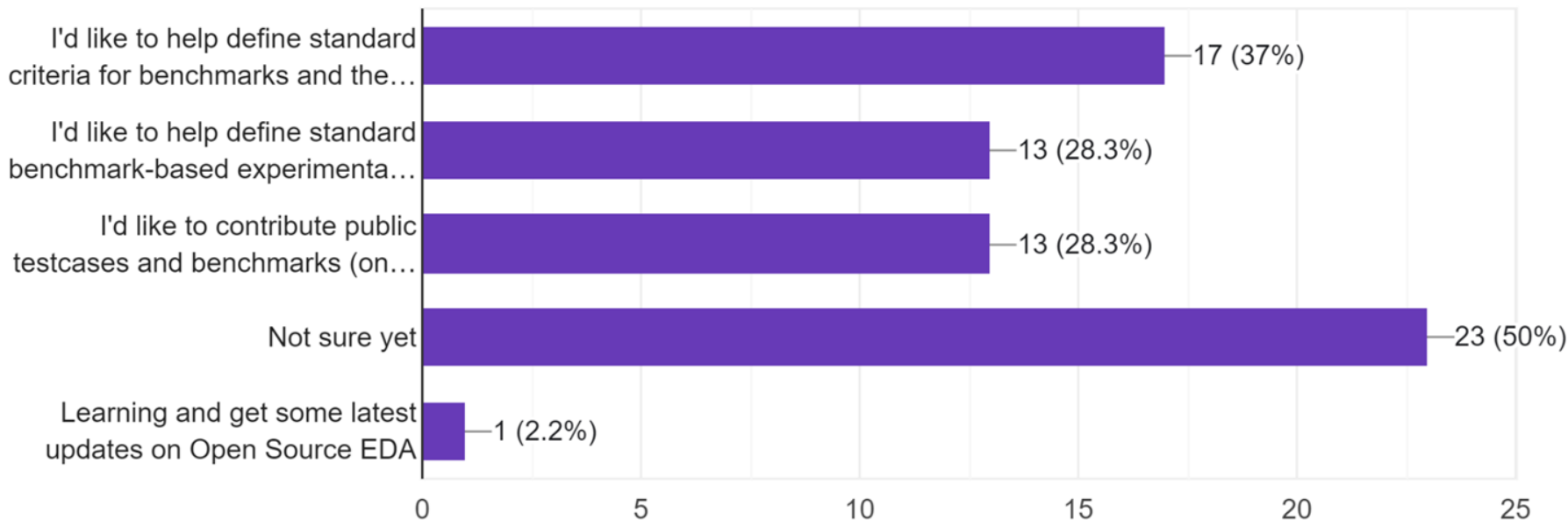
What is your interest in open-source EDA software?

46 responses



What is your interest in benchmarking of (academic) EDA?

46 responses



What would you most like to see discussed at the meeting?

Open-source EDA

- **Current** development of open-source EDA tools
- State of open source tools, and priorities/initiatives being planned.
- The **path forward** for open source community
- (1) Will open source EDA develop into an **ecosystem** that depends not just on volunteers at universities but where also commercial companies get established, providing e.g. support / tool certification for certain applications etc.? (2) Perspectives on open source **IP libraries** (e.g. RISC-V based) - will they become part of an open source design ecosystem?
- I am curious to learn more about the **OpenROAD** initiative and open-source **API standards** that allow "plug-and-play" in the PD flow along with **data harvesting**.
- What's the **impact** of OSS to **chip design** for the next 20 years.
- **Real experiences** of different open source usage models
- **Educational activities and advocacy** movements **worldwide** for Open-Source EDA.
- **What prevents companies** from not only adopting OSS EDA but also contributing to it?
- Opensource EDA tools impact on the **CHIPS ACT**

Data and Benchmarking

- **Verification**, standard benchmarks
- **Analog** design benchmarks
- Come up with a **distributed way to "maintain" designs** submitted to Open MPW at scale (much like GNU/Linux distribution packagers manage to maintain an impressive amount of FLOSS software packages)
- (1) Elements and commitments of **data and benchmarking infrastructure** that enable the field to **transparently** move forward. (2) Key ("core") **optimization problem statements** that are the most important for the field to advance. (3) Open enablement of **machine learning to advance optimization** methodologies.

Machine Learning

- How can we **accelerate adoption of ML in chip design** processes?

Agenda Part 1: Open-Source EDA

- “OpenROAD: 3 Years in Perspective” – Tom Spyrou, UC San Diego and Precision Innovations
- “SiliconCompiler” – Andreas Olofsson, Zero ASIC
- “Parameters exploration using Jupyter notebook and Google Vizier” – Johan Euphrosin, Google
- “Showcase and updates of the EPFL logic synthesis libraries (<https://github.com/lsils/lstools-showcase>)” – Siang-Yun (Sonia) Lee, EPFL
- “LiveHD and Anubis” – Sakshi Garg, UCSC
- “System-level tools (e.g., Instruction Set Simulator) recently open-sourced” – Ulf Schlichtmann, TU Munich
- “DFiant cloud solution that offers access to OSS EDA flows” – Oron Port, DFiant
- Late-Breaking News and Discussion (what next, what is needed, who can contribute ...)

Open-Source EDA - Late-Breaking News and Discussion

- Path forward to an ecosystem?
- Standards (APIs, data)?
- Real experiences and impact on chip design?
- Educational initiatives and advocacy?

Agenda Part II: Data and Benchmarking

- “FPGA macro placement benchmark suite” – Ismail Bustany, AMD
- “New repository of benchmarks and best results targeting superconducting electronics (<https://github.com/lsils/SCE-benchmarks>)” – Siang-Yun (Sonia) Lee, EPFL
- “Efforts toward open data and benchmarking in the TILOS AI Institute: MacroPlacement and SpecPart” – Andrew Kahng, UCSD
- “Circuit Training (https://github.com/google-research/circuit_training), the open-source library for floorplanning using RL that my team and Google has open sourced recently as described in the ‘A graph placement methodology for fast chip design’ paper” – Sergio Guadarrama, Google
- Late-Breaking News and Discussion (what next, what is needed, who can contribute ...)

Data and Benchmarking - Late-Breaking News and Discussion

- **Verification benchmarking**
- **Analog design benchmarking**
- **Principles, and how to enable the field to transparently move forward?**
 - Data: enablements and designs that are “scalable and sharable”
- **Core optimization problems that need progress**
 - Forcing optimization out of comfort zones: → DL, cloud, ... ; flow-relevant benchmarking, ...
- **Ethical, fair benchmarking**
 - Transparency, openness
 - Figures of merit
 - Measurement processes
- **Followups to survey: form working groups?**
 - Define benchmarking methodologies
 - Provide benchmarks and data

Agenda Part III: New Research Foundations

- “Push for an Open Hardware Technology Commons in Coordination with the NIST National Semiconductor Technology Center” – Antonino Tumeo, Pacific Northwest National Laboratory
- “How persons developing flows and other work products can share those with colleagues” – David Junkin, Cadence
- Late-Breaking News and Discussion (what next, what is needed, who can contribute ...)

Research Foundations - Late-Breaking News and Discussion

- Hardware commons?
- Sharing of scripts and reproducible research ?!?
 - Will we require research results to be reproducible?
- Working groups and volunteers?
 - Core EDA optimization problems (to benchmark and roadmap)
 - Key gaps in open-source EDA (to fill in)