A Report
On

Designing Various circuits using Quantum Dots cellular automata(QCA)

By

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Under the guidance of

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Abstract

In the near future ,the era of “Beyond CMOS” will start as the scaling of the current CMOS technology will reach the fundamental limit. QCA (Quantum-dot Cellular Automata) is the transistor less computation paradigm which can replace the current CMOS technology in future.In this report we first discuss the basic concepts and gates for better understanding of QCA Technology.Later we discuss an approach to design 1 bit full adder using quantum cellular automata with the help of QCA Designer.To design the circuit,we first designed the 5 input majority gate which is the basic building block of the circuit.After verifying the outputs of our full adder, we move on to some statistics related to out design and conclude the report based on out observations and results.

Introduction

The concept of “Moore’s Law” refers to the continuous scaling of horizontal and vertical physical feature sizes of silicon based complementary metal oxide semiconductor (CMOS) to double of its size every year. This theory was one of the first theories that led to massive expansion and development of technologies around semiconductor and electronic devices. Although this theory has led to decrement of size of Semiconductor to 5 nm in the year 2020, [1] Many scientists believe that the moore’s law is reaching its limits where no compression or scaling of semiconductor is possible as it shows many effects that reduces the power capacity and efficiency of of chips while the cost of these might increase. Thus many Researchers and scientists are looking towards future technologies like quantum dots, Carbon nanotubes, MESO technology etc. that could potentially replace CMOS in decades to come. While these technologies are yet to be officially in use, Let us look at one such technology and understand what it holds for the future.[2]

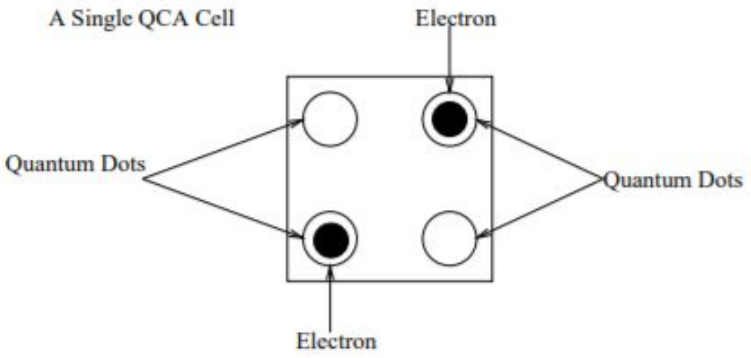
Problems in Current technology

- Physical challenges: Due to Decrease in size of transistors, the increment of tunneling and leakage currents, thus creating various short channeling effects and impacting the performance and functionality of CMOS devices.
- Power-thermal challenges: These are because of the ever increasing number of transistors integrated per unit-area, which demands larger power consumption and higher thermal dissipation. [3]
- Technological challenges: These are the results from the incompetence of lithography-based techniques to provide the resolution below the wavelength of the light to manufacture to CMOS devices.
- Economical challenges: As the transistors are reaching their potential, More money is spent on research and development. While not many alternative technologies are currently in existence, fab, and testing that may reach a point where it will be not affordable from an economic point of view.[4]

QCA(Quantum dots cellular automata)

Quantum-dot Cellular Automata (QCA) is a novel nano-scale computing mechanism that can represent binary information based on spatial distribution of electron charge configuration in chemical molecules. Quantum Dot Cellular Automata is an alternate challenging quantum phenomenon that provides a completely different computational platform to design digital logic circuits using quantum dots. This device has the potential to greatly simplify the construction of circuits because every component of the circuit is represented by a cell and only one type of gate (the "majority gate") is needed.The basic structure of a quantum cell is given below.[5]

Fig. 1 Basic Quantum cell structure.



From the above diagram, We can see that the basic cell structure contains four electron wells i.e Quantum dots.
In QCA, the cells operate using Coulombic interaction.
The electrons are transferred from one well to another by charge repulsion or attraction. Because of this no current flows between the cells and no power (or information) is dissipated by the internals of the cell. Conservative estimates indicate that room temperature devices could be clocked in the 1-10 terahertz range and be 100 times more dense than a CMOS device at the end of the CMOS curve.[4]

Fundamentals of QCA

As discussed above, A QCA cell contains 4 quantum dots for which two electrons can occupy. With the help of tunneling junctions and potential barriers which are regulated by electric fields and coulombic forces will prohibit electrons from overflow or to restrict electrons from moving in unorganised manner, In general, any isolate cell can be in any one of the three states, Null state where the electron is free to move to any state as the barriers are lowered. Where the other states depends on the polarization states of the cell i.e. They can either maximise or minimize the energy states of the cell when the barrier is raised. These states are denoted by Polarization value P where it can possess the values -1 and 1.[5]

- The polarization value P = -1 indicates the binary value "0"
- The polarization value P = +1 indicates the binary value "1"

These cells can be represented in two orientations based on their applications.

- 45-Degree orientation
- 90-Degree orientation

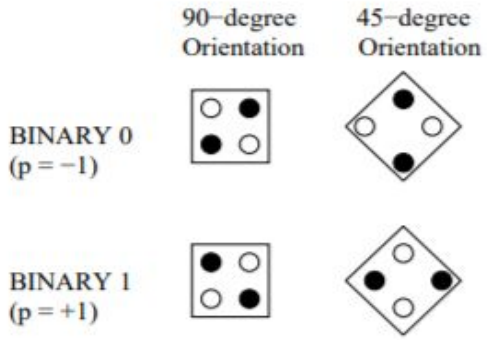


Figure 2. Diagram of QCA cells of different orientations.

How does QCA cells work for transmitting the data?

To transmit any data, the QCA cells should be placed in such a way that whenever we pass any data through the input, the cells connected should change due to coulombic repulsion and attractions. Thus, whenever the input polarization is changed through external stimulation, the values of output are changed accordingly. The arrangement of cells is done by using quantum wires and gates.

Quantum Wire

To propagate the values of binary digits we use quantum dot cells in a line structure next to each other with the same polarity to transmit the data. These line structures of quantum dots are known as quantum wires. Whenever the data needs to be sent, The polarization of the first cell is changed which will trigger the next cells due to coulombic repulsions. Thus all the electrons present in the cells are adjusted accordingly. So the data that is received at the last cell gives the changed value through which the data is recorded. [7]

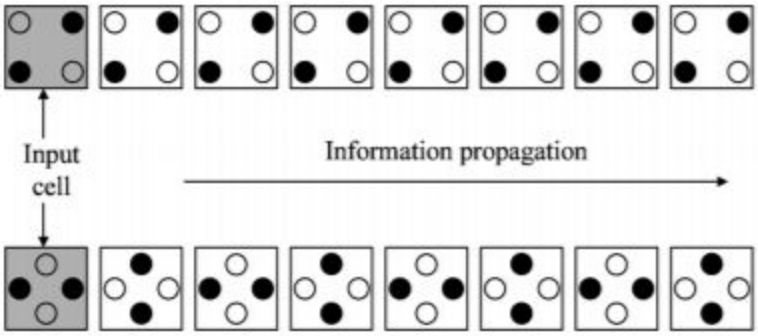


Figure. 3 Propagation of information using a quantum wire.

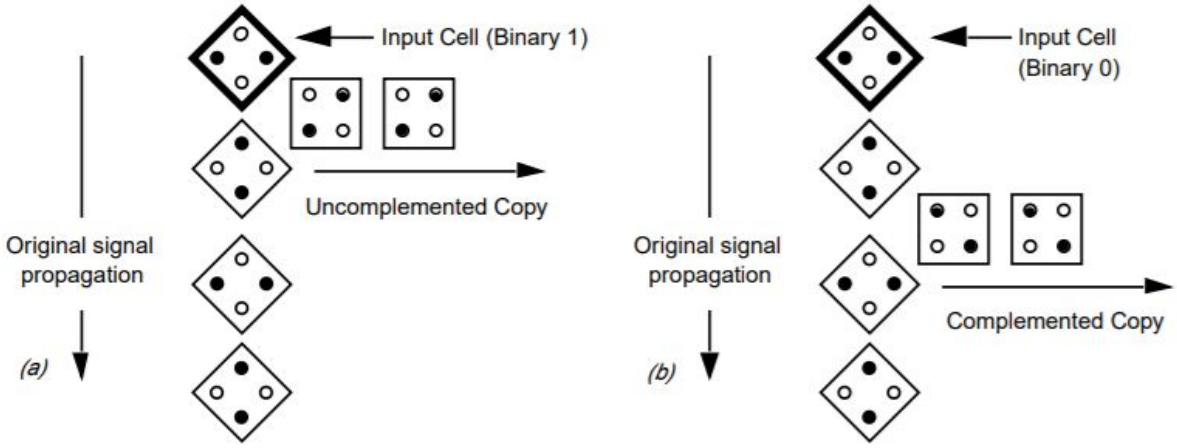


Figure. 4 Propagation of information using a quantum wire in a 45° Orientation if the (a) Input is 1
(b) Input is 0

Designing various circuits using QCA

Inverter

One of the Advantages of QCA is that we can even design various large circuits using three simple basic circuits which are, Quantum wire, QCA Inverter and QCA Majority gate. A simple inverter can be designed by placing cells diagonally so that the polarizations of input and output cells are opposite to each other as shown below.

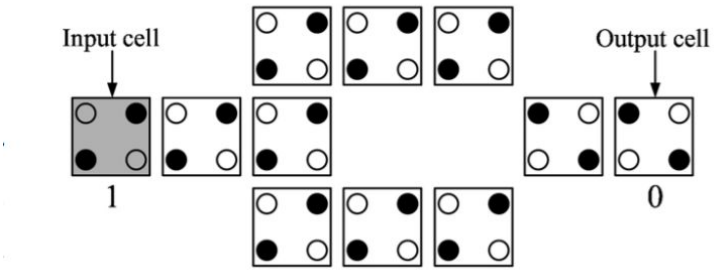


Figure. 5 Diagram of QCA inverter.

From the above diagram we can clearly see that the input is of "-1" polarization while the circuit is of polarization "1"

Majority Gate

In a 3 input majority gate, inputs are given such that the majority polarisation wins and then propagates to become the output. I.e Its logic equation is given as

F = AB + BC + AC, where A, B, and C are inputs and F is the single output

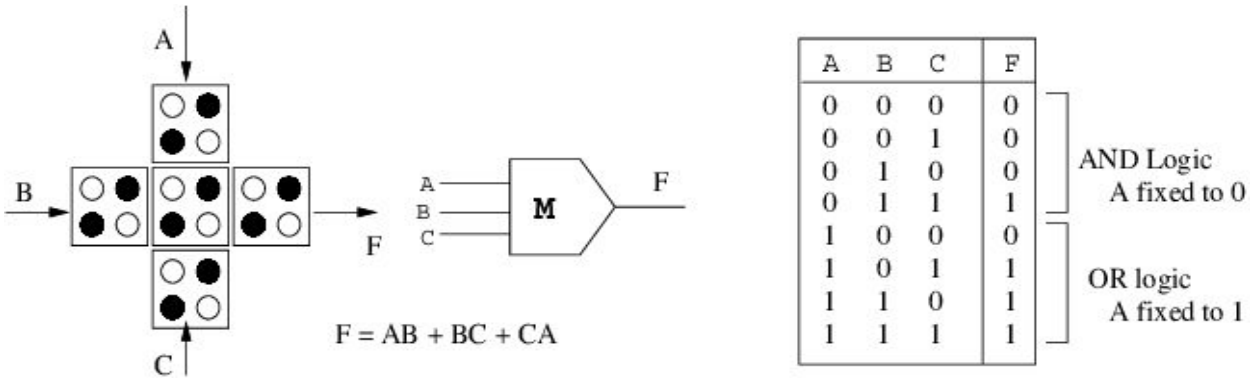


Figure. 6 (a) Diagram of QCA 3-input majority gate.
(b) the Logic table of majority gate.

5-Input majority gate is similar to that of 3-input majority but with 5 inputs deciding the output based on inputs.

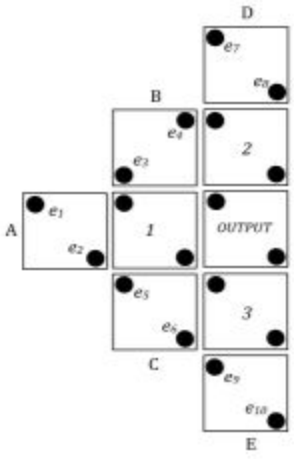


Figure. 7 (a) Diagram of QCA 5-input majority gate.

Table 1 Truth table of MV_5 based on sum of inputs

Σ (A, B, C, D, E)	MV (A, B, C, D, E)
0	0
1	0
2	0
3	1
4	1
5	1

(b) Shows the Logic table of majority gate.

In the above given diagram, the cells are placed at 2nm apart such that the potential and coulomb attraction force between them will make the circuit stable. In this project we are using these above circuits to draw various circuits.[6]

Understanding the QCA clocking

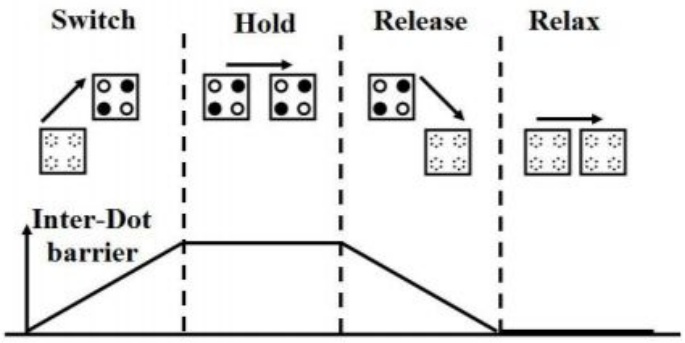
As the QCA circuits are inherently pipelined at the gate level, and the timing of signal delivery requires that all the signals for a given gate signal simultaneously. In particular, each QCA wire inherently holds state information for a clock cycle because the wire is constructed from QCA devices, and the state is held in the position of the charge on two devices which are physically interacting. Due to this and other QCA specific features, QCA physical design solves a number of interesting problems that are different from traditional VLSI physical design.

Unlike in CMOS circuits,in QCA There are four clock states in general, namely

1. Switch
2. Hold
3. Release
4. Relax

While performing any activity in QCA, first comes the switch phase where the interdot barrier is systematically raised while the QCA cell is settled down to 1st ground state polarization while tunneling. Once it is arrived at 1st ground state, the intedot barrier will be passed to hold state where the interdot barrier is set high. This will suppress the electrons tunneling and will maintain the ground state (also called as 2nd ground state) until the channel gets ready. In the release phase, the interdot barriers are lowered and the electrons gain kinetic energy and will start to mobilize the electrons to move to the destination. Once the electrons are sent across, the cell comes to a relaxed state where the cell is unpolarized. In general in the timing diagrams, The polarization of the cell is determined by values where the cell is in switch state or usually in the hold state if there's any intentional delay is given. In release and relax states, the unpolarized wells or dots have no effect in determining the polarization state of the cell.The clock signals (through an induced electric field) can be generated by CMOS wires embedded below the QCA plane. [5]

Figure 8 Timing diagram of a typical QCA cell.



Designing various circuits using QCA

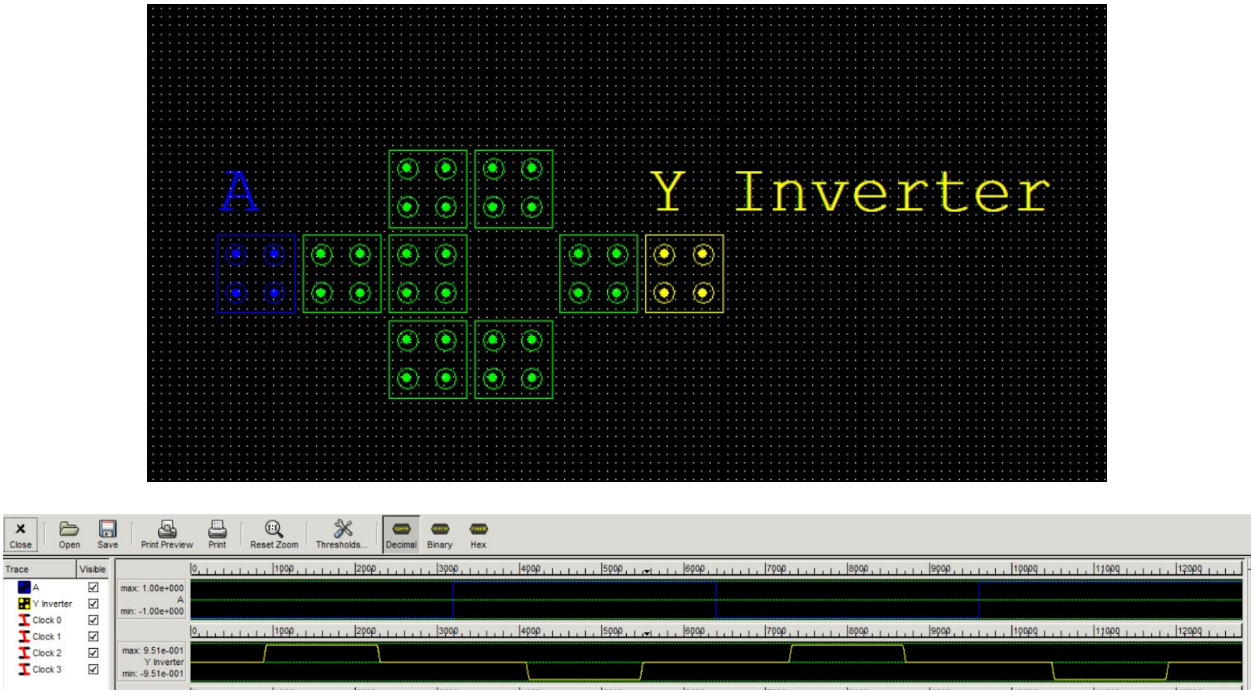
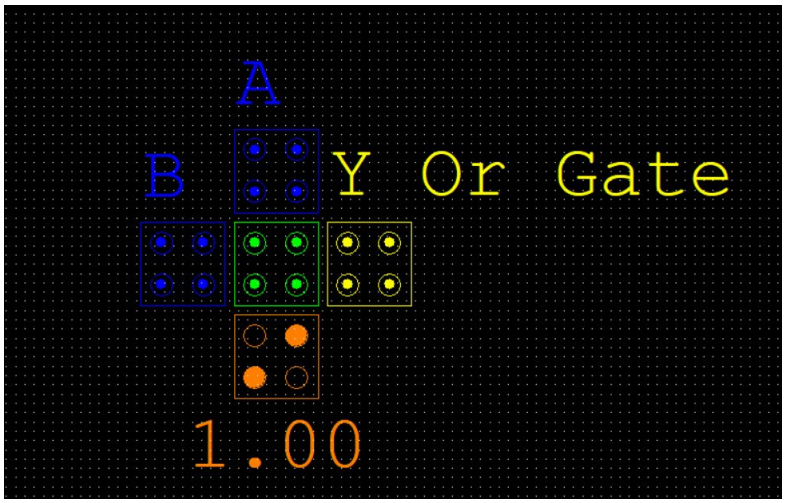


Figure 9 Circuit and Timing diagram of a Inverter



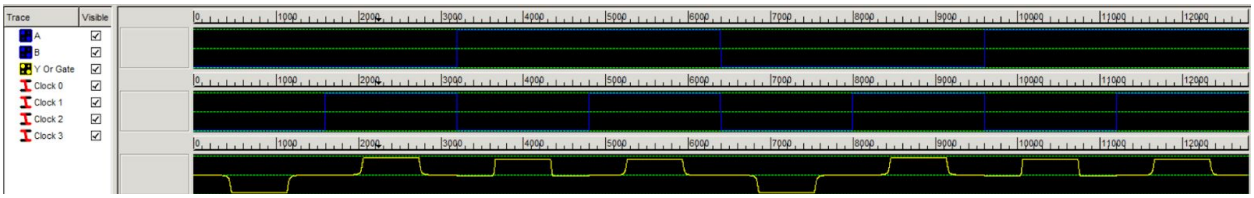


Figure 10 Circuit and Timing diagram of a Or gate

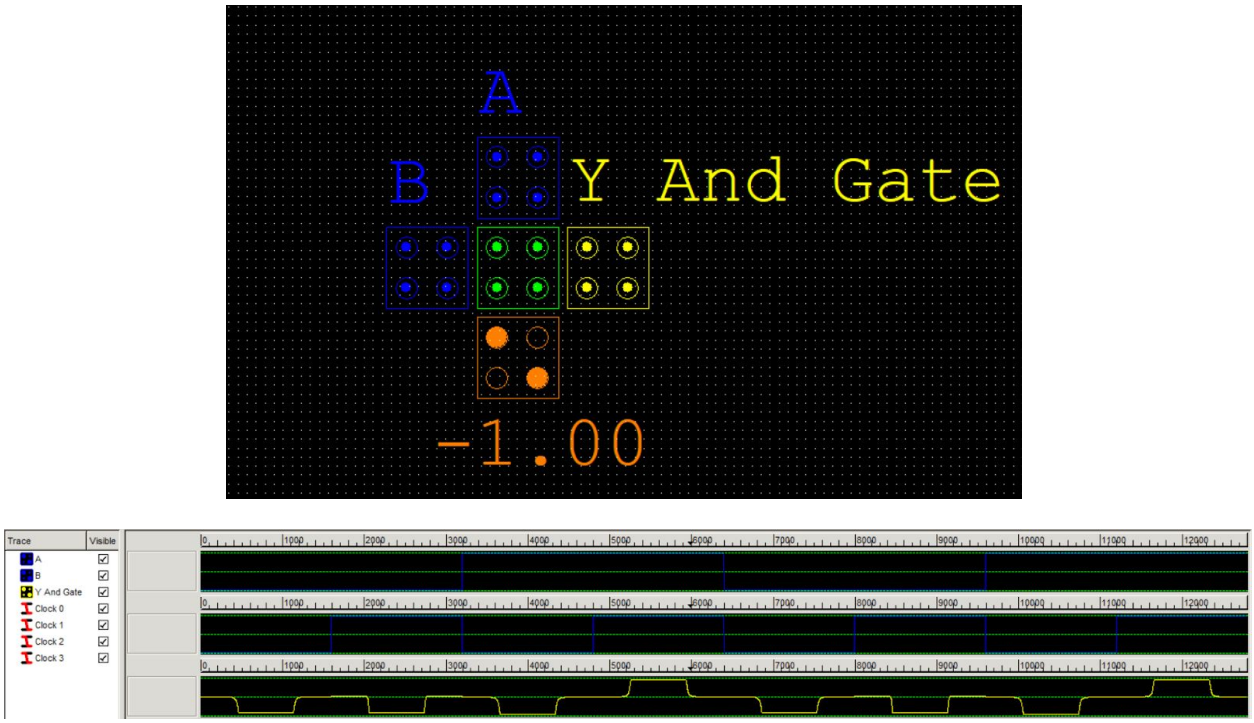


Figure 11 Circuit and Timing diagram of a And gate

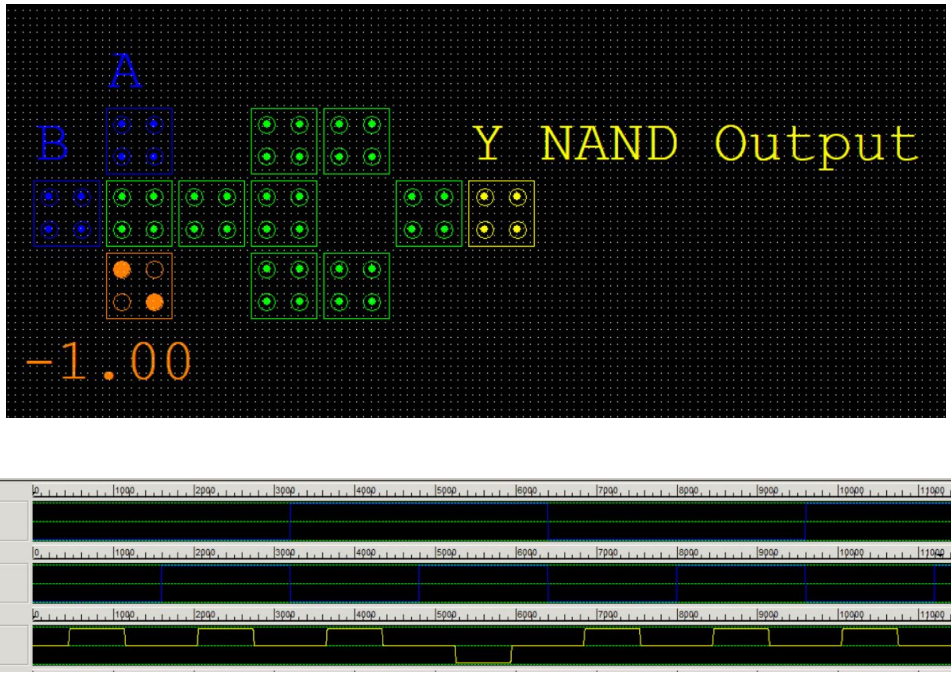


Figure 12 Circuit and Timing diagram of a Nand gate

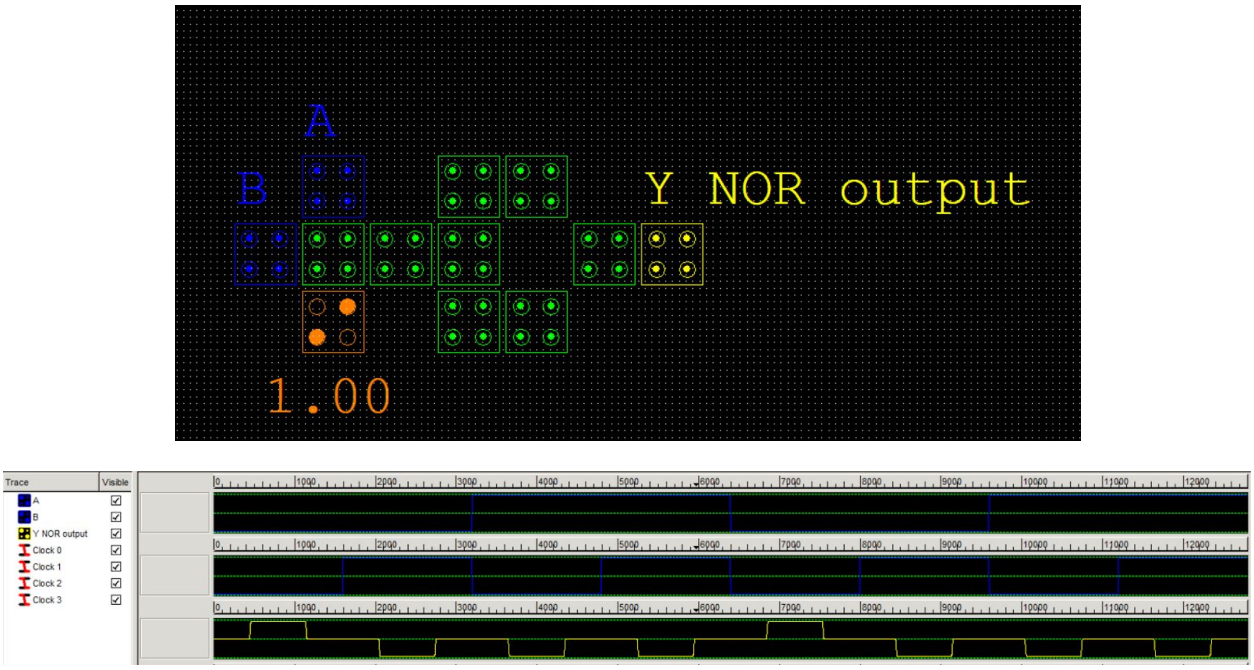


Figure 13 Circuit and Timing diagram of a Nor gate

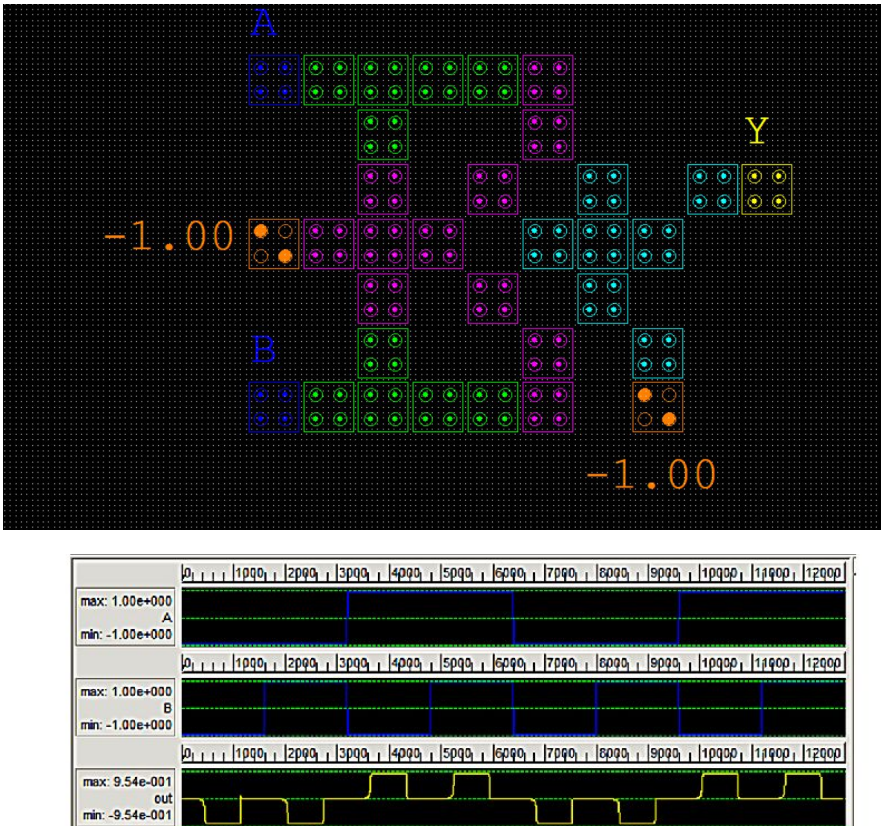


Figure 14 Circuit and Timing diagram of a Xor gate

Figure 15 Circuit and Timing diagram of a 3 input majority gate

Designing Full adder using QCA:

As discussed above we have designed and verified the outputs of MV5 (5-input Majority voter), we now use this as a building block to the full adder circuit. The block diagram is given below.

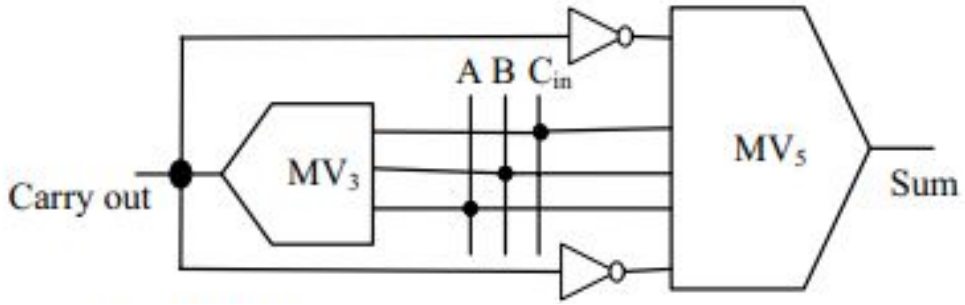


Figure 16 Circuit diagram of Full adder circuit using MV5

We use 2 MV5's and two NOT gate gates to complete the circuit and the dark circles represent links between different layers.The designs have been simulated and verified using QCADesigner which are the only available tools for QCA layout design and verification.

This QCA full-adder mainly consists of three layers. The main layer has 34 q-cells, the second layer has 4 q-cells and the third layer contains 10 q-cells. In Total, it requires 48 q-cells and 3 clock phases to get the (Sum and Carry). Using QCADesigner, complexity, time delay and area consumption of QCA circuits can easily be calculated .Here, complexity means the number of cells used to design the FA. The "**Latency**" indicates the number of clock zones used.The proposed design has less area count and less no of cells.This makes the circuit look dense and compact which can be implemented in lesser areas when compared to previous proposed versions.[6]

Proposed Design of Full Adder Using QCA Designer:

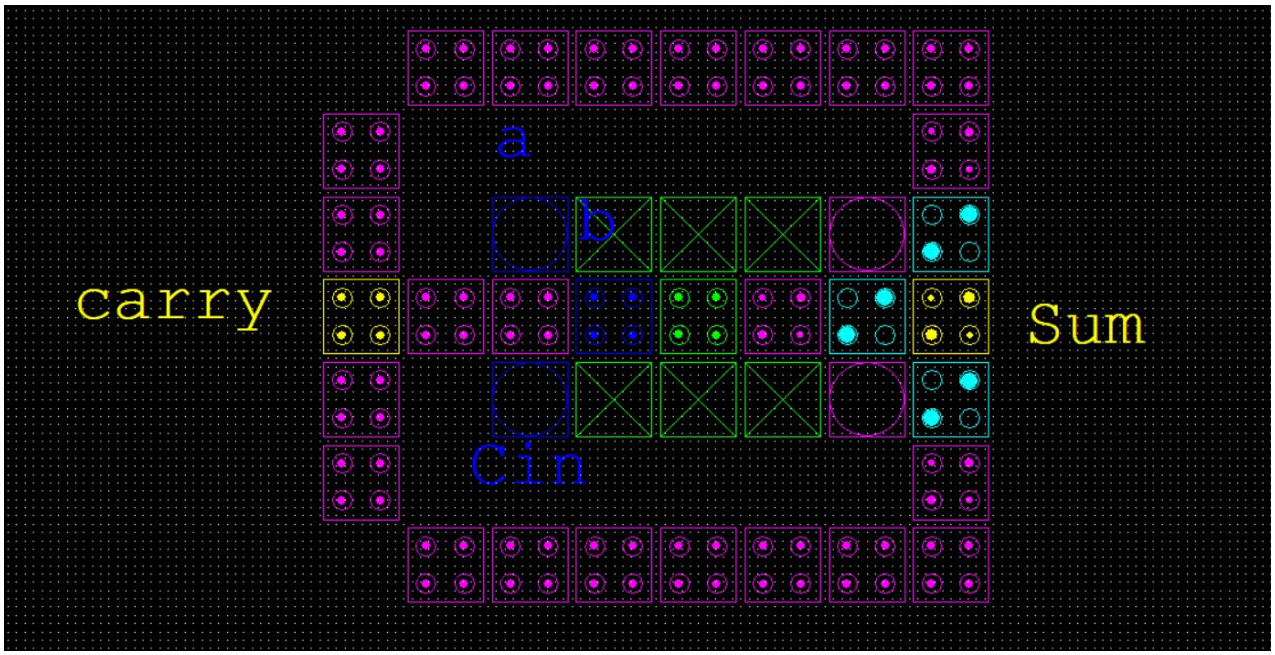
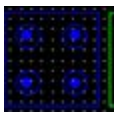
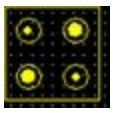


Figure 17 Circuit diagram of Full adder

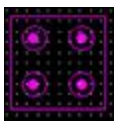
The above circuit is the top view for full adder which consists of 3 inputs(a,b,C_{in}) and two outputs(Sum and Carry) which performs simple addition and output respective bits.The significance of different colours of cells in the circuit are mentioned below.



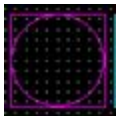
Blue cells represent input cells with clock 0(No polarisation given)



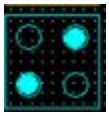
Yellow cells represent output cells with clock zero(with +0.257 polarisation default set in software)



Pink cells represent cells in the circuit with clock 1(with +0.001 polarisation default set in software)



Pink cells represent cells in the circuit with clock 1 and used to link different layers in the circuit(with -0.004 polarisation default set in software.



Cyan cells represent cells in the circuit with clock 2(with +0.7684 polarisation default set in software)

Statistics related to the FA circuit:

Power dissipation:

The power dissipated from a single cell depends on the rate of change of the clock and the tunneling energy. The power dissipation of a QCA circuit in a single clock phase can be simply calculated by adding the power dissipated by each majority gate and inverter.

```
Total energy dissipation (Sum_Ebath): 1.84e-002 eV (Error: +/- -1.98e-003 eV)
Average energy dissipation per cycle (Avg_Ebath): 1.67e-003 eV (Error: +/- -1.80e-004 eV)
```

These values are generated from QCA Designer-E software which uses the method of coherence vector energy simulation with 500000 samples.

Reliability of proposed QCA circuits

For some circuits, the relationship between total reliability and components reliability is unknown. But as an example for an adder design, the total reliability is linearly dependent on the defect rates of the circuit's components (wires and gates). However, the effect of wires and gates defects on the total reliability of the system is not the same. The reliability of the gates has a direct effect on the total reliability while the reliability of the wires has a four times effect on the total reliability of the circuit. In the other words, the reliability of wires highly affects the total reliability of the circuit.

Simulation Results

The Proposed QCA Full adder is designed and simulated in QCA designer 2.0.3 and QCA designer-E is used for the analysis of Energy dissipation. The size of each quantum cell is 18 nm × 18 nm. In addition, there is a distance of 2 nm between the neighboring cells. Therefore, the occupied area of a QCA layout can be calculated as follows:

Area=(maximum longitudinal cell number) ×(maximum transversal cell number)×400 nm^2.

A generalized cost function for QCA circuits was first introduced by Liu and others as follows:

$$\mathrm{QCA}_{\mathrm{cost}} = \left(M^k + I + C^l\right) \times T^p. \quad k.l.p \geq 1.$$

where **M** denotes the number of majority gates, **I** the number of inverters, C the number of crossovers, and **T** the delay of the circuit. Moreover, **k, l,** and **p** denote the exponential weightings for majority gate count, crossover count, and delay, respectively. Because the number of the majority gates is related to complexity and energy dissipation, a double weight is considered for the **M** parameter, that is, **k = 2**. In addition, this issue is also true for the **C** parameter, as the number of crossovers is related to the complexity and fabrication difficulty. Therefore, in the general case, the QCA cost function can be expressed as follows:

$$\mathrm{QCA}_{\mathrm{cost}} = \left(M^2 + I + C^2\right) T.$$

Parameters	Values
Number of samples	12800
Convergence Tolerance	0.001000
Radius of effect[nm]	65.0000
Relative permittivity	12.9000
Clock High	9.800e-022
Clock Low	3.800e-023
Clock Shift	0.000e+00
Clock Amplitude factor	2.00000
Cell height	18.00nm
Dot diameter	5.000
Cell width	18.00nm

Table 1 *Utilized parameters for "bistable approximation" engine in our simulation*

Figure 18 simulations results of proposed QCA Full adder.

Conclusion

Finally we can conclude that the Modern day CMOS technology is power drinkers and we have also seen power analysis of the Quantum Dot Cellular Automata circuits, It has consumed a very less Amount of energy and Power. We have designed and simulated the QCA circuits in QCA designer and for energy dissipation we used QCA designer-E, we designed Full adder with total 48 cells (34 in main layer, 4 in layer 1,10 in layer2).

Factor description	**Low power CMOS**	**Novel QCA**
Power	4.578 uw[9]	0.0445e-22w
Area	158 um^2[10]	0.03um^2

Table 2 *comparison of Low power CMOS vs Novel QCA.*

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