

Lab Report III: Operational Amplifiers

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Lab 7: Operational Amplifiers

Objective

The objective of this lab is to familiarize ourselves with the orientation and function of an op amp within a circuit and understand the two op-amp rules when building various amplifiers.

Question 1

Recreate the circuit in Fig. 2 using an LM741CN op-amp. Breadboard setup with $V_{CC} = 15.03\text{ V}$, $V_{EE} = -15.08\text{ V}$, $R_g = R_{in} = 10\text{ k}\Omega$. Set the waveform amplitude to 328 mV peak-to-peak.

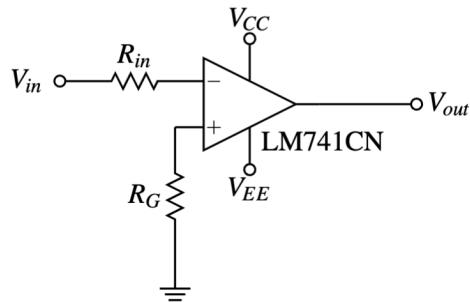


Figure 7.2: Basic Op Amp circuit (inverting comparator).

Figure 1

When viewing our waveforms, we set our amplitude to be 160 mV_{p.p.}, falling within the given limits of 50 mV and 300 mV.

Below are our observed waveforms in order of frequencies 135 Hz, 1.35 kHz, 4.2 kHz, and 25.05 kHz.

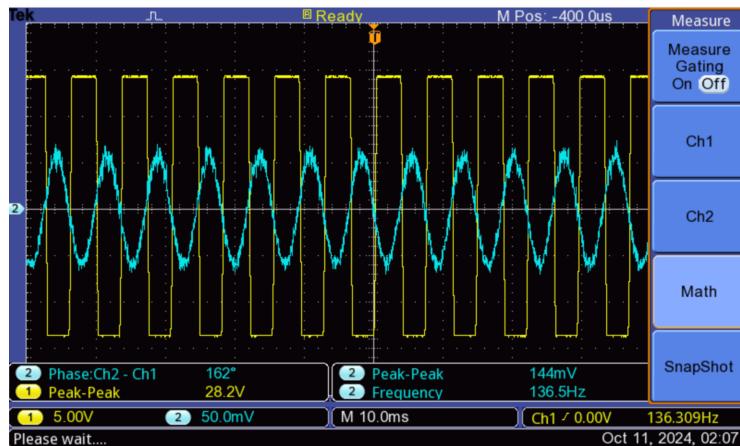


Figure 2

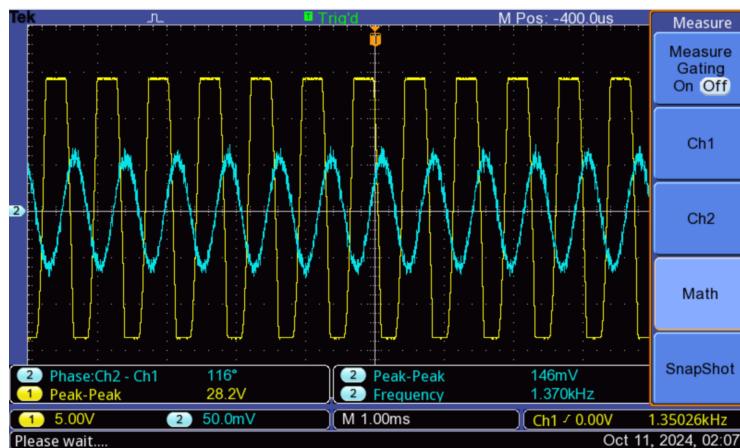


Figure 3

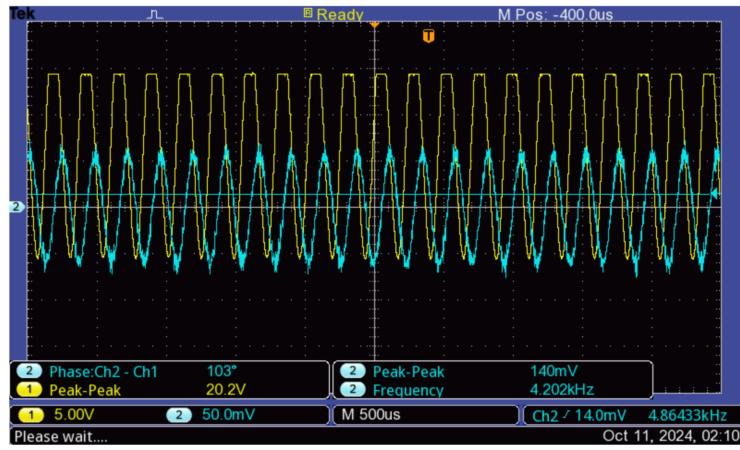


Figure 4

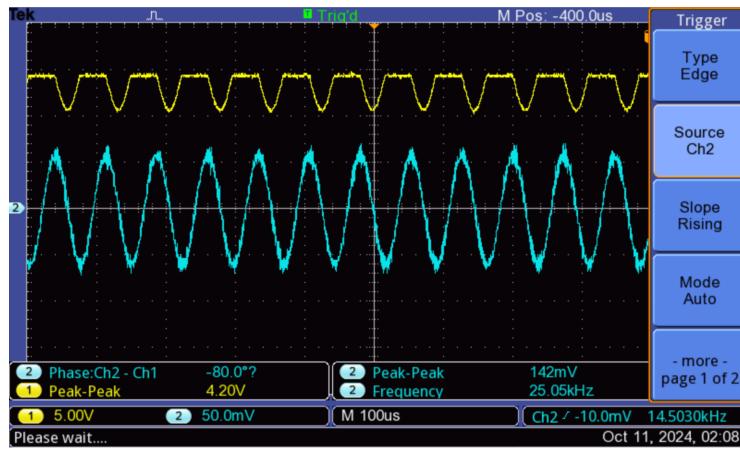


Figure 5

Our op-amp does not continue to compare throughout all frequencies and appears to stop comparing at a frequency of 3.2 kHz, the waveform for which is shown below.

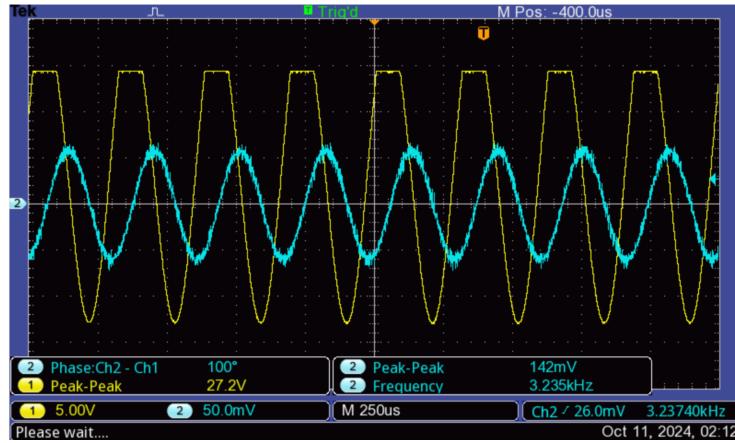


Figure 6: Waveform at 3.2 kHz

”Comparating” refers to the op-amp’s attempt to output a voltage very close to either the positive rail, V_{CC} , or the negative rail, V_{EE} , depending on whether V_{in} is less than or greater than the reference voltages V_{CC} or V_{EE} . This behavior is due to its significant open-loop gain. At a certain frequency, V_{out} decreased, making the gain smaller and more difficult to maintain.

At a certain frequency, V_{out} decreased making the gain smaller making it more difficult to compare changing voltages.

Question 2

Build the amplifier in Fig. 3, measuring gain as $-R_f/R_{in}$ with a ratio of 100.

Table 1: Gain measurements for ratio of 10

Frequency (Hz)	V_{in} (mV)	V_{out} (mV)
100	328	2880
1k	328	2880
10k	328	2880
100k	328	3240

Table 2: Gain measurements for ratio of 100

Frequency (Hz)	V_{in} (mV)	V_{out} (V)
100	304	25.8
1k	304	25.8
10k	312	25.2
40k	312	25.2
100k	320	25.8

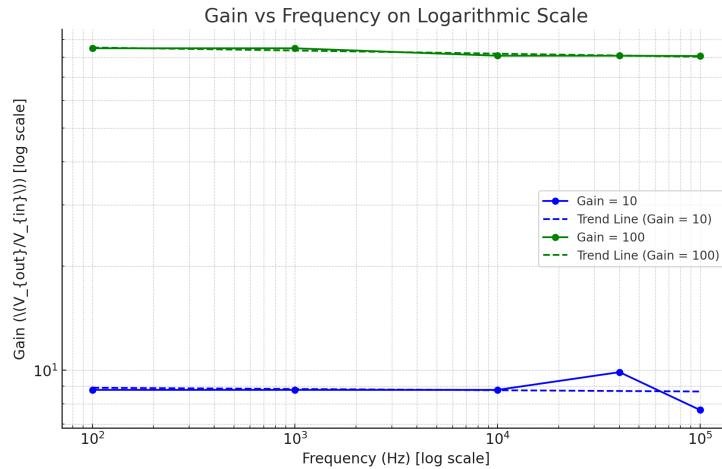


Figure 7: Gain vs. Frequency on Logarithmic Scale for Gain = 10 and Gain = 100 with Trend Lines. The plot illustrates the relationship between the frequency of the input signal and the gain of the amplifier, showing a decrease in gain at higher frequencies for both configurations.

The plot shows how the gain behaves across a range of frequencies for two different gain settings: 10 and 100.

- **Gain = 10:** The gain remains relatively stable across the lower frequencies but shows a noticeable decline as the frequency approaches 100 kHz. This behavior indicates that the amplifier can maintain its gain effectively up to a certain frequency, after which it starts to lose efficiency, possibly due to limitations in the op-amp's open-loop gain or bandwidth.
- **Gain = 100:** Similar to the Gain = 10 scenario, the gain starts high and remains fairly consistent at lower frequencies but experiences a drop as the frequency increases. The gain decreases more sharply compared to the Gain = 10 setting, indicating that higher gain configurations are more susceptible to frequency-related losses.

The trend lines (dashed) demonstrate the overall decreasing trend of gain with increasing frequency, which is typical for amplifiers as they approach

their frequency limits or bandwidth constraints. This drop in gain at higher frequencies is due to the op-amp's inability to respond quickly enough to the rapid changes in the input signal, leading to reduced amplification.

Question 3

Using the two fundamental op-amp rules:

1. The output adjusts itself to make the voltage difference between the inverting and non-inverting inputs as close to zero as possible.
2. The inputs draw no current.

We can understand how the gain of the inverting amplifier is determined. Since no current flows into the inputs of the op-amp, the current through the feedback resistor R_f must equal the current through the input resistor R_{in} . This creates a voltage difference that is directly proportional to the input voltage V_{in} , scaled by the ratio R_f/R_{in} .

The op-amp works to minimize the voltage difference between its inputs by adjusting the output voltage V_{out} . As a result, the output voltage is given by the expression $V_{out} = -\frac{R_f}{R_{in}}V_{in}$, which represents the gain of the inverting amplifier. Additionally, because there is no current through R_g , the inverting input behaves like an extended virtual ground.

Question 4

Using the summing amplifier configuration, we measured the output voltage V_{out} for different combinations of input voltages V_1 and V_2 , and resistances R_1 , R_2 , and R_f .

The output voltage V_{out} is given by:

$$V_{out} = - \left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 \right)$$

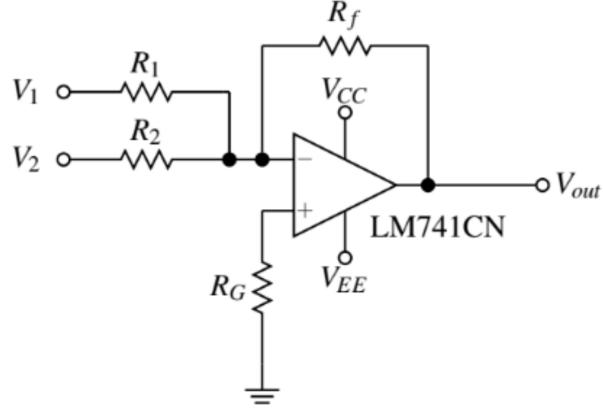


Figure 7.4: Summing (also inverting) amplifier.

Figure 8

Below is the table of our measurements:

Table 3: Summing Amplifier Measurements

V_1 (V)	V_2 (V)	R_1 (kΩ)	R_2 (kΩ)	R_f (kΩ)	V_{out} (V)
2.5	2.5	1	1	1	-0.48
2.5	2.5	10	10	1	-4.92
5	5	10	10	10	-9.9
5	5	100	10	10	-5.4
5	5	10	10	1	-0.99
7.5	7.5	10	10	1	-1.47

We observed that whenever R_f was significantly larger than R_1 and R_2 , V_{out} became overloaded due to an excessive amplification factor. This caused the output to default to the breadboard's maximum voltage of approximately 15 V.

Question 5

We are now tasked with using the data collected from Question 4 to derive an equation for V_{out} as a function of V_1 , V_2 , R_1 , R_2 , and R_f . Additionally, we need to generalize this formula for V_n and R_n .

Since V_{out} is consistently negative, and we are working with an inverting amplifier, we can assume the gain is given by $-\frac{R_f}{R_{in}}$. Given n values for R_{in} , we can express a portion of V_{out} as:

$$V_{\text{out}} = -\frac{R_f}{R_1} + \dots + -\frac{R_f}{R_n}$$

Since gain is dimensionless, but V_{out} is measured in volts, we multiply by the input voltages V_{in} to obtain:

$$V_{\text{out}} = -\frac{R_f}{R_{\text{in}}} \times V_{\text{in}}$$

By combining these concepts, we derive the general solution:

$$V_{\text{out}} = -\frac{R_f}{R_1} V_1 + \dots + -\frac{R_f}{R_n} V_n$$

To match this to the summing (inverting) amplifier, the equation simplifies to:

$$V_{\text{out}} = -\frac{R_f}{R_1} V_1 - \frac{R_f}{R_2} V_2$$

Applying our data to this formula yields a calculated V_{out} that closely matches the measured V_{out} , with an error of approximately 1.8%.

As noted in Question 4, if the calculated V_{out} exceeds the limits of V_{EE} or V_{CC} , the output will become overloaded and default to the voltage of the positive (+) or negative (-) rail.

Bonus Question

Using the summing amplifier configuration from Questions 4 and 5, with $R_1 = R_2 = R_f$, we applied sine waves to both inputs. Initially, we set both input frequencies to 10 kHz, and then varied them to observe the interaction between the waves.

When the frequencies were close to each other, the resulting output appeared as a single sine wave, demonstrating constructive interference. However, as the frequencies diverged, the output displayed a superposition of waves. This resulted in distinct wave packets, where each packet contained segments of individual sine waves corresponding to the different input frequencies.

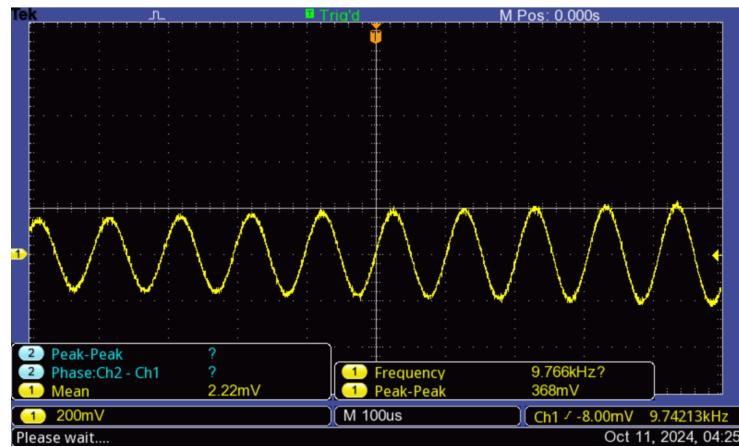


Figure 9: $f_1 = f_2 = 10\text{kHz}$

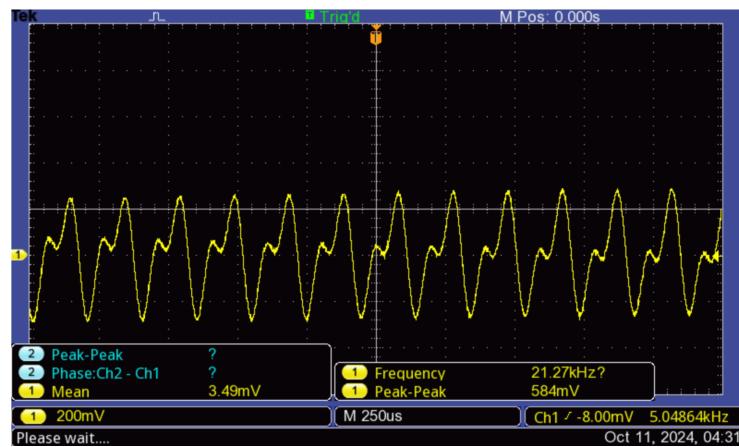


Figure 10: $f_1 = 10\text{kHz}$ $f_2 = 12\text{kHz}$

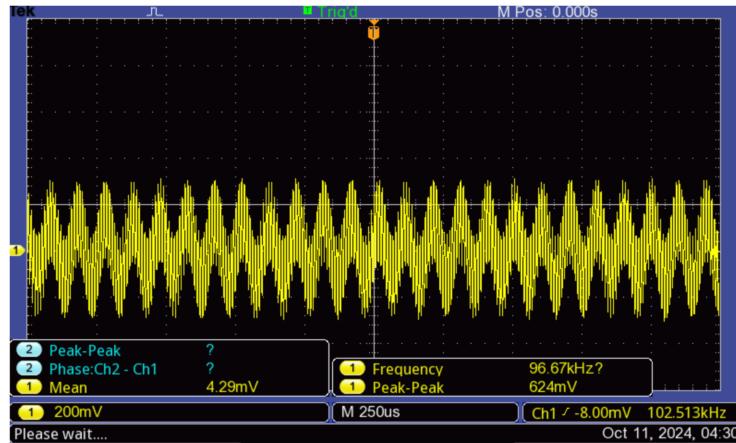


Figure 11: $f_1 = 10\text{kHz}$ $f_2 = 100\text{kHz}$

Observations include:

- $f_1 = f_2 = 10\text{kHz}$: Waves perfectly superimpose.
- $f_1 = 10\text{kHz}, f_2 = 12\text{kHz}$: Slight divergence observed.
- $f_1 = 10\text{kHz}, f_2 = 100\text{kHz}$: Distinct superposition patterns.

Lab 8: Operational Amplifiers II

Introduction

In this lab, we explored three different operational amplifier (op-amp) circuits: an integrator, a comparator without feedback, and a comparator with feedback (Schmitt trigger). The objective was to build, observe, and analyze the behavior of these circuits.

Question 1

Objective: Build an op-amp integrator circuit using a capacitor C_f and input resistance R_{in} , and determine the frequency range over which the circuit produces the integral of V_{in} .

Procedure:

- A square wave input was applied to the circuit.
- The output waveforms were observed at various frequencies using an oscilloscope.

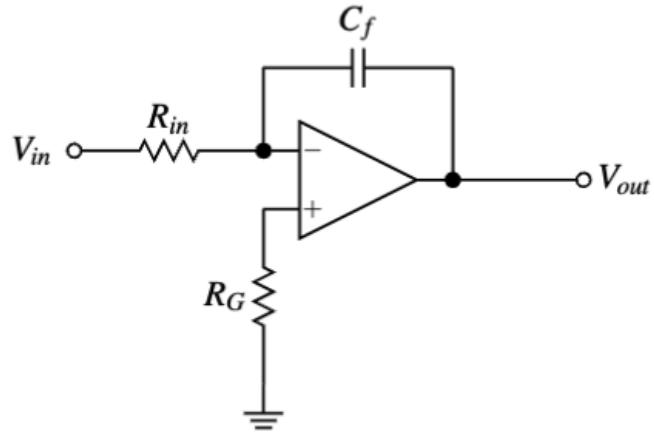


Figure 8.2: Op Amp Integrator.

Figure 12: Output waveforms at various frequencies

Observation: At lower frequencies, the circuit effectively integrates the input, resulting in a triangular waveform. As the frequency increases, the integration behavior diminishes, producing a distorted output.

Below are the output waveforms displaying the frequency range in practice in the following order; 900Hz, 9.8kHz, 121kHz, 422kHz

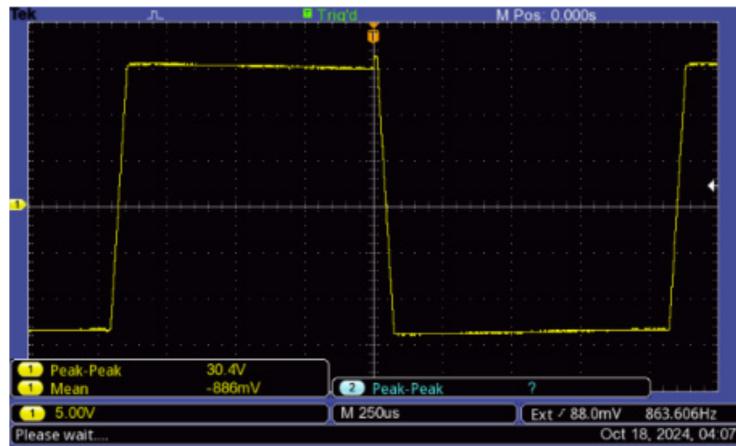


Figure 13

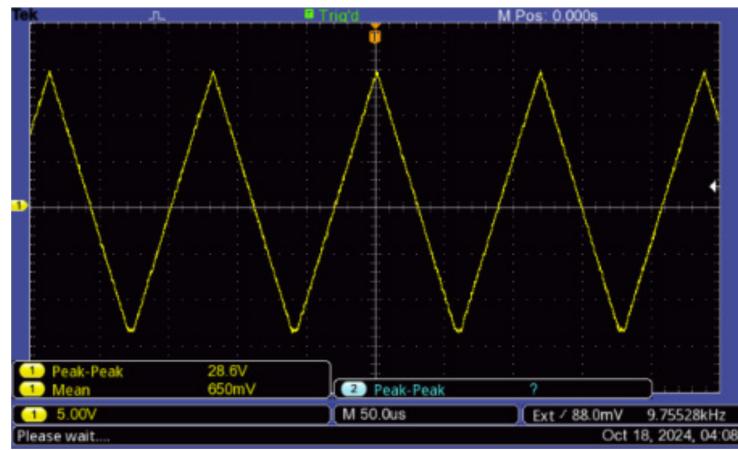


Figure 14

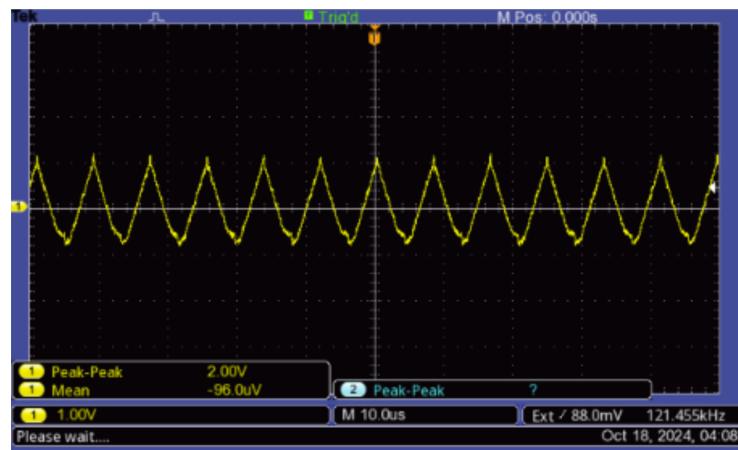


Figure 15

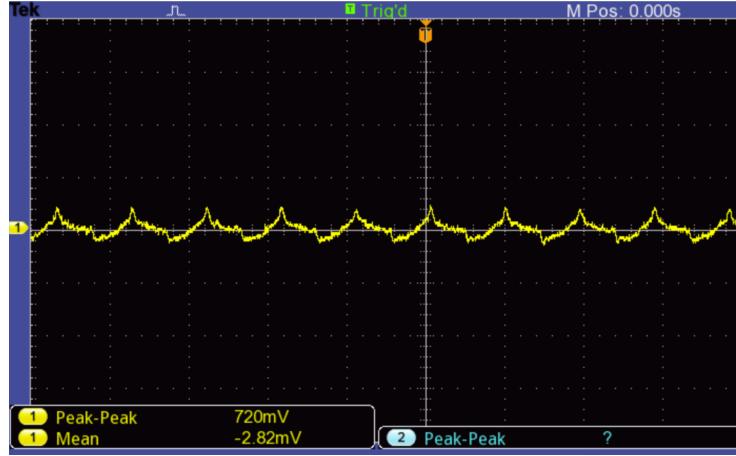


Figure 16

Question 2

Using our knowledge of RC circuits, as well as the op-amp rules:

1. The output attempts to do whatever is necessary to make the voltage difference between the two inputs zero.
2. The inputs draw no current.

We can derive the relationship between the input and output of the integrator as follows:

Since no current flows through the inputs, I_{in} does not split, so $I_C = I_R$. Using Ohm's law:

$$I_R = \frac{V_{R_{\text{in}}}}{R_{\text{in}}} \quad \text{where} \quad V_{R_{\text{in}}} = V_{\text{in}} - V^-$$

This simplifies to:

$$I_R = \frac{V_{\text{in}} - V^-}{R_{\text{in}}}$$

Using rule (2), V^- equals 0, acting as a virtual ground, so:

$$I_R = \frac{V_{\text{in}}}{R_{\text{in}}}$$

The capacitor current I_C is given by:

$$I_C = C \frac{dV_{\text{out}}}{dt}$$

Since $I_C = I_R$, we have:

$$C \frac{dV_{\text{out}}}{dt} = \frac{V_{\text{in}}}{R_{\text{in}}}$$

Integrating both sides with respect to time:

$$V_{\text{out}} = \frac{1}{R_{\text{in}} C} \int V_{\text{in}} dt$$

Compared to an RC filter, an op-amp requires a stable V_{in} or power supply, while an RC filter is dependent on having a proper capacitor as it charges over time.

For the output magnitudes, an op-amp is constrained by the limits of the positive and negative rails, whereas an RC filter is constrained by the current voltage charge of the capacitor.

Question 3

Using the following components: $R_1 = 10 \text{ k}\Omega$, $R_2 = 2 \text{ k}\Omega$, $V_{CC} = +15 \text{ V}$, and V_{in} as a 4 V peak-to-peak sine wave with no DC offset, we applied an external DC voltage source for V_{DC} . We varied V_{DC} between 0 and 5.5 V, observing V_{out} on the oscilloscope.

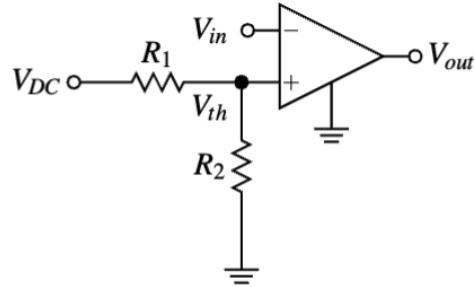


Figure 8.3: Comparator with reference voltage.

Figure 17

The waveforms below illustrate our observations. At $V_{DC} = 5.5 \text{ V}$, the threshold voltage V_{th} exceeds the amplitude of V_{in} . In the waveforms, V_{in} is shown in blue, while V_{out} and V_{th} are represented in yellow. The left set of waveforms displays V_{out} versus V_{in} , while the right set shows V_{th} versus V_{in} .

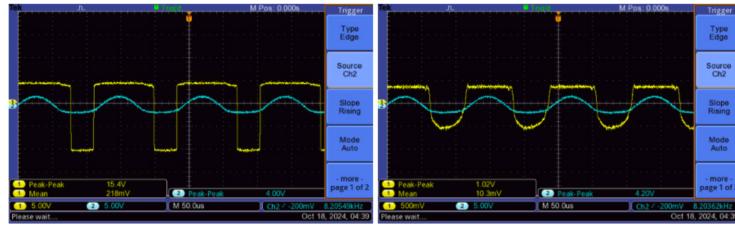


Figure 18: $V_{DC} = 0 \text{ V}$

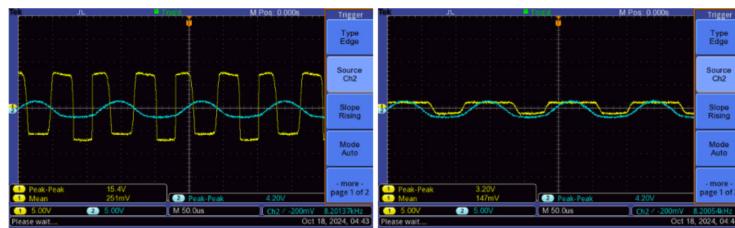


Figure 19: $V_{DC} = 5.5 \text{ V}$

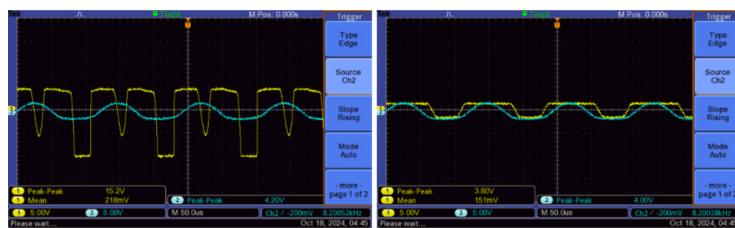


Figure 20: $V_{DC} = 2.3 \text{ V}$

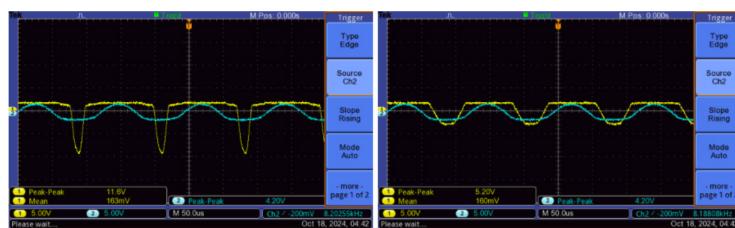


Figure 21: $V_{DC} = 3.2 \text{ V}$

Explanation of Graphs

$V_{DC} = 0 \text{ V}$: At this setting, the output voltage V_{out} (yellow) switches between high and low levels, correlating with the zero-crossing points of the input sine

wave V_{in} (blue). The threshold voltage V_{th} is relatively low, allowing the comparator to respond quickly to changes in V_{in} .

$V_{\text{DC}} = 5.5 \text{ V}$: Here, the threshold voltage V_{th} exceeds the amplitude of V_{in} . This results in V_{out} switching states only when V_{in} crosses this higher threshold, causing less frequent transitions. This demonstrates how a higher V_{DC} delays the comparator's response, reducing switching frequency.

$V_{\text{DC}} = 2.3 \text{ V}$: At this intermediate setting, V_{th} is higher than in the first case but lower than in the second. The switching frequency of V_{out} is also intermediate, showing delayed transitions compared to $V_{\text{DC}} = 0 \text{ V}$, but more frequent than at $V_{\text{DC}} = 5.5 \text{ V}$.

$V_{\text{DC}} = 3.2 \text{ V}$: For this value, the threshold voltage is balanced, and the waveform behavior reflects the stable transition points based on the intermediate threshold voltage.

Question 4

In this experiment, we measured the upper and lower threshold voltages for the comparator circuit with and without the feedback resistor R_3 .

Without R_3 :

- Lower threshold: $3.5 \text{ V } V_{\text{DC}}$
- Higher threshold: $5.0 \text{ V } V_{\text{DC}}$

With R_3 :

- Lower threshold: $2.2 \text{ V } V_{\text{DC}}$
- Higher threshold: $4.1 \text{ V } V_{\text{DC}}$

The following graphs illustrate the observed waveforms for both cases:



Figure 22: Without R_3 : Low Threshold ($V_{th} = 3.5$ V)

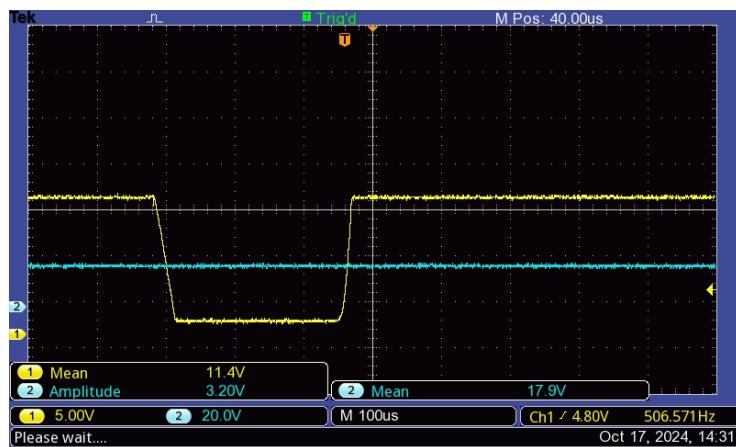


Figure 23: Without R_3 : High Threshold ($V_{th} = 5.0$ V)

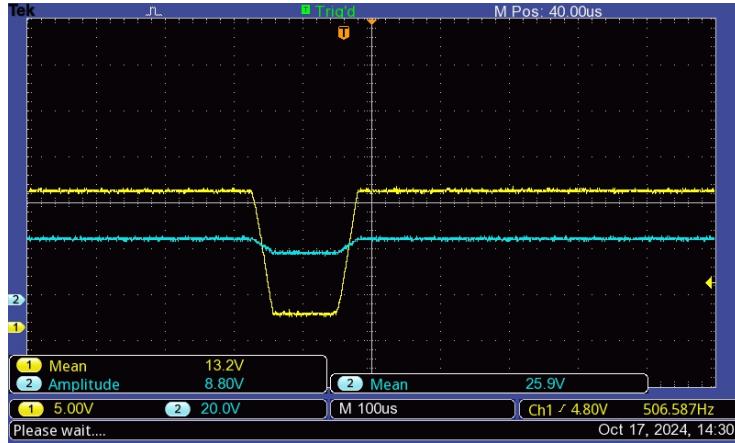


Figure 24: With R_3 : Low Threshold ($V_{th} = 2.2$ V)



Figure 25: With R_3 : High Threshold ($V_{th} = 4.1$ V)

Explanation of Graphs

Without R_3 :

- **Low Threshold ($V_{th} = 3.5$ V):**

The comparator switches its output state when the input voltage V_{in} crosses the lower threshold of 3.5 V. In the graph, V_{out} (yellow) transitions from high to low as V_{in} (blue) falls below this threshold. Without feedback, the switching is sharp and immediate, with no hysteresis present.

- **High Threshold ($V_{th} = 5.0$ V):**

Similarly, V_{out} switches from low to high when V_{in} exceeds the upper

threshold of 5.0 V. In the graph, we see a sharp transition as V_{in} crosses the threshold. The absence of hysteresis results in straightforward switching behavior.

With R_3 :

- **Low Threshold ($V_{th} = 2.2 \text{ V}$):**

Introducing the feedback resistor R_3 shifts the lower threshold to 2.2 V. The output V_{out} (yellow) switches from high to low only when V_{in} (blue) drops below this threshold. The hysteresis stabilizes the output, reducing sensitivity to noise and preventing frequent switching.

- **High Threshold ($V_{th} = 4.1 \text{ V}$):**

The feedback reduces the upper threshold to 4.1 V. V_{out} switches from low to high when V_{in} exceeds this threshold. The hysteresis introduces a “dead zone” between the two thresholds, enhancing noise immunity and reducing unnecessary toggling.

Summary:

Without R_3 , the comparator switches states sharply at the lower (3.5 V) and upper (5.0 V) thresholds, making it susceptible to noise. With R_3 , hysteresis is introduced, shifting the thresholds to 2.2 V and 4.1 V. This stabilizes the output, prevents rapid toggling, and improves performance in noisy environments by creating a memory effect.

Question 5

Using the same circuit as above with R_3 connected, we observed the hysteresis curve directly by connecting both the input and output of the circuit to the oscilloscope in XY mode. Channel 1 (horizontal axis) displayed the triangle wave input V_{in} , and Channel 2 (vertical axis) displayed the output V_{out} .

Initially, we observed the hysteresis curve using a triangle wave input with no DC offset. As we varied the DC offset, we noted the following behavior:

- When increasing the DC offset positively, the bottom line of the hysteresis loop was displayed.
- When decreasing the DC offset negatively, the top line of the hysteresis loop appeared.

This behavior shows that the hysteresis curve depends on the input signal’s relationship to the threshold voltages. Below are the screenshots from the oscilloscope in XY mode, illustrating the hysteresis behavior.

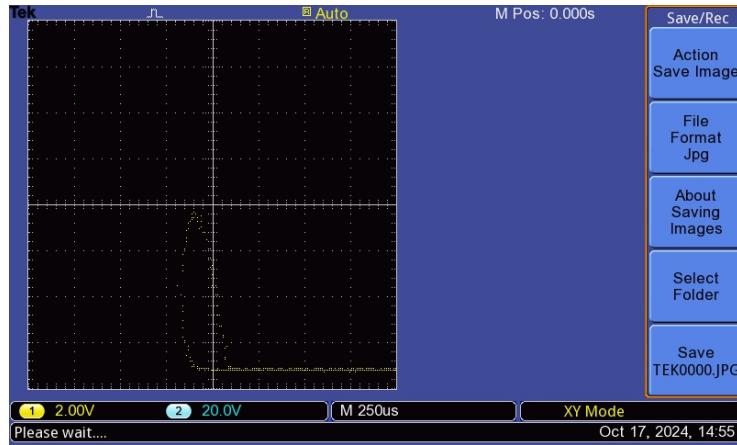


Figure 26: Hysteresis curve showing the bottom line when the DC offset is increased positively.

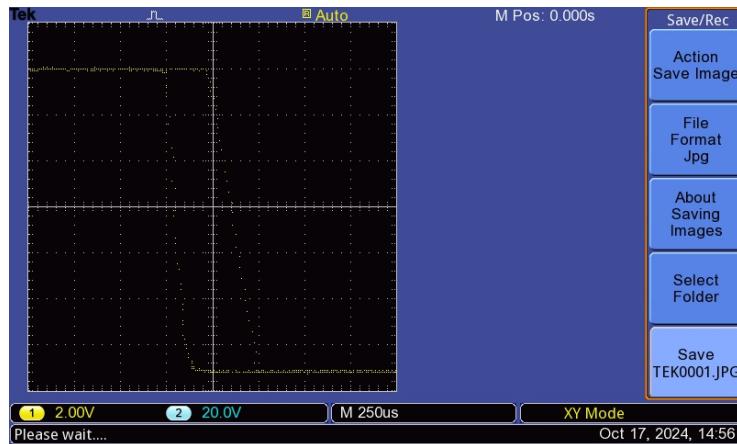


Figure 27: Hysteresis curve showing the top line when the DC offset is decreased negatively.

Explanation:

In XY mode, the hysteresis loop provides a visual representation of the input-output relationship of the Schmitt trigger. The curve shows how the output V_{out} changes state at different input voltages V_{in} due to the feedback resistor R_3 , which introduces hysteresis. By varying the DC offset, we could observe how the hysteresis loop behaves, highlighting the switching behavior of the comparator circuit. We see this loop on the graph as the input signal moves between the upper and lower thresholds, demonstrating the memory effect of the Schmitt trigger.

Question 6

Using our knowledge of RC circuits, as well as the op-amp rules:

1. The output attempts to do whatever is necessary to make the voltage difference between the two inputs zero.
2. The inputs draw no current.

We can relate V_{th} , V_{DC} , V_{out} , R_1 , R_2 , and R_3 in a single equation. According to Kirchhoff's law, the voltage at V_{th} equals V^+ . Therefore, we can write:

$$I_1 = \frac{V_{\text{DC}} - V_{\text{th}}}{R_1}, \quad I_2 = \frac{V_{\text{th}}}{R_2}, \quad I_3 = \frac{V_{\text{out}} - V_{\text{th}}}{R_3}$$

From rule (1), we know that $I_1 + I_3 = I_2$.

Substituting our current formulas into the above equation, we get:

$$\frac{V_{\text{DC}} - V_{\text{th}}}{R_1} + \frac{V_{\text{out}} - V_{\text{th}}}{R_3} = \frac{V_{\text{th}}}{R_2}$$

After simplifying, we derive the following equation for V_{th} :

$$V_{\text{th}} = \frac{R_2 R_3 V_{\text{DC}} + R_1 R_2 V_{\text{out}}}{R_1 R_2 + R_1 R_3 + R_2 R_3}$$

Using this equation, we can predict the threshold voltages from above. With $V_{\text{DC}} = 10 \text{ V}$ and V_{out} at its maximum ($\approx 15 \text{ V}$), we calculate the threshold for V_{out} to transition away from its maximum as $V_{\text{in}} = 4.52 \text{ V}$. This is close to our measured maximum threshold voltage of 4.96 V .

At V_{out} minimum ($\approx 1.5 \text{ V}$), using the formula for V_{th} , we find the transition occurs at $V_{\text{in}} = 2.89 \text{ V}$, which aligns closely with our measured minimum threshold voltage of 2.80 V .

A Schmitt trigger swaps V_{out} between high and low voltages, exhibiting hysteresis. This means the threshold for switching from low to high voltage ($V_{\text{th}-}$) is lower than the threshold for switching from high to low voltage ($V_{\text{th}+}$). Hysteresis helps prevent noise from causing random transitions, as significant changes in V_{in} are required to switch V_{out} back to its original state.

The hysteresis in a Schmitt trigger arises from positive feedback through R_3 . When V_{out} is high, V_{th} increases, raising the threshold voltage. Conversely, when V_{out} is low, V_{th} decreases, lowering the threshold voltage. This behavior stabilizes the circuit by preventing rapid toggling due to minor input fluctuations.

The mathematical reasoning is derived from rule (2), which ensures no current is drawn by the inputs. Rule (1) explains why V^+ is equal to V^- , leading to the observed switching behavior and the variation in V_{th} with V_{in} .

Question 7

For the final part of this lab, we were asked to construct the circuit shown in Figure 8.5, a relaxation oscillator using a TL071 op-amp.

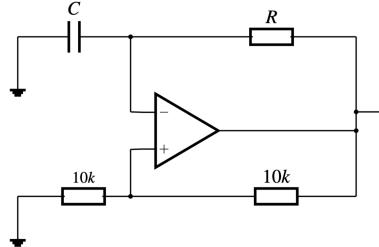


Figure 8.5: Relaxation Oscillator

Figure 28: Relaxation Oscillator Circuit

We varied the resistor R and capacitor C components and recorded the oscillations using an oscilloscope. The component values of R and C , along with the frequency of the resulting oscillation, are summarized in the table below.

C (nF)	R (k Ω)	f (kHz)
1.0	161	2.22
10.5	161	0.216
3.36	161	0.684
3.36	20.1	6.24
3.36	44.3	2.89
10.5	44.3	0.913
10.5	20.1	2.03
1.0	44.3	9.14
1.0	20.1	19.6

Table 4: Recorded values of C , R , and the resulting oscillation frequency f

From our data, we observed that the output frequency is inversely proportional to the product of R and C . In other words, the relationship can be described by the equation:

$$f = \frac{1}{RC}$$

This confirms the theoretical behavior of a relaxation oscillator, where the oscillation frequency depends on the time constant RC .

Lab 9: Operational Amplifiers III

Objective

The objective of this lab is to further explore the different kinds of circuits created using op-amps, including a gyrating circuit and an active notch filter.

Part I: Gyrating Circuits

The first question asks us to recreate the circuit shown below in Fig. 1a using a TL071 op-amp. We use our breadboard to set up two external voltage sources as $V_{CC} = +15V$ and $V_{EE} = -15V$. Our capacitor value is 10nF , and both R_L and R_I are set equal to $1\text{k}\Omega$.

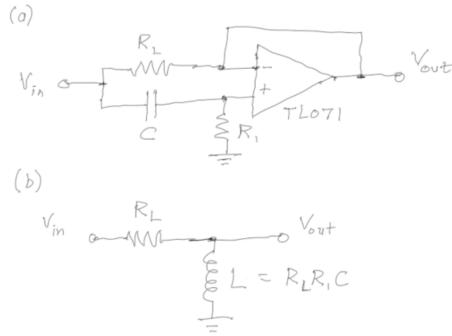


Figure 1. (a) Gyrator circuit. (b) Equivalent circuit to the gyrator.

Figure 29: Gyrator circuit

Below is the recorded data showing $V_{0,out}$, $V_{0,in}$, and the phase shift ϕ at various frequencies:

f (Hz)	$V_{0,\text{out}}$ (V)	$V_{0,\text{in}}$ (V)	Phase shift (°)
400	0.160	4.6	100
1k	0.368	4.6	88
4k	1.26	4.64	76.5
10k	2.66	4.64	54.8
50k	4.48	4.64	14.9
80k	4.6	4.68	7.59
100k	4.64	4.64	5.03
150k	4.72	4.72	1.62
200k	4.72	4.72	0
300k	4.72	4.72	-4.46
400k	4.72	4.72	-7.94

Table 5: Recorded data for gyrator circuit

Below are plots of both gain ($V_{0,\text{out}}/V_{0,\text{in}}$) and phase shift (ϕ) plotted as functions of frequency:

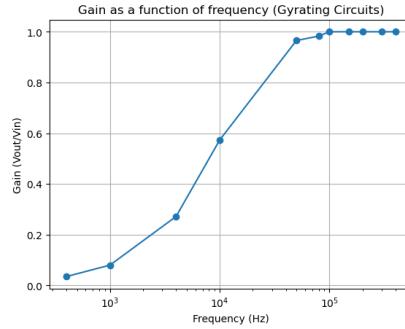


Figure 30: Gain as a function of frequency

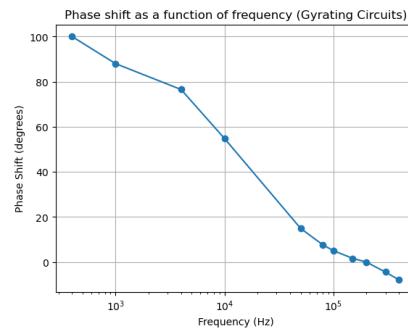


Figure 31: Phase shift as a function of frequency

To verify these dependencies, we compare the gain and phase shift of the gyrating circuit with a simple RL circuit as shown below:

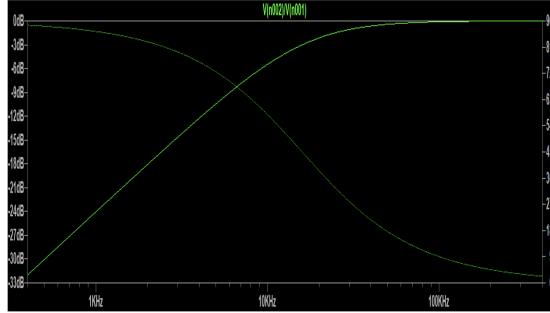


Figure 32: Simulation of RL Circuit showing gain and phase vs frequency

From this we can see that the gyrating circuit has a gain that increases with frequency, while the phase shift decreases with frequency. This is opposite to the behavior of the RL circuit, which has a gain that decreases

Explanation of Graphs for FYR 1

Yes, it makes sense that these circuits will behave differently with gain versus frequency due to their distinct configurations and the components involved. The gyrator circuit, which simulates inductance using a capacitor and operational amplifier, exhibits frequency-dependent behavior. As the frequency increases, the gain and phase shift change significantly. This is attributed to the circuit's design, where the reactive components (capacitor and simulated inductance) determine the impedance and thus influence the gain and phase response over varying frequencies.

Part II: Active Notch Filter

The second part involves recreating the circuit shown in Fig. 3 using a TL071 op-amp. We use $V_{CC} = +15V$, $V_{EE} = -15V$, $C = 10\text{nF}$, and all resistors set to $1\text{k}\Omega$. The notch frequency is calculated as $f_{\text{notch}} = \frac{1}{2\pi RC} \approx 16\text{kHz}$.

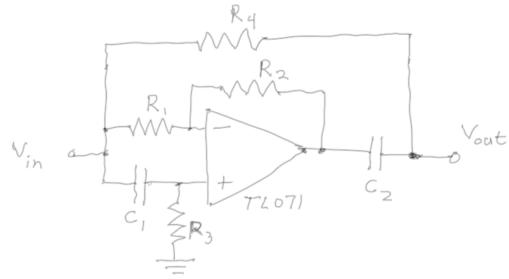


Figure 3. Active notch filter circuit.

Figure 33: Active Notch Filter circuit

The recorded data showing $V_{0,\text{out}}$, $V_{0,\text{in}}$, and phase shift ϕ at various frequencies are presented below:

f (Hz)	$V_{0,\text{out}}$ (V)	$V_{0,\text{in}}$ (V)	Phase shift (°)
1k	4.6	4.6	-8.35
5k	3.68	4.6	-37.6
8k	2.56	4.52	-55.2
10k	1.76	4.48	-65.9
13k	0.680	4.48	76.5
15k	0.200	4.52	106
16k	0.360	4.44	78.6
19k	1.12	4.48	73.4
22k	1.68	4.48	65.4
28k	2.6	4.52	54.3
50k	3.88	4.6	-8.61
164	4.6	4.6	30

Table 6: Recorded data for Active Notch Filter

Below is a plot of the gain ($V_{0,\text{out}}/V_{0,\text{in}}$) as a function of frequency:

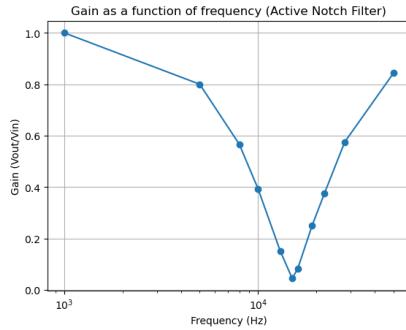


Figure 34: Gain as a function of frequency

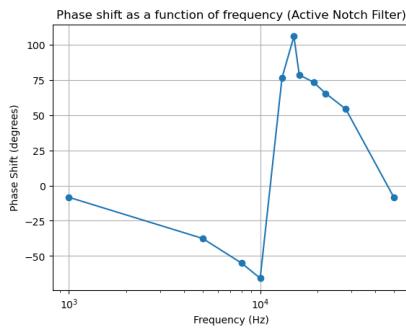


Figure 35: Gain as a function of frequency

The notch filter effectively blocks frequencies near $f_{\text{notch}} \approx 16 \text{ kHz}$ with a bandwidth from approximately 10kHz to 19kHz. The phase shift behavior is also recorded for various frequencies.