Lab Report 2: Lab 4-6

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Lab 4: Diodes

Important Concepts

- **Diode**: A semiconductor device that allows current to flow in one direction only. It has two terminals: an anode (+) and a cathode (-).
- **Voltage Divider**: A circuit used to create a voltage less than or equal to the input voltage.
- **Diode Forward Voltage Drop**: Typically around 0.7V for silicon diodes.
- **Zener Diode**: Designed to operate in reverse bias, with a specified breakdown voltage.

Equations

- **Diode Equation**:

$$I = I_s \left(e^{\frac{V}{nV_T}} - 1 \right)$$

- **Voltage Divider**:

$$V_{out} = V_{in} \cdot \frac{R_2}{R_1 + R_2}$$

- **Ripple Voltage**:

$$V_{ripple} = \frac{I_{load}}{fC}$$

0.1 FYR Questions

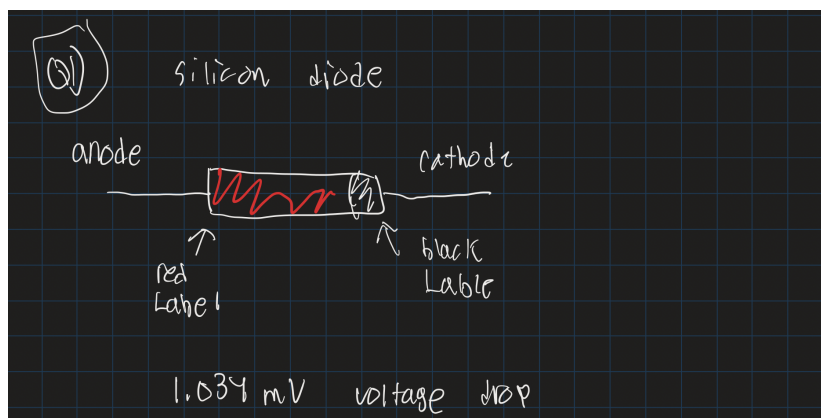1. **Diode Identification and Voltage Drop:**

Figure 1: Drawing of Diode

2. **Diode Circuits:** The diode behaves like a switch; it is on when forward-biased (Vin ¿ 0.7V), and off otherwise.

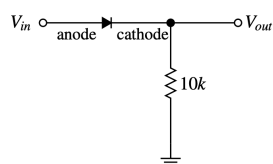The Yellow line represents the Vin, the Blue line represents the Vout.
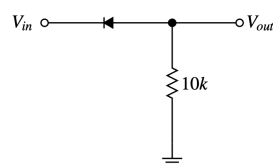

Figure 4.1: Diode Circuit 1.

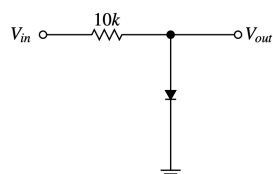Figure 4.2: Diode Circuit 2.

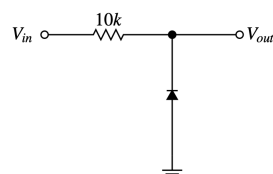Figure 4.3: Diode Circuit 3.

Figure 4.4: Diode Circuit 4.
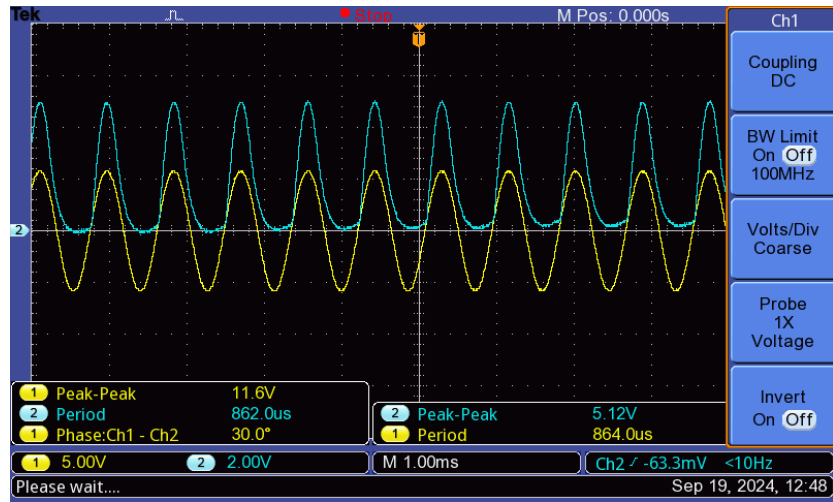
Figure 2: Circuits For This Question

Figure 3: Circuit 1 Results

Description: A forward-biased diode in series with a resistor.

Expected Behavior: The diode will conduct (be "on") when the input voltage Vin is greater than the forward voltage of the diode (about 0.7V for a silicon diode). When the input drops below 0.7V, the diode will be off, and Vout will be near zero.

Oscilloscope Data: In the graph, you can see that the yellow waveform (Vin) is sinusoidal, and the blue waveform (Vout) shows clipping at approximately 0.7V, confirming that the diode only conducts when Vin¿0.7V.
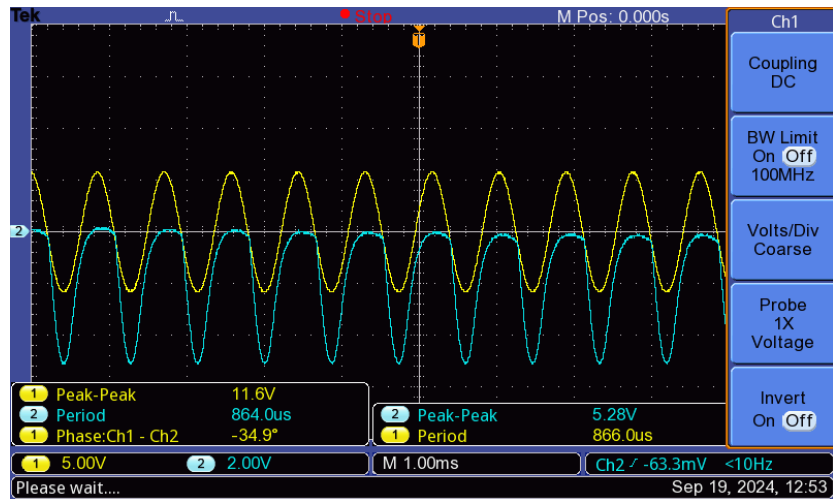

Figure 4: Circuit 2 Results

Description: A reverse-biased diode in series with a resistor.

Expected Behavior: In this case, the diode will not conduct under normal forward voltage conditions, as it is reverse-biased. Hence, Vout will be almost zero throughout the entire cycle of = Vin.

Oscilloscope Data: The second graph shows that the blue waveform (Vout) is almost flat, indicating the diode is not conducting, as expected for a reverse-biased diode.
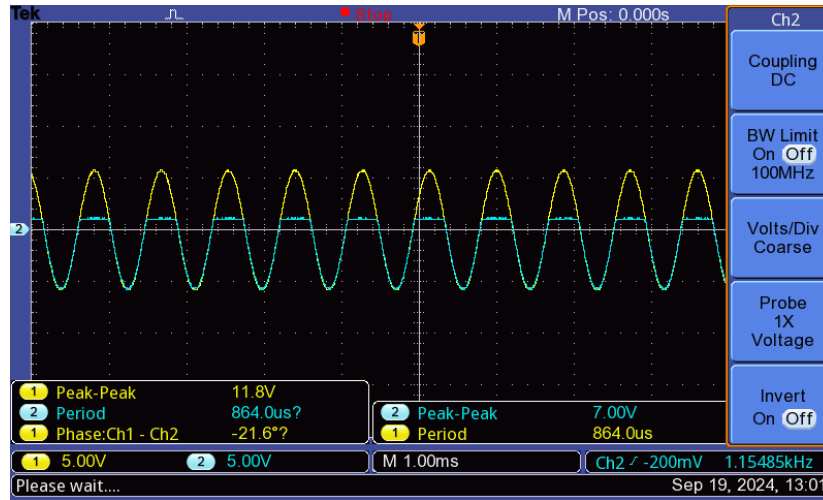
Figure 5: Circuit 3 Results

Description: A forward-biased diode, with the diode grounded.

Expected Behavior: Similar to Circuit 1, but this time, the diode is connected to the ground. The output Vout will be clamped at 0.7V during the positive cycle of Vin, and the diode will conduct when ¿ 0.7V. Vin¿0.7V.

Oscilloscope Data: In the third graph, the blue waveform again shows clipping at around 0.7V, indicating that the diode is conducting when Vin¿0.7V, and is off otherwise.

Figure 6: Circuit 4 Results

Description: A reverse-biased diode, similar to Circuit 2 but with reversed polarity.

Expected Behavior: The diode will not conduct during the positive cycles of Vin, but it may conduct slightly during negative cycles if the reverse breakdown voltage is reached. However, for most practical situations, the output will be near zero.

Oscilloscope Data: The fourth graph shows minimal activity on the blue waveform (Vout), confirming that the diode remains off, as expected for a reverse-biased diode.s
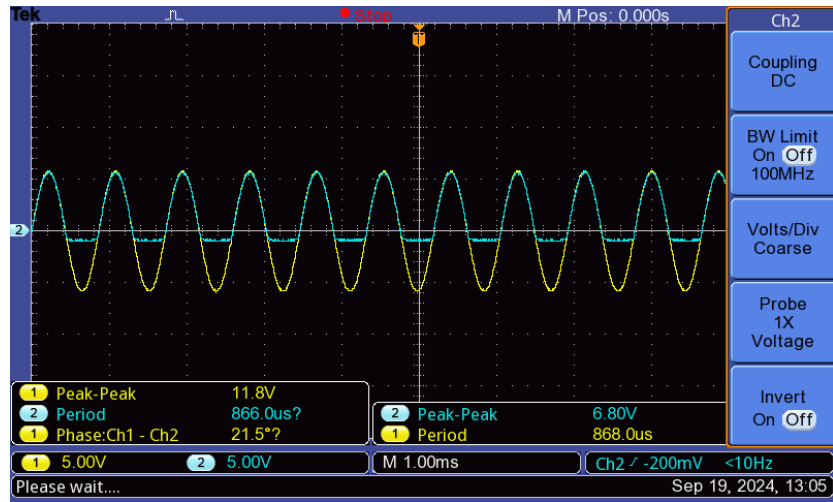
3.**Voltage Clamp Circuit:** Adjusting the +1V shifted the output. The diode was **on** when Vin exceeded the forward voltage and bias.

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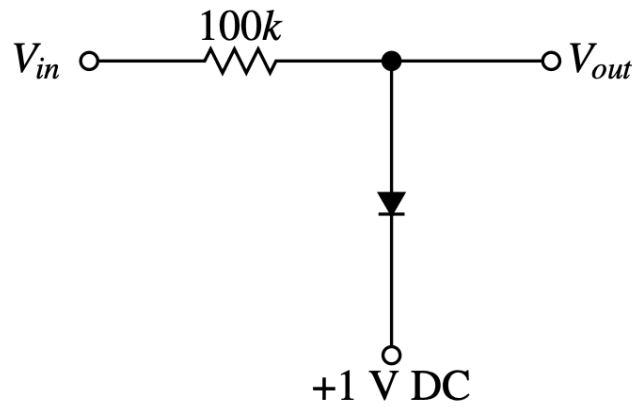Figure 7: Circuit For Question 3
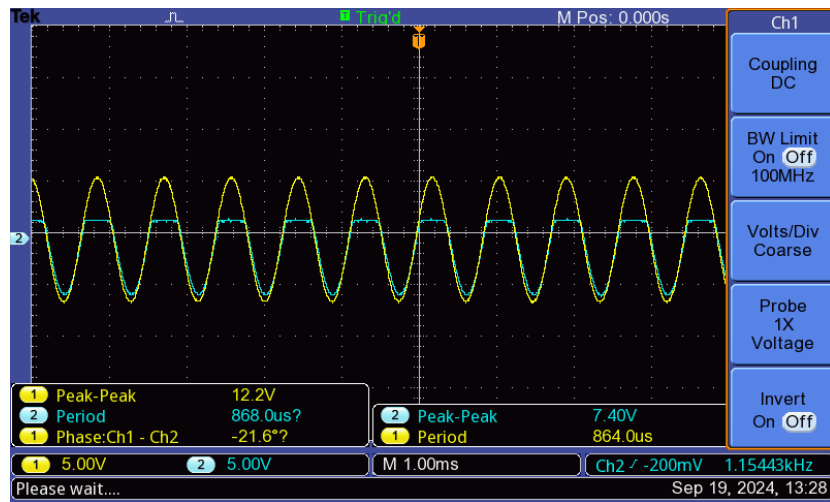

Figure 8: Circuit with +1V Shift. We can see that on Vout we are seeing a 1V shift will keeping the negative cycle.
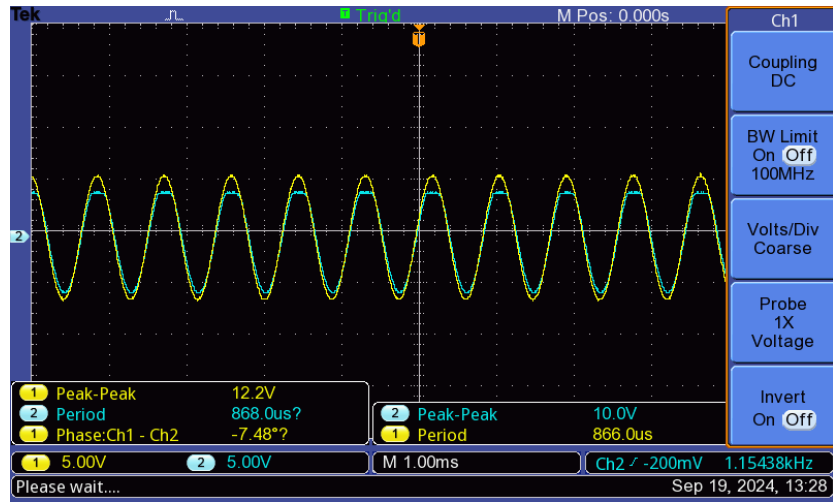
Figure 9: Circuit with 3.5V Shift. We can see that on Vout we are seeing a 3.5V shift will keeping the negative cycle.

4.**Two Diode Circuit** Sketched regions where D1 and D2 were on and off, showing rectification.
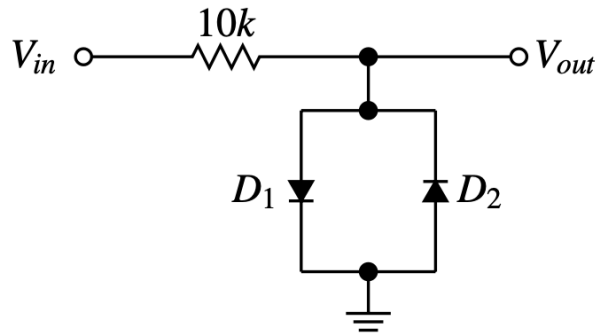
Figure 10: Circuit for Question 4
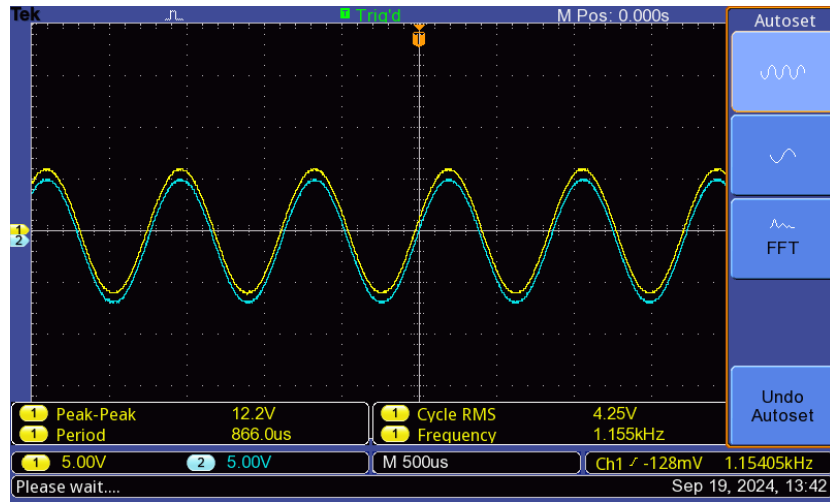
Figure 11: Circuit Results

Explanation of Diode Behavior: D1 (Forward Biased): When the input signal is positive, D1 conducts and the output voltage is clamped near 0.7V. D2 (Forward Biased): When the input signal is negative, D2 conducts and the output is clamped near -0.7V.

Regions of On and Off States: D1 is on during the positive half-cycle of the input waveform when Vin $\geq$ 0.7V. D2 is on during the negative half-cycle of the input waveform when Vin$\leq$-0.7V. During these times, the output is clamped to the diode's forward voltage, limiting the maximum and minimum values of Vout.

5.**Ripple and DC** The plot of $VDC/Vripple$ versus R indicated a smoother rectification with higher resistance.
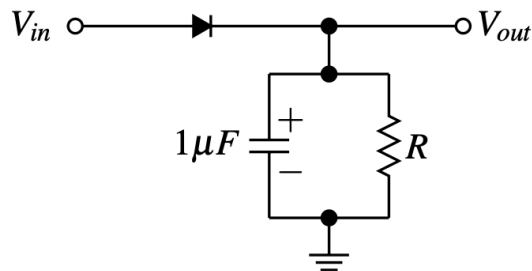
Figure 12: Circuit For Question 5

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Question 5

We used a capacitor with a capacitance of $C = 0.94\,\mu F$ and resistances of $R_1 = 106.4\,k\Omega$ and $R_2 = 48.7\,k\Omega$. The circuit was set at a frequency of 1.5 kHz.

The ripple voltage V_{ripple} is defined as:

$$V_{ripple} = V_{\max} - V_{\min}$$

The DC voltage V_{DC} is given by:

$$V_{DC} = \frac{V_{\max} + V_{\min}}{2}$$

We recorded the following values for different resistances:

Filtering Resistance (R)	V_{ripple} (V)	V_{DC} (V)
100 kΩ	0.6	4.44
50 kΩ	0.4	4.76
10 kΩ	0.2	4.86
5 kΩ	0.8	4.2
200 Ω	3.4	1.51
500 Ω	3.0	2.32

Table 1: Measured ripple voltage V_{ripple} and DC voltage V_{DC} for different filtering resistances.
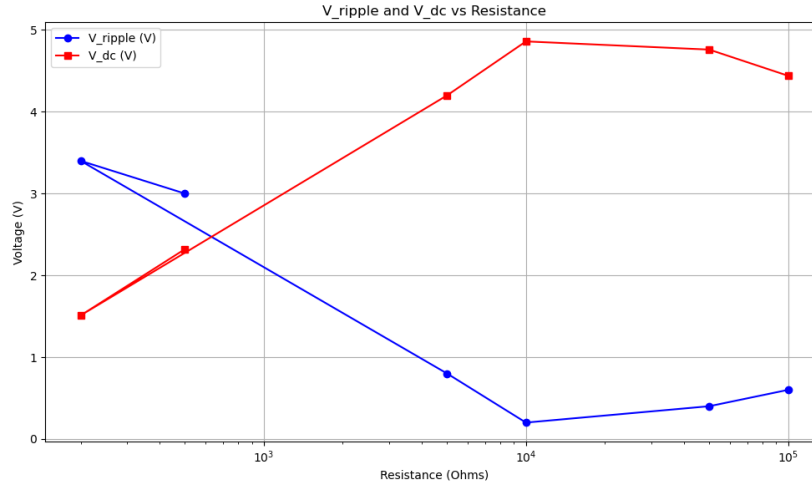
Figure 13: Graph of $VDC/Vripple$ versus R

6.**I-V Curve of Zener Diode**: The Zener diode conducted in reverse once the 5V breakdown voltage was reached.
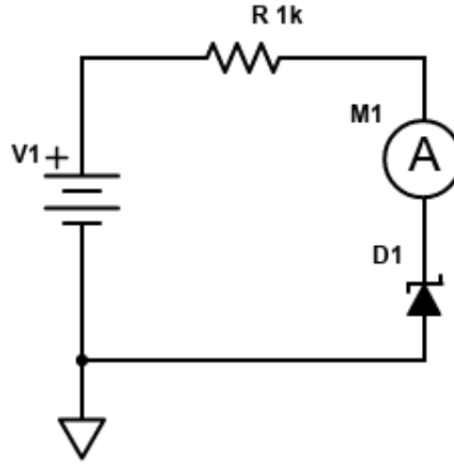
Figure 14: Graph of $VDC/Vripple$ versus R

We used a Zener diode with a forward voltage of 0.702V. The resistor was set at $R = 47.6\,k\Omega$. The goal was to limit the current to 50 mA.

From Ohm's law:

$$R = \frac{V}{I} = \frac{5\,\text{V}}{0.05\,\text{A}} = 100\,\Omega$$

Measured I-V Data: The following table presents the measured current for different voltage values across the Zener diode.

V (Volts)	I (Amperes)
1.0	2.6 mA
2.0	9.8 mA
3.0	19.6 mA
4.0	28.6 mA
5.6	36.1 mA
6.0	46.5 mA
7.0	55.6 mA
8.0	63.5 mA
9.0	73.1 mA
10.0	82.1 mA
15.0	125.1 mA
19.0	145.1 mA

Maximum Current: The maximum current measured was 145.1 mA at 19V.
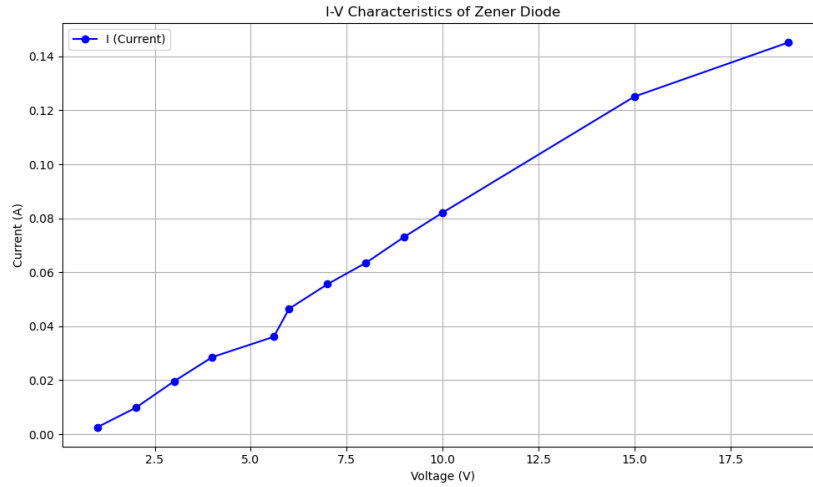
Figure 15: Graph of $VDC/Vripple$ versus R

Lab 5: BPJ Transistors

Important Concepts

- **Bipolar Junction Transistor (BJT)**: A type of transistor that uses both electron and hole charge carriers. - **NPN and PNP Transistors**: These are two types of BJTs. In NPN, current flows from the collector to the emitter when the base is forward biased. In PNP, the current flows in the opposite direction. - **Current Gain** (β): Defined as the ratio of the collector current (I_C) to the base current (I_B).

$$\beta = \frac{I_C}{I_B}$$

- **Saturation Voltage** ($V_{CE(sat)}$): The minimum collector-emitter voltage where the transistor is still in the active mode.

Equations

- **Collector Current**:

$$I_C = \beta I_B$$

- **Saturation Voltage**:

$$V_{CE(sat)} \approx 0.2\,\text{V}$$

- **Transistor Current Relations**:

$$I_E = I_C + I_B$$

where I_E is the emitter current.

FYR Questions

1. **Transistor Diode Drops**: We measured the diode drops for different transistors using the diode setting on a multimeter. Below are the measured forward voltage drops for each transistor:

- **3904 (PNP)**: 0.697 V drop

- **3906 (NPN)**: 0.700 V drop

- **2N2222 (PNP)**: 0.652 V drop

Explanation: The measured voltage drops correspond to the forward voltage required to turn on the diode within the transistor, which is typically between 0.6V and 0.7V for silicon-based devices. Here's an explanation for each:

- **PNP Transistors (3904 and 2N2222)**: The forward voltage drop for these PNP transistors is approximately 0.697V and 0.652V respectively. This value is close to the typical forward voltage for silicon-based diodes (0.7V). The slightly lower value for the 2N2222 may be due to manufacturing variations or slight differences in the materials used.

- **NPN Transistor (3906)**: The NPN transistor shows a forward voltage drop of 0.700V, which aligns well with the typical forward voltage for silicon diodes. This is the voltage required to forward bias the base-emitter junction of the transistor.

These small differences in voltage drop can be attributed to the variations in the semiconductor materials or the specific doping levels used in each transistor. However, all values fall within the expected range for silicon-based BJTs.

2. **Transistor Circuit Measurements**:

In this question, we analyzed two cases with different base currents. Below are the measured results for both Case A and Case B.

Case A:
For Case A, we set the following parameters:

- $R_B = 200\,k\Omega$

- $R_C = 2\,k\Omega$

- $V_{CC} = 10\,V$

- $I_B = 20\,\mu A$

The base current I_B was set to 20 μA, and we varied V_{CC} to measure the corresponding collector current I_C and the collector-emitter voltage V_{CE}. The results are shown in the table below:

V_{CC} (V)	I_C (μA)	V_{CE} (mV)
10.0	1.0	-915
9.0	0.9	-805
8.0	0.8	-720
6.8	0.7	-625
6.0	0.7	-563
5.0	0.6	-494
4.0	0.5	-384
3.5	0.5	-36
1.5	0.3	-28
1.0	0.2	-25
0.0	0.1	-22.8

Case B:
For Case B, we set the following parameters:

- $R_B = 100\,\Omega$

- $R_C = 2\,k\Omega$

- $V_{CC} = 10\,V$

- $I_B = 40\,\mu A$

The base current I_B was set to 40 μA, and we varied V_{CC} to measure the corresponding collector current I_C and the collector-emitter voltage V_{CE}. The results are shown in the table below:

V_{CC} (V)	I_C (μA)	V_{CE} (mV)
9.7	1.0	-957
8.5	0.9	-834
7.4	0.8	-721
6.0	0.6	-586
5.0	0.6	-461
4.0	0.5	-39
2.7	0.4	-28
2.0	0.3	-24
1.0	0.2	-25
0.0	0.1	-28

Analysis:
- As V_{CC} decreases, the collector current I_C decreases in both cases, but I_C is larger in Case B due to the higher base current.

- The collector-emitter voltage V_{CE} also decreases and becomes less negative, especially in Case A, as the transistor approaches saturation.
- In Case B, saturation occurs at a higher I_C due to the larger base current, indicating the higher current gain (β) in Case B.
- Biggest drop happend around 3.5V, where V_{CE} dropped from -384mV to -36mV. This is likely due to the transistor entering saturation mode, where the collector current is nearly constant and the voltage drop across the collector-emitter junction is minimized.
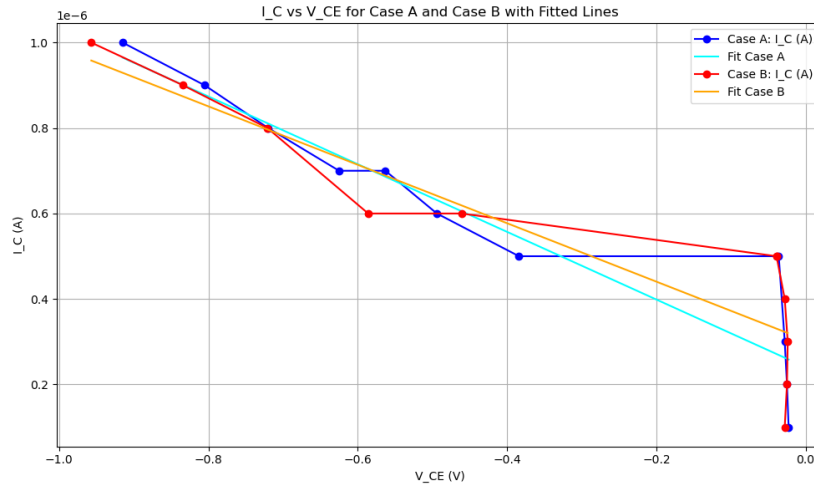
Graph:

Figure 16: I_C vs V_{CE} Plot, with fit function for measured data

3. **Saturation Voltage and Current Gain**:
Case A:
- Base current $I_B = 20\,\mu A$
- The estimated saturation voltage for Case A is:

$$V_{CE(sat)} \approx -25\,\text{mV}$$

- The current gain β for Case A was calculated using $\beta = \frac{I_C}{I_B}$. The values of β increase with V_{CE}, reaching higher values before flattening out as the transistor approaches saturation.

Case B:
- Base current $I_B = 40\,\mu A$
- The estimated saturation voltage for Case B is:

$$V_{CE(sat)} \approx -28\,\text{mV}$$

- The current gain β for Case B is higher than Case A, indicating greater amplification due to the increased base current.

Conclusion: From the plots, we can see that both transistors enter saturation at approximately similar values of $V_{CE(sat)}$, with Case B showing a slightly higher β due to the higher base current. These results align with the expected behavior of the transistor in active and saturation regions.

4. **Collector Current vs Base-Emitter Voltage**: - Use the Ebers-Moll equation to describe the relationship between collector current and base-emitter voltage:

$$I_C = I_S \left(e^{\frac{V_{BE}}{kT}} - 1 \right)$$

- Plot I_C vs V_{BE} on a logarithmic scale.

5. **Sine Wave Amplification**: - Sketch and describe the voltage behavior for the transistor in the circuit for both small and large input signals.

6. **Undistorted Sine Wave**: - Report the DC offset and amplitude you used to produce an undistorted sine wave.