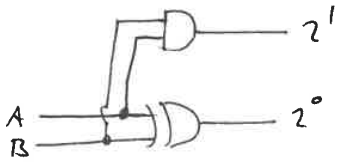
Flip Flops 1 handout

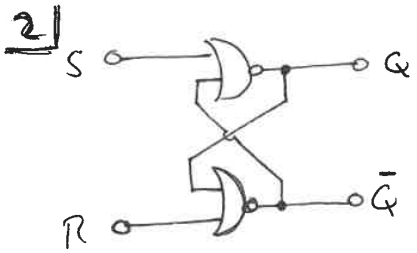
1

A	B	A+B
0	0	0 0
0	1	0 1
1	0	0 1
1	1	1 0

↑ AND 2^1 ↑ XOR 2^0



2



NOR

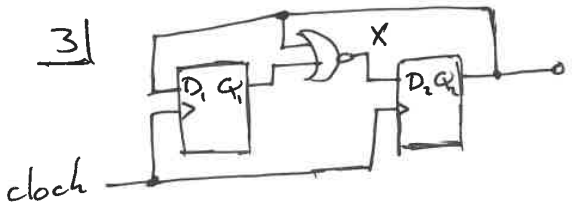
A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

Assume Q starts low and R and S start low
=> $\bar{Q}$ starts high!

S changed to high: Q stays low, $\bar{Q}$ stays high
S changed back to low: Q stays low, $\bar{Q}$ stays high
R changed to high: $\bar{Q}$ goes low, Q goes high.
R changed back to low: $\bar{Q}$ stays low, Q stays high
S changed to high: Q goes low $\bar{Q}$ goes high

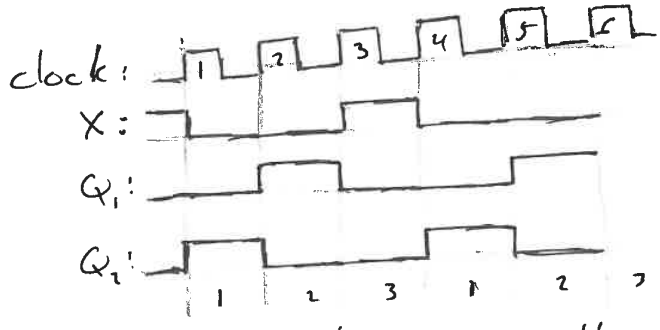
so changing R to high saves bit, S resets.
so diagram labeled bad! flip S↔R and acts like our NAND SR latch with changing 0→1 doing the action changing 1→0 on NAND created changes

3



D	Q
0	0
1	1

Q changes on + edge clock!
Assume Q_1 and Q_2 start low
NOR gates flips immediately!
D flop changes based on what D was!



divide by 3 circuit!!

X (NOR) changes immediately when either Q_1 or Q_2 go high
Q_2 changes depending on X at instant clock has goes +
Q_1 changes depending on Q_2 at instant clock goes +