# Processors & Pipelines

Important concepts from CS:APP 4.4

**These slides adapted from materials provided by the textbook authors.**

# Real-World Pipelines: Car Washes

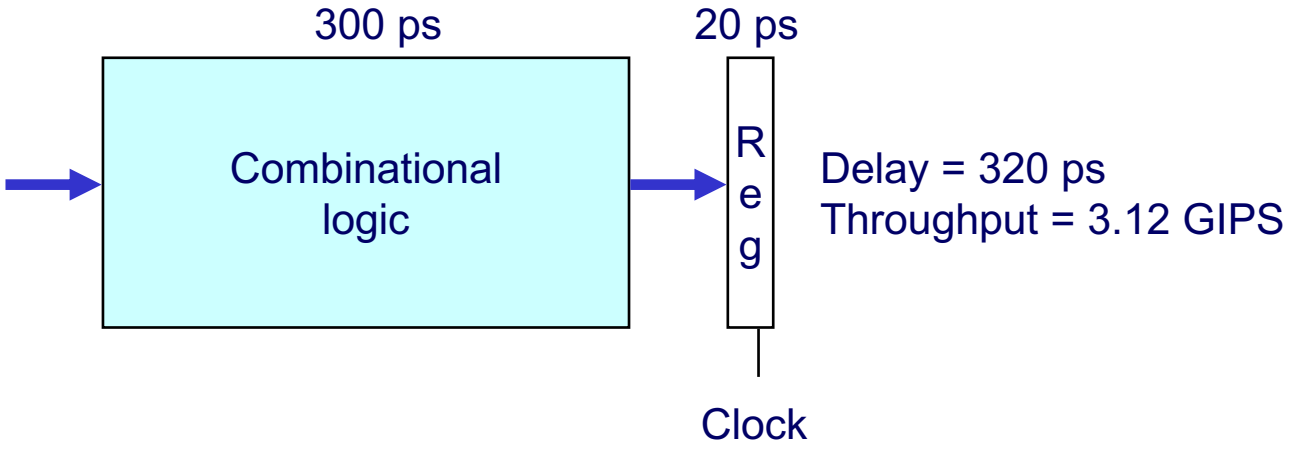
**Sequential**


**Parallel**

**Pipelined**

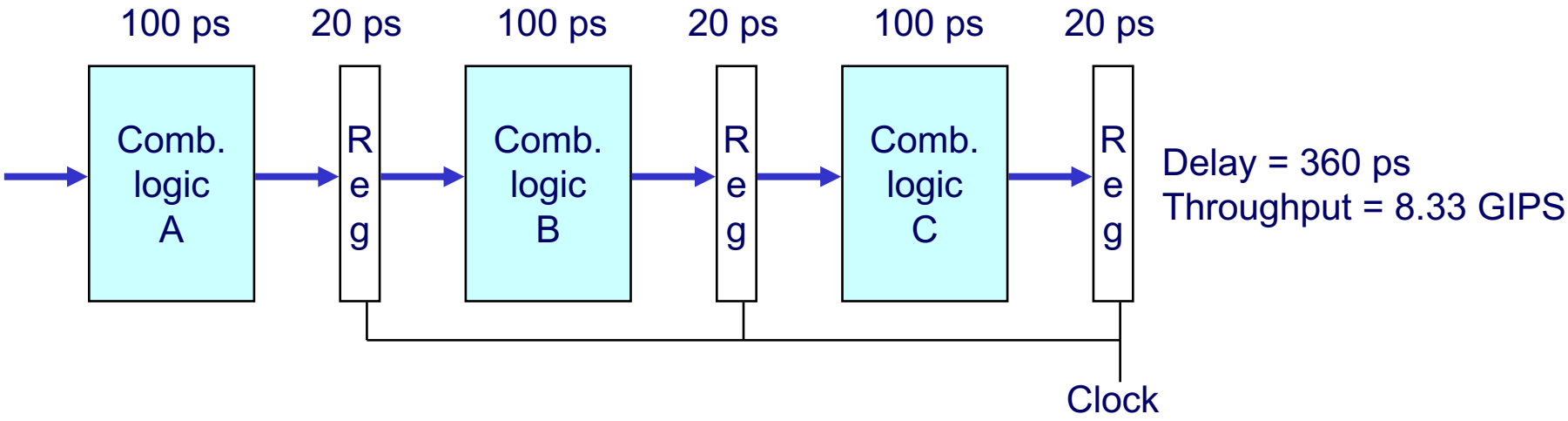
- **Idea**
  - Divide process into independent stages
  - Move objects through stages in sequence
  - At any given times, multiple objects being processed

# Computational Example




- **System**
  - Computation requires total of 300 picoseconds
  - Additional 20 picoseconds to save result in register
  - Must have clock cycle of at least 320 ps

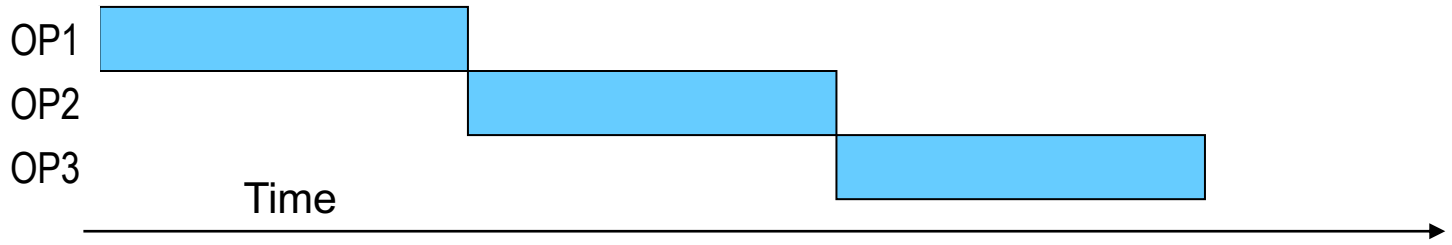
# 3-Way Pipelined Version




- **System**
  - Divide combinational logic into 3 blocks of 100 ps each
  - Can begin new operation as soon as previous one passes through stage A.
    - Begin new operation every 120 ps
  - Overall latency increases
    - 360 ps from start to finish

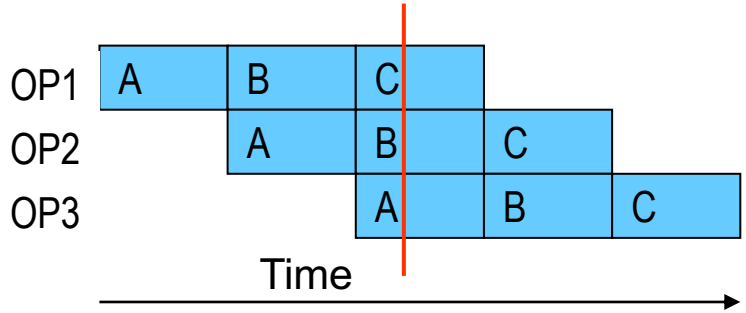
# Pipeline Diagrams

- **Unpipelined**



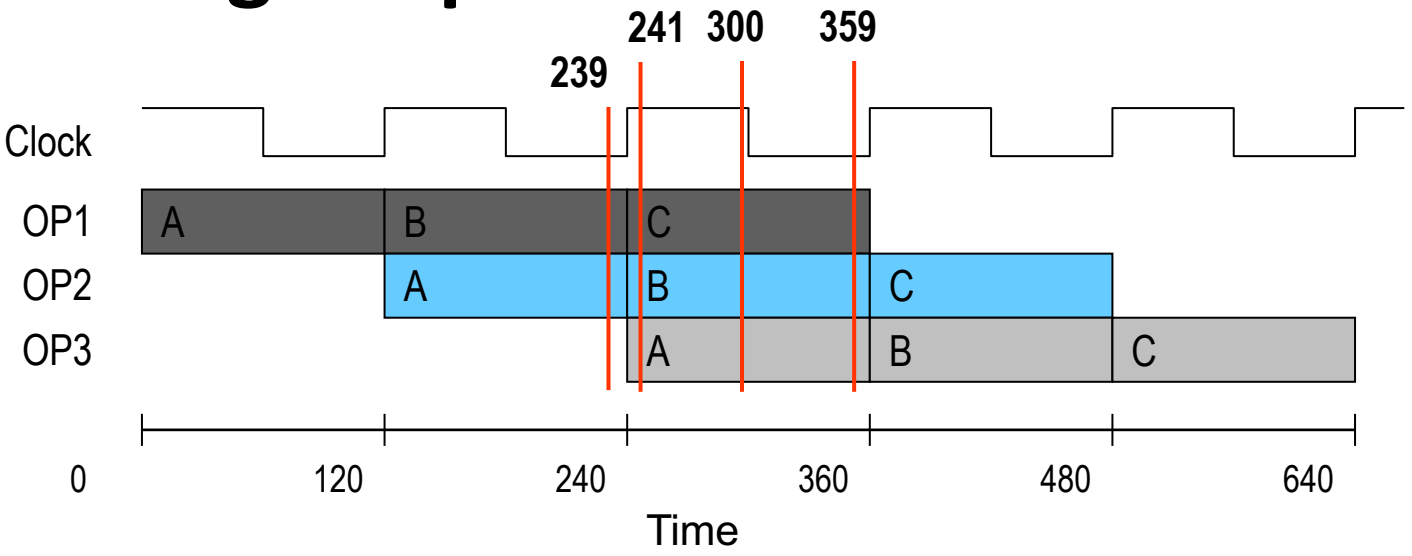

  - Cannot start new operation until previous one completes

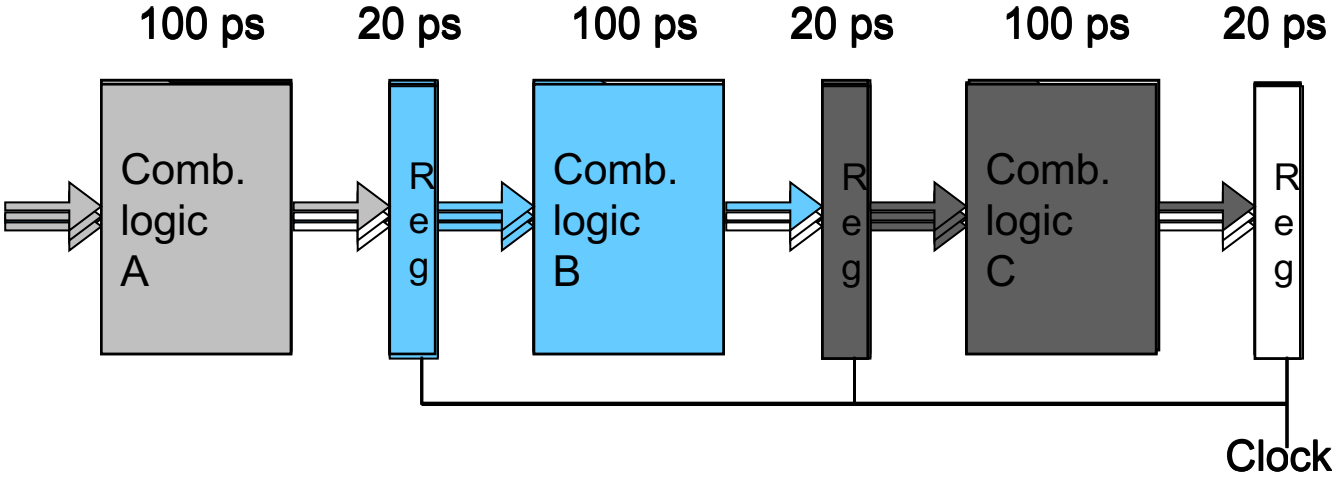
- **3-Way Pipelined**



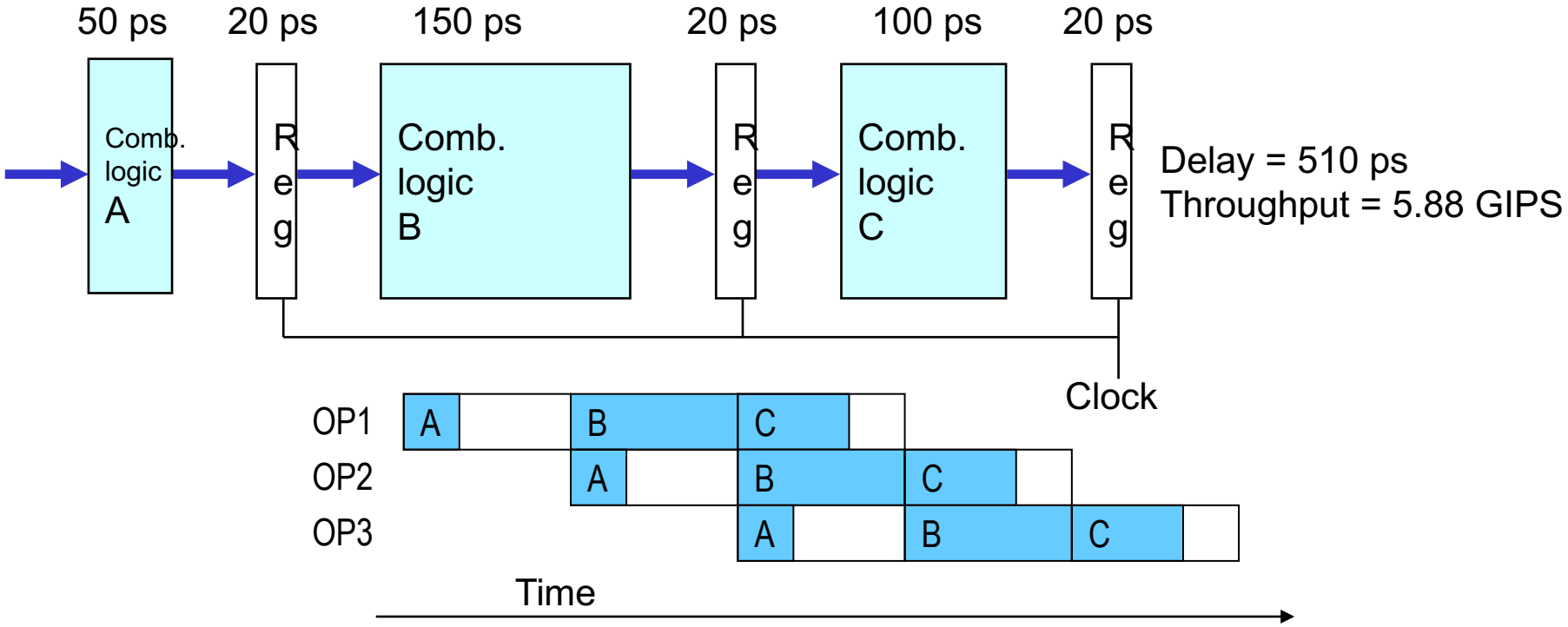

  - Up to 3 operations in process simultaneously

# Operating a Pipeline



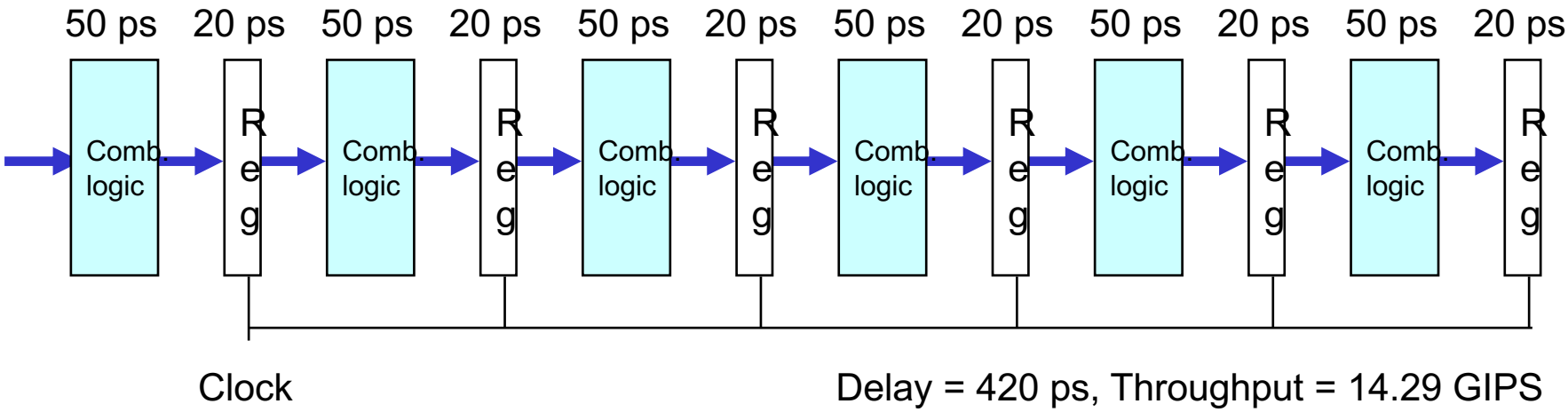



# Limitations: Nonuniform Delays




- Throughput limited by slowest stage
- Other stages sit idle for much of the time
- Challenging to partition system into balanced stages

# Limitations: Register Overhead




- As try to deepen pipeline, overhead of loading registers becomes more significant
- Percentage of clock cycle spent loading register:
  - 1-stage pipeline: 6.25%
  - 3-stage pipeline: 16.67%
  - 6-stage pipeline: 28.57%
- High speeds of modern processor designs obtained through very deep pipelining