Department of Computer Science
UNIVERSITY OF COLORADO BOULDER

Design and Analysis of Operating Systems CSCI 3753

Dr. David Knox
University of Colorado Boulder

These slides adapted from materials provided by the textbook authors.

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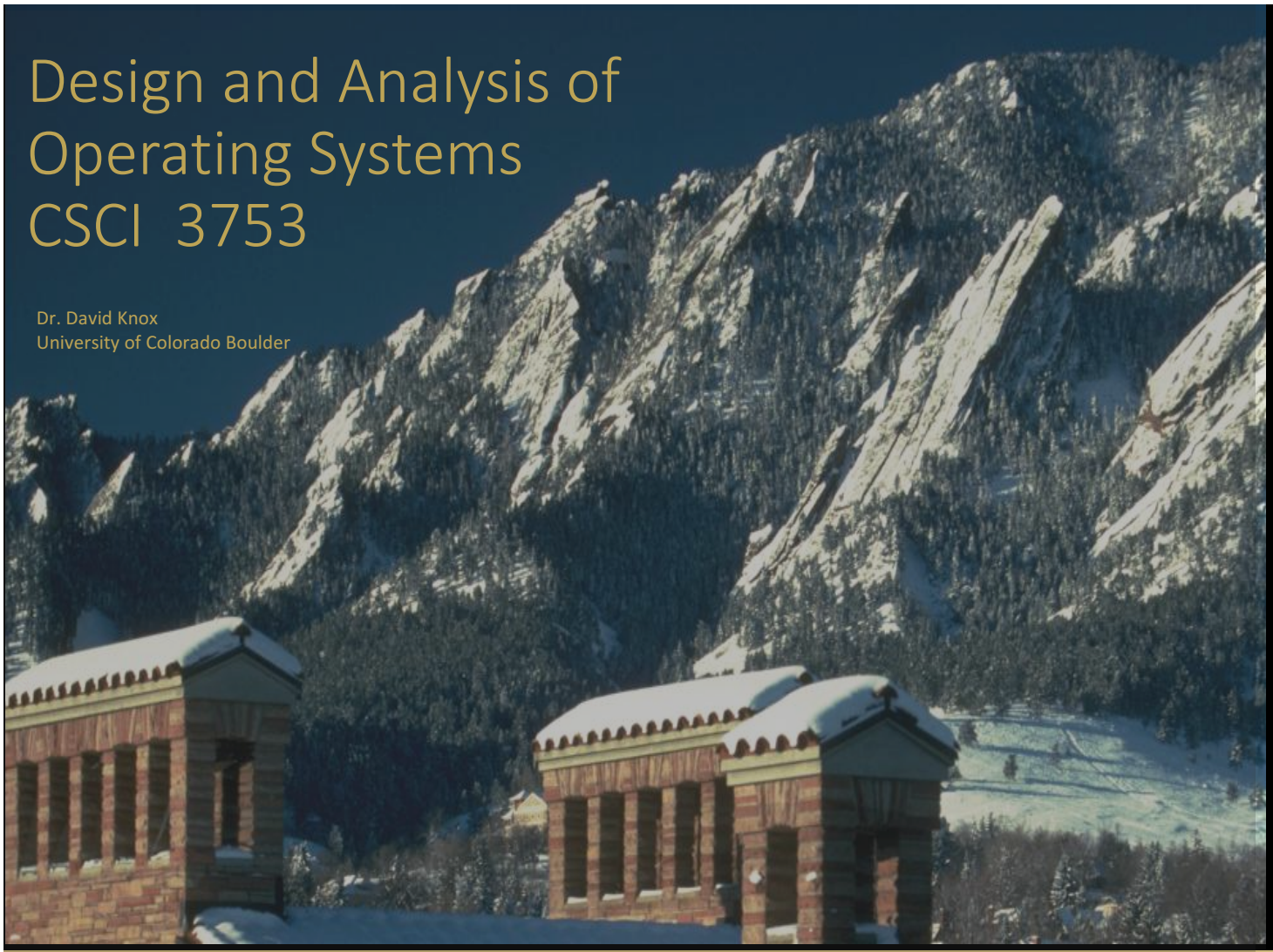

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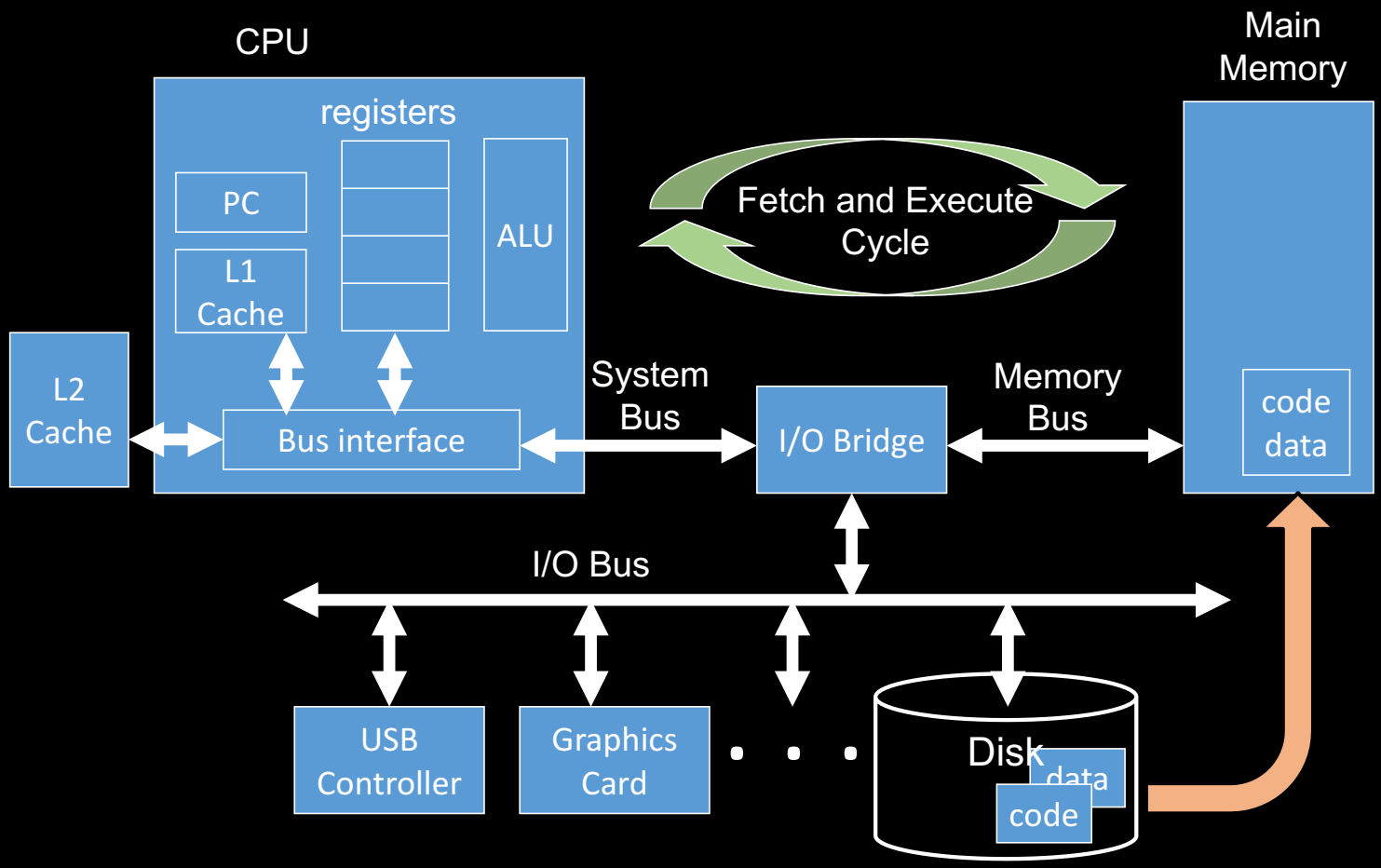
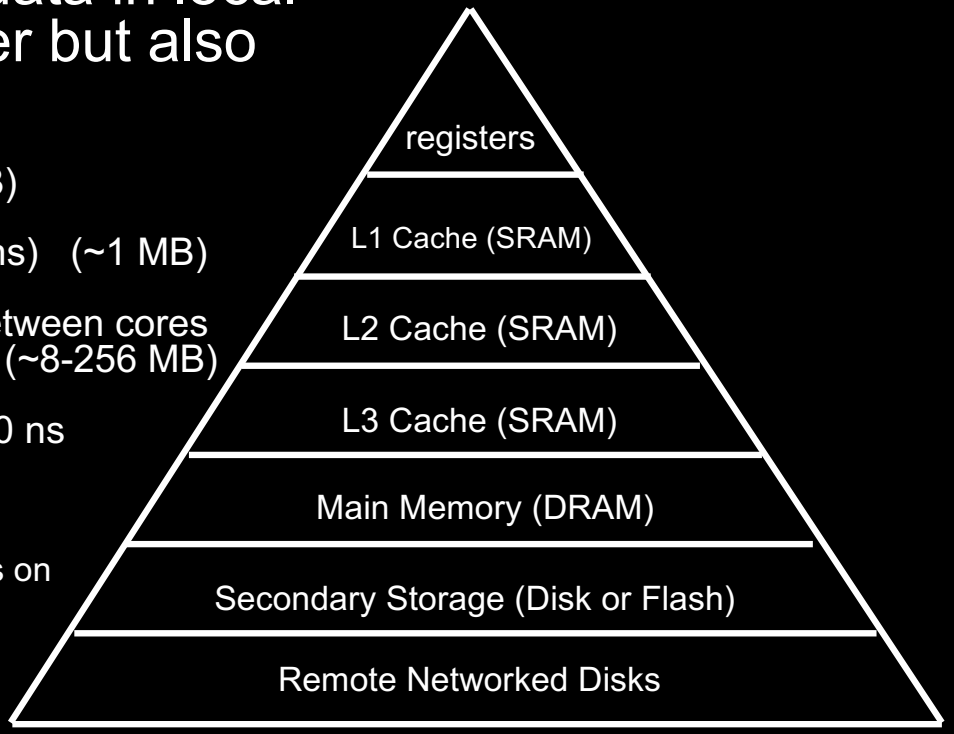
Memory Management

Memory Management



Memory Hierarchy

- cache frequently accessed instructions and/or data in local memory that is faster but also more expensive
  - L1 = 1 clock cycle (~16 KB)
  - L2 = 4-5 clock cycles (~1 ns) (~1 MB)
  - L3 caches often shared between cores ~40 clock cycles (~10 ns) (~8-256 MB)
  - RAM = ~100 cycles/~10-50 ns
  - Permanent storage:
    - Flash = 10-100 μs (depends on read/write,flash type, etc.)
    - Disk = 10 ms (10^7 ns)



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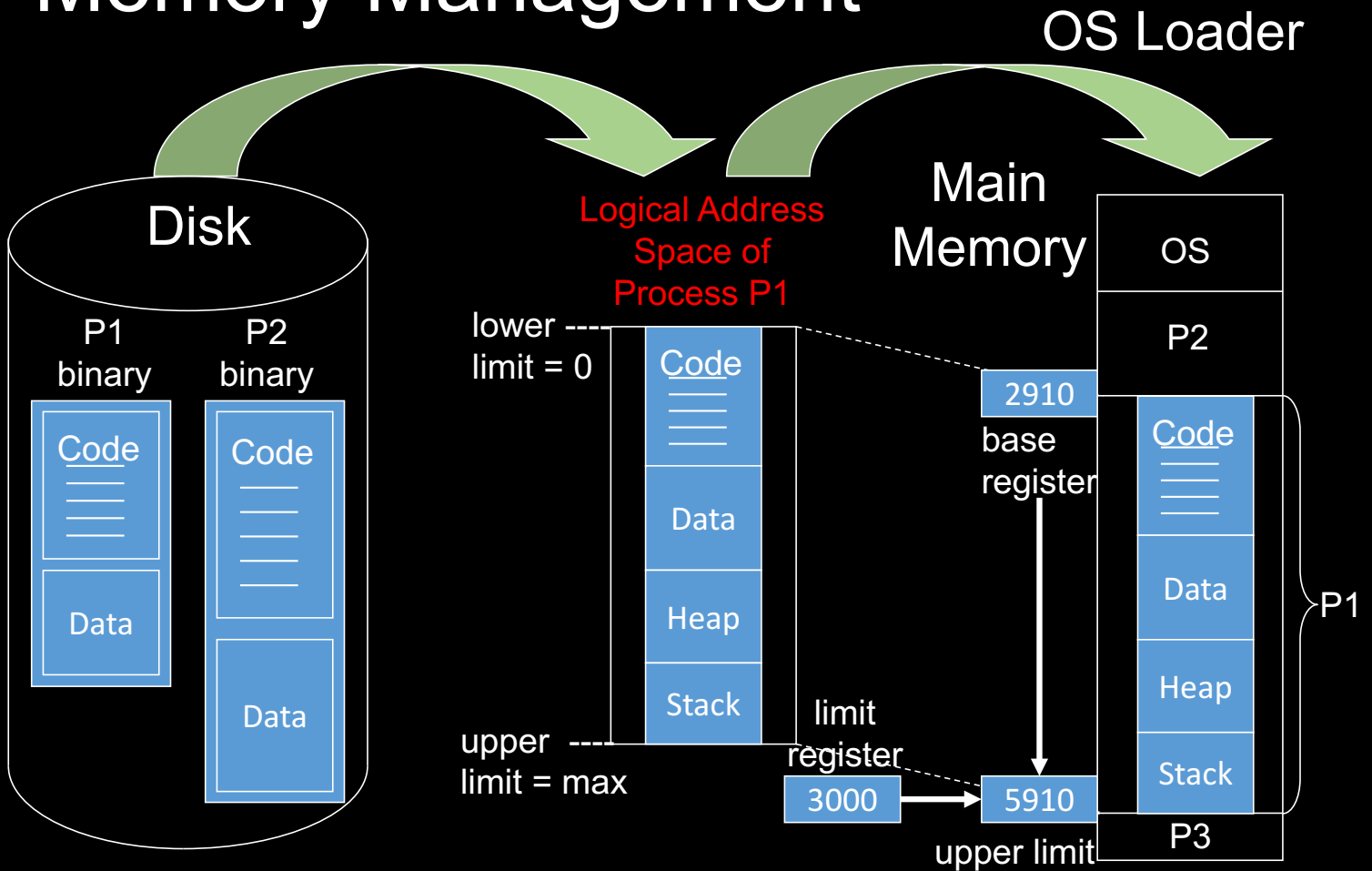
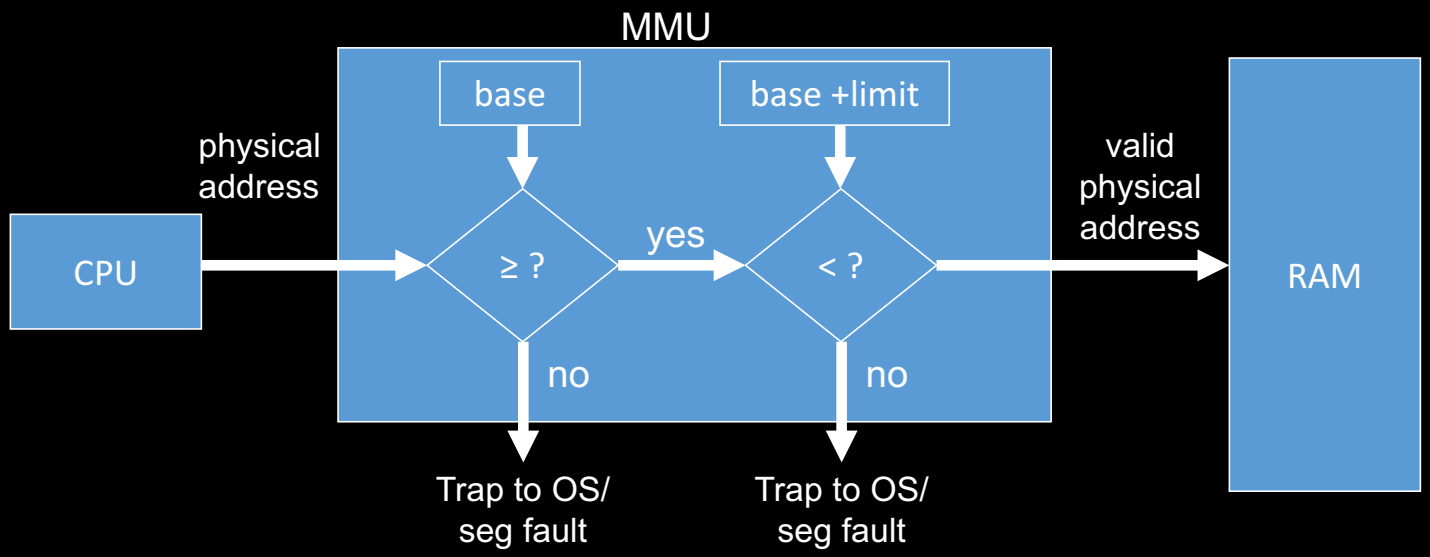


Memory Management Unit

- MMU needs to check if physical memory access is out of bounds



Memory Management

Memory Hierarchy

Memory Hierarchy

- Caches hold multiple units of memory (typically 64 bytes each)
- What is the behavior if data is written?
  - Write-through
    - Changes are written immediately to memory (and between caches)
    - Good for consistency
    - Bad for performance
  - Write-back (or write-behind)
    - Lazy write to memory (written later, maybe not until eviction of memory line from cache)
    - Good for performance
    - Bad for consistency (possible loss of data?)
  - Write-allocate (handling a cache miss, combines with previous behaviors)
    - Data sent to memory on cache miss
    - OR Load memory and update data in cache

Loading Tasks into Memory

Loading Tasks into Memory

- Using contiguous memory to hold task
- Task is stored as Code and Data on disk
- Task contains Code, Data, Stack, and Heap in memory

- Multiple tasks can be loaded in memory at the same time
- Kernel is responsible for protecting task memory from other tasks
  - Memory Management Unit (MMU) is used to validate all addresses
  - Each task needs a base and limit register
  - Context switch must save/restore these address registers

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