CSPB 2400 - Park - Computer Systems

Started on	Monday, 8 April 2024, 10:52 PM
State	Finished
Completed on	Monday, 8 April 2024, 11:21 PM
Time taken	28 mins 42 secs
Marks	18.75/20.00
Grade	**9.38** out of 10.00 (**94**%)

Question **1**

Correct

Mark 1.00 out of 1.00

Pick all which are correct. You are penalized for incorrect answers.

The TLB...

Select one or more:

- [ ] a. is a four-level structure used to establish page mappings
- [ ] b. uses the physical address to determine access permissions
- [x] c. acts as a cache for page table entries ✔
- [x] d. is accessed on each memory reference ✔

Question **2**

Correct

Mark 1.00 out of 1.00

When using a computer with virtual memory, which of the following are true (more than one may be true). You are penalized for incorrect answers.

Select one:

- a. No process may access the memory of another process.
- b. It is possible to share the memory of another process. ✔
- c. All processes can always access the memory of other processes.

Question **3**

Correct

Mark 4.00 out of 4.00

A computer has a 32-bit virtual address space and a 30-bit physical address with a virtual memory system with a 8192 (8KB) byte pagesize. Determine each of the following (expressed as a base-10 number of bits).

- The Virtual Page Number (VPN) is 19 ✔ bits wide
- The Virtual Page Offset (VPO) is 13 ✔ bits wide
- The Physical Page Nummber (PPN) is 17 ✔ bits wide
- The Physical Page Offset (PPO) is 13 ✔ bits wide

Question **4**

Correct

Mark 4.00 out of 4.00

A computer has a 32-bit virtual address space and a 24-bit physical address with a virtual memory system with a 512 byte pagesize. Determine each of the following (expressed as a base-10 number of bits).

- The Virtual Page Number (VPN) is 23 ✔ bits wide
- The Virtual Page Offset (VPO) is 9 ✔ bits wide
- The Physical Page Nummber (PPN) is 15 ✔ bits wide
- The Physical Page Offset (PPO) is 9 ✔ bits wide

Question **5**

Partially correct

Mark 4.38 out of 5.00

Assume the following:

- The memory is byte addressable.
- Memory accesses are to 1-byte words (not to 4-byte words).
- Virtual addresses are 17 bits wide.
- Physical addresses are 18 bits wide.
- The page size is 4096 bytes.
- The TLB is 2-way associative tlb (E=2) with 4 sets (S=4) and a total of 8 entries .
- The TLB and a portion of the page table contents are as shown below

TLB

Set #	Way #0	Way #1
0:	V=Y;Tag=0x6 PPN=0x1f	V=Y;Tag=0x7 PPN=0x16
1:	V=Y;Tag=0x6 PPN=0x39	V=Y;Tag=0x7 PPN=0x15
2:	V=Y;Tag=0x6 PPN=0x0c	V=Y;Tag=0x7 PPN=0x0d
3:	V=Y;Tag=0x6 PPN=0x10	V=Y;Tag=0x7 PPN=0x1d

Page Table

VPN	PPN	V?	VPN	PPN	V?	VPN	PPN	V?	VPN	PPN	V?
0x00	0x3b	Y	0x08	0x3a	Y	0x10	0x0b	Y	0x18	0x1f	Y
0x01	0x31	Y	0x09	0x25	Y	0x11	-	-	0x19	0x39	Y
0x02	0x17	Y	0x0a	0x20	Y	0x12	0x2b	Y	0x1a	0x0c	Y
0x03	0x2d	Y	0x0b	-	-	0x13	0x1c	Y	0x1b	0x10	Y
0x04	0x1a	Y	0x0c	0x11	Y	0x14	0x0a	Y	0x1c	0x16	Y
0x05	0x09	Y	0x0d	0x02	Y	0x15	0x21	Y	0x1d	0x15	Y
0x06	0x06	Y	0x0e	0x1b	Y	0x16	0x22	Y	0x1e	0x0d	Y
0x07	-	-	0x0f	0x24	Y	0x17	0x27	Y	0x1f	0x1d	Y

Assume that memory address **0x7b39** has been referenced by a load instruction. Determine the virtual page number (VPN) and use that to compute the TLB index and tag that would be used to check the TLB for the translation entry. Indicate if the entry is in the TLB (Y/N).

Indicate if the memory reference has a valid entry in the page table whether it hits in the TLB or not.

Use the information from the page table to translate the VPN to a physical page number (PPN) and then the valid physical address (PA).

For entries that can not be determined (*e.g.* the PPN or PA if a translation doesn't exist), enter "-".

Virtual Page Number (VPN)	0x 07 ✔
Virtual Page Offset (VPO)	0x b39 ✔
TLB Index (TLBI)	0x 3 ✔
TLB Tag (TLBT)	0x 1 ✔
TLB Hit (Y/N)?	no ✔
Valid Entry in Page Table (Y/N)?	no ✔
Physical Page Number (PPN)	0x - ✔
Physical Address (PA)	0x 7b39 ✖

Question **6**

Partially correct

Mark 4.38 out of 5.00

Assume the following:

- The memory is byte addressable.
- Memory accesses are to 1-byte words (not to 4-byte words).
- Virtual addresses are 16 bits wide.
- Physical addresses are 18 bits wide.
- The page size is 4096 bytes.
- The TLB is 4-way associative tlb (E=4) with 4 sets (S=4) and a total of 16 entries .
- The TLB and a portion of the page table contents are as shown below

TLB

Set #	Way #0	Way #1	Way #2	Way #3
0:	V=Y;Tag=0x0 PPN=0x37	V=Y;Tag=0x1 PPN=0x03	V=Y;Tag=0x2 PPN=0x20	V=Y;Tag=0x3 PPN=0x25
1:	V=Y;Tag=0x0 PPN=0x22	V=Y;Tag=0x1 PPN=0x3e	V=Y;Tag=0x2 PPN=0x14	V=Y;Tag=0x3 PPN=0x2b
2:	V=Y;Tag=0x0 PPN=0x07	V=Y;Tag=0x2 PPN=0x00	V=Y;Tag=0x3 PPN=0x11	--
3:	V=Y;Tag=0x0 PPN=0x17	V=Y;Tag=0x1 PPN=0x04	V=Y;Tag=0x2 PPN=0x0e	--

Page Table

VPN	PPN	V?	VPN	PPN	V?
0x0	0x37	Y	0x8	0x20	Y
0x1	0x22	Y	0x9	0x14	Y
0x2	0x07	Y	0xa	0x00	Y
0x3	0x17	Y	0xb	0x0e	Y
0x4	0x03	Y	0xc	0x25	Y
0x5	0x3e	Y	0xd	0x2b	Y
0x6	-	-	0xe	0x11	Y
0x7	0x04	Y	0xf	-	-

Assume that memory address **0x61c6** has been referenced by a load instruction. Determine the virtual page number (VPN) and use that to compute the TLB index and tag that would be used to check the TLB for the translation entry. Indicate if the entry is in the TLB (Y/N).

Indicate if the memory reference has a valid entry in the page table whether it hits in the TLB or not.

Use the information from the page table to translate the VPN to a physical page number (PPN) and then the valid physical address (PA).

For entries that can not be determined (*e.g.* the PPN or PA if a translation doesn't exist), enter "-".

Virtual Page Number (VPN)	0x 6 ✔
Virtual Page Offset (VPO)	0x 1c6 ✔
TLB Index (TLBI)	0x 2 ✔
TLB Tag (TLBT)	0x 1 ✔
TLB Hit (Y/N)?	no ✔
Valid Entry in Page Table (Y/N)?	no ✔
Physical Page Number (PPN)	0x - ✔
Physical Address (PA)	0x 61c6 ✖