TEXAS INSTRUMENTS

TLV7031-Q1, TLV7041-Q1, TLV7032-Q1, TLV7042-Q1, TLV7034-Q1, TLV7044-Q1

SNOSDA5D – MAY 2020 – REVISED FEBRUARY 2023

TLV703x-Q1 and TLV704x-Q1 Rail-to-Rail, Low-Power Comparators

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C5
- Wide supply voltage range of 1.6 V to 6.5 V
- Quiescent supply current of 315 nA
- Low propagation delay of 3 µs
- Internal hysteresis of 6.5 mV
- Rail-to-rail common-mode input voltage
- Internal Power-On-Reset provides a known startup condition
- No phase reversal for overdriven inputs
- Push-pull output (TLV703x-Q1)
- Open-drain output (TLV704x-Q1)
- –40°C to 125°C Operating temperature
- Functional Safety Capable
  - Documentation available to aid functional safety system design (TLV70x1-Q1)
  - Documentation available to aid functional safety system design (TLV70x2-Q1)

2 Applications

- Telematics eCall
- Automotive head unit
- Instrument cluster
- Audio amplifier
- On-board (OBC) & wireless chargers

3 Description

The TLV703x-Q1/TLV704x-Q1 are low-voltage, nanopower comparators with rail-to-rail inputs. These comparators are applicable for space-critical and power conscious designs like infotainment, telematics, and head unit applications.

The TLV703x-Q1 and TLV704x-Q1 offer an excellent combination of power and speed. The benefit of fast response time at nanopower enables power-conscious systems to monitor and respond quickly to fault conditions. With an operating voltage range of 1.6 V to 6.5 V, these comparators are compatible with 1.8 V, 3 V, and 5 V systems.
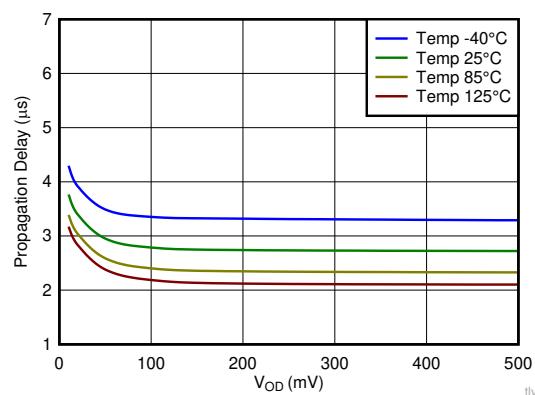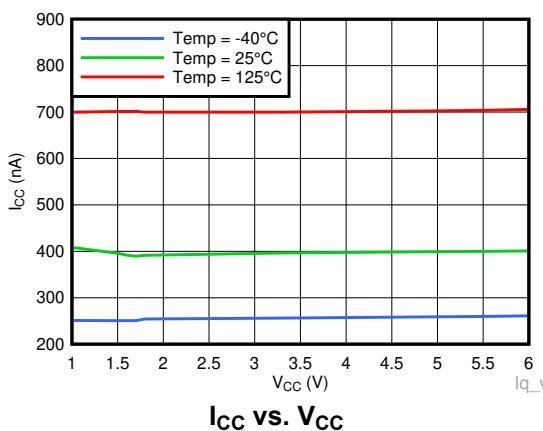
The TLV703x-Q1 and TLV704x-Q1 also ensure no output phase inversion with overdriven inputs and internal hysteresis, so engineers can use this family of comparators for precision voltage monitoring in harsh, noisy environments where slow-moving input signals must be converted into clean digital outputs.

The TLV703x-Q1 have a push-pull output stage capable of sinking and sourcing milliamps of current. The TLV704x-Q1 have an open-drain output stage that can be pulled beyond V_{CC}.

Device Information

PART NUMBERS	PACKAGE (PINS) [1]	BODY SIZE (NOM)
TLV7031-Q1, TLV7041-Q1	SC70 (5)	2.00 mm × 1.25 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
TLV7032-Q1, TLV7042-Q1	VSSOP (8)	3.00 mm x 3.00 mm
	SOT-23 (8)	2.90 mm x 1.60 mm
TLV7034-Q1, TLV7044-Q1	TSSOP (14)	4.40 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

I_{CC} vs. V_{CC}

Propagation Delay vs. Input Overdrive

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2021) to Revision D (February 2023)	**Page**
• Remove Preview Note from SOT-23 (8) package option for TLV7032-Q1 and TLV7042-Q1............................1	

Changes from Revision B (February 2021) to Revision C (October 2021)	**Page**
• Added link for new FIT Rate Report to the Features section..1	

Changes from Revision A (October 2020) to Revision B (February 2021)	**Page**
• Added Dual and Quad package options throughout 1	

Changes from Revision * (May 2020) to Revision A (October 2020)	**Page**
• Updated the numbering format for tables, figures, and cross-references throughout the document.................1	
• APL to RTM release..1	

5 Pin Configuration and Functions
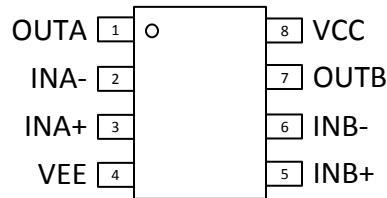
Figure 5-1. DBV, DCK Packages
5-Pin SOT-23, SC70
Top View

Table 5-1. Pin Functions

PIN		I/O [1]	DESCRIPTION
SOT-23, SC70	NAME		
1	OUT	O	Output
5	V_{CC}	P	Positive (highest) power supply
2	V_{EE}	P	Negative (lowest) power supply
4	IN–	I	Inverting input
3	IN+	I	Noninverting input

(1)   I = Input, O = Output, P = Power

Product Folder Links: *TLV7031-Q1 TLV7041-Q1 TLV7032-Q1 TLV7042-Q1 TLV7034-Q1 TLV7044-Q1*

Pin Functions: TLV7032/42
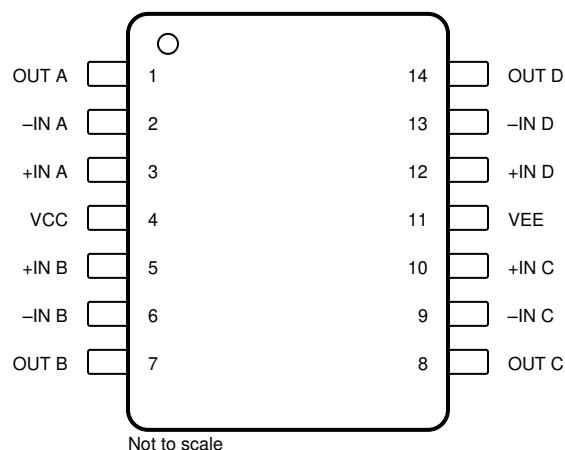
Figure 5-2. TLV7032/42 DGK, DDF Packages
8-Pin VSSOP, SOT-23
Top View

Table 5-2. Pin Functions: TLV7032/42

PIN		I/O	DESCRIPTION
NAME	NO.		
INA–	2	I	Inverting input, channel A
INA+	3	I	Noninverting input, channel A
INB–	6	I	Inverting input, channel B
INB+	5	I	Noninverting input, channel B
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
VEE	4	—	Negative (lowest) supply or ground (for single-supply operation)
VCC	8	—	Positive (highest) supply

Product Folder Links: *TLV7031-Q1 TLV7041-Q1 TLV7032-Q1 TLV7042-Q1 TLV7034-Q1 TLV7044-Q1*

5.1 Pin Functions: TLV7034/44

**Figure 5-3. TLV7034/44 PW Packages
14-Pin TSSOP
Top View**

Table 5-3. Pin Functions: TLV7034/44

PIN		I/O	DESCRIPTION
NAME	TSSOP		
–IN1 A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
–IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
NC	—	—	No internal connection
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
VEE	11	—	Negative (lowest) supply or ground (for single-supply operation)
VCC	4	—	Positive (highest) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Supply voltage $V_S = V_{CC} - V_{EE}$	−0.3	7	V
Input pins (IN+, IN−) [2]	$V_{EE} - 0.3$	7	V
Output (OUT) (push-pull)[3]	$V_{EE} - 0.3$	$V_{CC} + 0.3$	V
Output (OUT) (open-drain)	$V_{EE} - 0.3$	7	V
Output short-circuit duration[4]		10	s
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input terminals are diode-clamped to V_{EE}. Input signals that can swing 0.3V below V_{EE} must be current-limited to 10mA or less

(3) Output maximum is ($V_{CC} + 0.3$ V) or 7 V, whichever is less.

(4) Short-circuit to ground, one comparator per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage $V_S = V_{CC} - V_{EE}$	1.6	6.5	V
Input voltage range	$V_{EE} - 0.1$	$V_{CC} + 0.1$	V
Ambient temperature, T_A	−40	125	°C

6.4 Thermal Information (Single)

THERMAL METRIC [1]		TLV7031/TLV7041		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	297.2	278.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	224.7	186.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	200.1	113.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	141.2	82.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	198.9	112.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Thermal Information (Dual)

THERMAL METRIC [1]		TLV7032/TLV7042		UNIT
		DGK (VSSOP)	DDF (SOT-23)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	211.7	212.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.1	127.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	133.5	129.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	28.3	25.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	131.7	129.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Thermal Information (Quad)

THERMAL METRIC [1]		TLV7034/44		UNIT
		RTE (QFN)	PW (TSSOP)	
		16 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.4	131.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.2	60.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.5	74.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.6	12.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	40.5	73.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	24.1	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Product Folder Links: *TLV7031-Q1 TLV7041-Q1 TLV7032-Q1 TLV7042-Q1 TLV7034-Q1 TLV7044-Q1*

6.7 Electrical Characteristics

V_S = 1.8 V to 5 V, V_{CM} = V_S / 2; minimum and maximum values are at T_A = –40°C to +125°C (unless otherwise noted). Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input Offset Voltage	V_S = 1.8 V and 5 V, V_{CM} = V_S / 2		±0.1	±8	mV
V_{HYS}	Hysteresis	V_S = 1.8 V and 5 V, V_{CM} = V_S / 2, T_A = 25°C	2	6.5	17	mV
V_{CM}	Common-mode voltage range		V_{EE}		V_{CC} + 0.1	V
I_B	Input bias current			2		pA
I_{OS}	Input offset current			1		pA
V_{OH}	Output voltage high (push-pull only)	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA	4.65	4.8		V
V_{OL}	Output voltage low	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA		250	350	mV
I_{LKG}	Output leakage current (open-drain only)	V_S = 5 V, V_{ID} = +0.1 V (Output High), V_{PULLUP} = V_{CC}		100		pA
CMRR	Common-mode rejection ratio	V_{EE} < V_{CM} < V_{CC}, V_S = 5 V		73		dB
PSRR	Power supply rejection ratio	V_S = 1.8 V to 5 V, V_{CM} = V_S / 2		77		dB
I_{SC}	Short-circuit current	V_S = 5 V, sourcing (push-pull only)		35		mA
		V_S = 5 V, sinking		40		
I_{CC}	Supply current / Channel	V_S = 1.8 V, no load, V_{ID} = –0.1 V (Output Low)		390	900	nA

6.8 Switching Characteristics

Typical values are at T_A = 25°C, V_S = 5 V, V_{CM} = V_S / 2; C_L = 15 pF, input overdrive = 100 mV (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low (RP = 4.99 kΩ open-drain only)	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_{PLH}	Propagation delay time, low-to high (RP = 4.99 kΩ open-drain only)	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_R	Rise time (push-pull only)	Measured from 20% to 80%		4.5		ns
t_F	Fall time	Measured from 20% to 80%		4.5		ns
t_{ON}	Power-up time	During power on, V_{CC} must exceed 1.6V for 200 µs before the output will reflect the input..		200		µs

Product Folder Links: *TLV7031-Q1 TLV7041-Q1 TLV7032-Q1 TLV7042-Q1 TLV7034-Q1 TLV7044-Q1*

6.9 Electrical Characteristics (Dual)

V_S = 1.8 V to 5 V, V_{CM} = V_S / 2; minimum and maximum values are at T_A = –40°C to +125°C (unless otherwise noted). Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input Offset Voltage	V_S = 1.8 V and 5 V, V_{CM} = VS / 2		±0.1	±8	mV
V_{HYS}	Hysteresis	V_S = 1.8 V and 5 V, V_{CM} = VS / 2	3	10	25	mV
V_{CM}	Common-mode voltage range		V_{EE}		V_{CC} + 0.1	V
I_B	Input bias current			2		pA
I_{OS}	Input offset current			1		pA
V_{OH}	Output voltage high (push-pull only)	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA	4.65	4.8		V
V_{OL}	Output voltage low	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA		250	350	mV
I_{LKG}	Output leakage current (open-drain only)	V_S = 5 V, V_{ID} = +0.1 V (output high), V_{PULLUP} = V_{CC}		100		pA
CMRR	Common-mode rejection ratio	V_{EE} < V_{CM} < V_{CC}, V_S = 5 V		73		dB
PSRR	Power supply rejection ratio	V_S = 1.8 V to 5 V, V_{CM} = V_S / 2		77		dB
I_{SC}	Short-circuit current	VS = 5 V, sourcing (push-pull only)		29		mA
		VS = 5 V, sinking		33		
I_{CC}	Supply current / Channel	V_S = 1.8 V, no load, V_{ID} = –0.1 V (Output Low)		315	750	nA

6.10 Switching Characteristics (Dual)

Typical values are at T_A = 25°C, V_S = 5 V, V_{CM} = V_S / 2; CL = 15 pF, input overdrive = 100 mV (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low (RP = 4.99 kΩ open-drain only) [1]	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_{PLH}	Propagation delay time, low-to high (RP = 4.99 kΩ open-drain only) [1]	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_R	Rise time (push-pull only)	Measured from 20% to 80%		4.5		ns
t_F	Fall time	Measured from 20% to 80%		4.5		ns
t_{ON}	Power-up time	During power on, V_{CC} must exceed 1.6V for 200 µs before the output will reflect the input..		200		µs

(1)   The lower limit for RP is 650 Ω

6.11 Electrical Characteristics (Quad)

V_S = 1.8 V to 5 V, V_{CM} = V_S / 2; minimum and maximum values are at T_A = –40°C to +125°C (unless otherwise noted).
Typical values are at T_A = 25°C.

|	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input Offset Voltage	V_S = 1.8 V and 5 V, V_{CM} = VS / 2		±0.1	±8	mV
V_{HYS}	Hysteresis	V_S = 1.8 V and 5 V, V_{CM} = VS / 2	3	10	25	mV
V_{CM}	Common-mode voltage range		V_{EE}		V_{CC} + 0.1	V
I_B	Input bias current			2		pA
I_{OS}	Input offset current			1		pA
V_{OH}	Output voltage high (push-pull only)	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA	4.65	4.8		V
V_{OL}	Output voltage low	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA		250	350	mV
I_{LKG}	Output leakage current (open-drain only)	V_S = 5 V, V_{ID} = +0.1 V (output high), V_{PULLUP} = V_{CC}		100		pA
CMRR	Common-mode rejection ratio	V_{EE} < V_{CM} < V_{CC}, V_S = 5 V		73		dB
PSRR	Power supply rejection ratio	V_S = 1.8 V to 5 V, V_{CM} = V_S / 2		77		dB
I_{SC}	Short-circuit current	VS = 5 V, sourcing (push-pull only)		29		mA
		VS = 5 V, sinking		33		
I_{CC}	Supply current / Channel	V_S = 1.8 V, no load, V_{ID} = –0.1 V (Output Low)		315	750	nA

6.12 Switching Characteristics (Quad)

Typical values are at T_A = 25°C, V_S = 5 V, V_{CM} = V_S / 2; CL = 15 pF, input overdrive = 100 mV (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low (RP = 4.99 kΩ open-drain only) [1]	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_{PLH}	Propagation delay time, low-to high (RP = 4.99 kΩ open-drain only) [1]	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_R	Rise time (push-pull only)	Measured from 20% to 80%		4.5		ns
t_F	Fall time	Measured from 20% to 80%		4.5		ns
t_{ON}	Power-up time	During power on, V_{CC} must exceed 1.6V for t_{ON} before the output will reflect the input..		400		µs

(1) The lower limit for RP is 650 Ω

6.13 Timing Diagrams
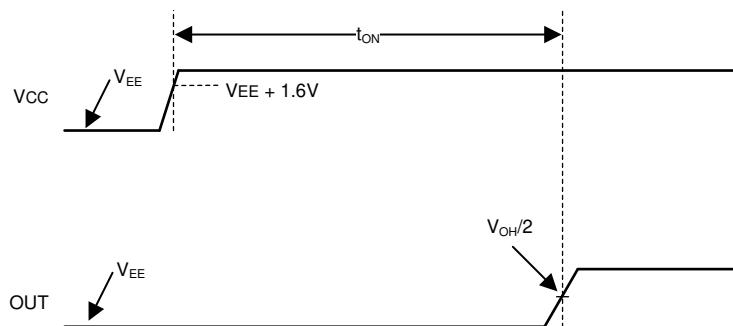
Figure 6-1. Start-Up Time Timing Diagram (IN+ > IN–)
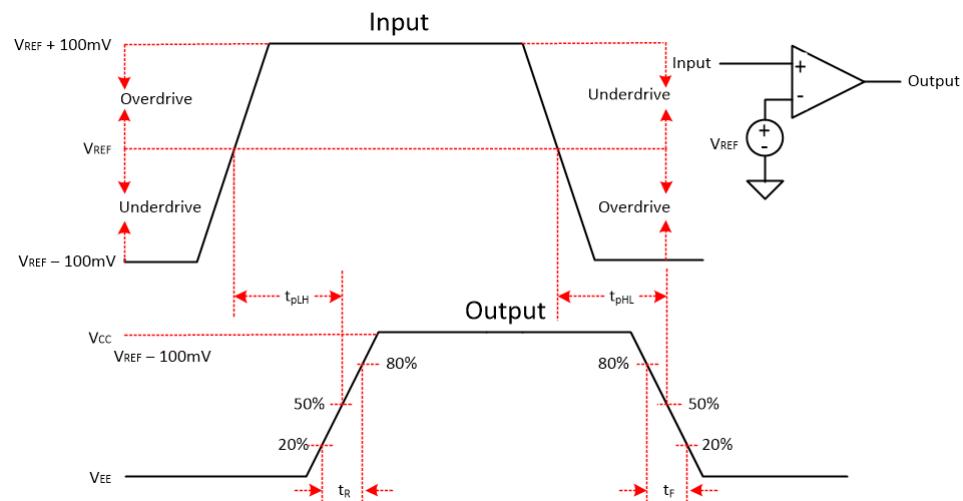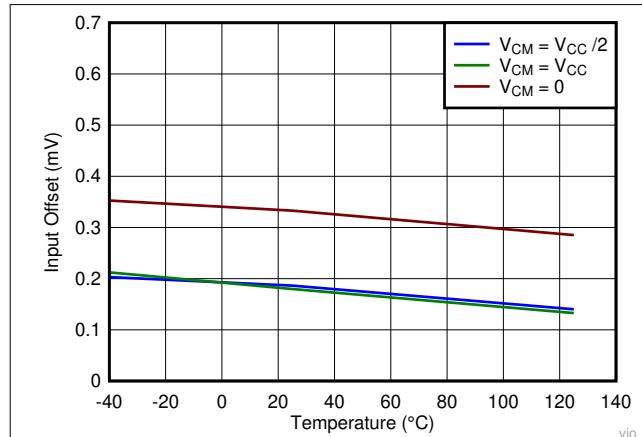
Figure 6-2. Propagation Delay Timing Diagram

Note

The propagation delays t_{pLH} and t_{pHL} include the contribution of input offset and hysteresis.

Product Folder Links: *TLV7031-Q1 TLV7041-Q1 TLV7032-Q1 TLV7042-Q1 TLV7034-Q1 TLV7044-Q1*
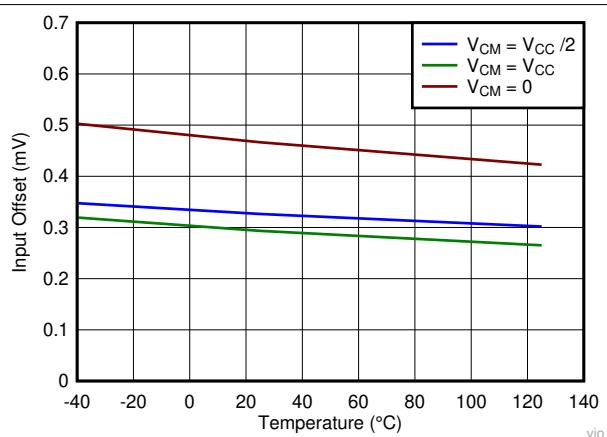
6.14 Typical Characteristics

$T_A = 25°C$, $V_{CC} = 5$ V, $V_{EE} = 0$ V, $V_{CM} = V_{CC}/2$, $C_L = 15$ pF
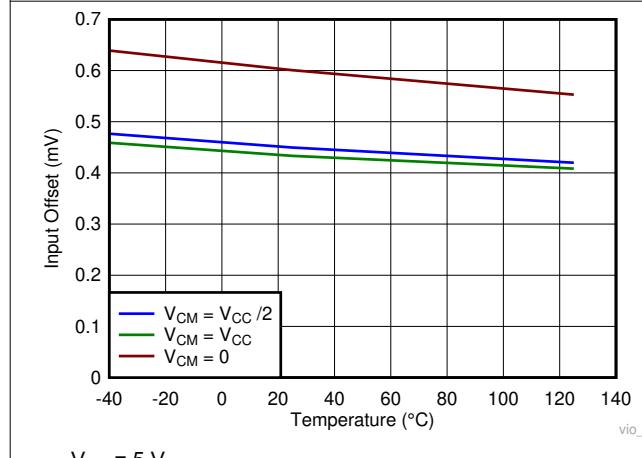
$V_{CC} = 1.8$ V

Figure 6-3. Input Offset vs Temperature
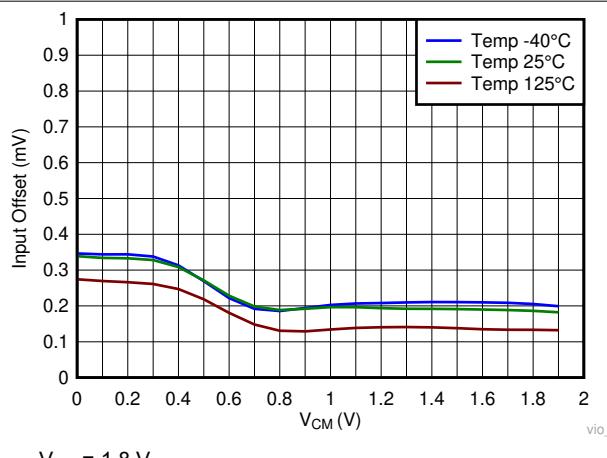
$V_{CC} = 3.3$ V

Figure 6-4. Input Offset vs Temperature
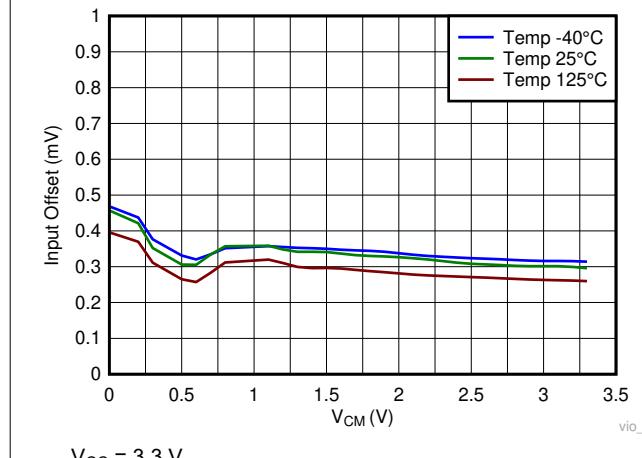
$V_{CC} = 5$ V

Figure 6-5. Input Offset vs Temperature
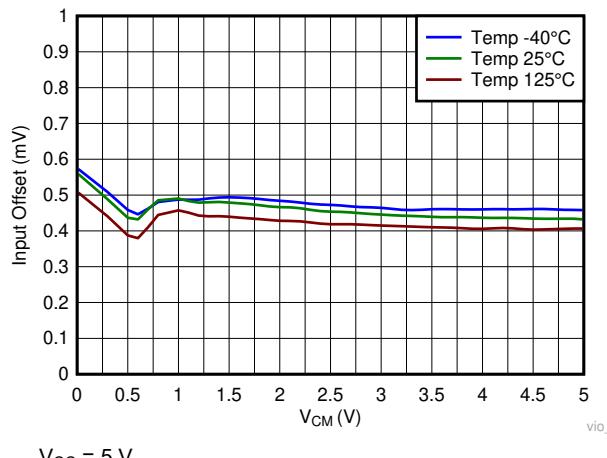
$V_{CC} = 1.8$ V

Figure 6-6. Input Offset Voltage vs V_{CM}

$V_{CC} = 3.3$ V

Figure 6-7. Input Offset Voltage vs V_{CM}

$V_{CC} = 5$ V

Figure 6-8. Input Offset Voltage vs V_{CM}

Product Folder Links: *TLV7031-Q1 TLV7041-Q1 TLV7032-Q1 TLV7042-Q1 TLV7034-Q1 TLV7044-Q1*

6.14 Typical Characteristics (continued)

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF

V_{CC} = 1.8 V to 5 V

TLV70x1
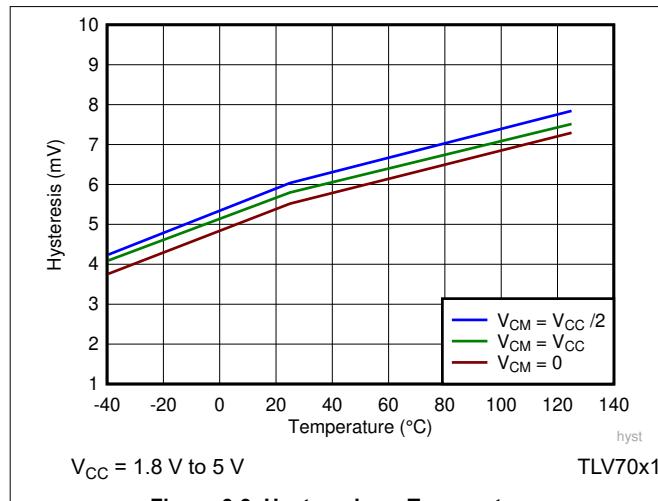
**Figure 6-9. Hysteresis vs Temperature**

V_{CC} = 1.8 V

TLV70x1
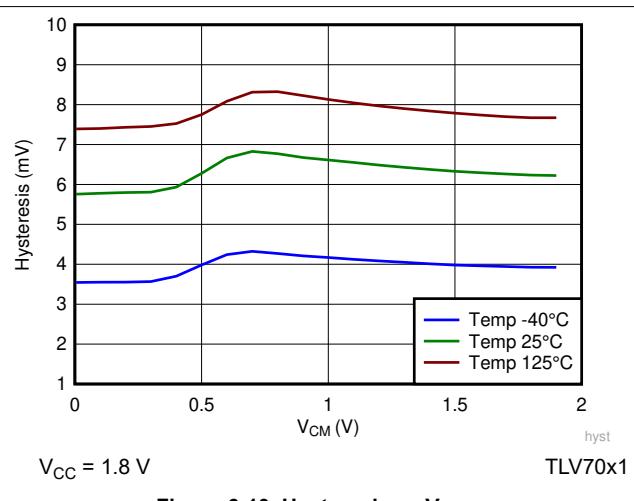
Figure 6-10. Hysteresis vs V_{CM}

V_{CC} = 3.3 V

TLV70x1
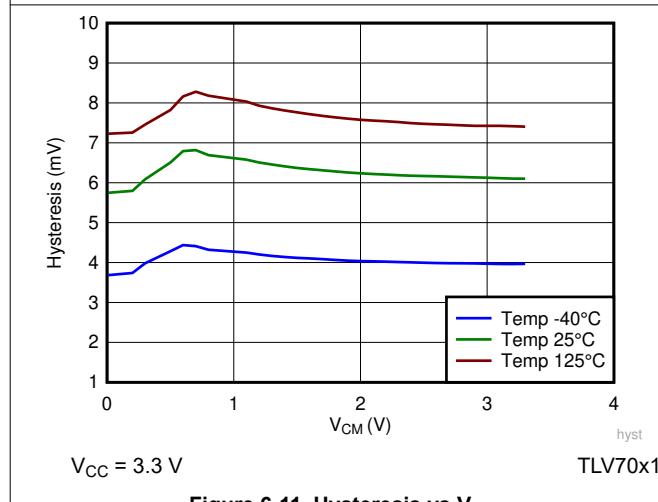
**Figure 6-11. Hysteresis vs V_{CM}**

V_{CC} = 5 V

TLV70x1
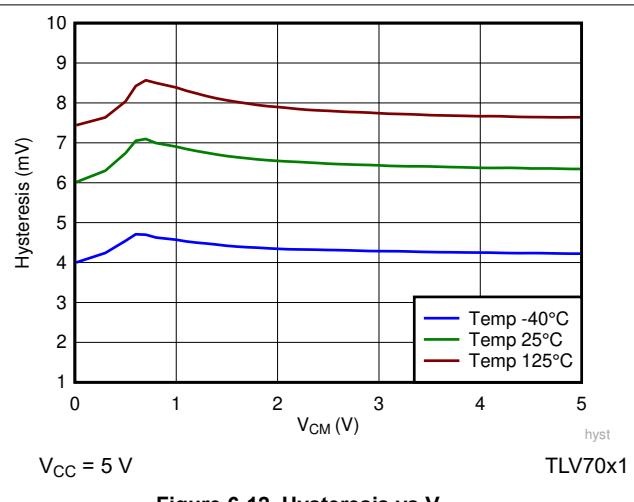
Figure 6-12. Hysteresis vs V_{CM}
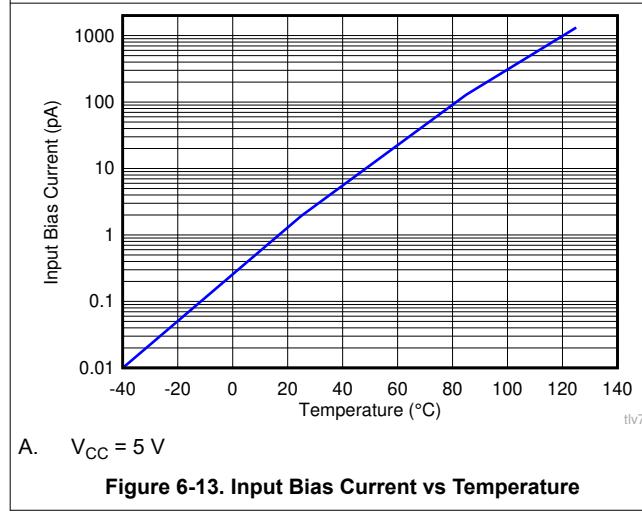
A. V_{CC} = 5 V

Figure 6-13. Input Bias Current vs Temperature

V_{CC} = 1.8 V

TLV703x
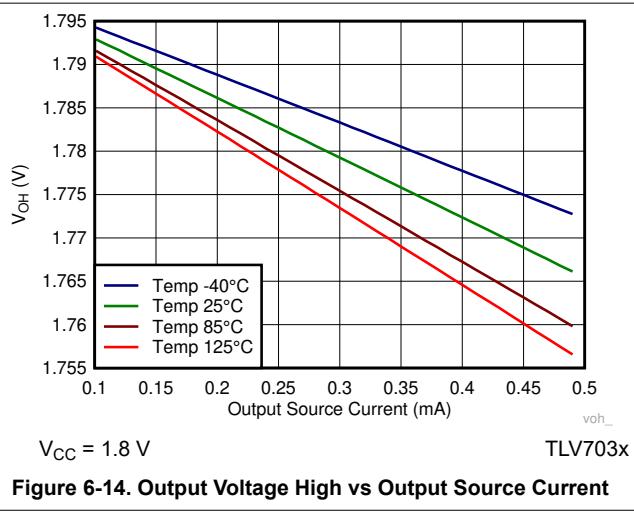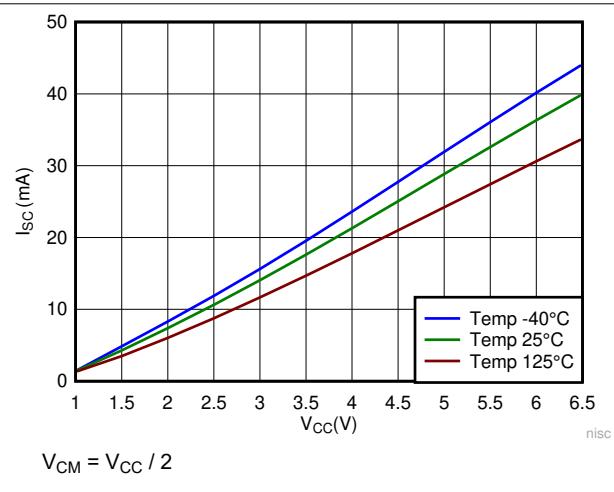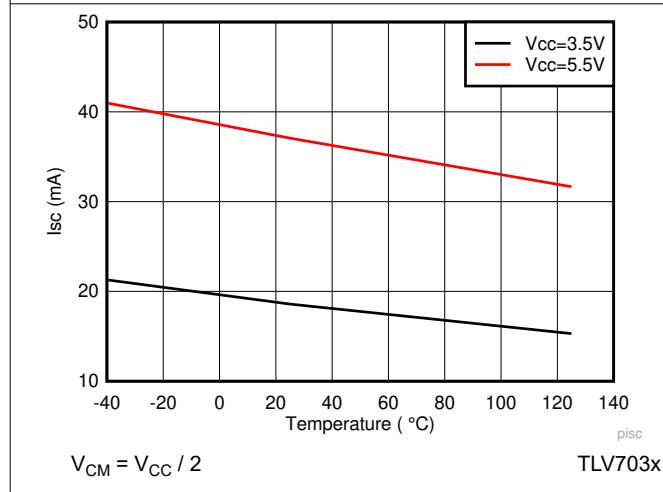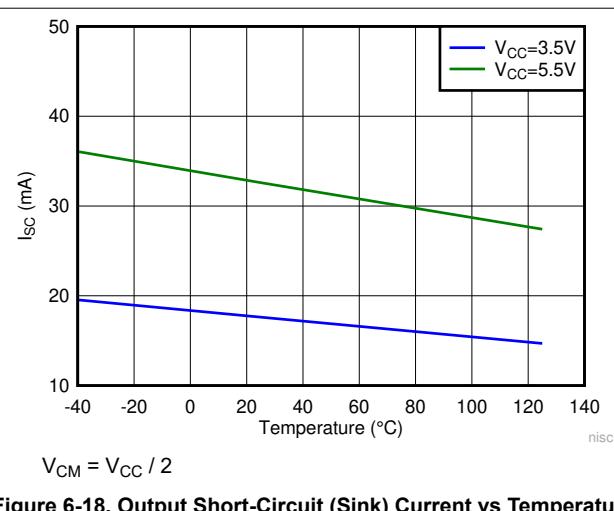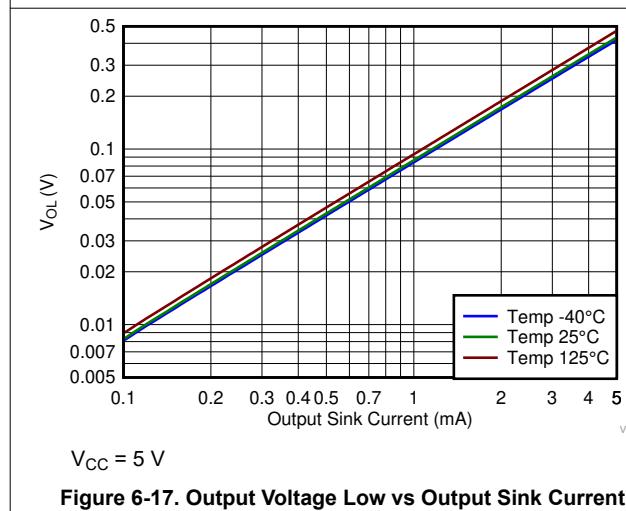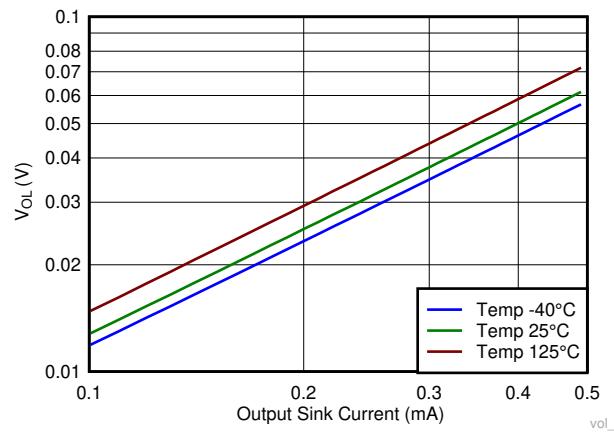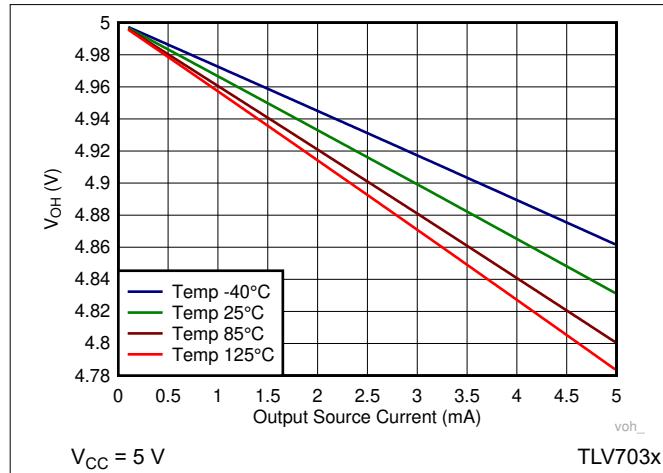
Figure 6-14. Output Voltage High vs Output Source Current

6.14 Typical Characteristics (continued)

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF

V_{CC} = 5 V

Figure 6-15. Output Voltage High vs Output Source Current

V_{CC} = 1.8 V

Figure 6-16. Output Voltage Low vs Output Sink Current

V_{CC} = 5 V

Figure 6-17. Output Voltage Low vs Output Sink Current

V_{CM} = V_{CC} / 2

Figure 6-18. Output Short-Circuit (Sink) Current vs Temperature

V_{CM} = V_{CC} / 2

Figure 6-19. Output Short-Circuit (Source) Current vs Temperature

V_{CM} = V_{CC} / 2

Figure 6-20. Output Short Circuit (Sink) vs V_{CC}

6.14 Typical Characteristics (continued)

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF

$V_{CM} = V_{CC} / 2$ TLV703x
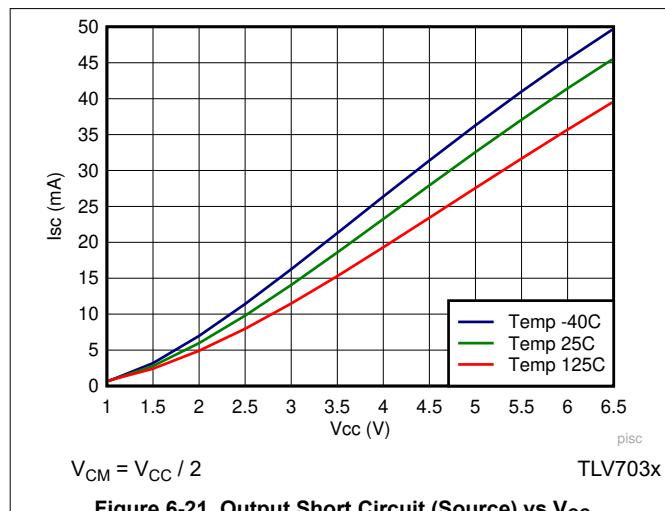
Figure 6-21. Output Short Circuit (Source) vs V_{CC}

$V_{CM} = V_{CC} / 2$ TLV70x2
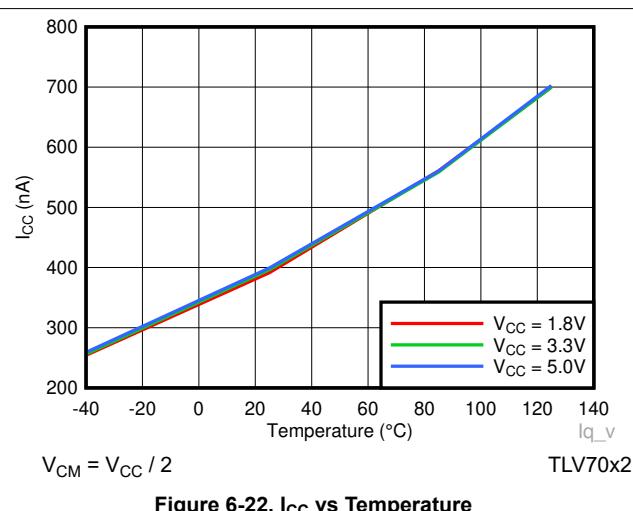
Figure 6-22. I_{CC} vs Temperature

$V_{CM} = V_{CC} / 2$ TLV70x2

Figure 6-23. I_{CC} vs V_{CC}

V_{OD} = 100 mV   TLV703x Rise only
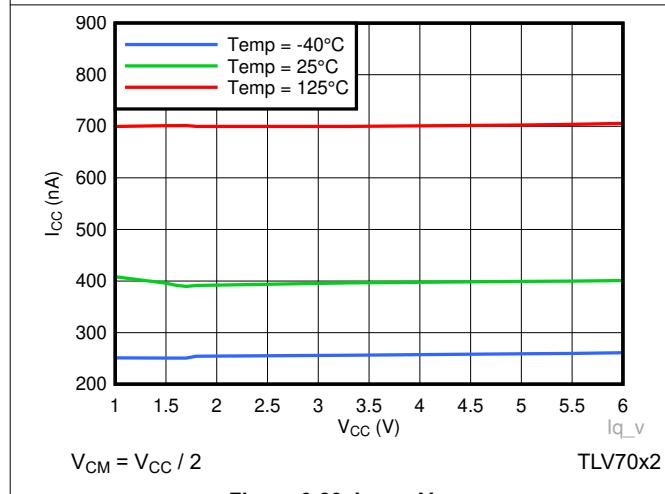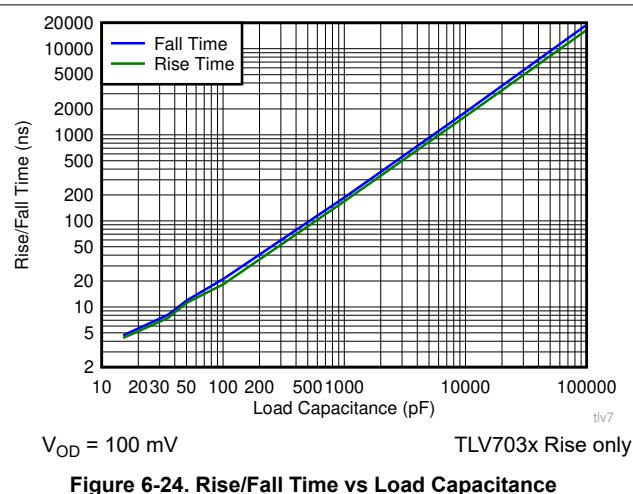
Figure 6-24. Rise/Fall Time vs Load Capacitance

V_{CC} = 3.3 V to 5 V   TLV703x
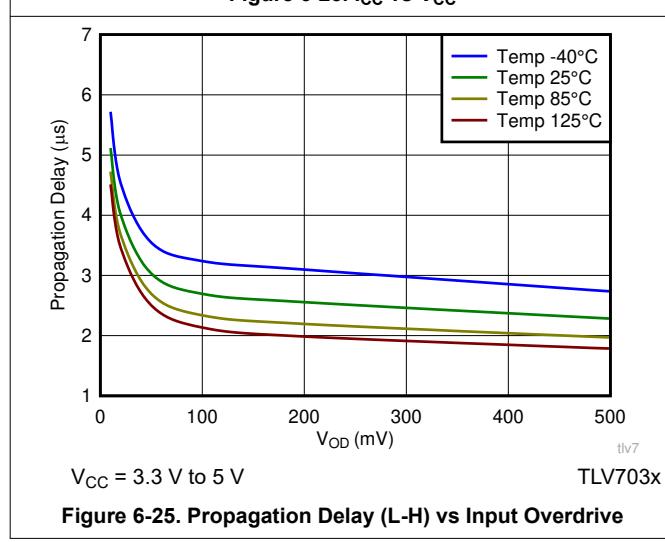
Figure 6-25. Propagation Delay (L-H) vs Input Overdrive

V_{CC} = 3.3 V to 5 V
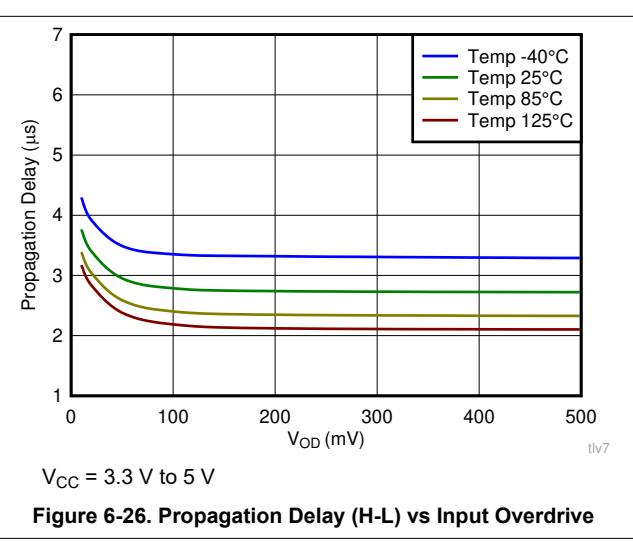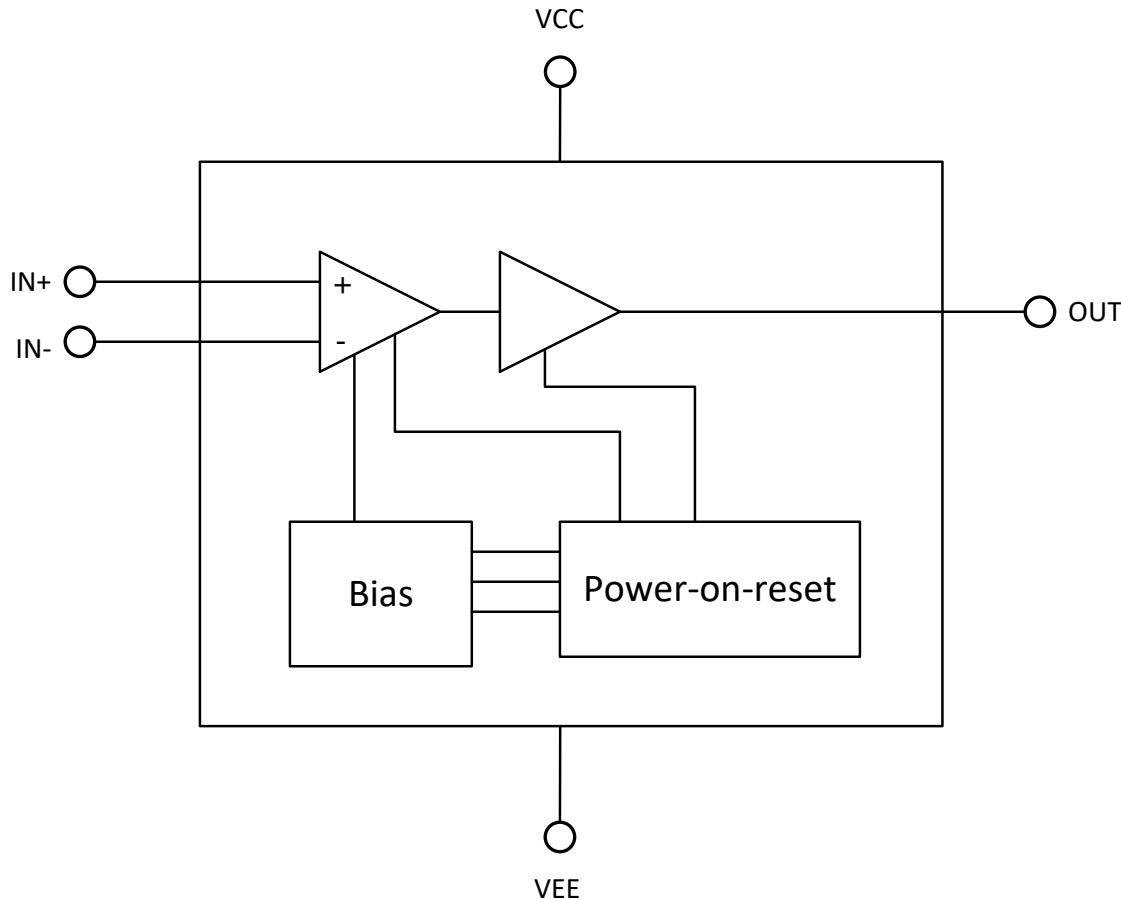
Figure 6-26. Propagation Delay (H-L) vs Input Overdrive

7 Detailed Description

7.1 Overview

The TLV703x-Q1 and TLV704x-Q1 devices are single-channel, nano-power comparators with push-pull and open-drain outputs. Operating from 1.6 V to 6.5 V and consuming only 315 nA, the TLV703x-Q1 and TLV704x-Q1 are designed for portable and industrial applications.

7.2 Functional Block Diagram

7.3 Feature Description

The TLV703x-Q1 and TLV704x-Q1 comparators are nanopower comparators that are capable of operating at low voltages. The TLV703x-Q1 and TLV704x-Q1 feature a rail-to-rail input stage capable of operating up to 100 mV beyond the V_{CC} power supply rail. The TLV703x-Q1 (push-pull) and TLV704x-Q1 (open-drain) also feature internal hysteresis.

7.4 Device Functional Modes

The TLV703x-Q1 and TLV704x-Q1 have a power-on-reset (POR) circuit. While the power supply (V_S) is less than the minimum supply voltage, either upon ramp-up or ramp-down, the POR circuitry is activated.

For the TLV703x-Q1, the POR circuit holds the output low (at V_{EE}) while activated.

For the TLV704x-Q1, the POR circuit keeps the output high impedance (logical high) while activated.

When the supply voltage is greater than, or equal to, the minimum supply voltage, the comparator output reflects the state of the differential input (V_{ID}).

7.4.1 Inputs

The TLV703x-Q1 and TLV704x-Q1 input common-mode extends from V_{EE} to 100 mV above V_{CC}. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase inversion of the comparator output occurs when the input pins exceed V_{CC} and V_{EE}.

The input of TLV703x-Q1 and TLV704x-Q1 is fault tolerant. It maintains the same high input impedance when V_{CC} is unpowered or ramping up. The input can be safely driven up to the specified maximum voltage (7 V) with V_{CC} = 0 V or any value up to the maximum specified. The V_{CC} is isolated from the input such that it maintains its value even when a higher voltage is applied to the input.

The input bias current is typically 1 pA for input voltages between V_{CC} and V_{EE}. The comparator inputs are protected from voltages below V_{EE} by internal diodes connected to V_{EE}. As the input voltage goes under V_{EE}, the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current typically doubles every 10°C temperature increases.

7.4.2 Internal Hysteresis

The device hysteresis transfer curve is shown in Figure 7-1. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:
- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and V_{IN-}. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise (7 mV for both TLV703x-Q1 and TLV704x-Q1).
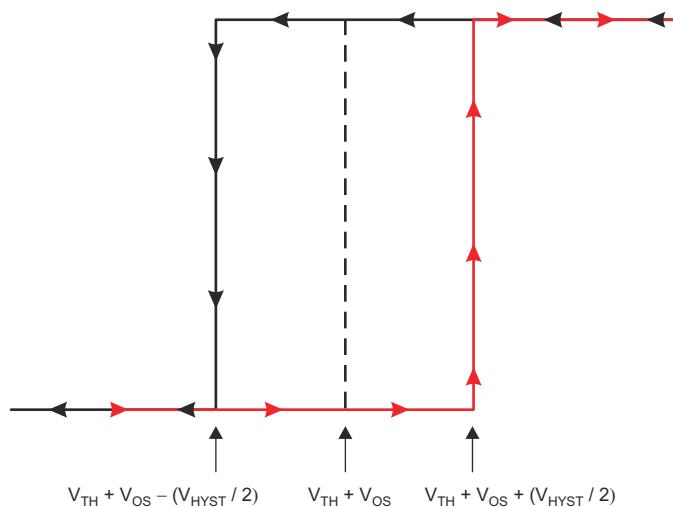
Figure 7-1. Hysteresis Transfer Curve

7.4.3 Output

The TLV703x-Q1 features a push-pull output stage eliminating the need for an external pullup resistor. On the other hand, the TLV704x-Q1 features an open-drain output stage enabling the output logic levels to be pulled up to an external source up to 6.5 V independent of the supply voltage.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TLV703x-Q1 and TLV704x-Q1 are nano-power comparators with reasonable response time. The comparators have a rail-to-rail input stage that can monitor signals beyond the positive supply rail with integrated hysteresis. When higher levels of hysteresis are required, positive feedback can be externally added. The push-pull output stage of the TLV703x-Q1 is optimal for reduced power budget applications and features no shoot-through current. When level shifting or wire-ORing of the comparator outputs is needed, the TLV704x-Q1 with its open-drain output stage is well suited to meet the system needs. In either case, the wide operating voltage range, low quiescent current, and small size of the TLV703x-Q1 and TLV704x-Q1 make these comparators excellent candidates for battery-operated and portable, handheld designs.

8.1.1 Inverting Comparator With Hysteresis for TLV703x-Q1

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in Figure 8-1. When V_{IN} at the inverting input is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2. Equation 1 defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \, || \, R3) + R2}$$

(1)

When V_{IN} is greater than V_A, the output voltage is low, very close to ground. In this case, the three network resistors can be presented as R2 || R3 in series with R1. Use Equation 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \, || \, R3}{R1 + (R2 \, || \, R3)}$$

(2)

Equation 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2}$$

(3)
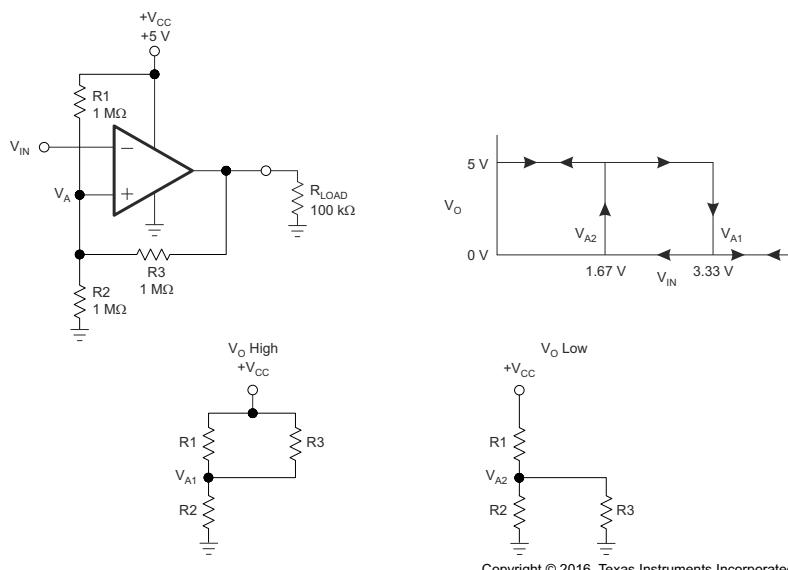
Figure 8-1. TLV703x-Q1 in an Inverting Configuration With Hysteresis

8.1.2 Noninverting Comparator With Hysteresis for TLV703x-Q1

A noninverting comparator with hysteresis requires a two-resistor network, as shown in Figure 8-2, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise to V_{IN1}. Use Equation 4 to calculate V_{IN1}.
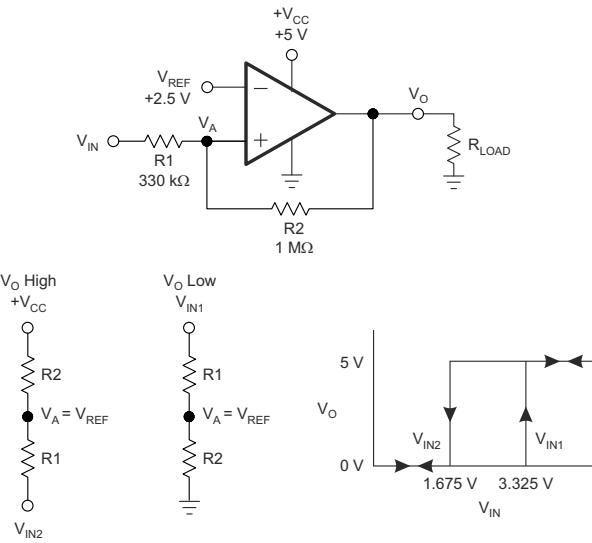
$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF}$$

(4)

When V_{IN} is high, the output is also high. For the comparator to switch back to a low state, V_{IN} must drop to V_{IN2} such that V_A is equal to V_{REF}. Use Equation 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF} (R1 + R2) - V_{CC} \times R1}{R2}$$

(5)

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2}$$

(6)

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Figure 8-2. TLV703x-Q1 in a Noninverting Configuration With Hysteresis

8.2 Typical Applications

8.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. Figure 8-3 shows a simple window comparator circuit.
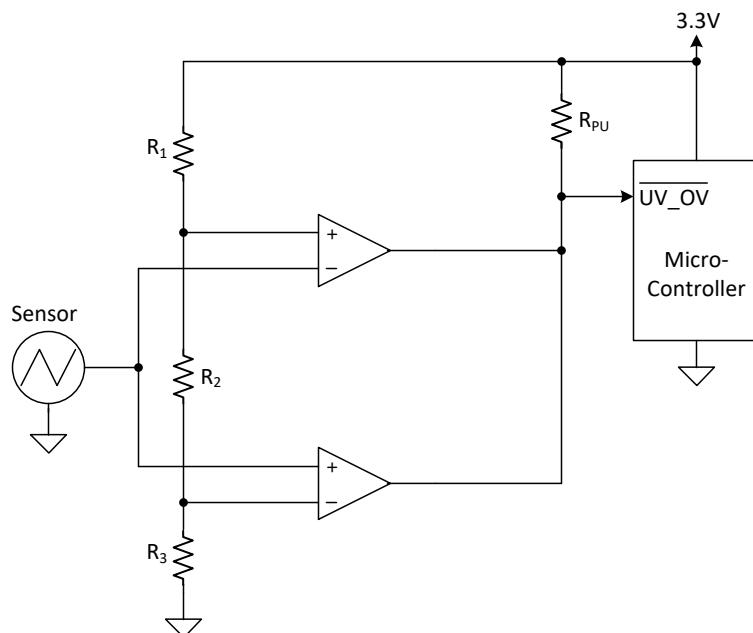
Figure 8-3. TLV704x-Q1-Based Window Comparator

8.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1 V
- Alert (logic low output) when an input signal is greater than 2.2 V
- Alert signal is active low
- Operate from a 3.3-V power supply

8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in Figure 8-3. Connect V_{CC} to a 3.3-V power supply and V_{EE} to ground. Make R1, R2, and R3 each 10-MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and V_{TH-}). With each resistor being equal, V_{TH+} is 2.2 V and V_{TH-} is 1.1 V. Large resistor values such as 10 MΩ are used to minimize power consumption. The sensor output voltage is applied to the inverting and noninverting inputs of the two TLV704x-Q1 devices. The TLV704x-Q1 is used for its open-drain output configuration. Using the TLV704x-Q1 allows the two comparator outputs to be wire-ored together. The respective comparator outputs are low when the sensor is less than 1.1 V or greater than 2.2 V. V_{OUT} is high when the sensor is in the range of 1.1 V to 2.2 V.

Product Folder Links: *TLV7031-Q1 TLV7041-Q1 TLV7032-Q1 TLV7042-Q1 TLV7034-Q1 TLV7044-Q1*

8.2.1.3 Application Curve
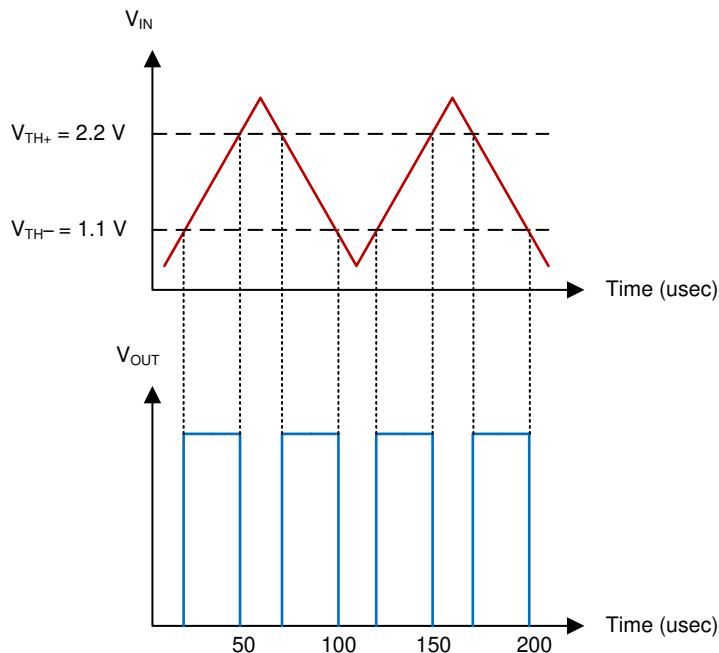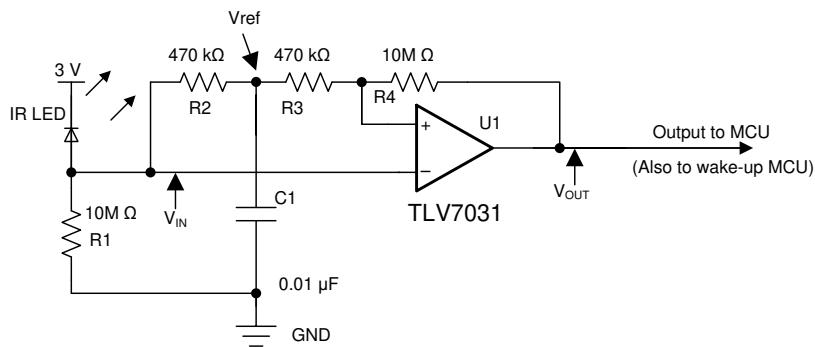
Figure 8-4. Window Comparator Results

8.2.2 IR Receiver Analog Front End

A single TLV703x-Q1 device can be used to build a complete IR receiver analog front end (AFE). The nanoamp quiescent current and low input bias current make it possible to be powered with a coin cell battery, which could last for years.

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Figure 8-5. IR Receiver Analog Front End Using TLV703x-Q1

8.2.2.1 Design Requirements

For this design, follow these design requirements:
- Use a proper resistor (R_1) value to generate an adequate signal amplitude applied to the inverting input of the comparator.
- The low input bias current I_B (2 pA typical) ensures that a greater value of R1 to be used.
- The RC constant value (R_2 and C_1) must support the targeted data rate (that is, 9,600 bauds) in order to maintain a valid tripping threshold.
- The hysteresis introduced with R_3 and R_4 helps to avoid spurious output toggles.

8.2.2.2 Detailed Design Procedure

The IR receiver AFE design is highly streamlined and optimized. R_1 converts the IR light energy induced current into voltage and applies to the inverting input of the comparator. The RC network of R_2 and C_1 establishes a reference voltage V_{ref}, which tracks the mean amplitude of the IR signal. The noninverting input is directly connected to V_{ref} through R_3. R_3 and R_4 are used to produce a hysteresis to keep transitions free of spurious toggles. To reduce the current drain from the coin cell battery, data transmission must be short and infrequent.

More technical details are provided in the TI TechNote *Low Power Comparator for Signal Processing and Wake-Up Circuit in Smart Meters* (SNVA808).

8.2.2.3 Application Curve
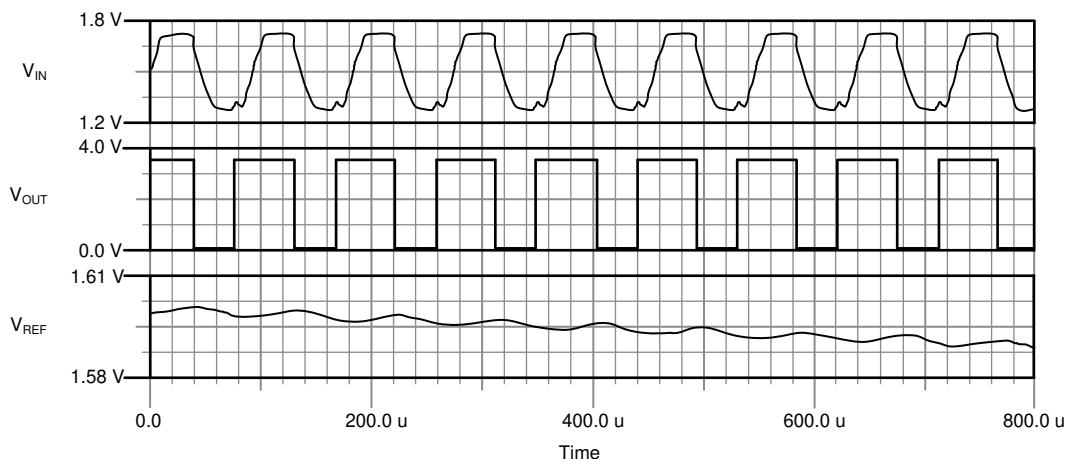
Figure 8-6. IR Receiver AFE Waveforms

8.2.3 Square-Wave Oscillator

A square-wave oscillator can be used as low-cost timing reference or system supervisory clock source.
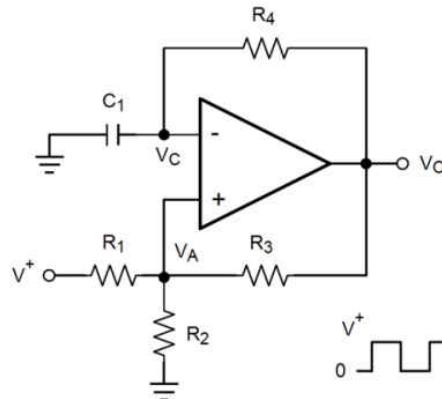
Figure 8-7. Square-Wave Oscillator

8.2.3.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor and resistor. The maximum frequency is limited by the propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which may help reduce BOM cost and board space.

8.2.3.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following section provides details to calculate these component values.
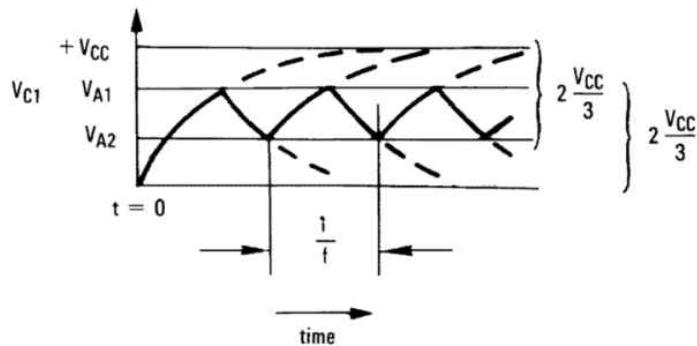
Figure 8-8. Square-Wave Oscillator Timing Thresholds

First consider the output of figure Figure 8-7 is high, which indicates the inverted input V_C is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4, and the voltage V_C increases until it is equal to the noninverting input. The value of V_A at the point is calculated by Equation 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \| R_3}$$

(7)

If $R_1 = R_2 = R_3$, then $V_{A1} = 2\,V_{CC}/3$

Product Folder Links: *TLV7031-Q1 TLV7041-Q1 TLV7032-Q1 TLV7042-Q1 TLV7034-Q1 TLV7044-Q1*

At this time the comparator output trips pulling down the output to the negative rail. The value of V_A at this point is calculated by Equation 8.

$$V_{A2} = \frac{V_{CC}(R_2 \| R_3)}{R_1 + R_2 \| R_3}$$

(8)

If $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The C_1 now discharges though the R_4, and the voltage V_{CC} decreases until it reaches V_{A2}. At this point, the output switches back to the starting state. The oscillation period equals the time duration from $2\,V_{CC}\,/\,3$ to $V_{CC}\,/\,3$ then back to $2\,V_{CC}\,/\,3$, which is given by $R_4 C_1 \times \ln2$ for each trip. Therefore, the total time duration is calculated as $2\,R_4 C_1 \times \ln2$. The oscillation frequency can be obtained by Equation 9:

$$f = 1/(2\ R4 \times C1 \times \ln2)$$

(9)

8.2.3.3 Application Curve

Figure 8-9 shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100\ k\Omega$
- $C_1 = 100\ pF$, $C_L = 20\ pF$
- $V+ = 5\ V$, $V- = GND$
- C_{stray} (not shown) from V_A to GND = 10 pF
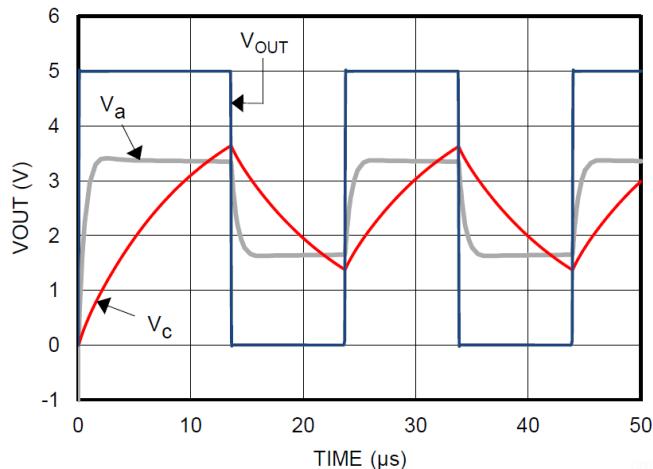
Figure 8-9. Square-Wave Oscillator Output Waveform

Product Folder Links: *TLV7031-Q1 TLV7041-Q1 TLV7032-Q1 TLV7042-Q1 TLV7034-Q1 TLV7044-Q1*

9 Power Supply Recommendations

The TLV703x-Q1 and TLV704x-Q1 have a recommended operating voltage range (V_S) of 1.6 V to 6.5 V. V_S is defined as $V_{CC} - V_{EE}$. Therefore, the supply voltages used to create V_S can be single-ended or bipolar. For example, single-ended supply voltages of 5 V and 0 V and bipolar supply voltages of +2.5 V and –2.5 V create comparable operating voltages for V_S. However, when bipolar supply voltages are used, it is important to realize that the logic low level of the comparator output is referenced to V_{EE}.

Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current.

10 Layout

10.1 Layout Guidelines

Figure 10-1 shows the typical connections for the TLV7031-Q1. To minimize supply noise, power supplies must be capacitively decoupled by a 0.1-μF ceramic capacitor in parallel with a 10-μF electrolytic capacitor. Comparators are very sensitive to input noise. Proper grounding (the use of a ground plane) helps to maintain the specified performance of the TLV70x1-Q1 family.

For best results, maintain the following layout guidelines:

1. Use a printed-circuit board (PCB) with a good, unbroken low-inductance ground plane.
2. Place a decoupling capacitor (0.1-μF ceramic, surface-mount capacitor) as close as possible to V_{CC}.
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.
5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. The top-side ground plane runs between the output and inputs.
6. The ground pin ground trace runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

10.2 Layout Example
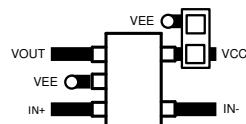
Figure 10-1. TLV7031-Q1 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV703x-Q1, TLV704x-Q1 device family. The DIP Adapter EVM can be requested at the Texas Instruments website through the product folder or purchased directly from the TI eStore.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV7031QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7031
TLV7031QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7031
TLV7031QDBVRQ1G4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7031
TLV7031QDBVRQ1G4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7031
TLV7031QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GP
TLV7031QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GP
TLV7032QDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2R4F
TLV7032QDDFRQ1.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2R4F
TLV7032QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7032
TLV7032QDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7032
TLV7034QPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7034Q
TLV7034QPWRQ1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7034Q
TLV7041QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7041
TLV7041QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7041
TLV7041QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GQ
TLV7041QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GQ
TLV7042QDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2R5F
TLV7042QDDFRQ1.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2R5F
TLV7042QDDFRQ1.B	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2R5F
TLV7042QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7042
TLV7042QDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7042
TLV7044QPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7044Q
TLV7044QPWRQ1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7044Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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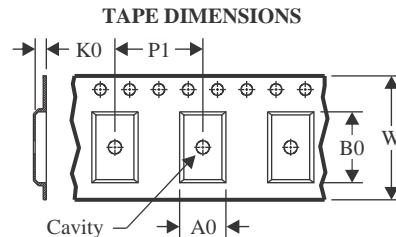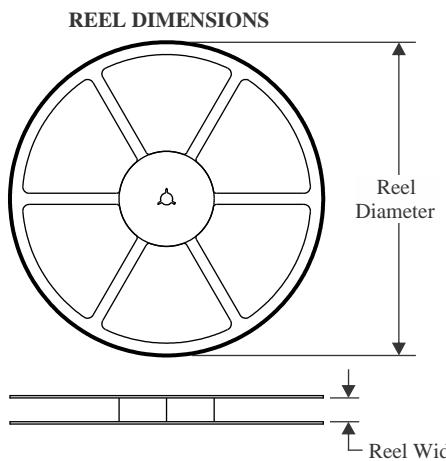
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV7031-Q1, TLV7032-Q1, TLV7034-Q1, TLV7041-Q1, TLV7042-Q1, TLV7044-Q1 :
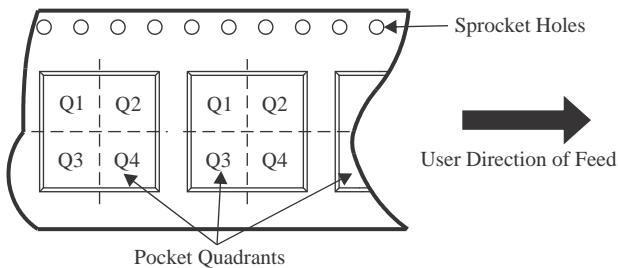
• Catalog : TLV7031, TLV7032, TLV7034, TLV7041, TLV7042, TLV7044

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product
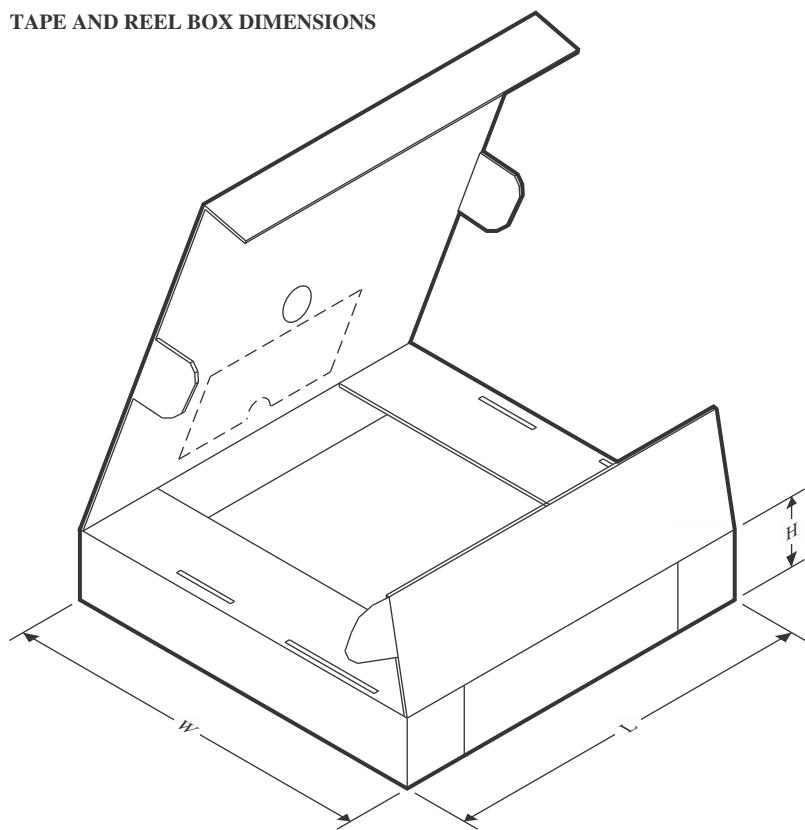
TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7031QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV7031QDBVRQ1G4	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV7031QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7032QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7032QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV7034QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV7041QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV7041QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7042QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7042QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV7044QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7031QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV7031QDBVRQ1G4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV7031QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0
TLV7032QDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV7032QDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV7034QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
TLV7041QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV7041QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0
TLV7042QDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV7042QDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV7044QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
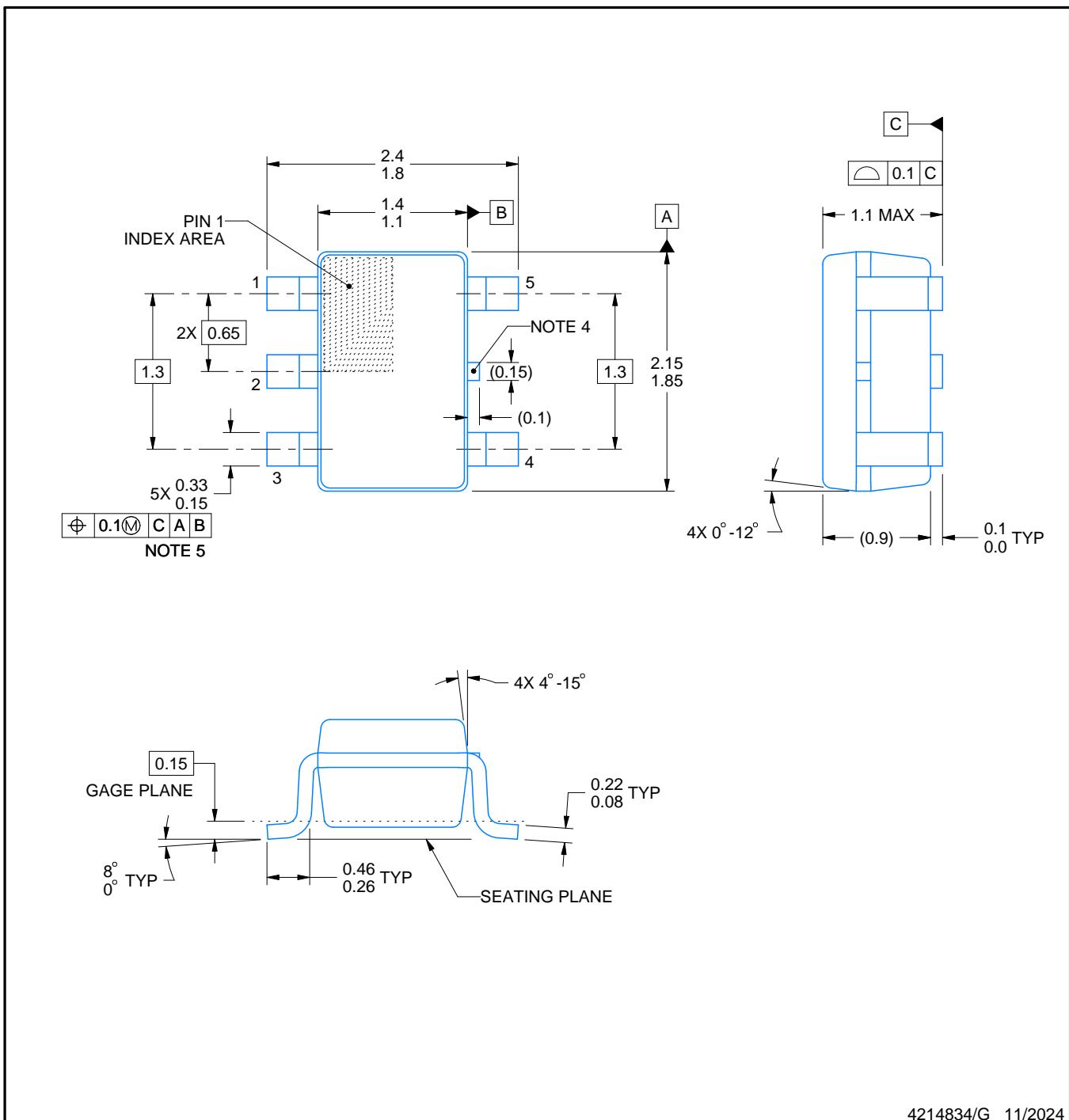
4214834/G   11/2024

NOTES:
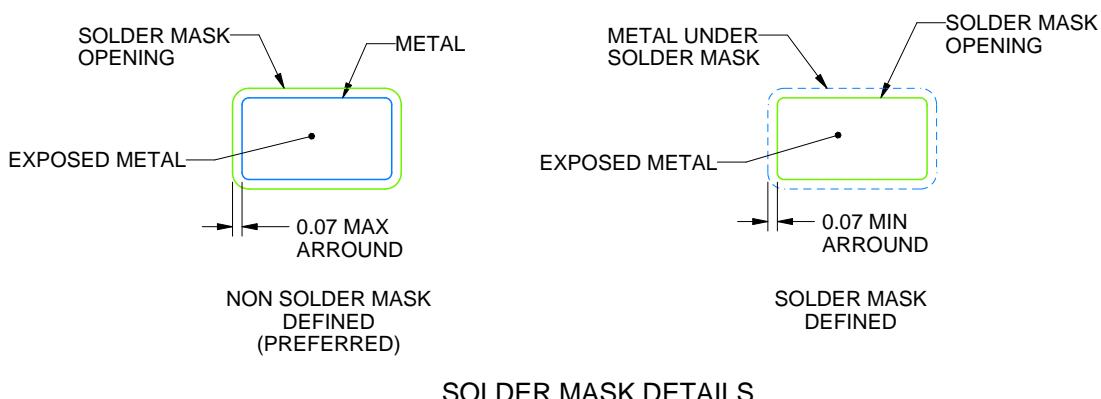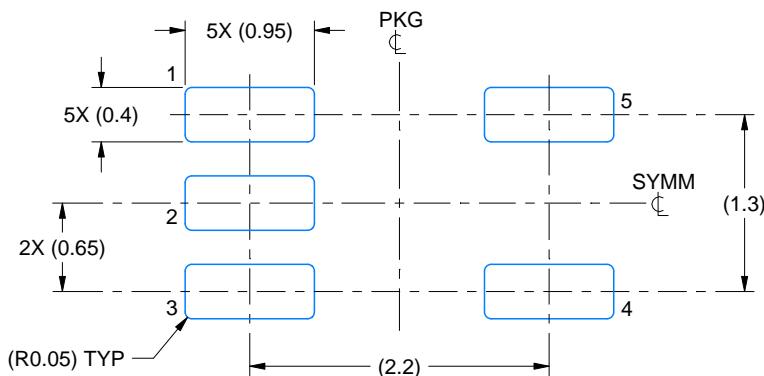
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

DCK0005A

5X (0.95)

PKG ℄

1

5X (0.4)

2

SYMM ℄

(1.3)

2X (0.65)

3

4

5

(R0.05) TYP

(2.2)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214834/G   11/2024

NOTES: (continued)
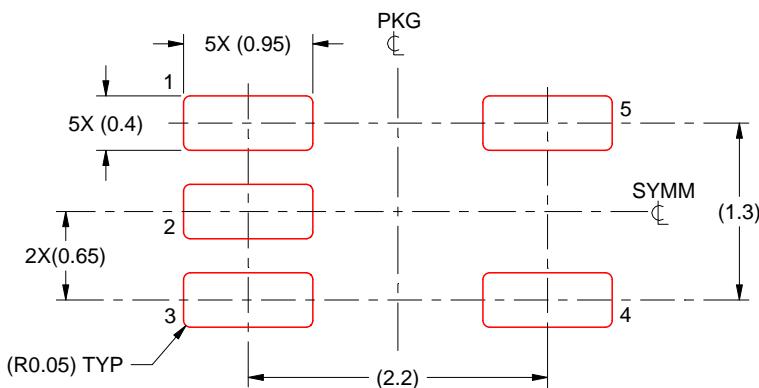
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G   11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
10. Board assembly site may have different recommendations for stencil design.
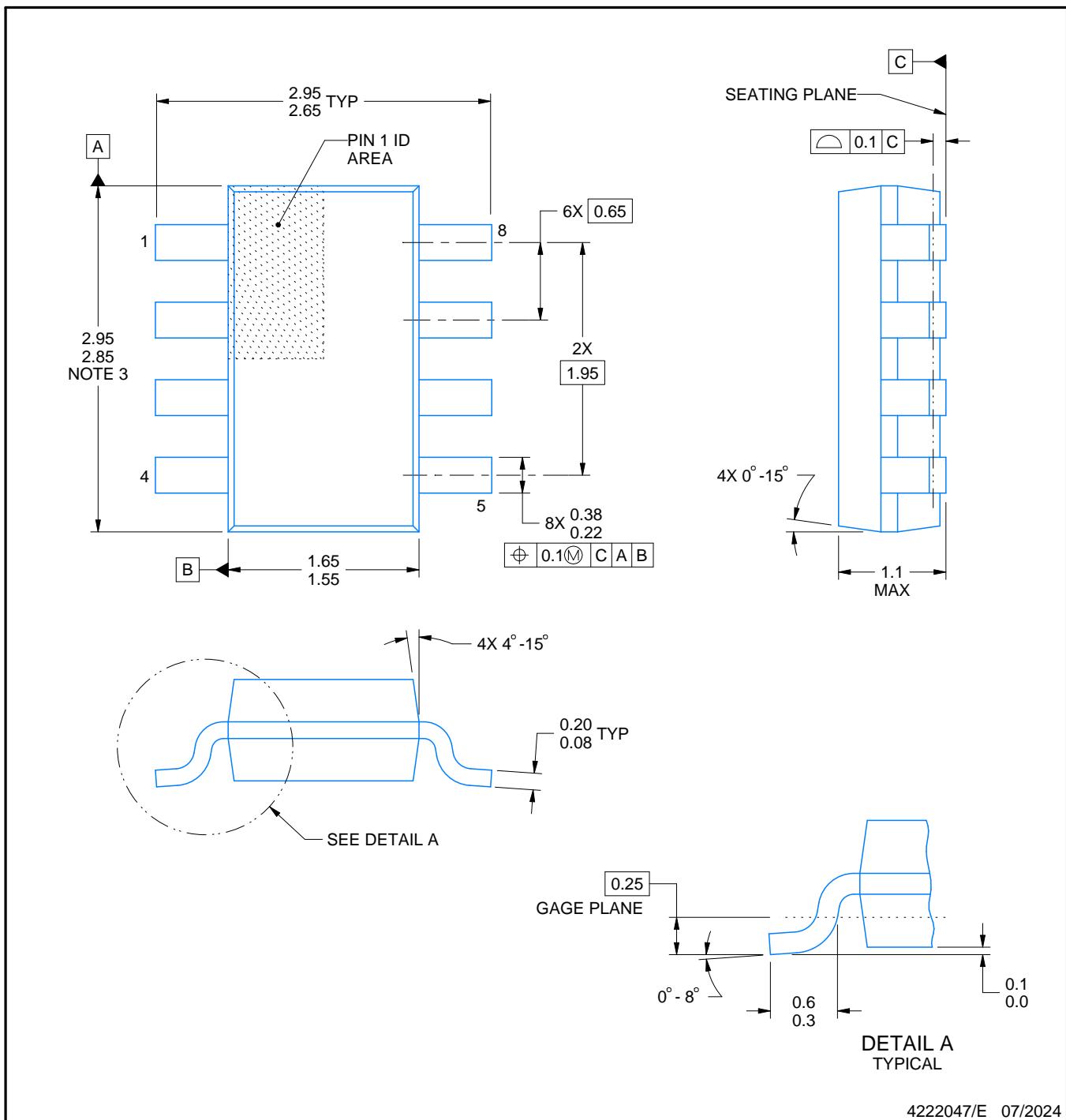
2.95 TYP
2.65

A

PIN 1 ID
AREA

2.95
2.85
NOTE 3

1

4

8

5

6X 0.65

2X
1.95

8X 0.38
0.22

⊕ 0.1 Ⓜ C A B

B 1.65
1.55

C

SEATING PLANE

⌒ 0.1 C

4X 0°-15°

1.1
MAX

4X 4°-15°

0.20 TYP
0.08

SEE DETAIL A

0.25

GAGE PLANE

0°- 8°

0.6
0.3

0.1
0.0

DETAIL A
TYPICAL

4222047/E   07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

8X (1.05)

1

8X (0.45)

6X (0.65)

4

(R0.05)
TYP

SYMM

8

SYMM

5

(2.6)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

0.05 MAX
ALL AROUND

EXPOSED
METAL

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MIN
ALL AROUND

EXPOSED
METAL

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/E   07/2024

NOTES: (continued)
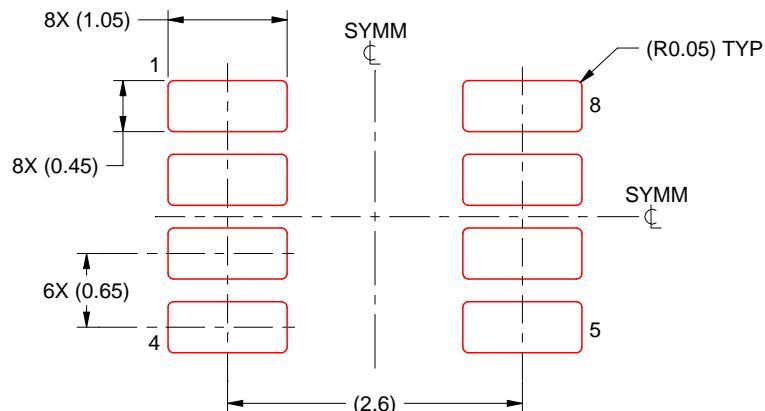
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (1.05)

1

8X (0.45)

6X (0.65)

4

SYMM

SYMM

(R0.05) TYP

8

5

(2.6)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E   07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

6.6 TYP
6.2

A

PIN 1 INDEX AREA

12X 0.65

1

14

2X
3.9

5.1
4.9
NOTE 3

7

8

14X 0.30
0.17

B

4.5
4.3
NOTE 4

⊕ 0.1 Ⓜ C A B

SEATING PLANE

C

◯ 0.1 C

4X (0°-12°)

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0.15
0.05

0°-8°

0.75
0.50

DETAIL A
TYPICAL

4220202/B   12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

PW0014A

TSSOP - 1.2 mm max height

14X (1.5)

SYMM

1

14X (0.45)

(R0.05) TYP

14

SYMM

12X (0.65)

7

8

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220202/B   12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

14X (1.5)

SYMM

1

14X (0.45)

(R0.05) TYP

14

SYMM

12X (0.65)

7

8

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B   12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
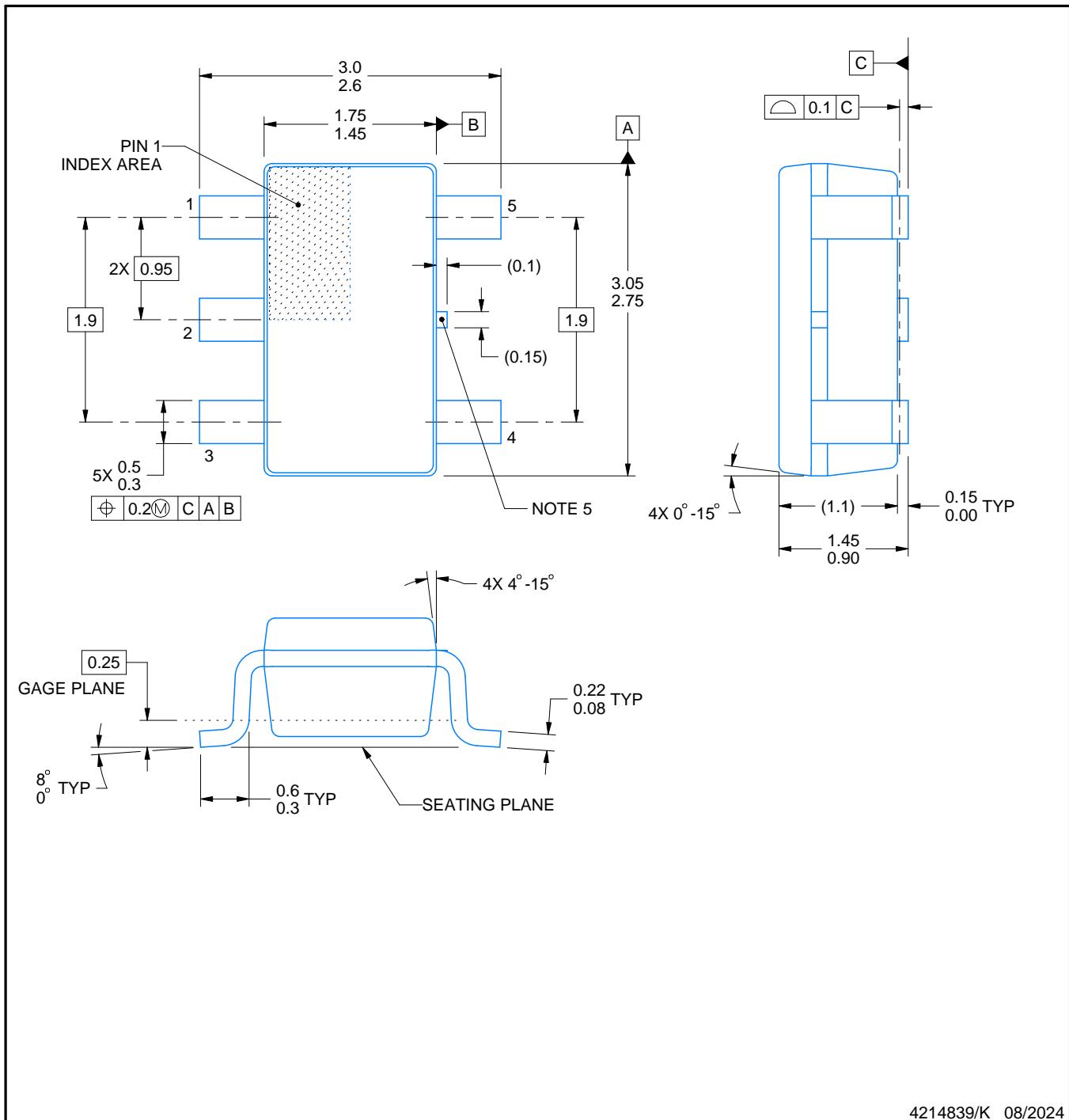
4214839/K   08/2024

NOTES:
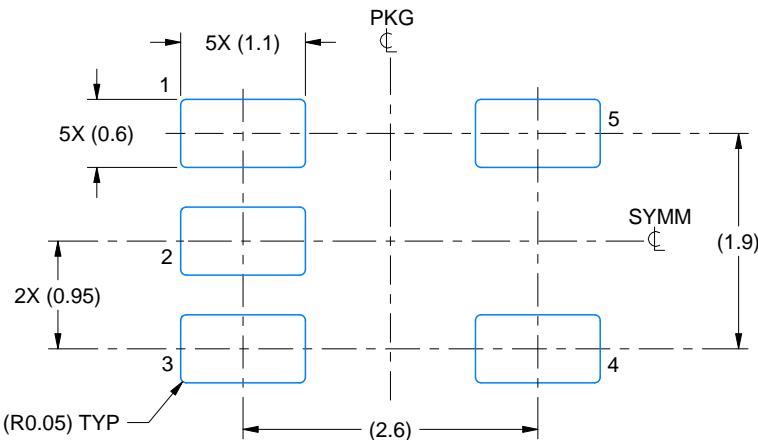
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.
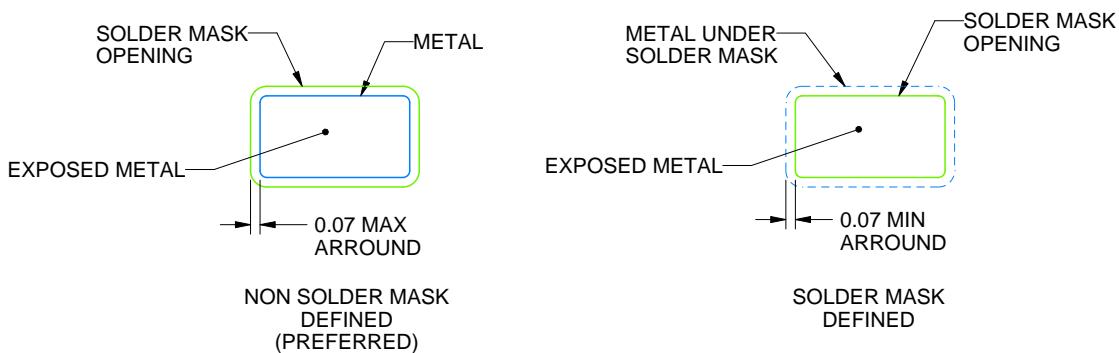
PKG

5X (1.1)

1

5X (0.6)

2

2X (0.95)

3

(R0.05) TYP

5

SYMM

(1.9)

4

(2.6)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214839/K   08/2024

NOTES: (continued)
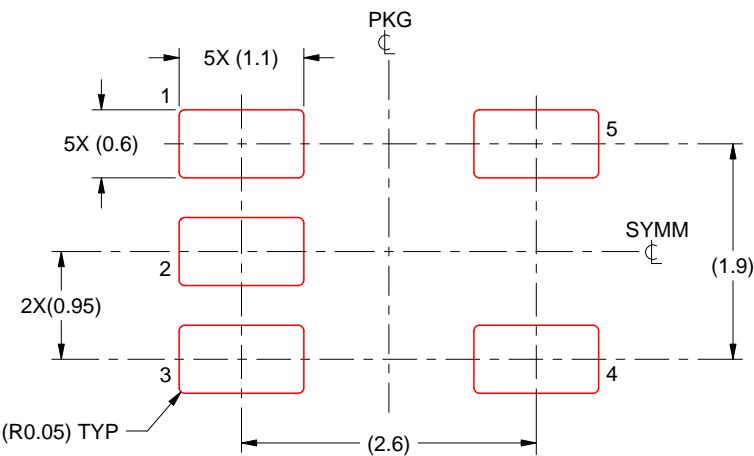
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PKG

5X (1.1)

1

5X (0.6)

5

SYMM

2

(1.9)

2X(0.95)

3

4

(R0.05) TYP

(2.6)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

4214862/A 04/2023
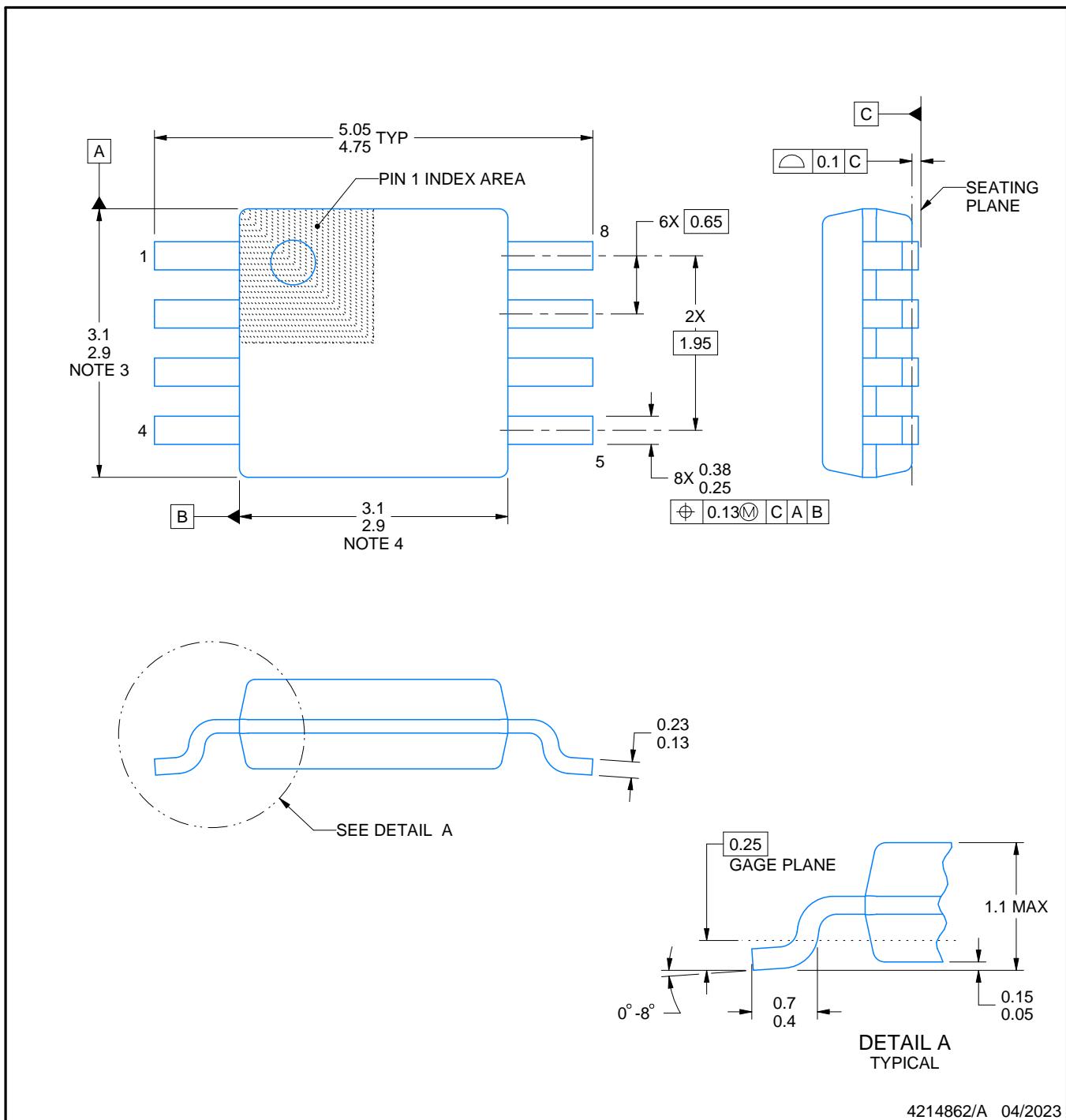
PowerPAD is a trademark of Texas Instruments.
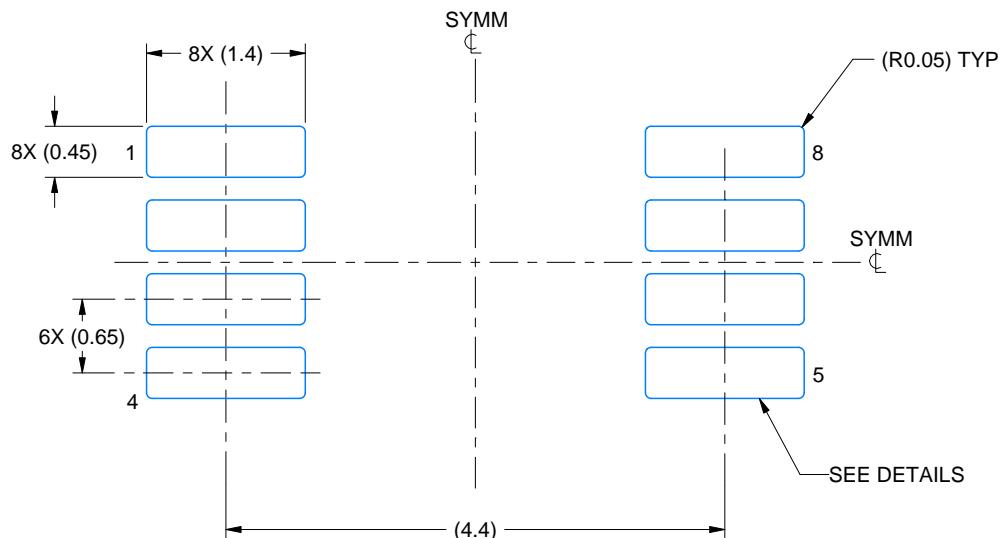
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

SYMM

8X (1.4)

8X (0.45) 1

(R0.05) TYP

8

SYMM

6X (0.65)

4

5

SEE DETAILS

(4.4)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214862/A   04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown
   on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

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SYMM

8X (1.4)

(R0.05) TYP

8X (0.45)   1

8

SYMM

6X (0.65)

4

5

(4.4)

SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A   04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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