MC9S12XDP512
Device User Guide
V01.12

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Semiconductor Products Sector
Motorola, Inc.

freescale™
semiconductor

Freescale Semiconductor, Inc.

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.00	02 Jun 03			Initial Version
V01.01	22. Jul 03			• Moved EWAIT function to PK7 • Added ECLKX2 function to PE7 • Moved TAGHI input to PE6 • Moved TAGLO input to PE5 • Corrected typo in figure 1-2 • Added Freeze Mode to section 4 • Modified PLL electrical parameters to TBD • Added four seperate interrupt vectors for PIT • Removed Regulator Current and Output Voltage Core and Output Voltage PLL from Table 27-2 • NVM Timing Characteristics Table A-11 maximum $f_{NVMOSC} = 80MHz$ • Modified ATD Operating Characteristics Table A-8 and A-9 to TBD • SPI Timing Characteristics set to TBD
V01.02	16.Aug 03			• Added XSRAM20K control register to memory map • Added XSRAM20K interrupt vector • Included XSRAM20K Block Guide • Added XGATE Software Trigger to **Table 5-1** • Added section **4.2.5 Register visibility in Emulation and Expanded modes**
V01.03	23. Aug 03			• Removed BDLC from **Table 5-1**

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.04	01.Sep 2003			• Corrected Table 0-1 Document References • Corrected Maskset number • Added Connectivity of NV bits in FCTL Register (FTX512k4) • corrected **Table 5-1** and added XGATE Software Error Interrupt
V01.05	22. Oct 2003			• Added EROMCTL functionality • Added XGATE Channel ID's to **Table 5-1** • Aded 3.3V/5V Operation on PC/PD/PE5 and PE6 • Added Pullup Devices on RESET/TEST and VREGEN Pin • Added ROMON/EROMON Description to **4.2 Chip Configuration Summary** • Removed Security Description
V01.06	10. Nov 2003			• updated section **4.2 Chip Configuration Summary** • updated section **4.2.5 Register visibility in Emulation and Expanded modes** • corrected $\overline{\text{XCLKS}}$ description • Added IQSTAT3 signal • Added SPI Master/Slave Mode Timing Characteristics • Renamed VDDX3/VSSX3 to VDDR2/VSSR2 and VDDR/VSSR to VDDR1/VSSR1 • Corrected several typos
V01.07				• Modiefied PD0-PD3 pin order
V01.08	29. Jan 2004			• Added **Section 1.6 Detailed Register Map** • BDM is visible on PPAGE=$FF at address $BF00-$BFFF if bdm active **Figure 1-3** • Modified XGATE Register Space $0380 - $03BF **Table 1-1** • Added LQFP144 PCB recommendation **Figure 28-1** • Updated Voltage Regulator Electrical Characteristics
V01.09	10. Feb 2004			• Added 3.3V I/O Characteristics
V01.10	28. Feb 2004			• Added 3.3V ATD Characteristics • Added IrDA to SCI feature List
V01.11	30. Mar 2004			• Added Internal Visibility Data to **Table 2-1** and to Signal Description • Added **Figure 1-2** Logical to Global Address Mapping

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.12	15. April 2004			• Modified **Table 15-1** COP Comfiguration • Change description for reduced input voltage thresholds on Port C, D and E and added I/O Characteristics **Table A-8**

The electrical characteristics given in Appendix A are preliminary and are subject to change.

For More Information On This Product,
Go to: www.freescale.com

Ordering Information

The following figure provides an ordering number example for the MC9S12XD-Family devices.

```
MC9S12X DP512   C FU
```

→ Package Option
→ Temperature Option
→ Device Title
→ Controller Family

Temperature Options
```
C = -40˚C to  85˚C
V = -40˚C to 105˚C
M = -40˚C to 125˚C
```

Package Options
```
FU =  80  QFP
PV = 112 LQFP
FV = 144 LQFP
```
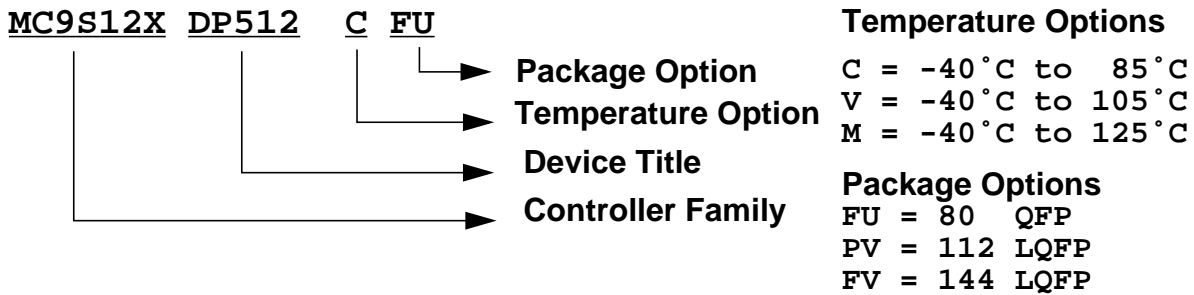
Figure 0-1 Order Partnumber Example

Document References

The Device Guide provides information about the MC9S12XDP512 device made up of standard HCS12 blocks and the HCS12 processor core.

This document is part of the customer documentation. A complete set of device manuals includes all the individual Block Guides of the implemented modules. In an effort to reduce redundancy all module specific information is located only in the respective Block Guide. If applicable, special implementation details of the module are given in the block description sections of this document.

See **Table 0-1** for names and versions of the referenced documents throughout the Device User Guide.

Table 0-1 Document References

User Guide	Version	Document Order Number
S12XCPU Reference Manual	V01	S12XCPUV1/D
External Bus Interface (S12XEBI) Block Guide	V01	S12XEBIV1/D
Module Mapping Control (S12XMMC) Block Guide	V01	S12XMMCV1/D
Interrupt (S12XINT) Block Guide	V01	S12XINTV1/D
Background Debug (S12XBDM) Block Guide	V01	S12XBDMV1/D
Debug (S12XDBG) Block Guide	V01	S12XDBGV1/D
Security (S12X9SEC) Block Guide	V01	S12X9SECV1/D
Clock and Reset Generator (CRG) Block User Guide	V05	S12CRGV5/D
Enhanced Capture Timer (ECT_16B8C) Block User Guide	V02	S12ECT16B8CV2/D
Analog to Digital Converter 10 Bit 16 Channel (ATD_10B16C) Block UserGuide	V04	S12ATD10B16CV4/D
Analog to Digital Converter 10 Bit 8 Channels (ATD_10B8C) Block User Guide	V03	S12ATD10B8CV3/D
Inter IC Bus (IIC) Block User Guide	V02	S12IICV2/D
Asynchronous Serial Interface (SCI) Block User Guide	V05	S12SCIV5/D
Serial Peripheral Interface (SPI) Block User Guide	V03	S12SPIV3/D

User Guide	Version	Document Order Number
Pulse Width Modulator 8 Bit 8 Channel (PWM_8B8C) Block User Guide	V01	S12PWM8B8CV1/D
512 K Byte Flash (FTX512K4) Block User Guide	V01	S12FTX512K4V1/D
4K Byte EEPROM (EETX4K) Block User Guide	V01	S12EETX4KV1/D
XGATE Block User Guide	V01	S12XGATEV1/D
Motorola Scalable CAN (MSCAN) Block User Guide	V03	S12MSCANV3/D
Voltage Regulator (VREG_3V3) Block User Guide	V03	S12VREG_3V3/D
Port Integration Module (PIM_9XD512) Block User Guide	V01	S12XDP512PIMV1/D
Oscillator (OSC_LCP) Block Guide	V01	S12OSCLCPV1/D
20K Byte SRAM XSRAM20K	V01	S12XSRAM20KV1/D
Periodic Interrupt Timer (PIT_24B4C) Block Guide	V01	S12PIT24B4CV1/D

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Section 1 Introduction

1.1 Overview

The MC9S12XD family will retain the low cost, power consumption, EMC and code-size efficiency advantages currently enjoyed by users of Motorola's existing 16-Bit MC9S12 MCU family.

Based around an enhanced S12 core, the MC9S12XD-Family will deliver 2 to 5 times the performance of a 25MHz S12 whilst retaining a high degree of pin and code compatibility with the S12.

The MC9S12XD-Family introduces the performance boosting XGATE module. Using enhanced DMA functionality, this parallel processing module offloads the CPU by providing high speed data processing and transfer between peripheral modules, RAM and I/O ports. Providing up to 80MIPS of performance additional to the CPU, the XGATE can access all peripherals and the RAM block.

The MC9S12XDP512 is composed of standard on-chip peripherals including 512Kbytes of Flash EEPROM, 20K bytes of RAM, 4K bytes of EEPROM, six asynchronous serial communications interfaces (SCI), three serial peripheral interfaces (SPI), an 8-channel IC/OC enhanced capture timer, an 8-channel, 10-bit analog-to-digital converter, a 16-channel, 10-bit analog-to-digital converters, an 8-channel pulse-width modulator (PWM), five   CAN 2.0 A, B software compatible modules (MSCAN12), two Inter-IC Bus blocks and a Periodic Interrupt Timer. The MC9S12XDP512 has full 16-bit data paths throughout. The non-multiplexed expanded bus interface available on the 144-Pin versions allows an easy interface to external memories.

The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. System power consumption can be further improved with the new "fast exit from STOP mode" feature.

In addition to the I/O ports available in each module, up to 25 further I/O ports are available with interrupt capability allowing Wake-Up from STOP or WAIT mode.

The MC9S12XDP512 will be available in 144-Pin LQFP with external bus interface and in 112-Pin LQFP or 80-Pin QFP package without external bus interface.

1.2 Features

- HCS12X Core
    - 16-bit HCS12X CPU
        i. Upward compatible with MC9S12 instruction set
        ii. Interrupt stacking and programmer's model identical to MC9S12
        iii. Instruction queue
        iv. Enhanced indexed addressing
        v. Enhanced instruction set
    - EBI (External Bus Interface)

- – MMC (Module Mapping Control)

  – INT (Interrupt Controller)

  – DBG (Debug module to monitor HCS12X CPU and XGATE bus activity)

  – BDM (Background Debug Mode)

- XGATE

  – Peripheral Co-Processor

  – Parallel processing module offloads the CPU by providing high speed data processing transfer between peripheral modules, RAM and I/O ports

- PIT Periodic Interrupt Timer

  – Four Timers with independent time-out periods

  – Time-out periods selectable between 1 and 2^{24} bus clock cycles

- CRG

  – Low Noise/Low Power Pierce oscillator

  – PLL

  – COP watchdog

  – Real time interrupt

  – Clock Monitor

  – Fast Wake-up from Stop Mode

- 8-bit ports with interrupt functionality

  – Digital filtering

  – Programmable rising or falling edge trigger

- Memory

  – 512K Flash EEPROM

  – 4K byte EEPROM

  – 20K byte RAM

- One 8-channel and one 16 channel Analog-to-Digital Converter

  – 10-bit resolution

  – External conversion trigger capability

- Five 1M bit per second, CAN 2.0 A, B software compatible modules

  – Five receive and three transmit buffers

  – Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit

  – Four separate interrupt channels for Rx, Tx, error and wake-up

  – Low-pass filter wake-up function

– Loop-back for self test operation

- Enhanced Capture Timer

  – 16-bit main counter with 7-bit prescaler

  – 8 programmable input capture or output compare channels

  – Four 8-bit or two 16-bit pulse accumulators

- 8 PWM channels

  – Programmable period and duty cycle

  – 8-bit 8-channel or 16-bit 4-channel

  – Separate control for each pulse width and duty cycle

  – Center-aligned or left-aligned outputs

  – Programmable clock select logic with a wide range of frequencies

  – Fast emergency shutdown input

  – Usable as interrupt inputs

- Serial interfaces

  – Six asynchronous Serial Communication Interfaces (SCI) with additional LIN support and selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths

  – Three Synchronous Serial Peripheral Interfaces (SPI)

- Two Inter-IC Bus modules (IIC)

  – Compatible with I2C Bus standard

  – Multi-master operation

  – Software programmable for one of 256 different serial clock frequencies

- On chip Voltage Regulator

  – Two parallel, linear voltage regulators with bandgap reference

  – Low Voltage detect (LVD) with Low Voltage Interrupt (LVI)

  – Power On Reset (POR) circuit

  – 3.3V - 5.5V operation

  – Low Voltage Reset (LVR)

  – Ultra Low Power Wake-up Timer

- 144 Pin LQFP, 112-Pin LQFP package and 80-Pin QFP package

  – I/O lines with 5V input and drive capability

  – Input threshold on external bus interface inputs switchable for 3.3V or 5V operation

  – 5V A/D converter inputs

  – Operation at 80MHz equivalent to 40MHz Bus Speed

- Development support
  - Single-wire background debug™ mode (BDM)
  - 4 on-chip hardware breakpoints

1.3 Modes of Operation

User modes

- Normal and Emulation Operating Modes
  - Normal Single-Chip Mode
  - Normal Expanded Mode
  - Emulation of Single Chip Mode
  - Emulation of Expanded Mode
- Special Operating Modes
  - Special Single-Chip Mode with active Background Debug Mode
  - Special Test Mode (**Motorola use only**)

Low power modes

- Stop Mode
- Pseudo Stop Mode
- Wait Mode

1.4 Block Diagram

Figure 1-1 shows a block diagram of the MC9S12XDP512 device.

Figure 1-1 MC9S12XDP512 Block Diagram

NXP

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512K Byte Flash

20K Byte RAM

4K Byte EEPROM

VDDR →
VSSR →
VREGEN ←
VDD1,2 ←
VSS1,2 ←

Voltage Regulator

BKGD ← Single-wire Background Debug Module

CPU12X

XFC ←
VDDPLL ←
VSSPLL ←
EXTAL →
XTAL ←
RESET →
TEST →

PLL — Clock and Reset Generation Module

Periodic Interrupt
COP Watchdog
Clock Monitor
Breakpoints

PTE / DDRE:
PE0 → XIRQ
PE1 → IRQ
PE2 ↔ R/W/WE
PE3 ↔ LSTRB/LDS/EROMCTL
PE4 ↔ ECLK
PE5 ↔ MODA/RE/TAGLO
PE6 ↔ MODB/TAGHI
PE7 ↔ ECLKX2/XCLKS

PTK / DDRK:
ADDR16 PK0 ↔ IQSTAT0
ADDR17 PK1 ↔ IQSTAT1
ADDR18 PK2 ↔ IQSTAT2
ADDR19 PK3 ↔ IQSTAT3
ADDR20 PK4 ↔
ADDR21 PK5 ↔
ADDR22 PK6 ↔ NOACC
EWAIT PK7 ↔ ROMCTL/EWAIT

8 Bit PPAGE Allows 4MByte Program space

PTA / DDRA:
ADDR15 PA7 ↔
ADDR14 PA6 ↔
ADDR13 PA5 ↔
ADDR12 PA4 ↔
ADDR11 PA3 ↔
ADDR10 PA2 ↔
ADDR9 PA1 ↔
ADDR8 PA0 ↔

PTB / DDRB:
ADDR7 PB7 ↔
ADDR6 PB6 ↔
ADDR5 PB5 ↔
ADDR4 PB4 ↔
ADDR3 PB3 ↔
ADDR2 PB2 ↔
ADDR1 PB1 ↔
UDS ADDR0 PB0 ↔

PTC / DDRC:
DATA15 PC7 ↔
DATA14 PC6 ↔
DATA13 PC5 ↔
DATA12 PC4 ↔
DATA11 PC3 ↔
DATA10 PC2 ↔
DATA9 PC1 ↔
DATA8 PC0 ↔

PTD / DDRD:
DATA7 PD7 ↔
DATA6 PD6 ↔
DATA5 PD5 ↔
DATA4 PD4 ↔
DATA3 PD3 ↔
DATA2 PD2 ↔
DATA1 PD1 ↔
DATA0 PD0 ↔

Non-Multiplexed External Bus Interface (EBI)

Timer 4 channel 16 bit with Prescaler for internal timebases

SCI3: RXD / TXD

Digital Supply 2.5V
VDD1,2 ←
VSS1,2

PLL Supply 2.5V
VDDPLL ←
VSSPLL

Analog Supply 3-5V
VDDA →
VSSA

I/O Supply 3-5V
VDDX1,2 →
VSSX1,2

Voltage Regulator 3-5V
VDDR1,2 →
VSSR1,2

SCI4: RXD / TXD
SCI5: RXD / TXD

ATD0:
VRH ←
VRL ←
VDDA ←
VSSA ←
AN0 ↔ PAD00
AN1 ↔ PAD01
AN2 ↔ PAD02
AN3 ↔ PAD03
AN4 ↔ PAD04
AN5 ↔ PAD05
AN6 ↔ PAD06
AN7 ↔ PAD07
(DDRAD0 & AD0)

ATD1:
VRH ← VRH
VRL ← VRL
VDDA ← VDDA
VSSA ← VSSA
AN0 ↔ PAD08
AN1 ↔ PAD09
AN2 ↔ PAD10
AN3 ↔ PAD11
AN4 ↔ PAD12
AN5 ↔ PAD13
AN6 ↔ PAD14
AN7 ↔ PAD15
AN8 ↔ PAD16
AN9 ↔ PAD17
AN10 ↔ PAD18
AN11 ↔ PAD19
AN12 ↔ PAD20
AN13 ↔ PAD21
AN14 ↔ PAD22
AN15 ↔ PAD23
(DDRAD1 & AD1)

Enhanced Multilevel Interrupt Module

XGATE Peripheral Co-Processor

Enhanced Capture Timer:
IOC0 ↔ PT0
IOC1 ↔ PT1
IOC2 ↔ PT2
IOC3 ↔ PT3
IOC4 ↔ PT4
IOC5 ↔ PT5
IOC6 ↔ PT6
IOC7 ↔ PT7
(DDRT / PTT)

SCI0: RXD / TXD → PS0 / PS1
SCI1: RXD / TXD → PS2 / PS3
SPI0: MISO / MOSI / SCK / SS → PS4 / PS5 / PS6 / PS7
(DDRS / PTS)

CAN0: RXCAN / TXCAN
CAN1: RXCAN / TXCAN
CAN2: RXCAN / TXCAN
CAN3: RXCAN / TXCAN
CAN4: RXCAN / TXCAN

SCI2: RXD / TXD

Module to Port Routing:
PM0
PM1
PM2
PM3
PM4
PM5
PM6
PM7
(DDRM / PTM)

IIC1: SDA / SCL
IIC0: SDA / SCL

PWM:
PWM0 — KWP0 ↔ PP0
PWM1 — KWP1 ↔ PP1
PWM2 — KWP2 ↔ PP2
PWM3 — KWP3 ↔ PP3
PWM4 — KWP4 ↔ PP4
PWM5 — KWP5 ↔ PP5
PWM6 — KWP6 ↔ PP6
PWM7 — KWP7 ↔ PP7
(DDRP / PTP)

KWJ0 ↔ PJ0
KWJ1 ↔ PJ1
KWJ2 ↔ PJ2 CS1
KWJ4 ↔ PJ4 CS0
KWJ5 ↔ PJ5 CS2
KWJ6 ↔ PJ6
KWJ7 ↔ PJ7
(DDRJ / PTJ)

SPI1: MISO / MOSI / SCK / SS
KWH0 ↔ PH0
KWH1 ↔ PH1
KWH2 ↔ PH2
KWH3 ↔ PH3

SPI2: MISO / MOSI / SCK / SS
KWH4 ↔ PH4
KWH5 ↔ PH5
KWH6 ↔ PH6
KWH7 ↔ PH7
(DDRH / PTH)

Signals shown in *Bold-Italics* are neither available on the 112 Pin nor on the 80 Pin Package Option
Signals shown in **Bold** are not available on the 80 Pin Package

1.5 Device Memory Map

Table 1-1 and **Figure 1-3** show the device memory map of the MC9S12XDP512.

Table 1-1 Device Memory Map

Address	Module	Size (Bytes)
$0000 - $0009	Port Integration Module (Ports A, B, C, D, E)	10
$000A -$000B	EBI (EIFCTL, MODE)	2
$000C -$000D	Port Integration Module (PUCR, RDRIV)	2
$000E - $000F	EBI (Reserved Register Space)	2
$0010 - $0017	MMC (Page Register)	8
$0018 - $0019	Reserved	2
$001A - $001B	Device ID register (PARTID)	2
$001C - $001D	Reserved	2
$001E - $001F	Port Integration Module	2
$0020 - $002F	DBG Module	16
$0030 - $0031	MMC	2
$0032 - $0033	Port Integration Module (Port K)	2
$0034 - $003F	Clock and Reset Generator	12
$0040 - $007F	Enhanced Capture Timer 16-bit 8 channels	64
$0080 - $00AF	Analog to Digital Converter 10-bit 16 channel(ATD1)	48
$00B0 - $00B7	Inter IC Bus (IIC1)	8
$00B8 - $00BF	Serial Communications Interface (SCI2)	8
$00C0 - $00C7	Serial Communications Interface (SCI3)	8
$00C8 - $00CF	Serial Communications Interface (SCI0)	8
$00D0 - $00D7	Serial Communications Interface (SCI1)	8
$00D8 - $00DF	Serial Peripheral Interface (SPI0)	8
$00E0 - $00E7	Inter IC Bus (IIC0)	8
$00E8 - $00EF	Reserved	8
$00F0 - $00F7	Serial Peripheral Interface (SPI1)	8
$00F8 - $00FF	Serial Peripheral Interface (SPI2)	8
$0100- $010F	Flash Control Register	16
$0110 - $011B	EEPROM Control Register	12
$011C - $011F	XSRAM Control Register	4
$0120 - $012F	Interrupt Module (INT)	16
$0130 - $0137	Serial Communications Interface (SCI4)	8
$0138 - $013F	Serial Communications Interface (SCI5)	8
$0140 - $017F	Motorola Scalable Can (CAN0)	64

Table 1-1 Device Memory Map

Address	Module	Size (Bytes)
$0180 - $01BF	Motorola Scalable Can (CAN1)	64
$01C0 - $01FF	Motorola Scalable Can (CAN2)	64
$0200 - $023F	Motorola Scalable Can (CAN3)	64
$0240 - $027F	Port Integration Module (PIM)	64
$0280 - $02BF	Motorola Scalable Can (CAN4)	64
$02C0 - $02DF	Analog to Digital Converter 10bit 8channel (ATD0)	32
$02E0 - $02EF	Reserved	16
$02F0 - $02F7	Voltage Regulator	8
$02F8 - $02FF	Reserved	8
$0300 - $0327	Pulse Width Modulator 8 Channels	40
$0328 - $033F	Reserved	24
$0340 - $0367	Periodic Interrupt Timer	40
$0368 - $037F	Reserved	24
$0380 - $03BF	XGATE	64
$03C0 - $07FF	Reserved	1024
$0800 - $0BFF	1K paged EEPROM	1024
$0C00 - $0FFF	1K unpaged EEPROM	1024
$1000 - $1FFF	4K paged SRAM	4096
$2000 - $3FFF	8K unpaged SRAM	8192
$4000 - $7FFF	Fixed Flash EEPROM Array	16384
$8000 - $BFFF	Flash EEPROM Page Window	16384
$C000 - $FFFF	Fixed Flash EEPROM Array	16384

*Reserved register space shown in **Table 1-1** is register space which is not allocated to any module. This register space is reserved for future use. Writing to these locations have no effect. Read access to these locations returns zero.*

Figure 1-2 Logical to Global Address Mapping
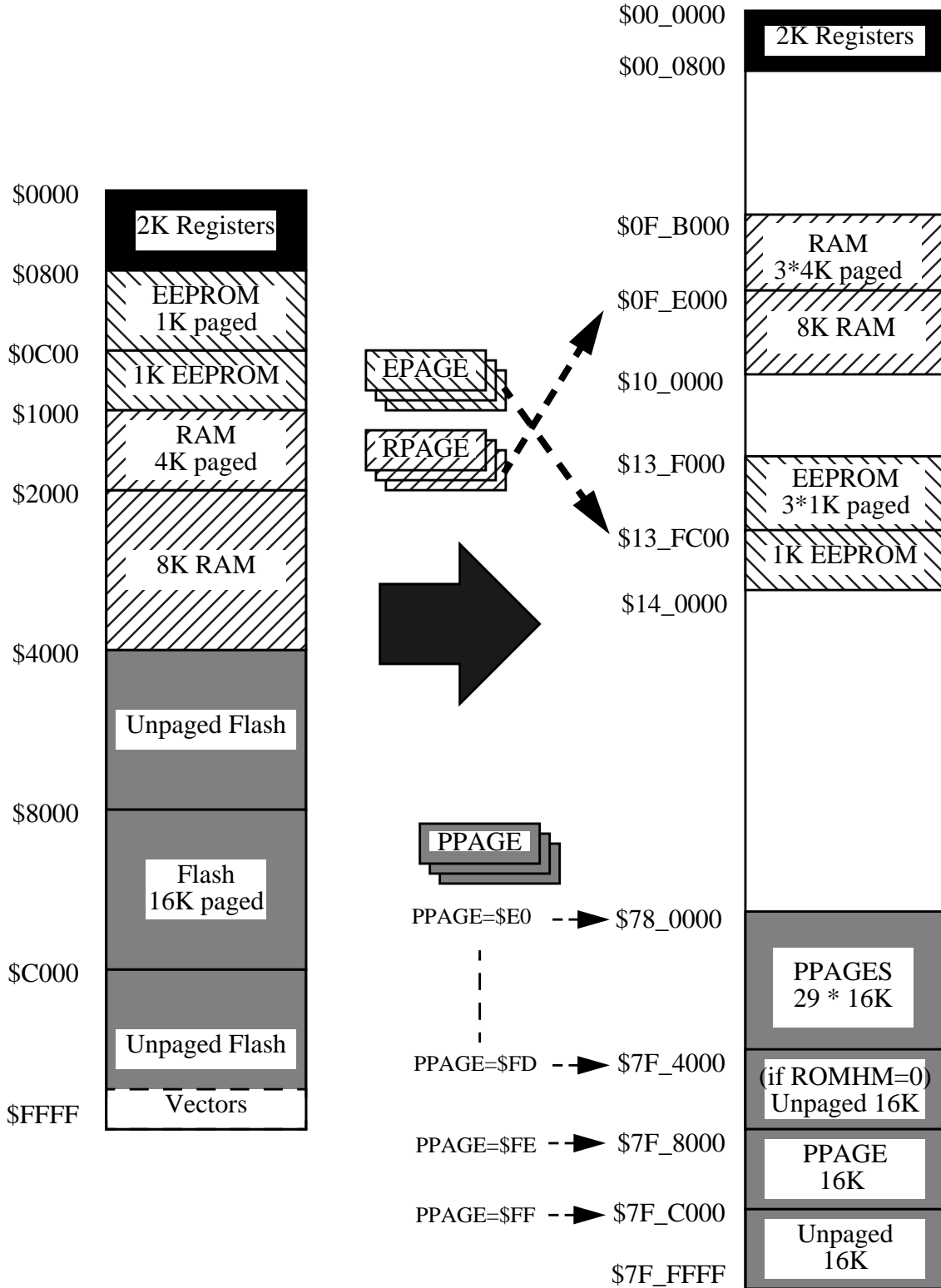
Figure 1-3 MC9S12XDP512 Memory Map

$0000 – $07FF	2K Register Space
$0800 – $0FFF	4K Bytes EEPROM four * 1K pages accessible through $0800 - $0BFF
$1000 – $3FFF	20K Bytes RAM five * 4K pages accessible through $1000 - $1FFF
$4000	1K, 2K, 4K or 8K Protected Sector
$4000 – $7FFF	16K Fixed Flash EEPROM
$8000 – $BFFF	16K Page Window thirtytwo * 16K Flash EEPROM Pages
$BF00 – $BFFF	BDM visible on PPAGE = $FF (If Active)
$C000 – $FFFF	16K Fixed Flash EEPROM
	2K, 4K, 8K or 16K Protected Boot Sector
$FF00 – $FFFF	BDM (If Active, except for specific BDM hardware commands, for details refer to BDM BlockGuide)

NORMAL SINGLE CHIP EXPANDED SPECIAL SINGLE CHIP

1.6 Detailed Register Map

The following tables show the detailed register map of the MC9S12XDP512.

$0000 - $0009   **Port Integration Module (PIM) Map 1 of 5**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0000	PORTA	Read: Write:	PA 7	PA6	PA5	PA4	PA3	PA2	PA1	PA 0
$0001	PORTB	Read: Write:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
$0002	DDRA	Read: Write:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
$0003	DDRB	Read: Write:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0

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$0000 - $0009   **Port Integration Module (PIM) Map 1 of 5**

$0004	PORTC	Read: Write:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
$0005	PORTD	Read: Write:	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
$0006	DDRC	Read: Write:	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
$0007	DDRD	Read: Write:	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
$0008	PORTE	Read: Write:	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
$0009	DDRE	Read: Write:	DDRE7	DDRE6	DDRE5	DDRE4	DDRE3	DDRE2	0	0

$000A - $000B   **External Bus Interface (S12XEBI) Map 1 of 2**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$000A	EIFCTL	Read: Write:	CS2E	CS1E	CS0E	NECLK	EDIV1	EDIV0	NCLKX2	EWAIT
$000B	MODE	Read: Write:	MODC	MODB	MODA	ITHRS	IVIS	0	0	0

$000C - $000D   **Port Integration Module (PIM) Map 2 of 5**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$000C	PUCR	Read: Write:	PUPKE	BKPUE	0	PUPEE	PUPDE	PUPCE	PUPBE	PUPAE
$000D	RDRIV	Read: Write:	RDPK	0	0	RDPE	RDPD	RDPC	RDPB	RDPA

$000E - $000F   **External Bus Interface (S12XEBI) Map 2 of 2**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$000E	Reserved	Read: Write:	0	0	0	0	0	0	0	0
$000F	Reserved	Read: Write:	0	0	0	0	0	0	0	0

$0010 - $0017   **Module Mapping Control (S12XMMC) Map 1 of 2**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0010	ITCR	Read: Write:	0	GP6	GP5	GP4	GP3	GP2	GP1	GP0
$0011	Reserved	Read: Write:	0	0	0	0	0	0	0	0
$0012	DIRECT	Read: Write:	DP15	DP14	DP13	DP12	DP11	DP10	DP9	DP8
$0013	MISC	Read: Write:	0	0	0	EROMON	EXSTR1	EXSTR0	ROMHM	ROMON

$0010 - $0017 **Module Mapping Control (S12XMMC) Map 1 of 2**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0014	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0015	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0016	RPAGE	Read:	RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0
		Write:								
$0017	EPAGE	Read:	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0
		Write:								

$0018 - $001B **Miscellaneous Peripheral**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0018	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0019	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$001A	PARTIDH	Read:	1	1	0	0	0	1	0	0
		Write:								
$001B	PARTIDL	Read:	0	0	0	0	0	0	0	0
		Write:								

$001C - $001D **Reserved**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$001D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$001E - $001F **Port Integration Module (PIM) Map 3 of 5**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001E	IRQCR	Read:	IRQE	IRQEN	0	0	0	0	0	0
		Write:	IRQE	IRQEN						
$001F	Reserved	Read:	0	0	0	0	0	0	0	
		Write:								

$0020 - $0027 **Debug Module (S12XDBG) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0020	DBGC1	Read:	ARM	0	XGSBPE	BDM	DBGBRK		COMRV	
		Write:		TRIG						
$0021	DBGSR	Read:	TBF	EXTF	0	0	0	SSF2	SSF1	SSF0
		Write:								
$0022	DBGTCR	Read:	TSOURCE		TRANGE		TRCMOD		TALIGN	
		Write:								

$0020 - $0027   Debug Module (S12XDBG) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0023	DBGC2	Read:	0	0	0	0	CDCM		ABCM	
		Write:								
$0024	DBGTBH	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
$0025	DBGTBL	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
$0026	DBGCNT	Read:	0	CNT						
		Write:								
$0027	DBGSCRX	Read:	0	0	0	0	SC3	SC2	SC1	SC0
		Write:								
$0028	DBGXCTL (COMPA/C)	Read:	0	NDB	TAG	0	RW	RWE	SRC	COMPE
		Write:								
$0028	DBGXCTL (COMPB/D)	Read:	SZE	SZ	TAG	0	RW	RWE	SRC	COMPE
		Write:								
$0029	DBGXAH	Read:	0	Bit 22	21	20	19	18	17	Bit 16
		Write:								
$002A	DBGXAM	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$002B	DBGXAL	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$002C	DBGXDH	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$002D	DBGXDL	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$002E	DBGXDHM	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$002F	DBGXDLM	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0030 - $0031   Module Mapping Control (S12XMMC) Map 2of 2

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0030	PPAGE	Read:	PIX7	PIX6	PIX5	PIX4	PIX3	PIX2	PIX1	PIX0
		Write:								
$0031	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0032 - $0033   Port Integration Module (PIM) Map 4 of 5

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0032	PORTK	Read:	PK7	PK6	PK5	PK4	PK3	PK2	PK1	PK0
		Write:								
$0033	DDRK	Read:	DDRK7	DDRK6	DDRK5	DDRK4	DDRK3	DDRK2	DDRK1	DDRK0
		Write:								

$0034 - $003F   Clock and Reset Generator (CRG) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0034	SYNR	Read:	0	0	SYN5	SYN4	SYN3	SYN2	SYN1	SYN0
		Write:			SYN5	SYN4	SYN3	SYN2	SYN1	SYN0
$0035	REFDV	Read:	0	0	0	0	REFDV3	REFDV2	REFDV1	REFDV0
		Write:					REFDV3	REFDV2	REFDV1	REFDV0
$0036	CTFLG	Read:	0	0	0	0	0	0	0	0
		Write:	Reserved For Factory Test							
$0037	CRGFLG	Read:	RTIF	PORF	LVRF	LOCKIF	LOCK	TRACK	SCMIF	SCM
		Write:	RTIF	PORF	LVRF	LOCKIF			SCMIF	
$0038	CRGINT	Read:	RTIE	ILAF	0	LOCKIE	0	0	SCMIE	0
		Write:	RTIE	ILAF		LOCKIE			SCMIE	
$0039	CLKSEL	Read:	PLLSEL	PSTP	0	ROAWAI	PLLWAI	CWAI	RTIWAI	COPWAI
		Write:	PLLSEL	PSTP		ROAWAI	PLLWAI	CWAI	RTIWAI	COPWAI
$003A	PLLCTL	Read:	CME	PLLON	AUTO	ACQ	FSTWKP	PRE	PCE	SCME
		Write:	CME	PLLON	AUTO	ACQ	FSTWKP	PRE	PCE	SCME
$003B	RTICTL	Read:	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		Write:	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
$003C	COPCTL	Read:	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		Write:	WCOP	RSBCK				CR2	CR1	CR0
$003D	FORBYP	Read:	0	0	0	0	0	0	0	0
		Write:	Reserved For Factory Test							
$003E	CTCTL	Read:	0	0	0	0		0	0	0
		Write:	Reserved For Factory Test							
$003F	ARMCOP	Read:	0	0	0	0	0	0	0	0
		Write:	Bit 7	6	5	4	3	2	1	Bit 0

$0040 - $007F   Enhanced Capture Timer 16 Bit 8 Channels (ECT) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0040	TIOS	Read:	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
		Write:	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
$0041	CFORC	Read:	0	0	0	0	0	0	0	0
		Write:	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0
$0042	OC7M	Read:	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
		Write:	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
$0043	OC7D	Read:	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0
		Write:	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0
$0044	TCNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0045	TCNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0046	TSCR1	Read:	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
		Write:	TEN	TSWAI	TSFRZ	TFFCA	PRNT			
$0047	TTOV	Read:	TOV7	TOV6	TOV5	TOV4	TOV3	TOV2	TOV1	TOV0
		Write:	TOV7	TOV6	TOV5	TOV4	TOV3	TOV2	TOV1	TOV0
$0048	TCTL1	Read:	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
		Write:	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
$0049	TCTL2	Read:	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
		Write:	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0

$0040 - $007F

Enhanced Capture Timer 16 Bit 8 Channels (ECT) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$004A	TCTL3	Read: Write:	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
$004B	TCTL4	Read: Write:	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
$004C	TIE	Read: Write:	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
$004D	TSCR2	Read: Write:	TOI	0	0	0	TCRE	PR2	PR1	PR0
$004E	TFLG1	Read: Write:	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
$004F	TFLG2	Read: Write:	TOF	0	0	0	0	0	0	0
$0050	TC0 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0051	TC0 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0052	TC1 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0053	TC1 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0054	TC2 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0055	TC2 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0056	TC3 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0057	TC3 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0058	TC4 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0059	TC4 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$005A	TC5 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$005B	TC5 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$005C	TC6 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$005D	TC6 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$005E	TC7 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$005F	TC7 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0060	PACTL	Read: Write:	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
$0061	PAFLG	Read: Write:	0	0	0	0	0	0	PAOVF	PAIF
$0062	PACN3 (hi)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

$0040 - $007F   **Enhanced Capture Timer 16 Bit 8 Channels (ECT) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0063	PACN2 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0064	PACN1 (hi)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0065	PACN0 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0066	MCCTL	Read: Write:	MCZI	MODMC	RDMCL	0 / ICLAT	0 / FLMC	MCEN	MCPR1	MCPR0
$0067	MCFLG	Read: Write:	MCZF	0	0	0	POLF3	POLF2	POLF1	POLF0
$0068	ICPAR	Read: Write:	0	0	0	0	PA3EN	PA2EN	PA1EN	PA0EN
$0069	DLYCT	Read: Write:	DLY7	DLY6	DLY5	DLY4	DLY3	DLY2	DLY1	DLY0
$006A	ICOVW	Read: Write:	NOVW7	NOVW6	NOVW5	NOVW4	NOVW3	NOVW2	NOVW1	NOVW0
$006B	ICSYS	Read: Write:	SH37	SH26	SH15	SH04	TFMOD	PACMX	BUFEN	LATQ
$006C	Reserved	Read: Write:	0	0	0	0	0	0	0	0
$006D	TIMTST	Read: Write:	0	0	0	0 Reserved For Factory Test	0	0	0	0
$006E	PTPSR	Read: Write:	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
$006F	PTMCPSR	Read: Write:	PTMPS7	PTMPS6	PTMPS5	PTMPS4	PTMPS3	PTMPS2	PTMPS1	PTMPS0
$0070	PBCTL	Read: Write:	0	PBEN	0	0	0	0	PBOVI	0
$0071	PBFLG	Read: Write:	0	0	0	0	0	0	PBOVF	0
$0072	PA3H	Read: Write:	PA3H7	PA3H6	PA3H5	PA3H4	PA3H3	PA3H2	PA3H1	PA3H0
$0073	PA2H	Read: Write:	PA2H7	PA2H6	PA2H5	PA2H4	PA2H3	PA2H2	PA2H1	PA2H0
$0074	PA1H	Read: Write:	PA1H7	PA1H6	PA1H5	PA1H4	PA1H3	PA1H2	PA1H1	PA1H 0
$0075	PA0H	Read: Write:	PA0H7	PA0H6	PA0H5	PA0H4	PA0H3	PA0H2	PA0H1	PA0H0
$0076	MCCNT (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0077	MCCNT (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0078	TC0H (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0079	TC0H (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$007A	TC1H (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$007B	TC1H (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

$0040 - $007F **Enhanced Capture Timer 16 Bit 8 Channels (ECT) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$007C	TC2H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$007D	TC2H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$007E	TC3H (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$007F	TC3H (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0080 - $00AF **Analog to Digital Converter 10-bit 16 Channels (ATD1) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0080	ATD1CTL0	Read:	0	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
		Write:								
$0081	ATD1CTL1	Read:	ETRIG SEL	0	0	0	ETRIG CH3	ETRIG CH2	ETRIG CH1	ETRIG CH0
		Write:								
$0082	ATD1CTL2	Read:	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ASCIF
		Write:								
$0083	ATD1CTL3	Read:	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		Write:								
$0084	ATD1CTL4	Read:	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		Write:								
$0085	ATD1CTL5	Read:	DJM	DSGN	SCAN	MULT	CD	CC	CB	CA
		Write:								
$0086	ATD1STAT0	Read:	SCF	0	ETORF	FIFOR	CC3	CC2	CC1	CC0
		Write:								
$0087	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0088	ATD1TEST0	Read:	U	U	U	U	U	U	U	U
		Write:	Reserved For Factory Test							
$0089	ATD1TEST1	Read:	0	0	0	0	0	0	0	0
		Write:	Reserved For Factory Test							
$008A	ATD1STAT2	Read:	CCF15	CCF14	CCF13	CCF12	CCF11	CCF10	CCF9	CCF8
		Write:								
$008B	ATD1STAT1	Read:	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		Write:								
$008C	ATD1DIEN0	Read:	IEN15	IEN14	IEN13	IEN12	IEN11	IEN10	IEN9	IEN8
		Write:								
$008D	ATD1DIEN	Read:	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
		Write:								
$008E	PORTAD0	Read:	PTAD15	PTAD14	PTAD13	PTAD12	PTAD11	PTAD10	PTAD9	PTAD8
		Write:								
$008F	PORTAD1	Read:	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
		Write:								
$0090	ATD1DR0H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0091	ATD1DR0L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0092	ATD1DR1H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0093	ATD1DR1L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0094	ATD1DR2H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0095	ATD1DR2L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0096	ATD1DR3H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0097	ATD1DR3L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0098	ATD1DR4H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0099	ATD1DR4L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009A	ATD1DR5H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009B	ATD1DR5L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009C	ATD1DR6H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009D	ATD1DR6L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009E	ATD1DR7H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009F	ATD1DR7L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00A0	ATD1DR8H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A1	ATD1DR8L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00A2	ATD1DR9H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A3	ATD1DR9L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00A4	ATD1DR10H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A5	ATD1DR10L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00A6	ATD1DR11H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A7	ATD1DR11L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00A8	ATD1DR12H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A9	ATD1DR12L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00AA	ATD1DR13H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00AB	ATD1DR13L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00AC	ATD1DR14H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00AD	ATD1DR14L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00AE	ATD1DR15H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00AF	ATD1DR15L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								

$00B0 - $00B7   Inter IC Bus (IIC1) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00B0	IBAD	Read:	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
		Write:								
$00B1	IBFD	Read:	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
		Write:								
$00B2	IBCR	Read:	IBEN	IBIE	MS/$\overline{\text{SL}}$	TX/$\overline{\text{RX}}$	TXAK	0	0	IBSWAI
		Write:						RSTA		
$00B3	IBSR	Read:	TCF	IAAS	IBB	IBAL	0	SRW	IBIF	RXAK
		Write:								
$00B4	IBDR	Read:	D7	D6	D5	D4	D3	D2	D1	D 0
		Write:								
$00B5	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00B6	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00B7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00B8 - $00BF   Asynchronous Serial Interface (SCI2) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00B8	SCI2BDH[1]	Read:	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
		Write:								
$00B9	SCI2BDL[1]	Read:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		Write:								
$00BA	SCI2CR1[1]	Read:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		Write:								
$00B8	SCI2ASR1[2]	Read:	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
		Write:								
$00B9	SCI2ACR1[2]	Read:	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
		Write:								
$00BA	SCI2ACR2[2]	Read:	0	0	0	0	0	BERRM1	BERRM0	BKDFE
		Write:								
$00BB	SCI2CR2	Read:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Write:								
$00BC	SCI2SR1	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								

$00B8 - $00BF   **Asynchronous Serial Interface (SCI2) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00BD	SCI2SR2	Read:	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
		Write:	AMAP			TXPOL	RXPOL	BRK13	TXDIR	
$00BE	SCI2DRH	Read:	R8	T8	0	0	0	0	0	0
		Write:		T8						
$00BF	SCI2DRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

NOTES:

1. Those registers are accessible if the AMAP bit in the SCI2SR2 register is set to zero
2. Those registers are accessible if the AMAP bit in the SCI2SR2 register is set to one

$00C0 - $00C7   **Asynchronous Serial Interface (SCI3) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00C0	SCI3BDH[1]	Read:	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
		Write:	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
$00C1	SCI3BDL[1]	Read:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		Write:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
$00C2	SCI3CR1[1]	Read:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		Write:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
$00C0	SCI3ASR1[2]	Read:	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
		Write:							BERRIF	BKDIF
$00C1	SCI3ACR1[2]	Read:	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
		Write:	RXEDGIE						BERRIE	BKDIE
$00C2	SCI3ACR2[2]	Read:	0	0	0	0	0	BERRM1	BERRM0	BKDFE
		Write:						BERRM1	BERRM0	BKDFE
$00C3	SCI3CR2	Read:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
$00C4	SCI3SR1	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								
$00C5	SCI3SR2	Read:	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
		Write:	AMAP			TXPOL	RXPOL	BRK13	TXDIR	
$00C6	SCI3DRH	Read:	R8	T8	0	0	0	0	0	0
		Write:		T8						
$00C7	SCI3DRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

NOTES:

1. Those registers are accessible if the AMAP bit in the SCI3SR2 register is set to zero
2. Those registers are accessible if the AMAP bit in the SCI3SR2 register is set to one

$00C8 - $00CF   Asynchronous Serial Interface (SCI0) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00C8	SCI0BDH[1]	Read:	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
		Write:								
$00C9	SCI0BDL[1]	Read:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		Write:								
$00CA	SCI0CR1[1]	Read:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		Write:								
$00C8	SCI0ASR1[2]	Read:	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
		Write:								
$00C9	SCI0ACR1[2]	Read:	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
		Write:								
$00CA	SCI0ACR2[2]	Read:	0	0	0	0	0	BERRM1	BERRM0	BKDFE
		Write:								
$00CB	SCI0CR2	Read:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Write:								
$00CC	SCI0SR1	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								
$00CD	SCI0SR2	Read:	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
		Write:								
$00CE	SCI0DRH	Read:	R8	T8	0	0	0	0	0	0
		Write:								
$00CF	SCI0DRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

NOTES:
1. Those registers are accessible if the AMAP bit in the SCI0SR2 register is set to zero
2. Those registers are accessible if the AMAP bit in the SCI0SR2 register is set to one

$00D0 - $00D7   Asynchronous Serial Interface (SCI1) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D0	SCI1BDH[1]	Read:	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
		Write:								
$00D1	SCI1BDL[1]	Read:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		Write:								
$00D2	SCI1CR1[1]	Read:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		Write:								
$00D0	SCI1ASR1[2]	Read:	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
		Write:								
$00D1	SCI1ACR1[2]	Read:	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
		Write:								
$00D2	SCI1ACR2[2]	Read:	0	0	0	0	0	BERRM1	BERRM0	BKDFE
		Write:								
$00D3	SCI1CR2	Read:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Write:								
$00D4	SCI1SR1	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								

$00D0 - $00D7 **Asynchronous Serial Interface (SCI1) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D5	SCI1SR2	Read:	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
		Write:								
$00D6	SCI1DRH	Read:	R8	T8	0	0	0	0	0	0
		Write:								
$00D7	SCI1DRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

NOTES:
1. Those registers are accessible if the AMAP bit in the SCI1SR2 register is set to zero
2. Those registers are accessible if the AMAP bit in the SCI1SR2 register is set to one

$00D8 - $00DF **Serial Peripheral Interface (SPI0) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D8	SPI0CR1	Read:	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		Write:								
$00D9	SPI0CR2	Read:	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		Write:								
$00DA	SPI0BR	Read:	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		Write:								
$00DB	SPI0SR	Read:	SPIF	0	SPTEF	MODF	0	0	0	0
		Write:								
$00DC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00DD	SPI0DR	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00DE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00DF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00E0 - $00E7 **Inter IC Bus (IIC0) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00E0	IBAD	Read:	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
		Write:								
$00E1	IBFD	Read:	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
		Write:								
$00E2	IBCR	Read:	IBEN	IBIE	MS/$\overline{SL}$	TX/$\overline{RX}$	TXAK	0	0	IBSWAI
		Write:						RSTA		
$00E3	IBSR	Read:	TCF	IAAS	IBB	IBAL	0	SRW	IBIF	RXAK
		Write:								
$00E4	IBDR	Read:	D7	D6	D5	D4	D3	D2	D1	D 0
		Write:								

$00E0 - $00E7   **Inter IC Bus (IIC0) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00E5	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00E6	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00E7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00E8 - $00EF   **Reserved**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00E8	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00E9	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00EA	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00EB	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00EC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00ED	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00EE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00EF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00F0 - $00F7   **Serial Peripheral Interface (SPI1) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00F0	SPI1CR1	Read: / Write:	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
$00F1	SPI1CR2	Read:	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		Write:				MODFEN	BIDIROE		SPISWAI	SPC0
$00F2	SPI1BR	Read:	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		Write:		SPPR2	SPPR1	SPPR0		SPR2	SPR1	SPR0
$00F3	SPI1SR	Read:	SPIF	0	SPTEF	MODF	0	0	0	0
		Write:								
$00F4	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00F5	SPI1DR	Read: / Write:	Bit7	6	5	4	3	2	1	Bit0
$00F6	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00F7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00F8 - $00FF Serial Peripheral Interface (SPI2) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00F8	SPI2CR1	Read:	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		Write:								
$00F9	SPI2CR2	Read:	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		Write:								
$00FA	SPI2BR	Read:	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		Write:								
$00FB	SPI2SR	Read:	SPIF	0	SPTEF	MODF	0	0	0	0
		Write:								
$00FC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00FD	SPI2DR	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00FE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0100 - $010F Flash Control Register (FTX512K4) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0100	FCLKDIV	Read:	FDIVLD	PRDIV8	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
		Write:								
$0101	FSEC	Read:	KEYEN1	KEYEN0	RNV5	RNV4	RNV3	RNV2	SEC1	SEC0
		Write:								
$0102	FTSTMOD	Read:	0	MRDS	MRDS	WRALL	0	0	0	0
		Write:								
$0103	FCNFG	Read:	CBEIE	CCIE	KEYACC	0	0	0	0	0
		Write:								
$0104	FPROT	Read:	FPOPEN	RNV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
		Write:								
$0105	FSTAT	Read:	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		Write:								
$0106	FCMD	Read:	0	CMDB[6:0]	CMDB[6:0]	CMDB[6:0]	CMDB[6:0]	CMDB[6:0]	CMDB[6:0]	CMDB[6:0]
		Write:								
$0107	FCTL	Read:	NV7	NV6	NV5	NV4	NV3	NV2	NV1	NV0
		Write:								
$0108	FADDRHI	Read:	FADDRHI	FADDRHI	FADDRHI	FADDRHI	FADDRHI	FADDRHI	FADDRHI	FADDRHI
		Write:								
$0109	FADDRLO	Read:	FADDRLO	FADDRLO	FADDRLO	FADDRLO	FADDRLO	FADDRLO	FADDRLO	FADDRLO
		Write:								
$010A	FDATAHI	Read:	FDATAHI	FDATAHI	FDATAHI	FDATAHI	FDATAHI	FDATAHI	FDATAHI	FDATAHI
		Write:								
$010B	FDATALO	Read:	FDATALO	FDATALO	FDATALO	FDATALO	FDATALO	FDATALO	FDATALO	FDATALO
		Write:								
$010C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0100 - $010F   Flash Control Register (FTX512K4) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$010D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$010E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$010F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0110 - $011B   EEPROM Control Register (EETX4K) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0110	ECLKDIV	Read:	EDIVLD	PRDIV8	EDIV5	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0
		Write:								
$0111	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0112	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0113	ECNFG	Read:	CBEIE	CCIE	0	0	0	0	0	0
		Write:								
$0114	EPROT	Read:	EPOPEN	RNV6	RNV5	RNV4	EPDIS	EPS2	EPS1	EPS0
		Write:								
$0115	ESTAT	Read:	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		Write:								
$0116	ECMD	Read:	0	CMDB[6:0]						
		Write:								
$0117	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0118	EADDRHI	Read:	0	0	0	0	0	EABHI		
		Write:								
$0119	EADDRLO	Read:	EABLO							
		Write:								
$011A	EDATAHI	Read:	EDHI							
		Write:								
$011B	EDATALO	Read:	EDLO							
		Write:								

$011C - $011F   Random Access Memory (XSAM20K) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$011C	XSCTRL	Read:	XSRE	0	0	0	0	XSAVIE	XSAVIF	XSCAVIF
		Write:								
$011D	XSXCUB	Read:	1	XSXCU6	XSXCU5	XSXC46	XSXCU3	XSXCU2	XSXCU1	XSXCU0
		Write:								
$011E	XSSRLB	Read:	1	XSSL6	XSSL5	XSSL4	XSSL3	XSSL2	XSSL1	XSSL0
		Write:								
$011F	XSSRUB	Read:	1	XSSU6	XSSU5	XSSU4	XSSU3	XSSU2	XSSU1	XSSU0
		Write:								

$0120 - $012F **Interrupt Module (S12XINT) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0120	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0121	IVBR	Read:	IVB_ADDR[7:0]							
		Write:								
$0122	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0123	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0124	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0125	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0126	INT_XGPRIO	Read:	0	0	0	0	0	XILVL[2:0]		
		Write:								
$0127	INT_CFADDR	Read:	INT_CFADDR[7:4]				0	0	0	0
		Write:								
$0128	INT_CFDATA0	Read:	RQST	0	0	0	0	PRIOLVL[2:0]		
		Write:								
$0129	INT_CFDATA1	Read:	RQST	0	0	0	0	PRIOLVL[2:0]		
		Write:								
$012A	INT_CFDATA2	Read:	RQST	0	0	0	0	PRIOLVL[2:0]		
		Write:								
$012B	INT_CFDATA3	Read:	RQST	0	0	0	0	PRIOLVL[2:0]		
		Write:								
$012C	INT_CFDATA4	Read:	RQST	0	0	0	0	PRIOLVL[2:0]		
		Write:								
$012D	INT_CFDATA5	Read:	RQST	0	0	0	0	PRIOLVL[2:0]		
		Write:								
$012E	INT_CFDATA6	Read:	RQST	0	0	0	0	PRIOLVL[2:0]		
		Write:								
$012F	INT_CFDATA7	Read:	RQST	0	0	0	0	PRIOLVL[2:0]		
		Write:								

$00130 - $0137 **Asynchronous Serial Interface (SCI4) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0130	SCI4BDH[1]	Read:	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
		Write:								
$0131	SCI4BDL[1]	Read:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		Write:								
$0132	SCI4CR1[1]	Read:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		Write:								
$0130	SCI4ASR1[2]	Read:	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
		Write:								
$0131	SCI4ACR1[2]	Read:	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
		Write:								

$00130 - $0137   **Asynchronous Serial Interface (SCI4) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0132	SCI4ACR2[2]	Read:	0	0	0	0	0	BERRM1	BERRM0	BKDFE
		Write:								
$0133	SCI4CR2	Read:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Write:								
$0134	SCI4SR1	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								
$0135	SCI4SR2	Read:	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
		Write:								
$0136	SCI4DRH	Read:	R8	T8	0	0	0	0	0	0
		Write:								
$0137	SCI4DRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

NOTES:

1. Those registers are accessible if the AMAP bit in the SCI4SR2 register is set to zero

2. Those registers are accessible if the AMAP bit in the SCI4SR2 register is set to one

$0138 - $013F   **Asynchronous Serial Interface (SCI5) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0138	SCI5BDH[1]	Read:	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
		Write:								
$0139	SCI5BDL[1]	Read:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		Write:								
$013A	SCI5CR1[1]	Read:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		Write:								
$0138	SCI5ASR1[2]	Read:	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
		Write:								
$0139	SCI5ACR1[2]	Read:	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
		Write:								
$013A	SCI5ACR2[2]	Read:	0	0	0	0	0	BERRM1	BERRM0	BKDFE
		Write:								
$013B	SCI5CR2	Read:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Write:								
$013C	SCI5SR1	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								
$013D	SCI5SR2	Read:	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
		Write:								
$013E	SCI5DRH	Read:	R8	T8	0	0	0	0	0	0
		Write:								
$013F	SCI5DRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

NOTES:

1. Those registers are accessible if the AMAP bit in the SCI5SR2 register is set to zero

2. Those registers are accessible if the AMAP bit in the SCI5SR2 register is set to one

$0140 - $017F **Motorola Scalable CAN - MSCAN (CAN0) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0140	CAN0CTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:	RXFRM		CSWAI		TIME	WUPE	SLPRQ	INITRQ
$0141	CAN0CTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM	SLPAK	INITAK
		Write:	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM		
$0142	CAN0BTR0	Read:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		Write:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
$0143	CAN0BTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
$0144	CAN0RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		Write:	WUPIF	CSCIF					OVRIF	RXF
$0145	CAN0RIER	Read:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		Write:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
$0146	CAN0TFLG	Read:	0	0	0	0	0	TXE2	TXE1	TXE0
		Write:						TXE2	TXE1	TXE0
$0147	CAN0TIER	Read:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		Write:						TXEIE2	TXEIE1	TXEIE0
$0148	CAN0TARQ	Read:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		Write:						ABTRQ2	ABTRQ1	ABTRQ0
$0149	CAN0TAAK	Read:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		Write:								
$014A	CAN0TBSEL	Read:	0	0	0	0	0	TX2	TX1	TX0
		Write:						TX2	TX1	TX0
$014B	CAN0IDAC	Read:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		Write:			IDAM1	IDAM0				
$014C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$014D	CAN0MISC	Read:	0	0	0	0	0	0	0	BOHOLD
		Write:								BOHOLD
$014E	CAN0RXERR	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								
$014F	CAN0TXERR	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
$0150 - $0153	CAN0IDAR0 - CAN0IDAR3	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$0154 - $0157	CAN0IDMR0 - CAN0IDMR3	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0158 - $015B	CAN0IDAR4 - CAN0IDAR7	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$015C - $015F	CAN0IDMR4 - CAN0IDMR7	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0160 - $016F	CAN0RXFG	Read:	FOREGROUND RECEIVE BUFFER see **Detailed MSCAN Foreground Receive and Transmit Buffer Layout**							
		Write:								
$0170 - $017F	CAN0TXFG	Read:	FOREGROUND TRANSMIT BUFFER see **Detailed MSCAN Foreground Receive and Transmit Buffer Layout**							
		Write:								

Detailed MSCAN Foreground Receive and Transmit Buffer Layout

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Extended ID	Read:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
$xxx0	Standard ID	Read:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
	CANxRIDR0	Write:								
	Extended ID	Read:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
$xxx1	Standard ID	Read:	ID2	ID1	ID0	RTR	IDE=0			
	CANxRIDR1	Write:								
	Extended ID	Read:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
$xxx2	Standard ID	Read:								
	CANxRIDR2	Write:								
	Extended ID	Read:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
$xxx3	Standard ID	Read:								
	CANxRIDR3	Write:								
$xxx4-	CANxRDSR0 -	Read:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
$xxxB	CANxRDSR7	Write:								
$xxxC	CANRxDLR	Read:					DLC3	DLC2	DLC1	DLC0
		Write:								
$xxxD	Reserved	Read:								
		Write:								
$xxxE	CANxRTSRH	Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		Write:								
$xxxF	CANxRTSRL	Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		Write:								
$xx10	Extended ID CANxTIDR0	Read: Write:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
	Standard ID	Read: Write:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
$xx10	Extended ID CANxTIDR1	Read: Write:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
	Standard ID	Read: Write:	ID2	ID1	ID0	RTR	IDE=0			
$xx12	Extended ID CANxTIDR2	Read: Write:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
	Standard ID	Read: Write:								
$xx13	Extended ID CANxTIDR3	Read: Write:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
	Standard ID	Read: Write:								
$xx14- $xx1B	CANxTDSR0 - CANxTDSR7	Read: Write:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
$xx1C	CANxTDLR	Read: Write:					DLC3	DLC2	DLC1	DLC0
$xx1D	CANxTTBPR	Read: Write:	PRIO7	PRIO6	PRIO5	PRIO4	PRIO3	PRIO2	PRIO1	PRIO0
$xx1E	CANxTTSRH	Read: Write:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
$xx1F	CANxTTSRL	Read: Write:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0

$0180 - $01BF **Motorola Scalable CAN - MSCAN (CAN1) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0180	CAN1CTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:	RXFRM		CSWAI		TIME	WUPE	SLPRQ	INITRQ
$0181	CAN1CTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM	SLPAK	INITAK
		Write:	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM		
$0182	CAN1BTR0	Read:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		Write:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
$0183	CAN1BTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
$0184	CAN1RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		Write:	WUPIF	CSCIF					OVRIF	RXF
$0185	CAN1RIER	Read:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		Write:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
$0186	CAN1TFLG	Read:	0	0	0	0	0	TXE2	TXE1	TXE0
		Write:						TXE2	TXE1	TXE0
$0187	CAN1TIER	Read:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		Write:						TXEIE2	TXEIE1	TXEIE0
$0188	CAN1TARQ	Read:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		Write:						ABTRQ2	ABTRQ1	ABTRQ0
$0189	CAN1TAAK	Read:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		Write:								
$018A	CAN1TBSEL	Read:	0	0	0	0	0	TX2	TX1	TX0
		Write:						TX2	TX1	TX0
$018B	CAN1IDAC	Read:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		Write:			IDAM1	IDAM0				
$018C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$018D	CAN1MISC	Read:	0	0	0	0	0	0	0	BOHOLD
		Write:								BOHOLD
$018E	CAN1RXERR	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								
$018F	CAN1TXERR	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
$0190	CAN1IDAR0	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$0191	CAN1IDAR1	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$0192	CAN1IDAR2	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$0193	CAN1IDAR3	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$0194	CAN1IDMR0	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0195	CAN1IDMR1	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0196	CAN1IDMR2	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0197	CAN1IDMR3	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0

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$0180 - $01BF   Motorola Scalable CAN - MSCAN (CAN1) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0198	CAN1IDAR4	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$0199	CAN1IDAR5	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$019A	CAN1IDAR6	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$019B	CAN1IDAR7	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$019C	CAN1IDMR4	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$019D	CAN1IDMR5	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$019E	CAN1IDMR6	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$019F	CAN1IDMR7	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$01A0 - $01AF	CAN1RXFG	Read: Write:	FOREGROUND RECEIVE BUFFER see **Detailed MSCAN Foreground Receive and Transmit Buffer Layout**							
$01B0 - $01BF	CAN1TXFG	Read: Write:	FOREGROUND TRANSMIT BUFFER see **Detailed MSCAN Foreground Receive and Transmit Buffer Layout**							

$01C0 - $01FF   Motorola Scalable CAN - MSCAN (CAN2) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$01C0	CAN2CTL0	Read: Write:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
$01C1	CAN2CTL1	Read: Write:	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM	SLPAK	INITAK
$01C2	CAN2BTR0	Read: Write:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
$01C3	CAN2BTR1	Read: Write:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
$01C4	CAN2RFLG	Read: Write:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
$01C5	CAN2RIER	Read: Write:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
$01C6	CAN2TFLG	Read: Write:	0	0	0	0	0	TXE2	TXE1	TXE0
$01C7	CAN2TIER	Read: Write:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
$01C8	CAN2TARQ	Read: Write:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
$01C9	CAN2TAAK	Read: Write:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
$01CA	CAN2TBSEL	Read: Write:	0	0	0	0	0	TX2	TX1	TX0
$01CB	CAN2IDAC	Read: Write:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0

$01C0 - $01FF   **Motorola Scalable CAN - MSCAN (CAN2) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$01CC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01CD	CAN2MISC	Read:	0	0	0	0	0	0	0	BOHOLD
		Write:								BOHOLD
$01CE	CAN2RXERR	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								
$01CF	CAN2TXERR	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
$01D0	CAN2IDAR0	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$01D1	CAN2IDAR1	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$01D2	CAN2IDAR2	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$01D3	CAN2IDAR3	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$01D4	CAN2IDMR0	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$01D5	CAN2IDMR1	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$01D6	CAN2IDMR2	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$01D7	CAN2IDMR3	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$01D8	CAN2IDAR4	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$01D9	CAN2IDAR5	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$01DA	CAN2IDAR6	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$01DB	CAN2IDAR7	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$01DC	CAN2IDMR4	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$01DD	CAN2IDMR5	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$01DE	CAN2IDMR6	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$01DF	CAN2IDMR7	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$01E0 - $01EF	CAN2RXFG	Read:	FOREGROUND RECEIVE BUFFER see **Detailed MSCAN Foreground Receive and Transmit Buffer Layout**							
		Write:								
$01F0 - $01FF	CAN2TXFG	Read:	FOREGROUND TRANSMIT BUFFER see **Detailed MSCAN Foreground Receive and Transmit Buffer Layout**							
		Write:								

$0200 - $023F   **Motorola Scalable CAN - MSCAN (CAN3)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0200	CAN3CTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:	RXFRM		CSWAI		TIME	WUPE	SLPRQ	INITRQ
$0201	CAN3CTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM	SLPAK	INITAK
		Write:	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM		
$0202	CAN3BTR0	Read:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		Write:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
$0203	CAN3BTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
$0204	CAN3RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		Write:	WUPIF	CSCIF					OVRIF	RXF
$0205	CAN3RIER	Read:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		Write:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
$0206	CAN3TFLG	Read:	0	0	0	0	0	TXE2	TXE1	TXE0
		Write:						TXE2	TXE1	TXE0
$0207	CAN3TIER	Read:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		Write:						TXEIE2	TXEIE1	TXEIE0
$0208	CAN3TARQ	Read:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		Write:						ABTRQ2	ABTRQ1	ABTRQ0
$0209	CAN3TAAK	Read:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		Write:								
$020A	CAN3TBSEL	Read:	0	0	0	0	0	TX2	TX1	TX0
		Write:						TX2	TX1	TX0
$020B	CAN3IDAC	Read:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		Write:			IDAM1	IDAM0				
$020C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$020D	Reserved	Read:	0	0	0	0	0	0	0	BOHOLD
		Write:								BOHOLD
$020E	CAN3RXERR	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								
$020F	CAN3TXERR	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
$0210	CAN3IDAR0	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$0211	CAN3IDAR1	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$0212	CAN3IDAR2	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$0213	CAN3IDAR3	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$0214	CAN3IDMR0	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0215	CAN3IDMR1	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0216	CAN3IDMR2	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0217	CAN3IDMR3	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0218	CAN3IDAR4	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0

$0200 - $023F **Motorola Scalable CAN - MSCAN (CAN3)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0219	CAN3IDAR5	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$021A	CAN3IDAR6	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$021B	CAN3IDAR7	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$021C	CAN3IDMR4	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$021D	CAN3IDMR5	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$021E	CAN3IDMR6	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$021F	CAN3IDMR7	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0220 - $022F	CAN3RXFG	Read:	FOREGROUND RECEIVE BUFFER see **Detailed MSCAN Foreground Receive and Transmit Buffer Layout**							
		Write:								
$0230 - $023F	CAN3TXFG	Read:	FOREGROUND TRANSMIT BUFFER see **Detailed MSCAN Foreground Receive and Transmit Buffer Layout**							
		Write:								

$0240 - $027F **Port Integration Module PIM_9DX (PIM) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0240	PTT	Read: Write:	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
$0241	PTIT	Read: Write:	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
$0242	DDRT	Read: Write:	DDRT7	DDRT7	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
$0243	RDRT	Read: Write:	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
$0244	PERT	Read: Write:	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
$0245	PPST	Read: Write:	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
$0246	Reserved	Read: Write:	0	0	0	0	0	0	0	0
$0247	Reserved	Read: Write:	0	0	0	0	0	0	0	0
$0248	PTS	Read: Write:	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
$0249	PTIS	Read: Write:	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
$024A	DDRS	Read: Write:	DDRS7	DDRS7	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
$024B	RDRS	Read: Write:	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
$024C	PERS	Read: Write:	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0

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$0240 - $027F   **Port Integration Module PIM_9DX (PIM) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$024D	PPSS	Read: Write:	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
$024E	WOMS	Read: Write:	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
$024F	Reserved	Read: Write:	0	0	0	0	0	0	0	0
$0250	PTM	Read: Write:	PTM7	PTM6	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
$0251	PTIM	Read: Write:	PTIM7	PTIM6	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
$0252	DDRM	Read: Write:	DDRM7	DDRM7	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
$0253	RDRM	Read: Write:	RDRM7	RDRM6	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0
$0254	PERM	Read: Write:	PERM7	PERM6	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
$0255	PPSM	Read: Write:	PPSM7	PPSM6	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
$0256	WOMM	Read: Write:	WOMM7	WOMM6	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
$0257	MODRR	Read: Write:	0	MODRR6	MODRR5	MODRR4	MODRR3	MODRR2	MODRR1	MODRR0
$0258	PTP	Read: Write:	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
$0259	PTIP	Read: Write:	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
$025A	DDRP	Read: Write:	DDRP7	DDRP7	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
$025B	RDRP	Read: Write:	RDRP7	RDRP6	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
$025C	PERP	Read: Write:	PERP7	PERP6	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
$025D	PPSP	Read: Write:	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSS0
$025E	PIEP	Read: Write:	PIEP7	PIEP6	PIEP5	PIEP4	PIEP3	PIEP2	PIEP1	PIEP0
$025F	PIFP	Read: Write:	PIFP7	PIFP6	PIFP5	PIFP4	PIFP3	PIFP2	PIFP1	PIFP0
$0260	PTH	Read: Write:	PTH7	PTH6	PTH5	PTH4	PTH3	PTH2	PTH1	PTH0
$0261	PTIH	Read: Write:	PTIH7	PTIH6	PTIH5	PTIH4	PTIH3	PTIH2	PTIH1	PTIH0
$0262	DDRH	Read: Write:	DDRH7	DDRH7	DDRH5	DDRH4	DDRH3	DDRH2	DDRH1	DDRH0
$0263	RDRH	Read: Write:	RDRH7	RDRH6	RDRH5	RDRH4	RDRH3	RDRH2	RDRH1	RDRH0
$0264	PERH	Read: Write:	PERH7	PERH6	PERH5	PERH4	PERH3	PERH2	PERH1	PERH0
$0265	PPSH	Read: Write:	PPSH7	PPSH6	PPSH5	PPSH4	PPSH3	PPSH2	PPSH1	PPSH0

$0240 - $027F **Port Integration Module PIM_9DX (PIM) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0266	PIEH	Read: Write:	PIEH7	PIEH6	PIEH5	PIEH4	PIEH3	PIEH2	PIEH1	PIEH0
$0267	PIFH	Read: Write:	PIFH7	PIFH6	PIFH5	PIFH4	PIFH3	PIFH2	PIFH1	PIFH0
$0268	PTJ	Read: Write:	PTJ7	PTJ6	PTJ5	PTJ4	0	PTJ2	PTJ1	PTJ0
$0269	PTIJ	Read: Write:	PTIJ7	PTIJ6	PTIJ5	PTIJ4	0	PTIJ2	PTIJ1	PTIJ0
$026A	DDRJ	Read: Write:	DDRJ7	DDRJ7	DDRJ5	DDRJ4	0	DDRJ2	DDRJ1	DDRJ0
$026B	RDRJ	Read: Write:	RDRJ7	RDRJ6	RDRJ5	RDRJ4	0	RDRJ2	RDRJ1	RDRJ0
$026C	PERJ	Read: Write:	PERJ7	PERJ6	PERJ5	PERJ4	0	PERJ2	PERJ1	PERJ0
$026D	PPSJ	Read: Write:	PPSJ7	PPSJ6	PPSJ5	PPSJ4	0	PPSJ2	PPSJ1	PPSJ0
$026E	PIEJ	Read: Write:	PIEJ7	PIEJ6	PIEJ5	PIEJ4	0	PIEJ2	PIEJ1	PIEJ0
$026f	PIEJ	Read: Write:	PIFJ7	PIFJ6	PIFJ5	PIFJ4	0	PIFJ2	PIFJ1	PIFJ0
$0270	Reserved	Read: Write:	0	0	0	0	0	0	0	0
$0271	PT1AD0	Read: Write:	PT1AD07	PT1AD06	PT1AD05	PT1AD04	PT1AD03	PT1AD02	PT1AD01	PT1AD00
$0272	Reserved	Read: Write:	0	0	0	0	0	0	0	0
$0273	DDR1AD0	Read: Write:	DDR1 AD07	DDR1 AD06	DDR1 AD05	DDR1 AD04	DDR1 AD03	DDR1 AD02	DDR1 AD01	DDR1 AD01
$0274	Reserved	Read: Write:	0	0	0	0	0	0	0	0
$0275	RDR1AD0	Read: Write:	RDR1 AD07	RDR1 AD06	RDR1 AD05	RDR1 AD04	RDR1 AD03	RDR1 AD02	RDR1 AD01	RDR1 AD00
$0276	Reserved	Read: Write:	0	0	0	0	0	0	0	0
$0277	PER1AD0	Read: Write:	PER1AD 07	PER1AD 06	PER1AD 05	PER1AD 04	PER1AD 03	PER1AD 02	PER1AD 01	PER1AD 00
$0278	PT0AD1	Read: Write:	PT0AD1 23	PT0AD1 22	PT0AD1 21	PT0AD1 20	PT0AD1 19	PT0AD1 18	PT0AD1 17	PT0AD1 16
$0279	PT1AD1	Read: Write:	PT1AD1 15	PT1AD1 14	PT1AD1 13	PT1AD1 12	PT1AD1 11	PT1AD1 10	PT1AD1 9	PT1AD1 8
$027A	DDR0AD1	Read: Write:	DDR0 AD1 23	DDR0 AD1 22	DDR0 AD1 21	DDR0 AD1 20	DDR0 AD1 19	DDR0 AD1 18	DDR0 AD1 17	DDR0 AD1 16
$027B	DDR1AD1	Read: Write:	DDR1 AD1 15	DDR1 AD1 14	DDR1 AD1 13	DDR1 AD1 12	DDR1 AD1 11	DDR1 AD1 10	DDR1 AD1 9	DDR1 AD1 8
$027C	RDR0AD1	Read: Write:	RDR0 AD1 23	RDR0 AD1 22	RDR0 AD1 21	RDR0 AD1 20	RDR0 AD1 19	RDR0 AD1 18	RDR0 AD1 17	RDR0 AD1 16

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$0240 - $027F   Port Integration Module PIM_9DX (PIM) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$027D	RDR1AD1	Read:	RDR1AD1 15	RDR1AD1 14	RDR1AD1 13	RDR1AD1 12	RDR1AD1 11	RDR1AD1 10	RDR1AD1 9	RDR1AD1 8
		Write:								
$027E	PER0AD1	Read:	PER0AD1 23	PER0AD1 22	PER0AD1 21	PER0AD1 20	PER0AD1 19	PER0AD1 18	PER0AD1 17	PER0AD1 16
		Write:								
$027F	PER1AD1	Read:	PER1AD1 15	PER1AD1 14	PER1AD1 13	PER1AD1 12	PER1AD1 11	PER1A1D 10	PER1AD1 9	PER1AD1 8
		Write:								

$0280 - $02BF   Motorola Scalable CAN - MSCAN (CAN4) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0280	CAN4CTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:								
$0281	CAN4CTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	BORM	WUPM	SLPAK	INITAK
		Write:								
$0282	CAN4BTR0	Read:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		Write:								
$0283	CAN4BTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:								
$0284	CAN4RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		Write:								
$0285	CAN4RIER	Read:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		Write:								
$0286	CAN4TFLG	Read:	0	0	0	0	0	TXE2	TXE1	TXE0
		Write:								
$0287	CAN4TIER	Read:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		Write:								
$0288	CAN4TARQ	Read:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		Write:								
$0289	CAN4TAAK	Read:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		Write:								
$028A	CAN4TBSEL	Read:	0	0	0	0	0	TX2	TX1	TX0
		Write:								
$028B	CAN4IDAC	Read:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		Write:								
$028C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$028D	CAN4MISC	Read:	0	0	0	0	0	0	0	BOHOLD
		Write:								
$028E	CAN4RXERR	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								
$028F	CAN4TXERR	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
$0290	CAN4IDAR0	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
$0291	CAN4IDAR1	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								

$0280 - $02BF   **Motorola Scalable CAN - MSCAN (CAN4) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0292	CAN4IDAR2	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$0293	CAN4IDAR3	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$0294	CAN4IDMR0	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0295	CAN4IDMR1	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0296	CAN4IDMR2	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0297	CAN4IDMR3	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0298	CAN4IDAR4	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$0299	CAN4IDAR5	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$029A	CAN4IDAR6	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$029B	CAN4IDAR7	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$029C	CAN4IDMR4	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$029D	CAN4IDMR5	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$029E	CAN4IDMR6	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$029F	CAN4IDMR7	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$02A0 - $02AF	CAN4RXFG	Read:	FOREGROUND RECEIVE BUFFER see **Detailed MSCAN Foreground Receive and Transmit Buffer Layout**							
		Write:								
$02B0 - $02BF	CAN4TXFG	Read:	FOREGROUND TRANSMIT BUFFER see **Detailed MSCAN Foreground Receive and Transmit Buffer Layout**							
		Write:								

$02C0 - $02DF   **Analog to Digital Converter 10 Bit 8 Channel (ATD0) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$02C0	ATD0CTL0	Read:	0	0	0	0	0	WRAP2	WRAP1	WRAP0
		Write:								
$02C1	ATD0CTL1	Read:	ETRIG SEL	0	0	0	0	ETRIG CH2	ETRIG CH1	ETRIG CH0
		Write:								
$02C2	ATD0CTL2	Read:	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ASCIF
		Write:								
$02C3	ATD0CTL3	Read:	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		Write:								
$02C4	ATD0CTL4	Read: Write:	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
$02C5	ATD0CTL5	Read:	DJM	DSGN	SCAN	MULT	0	CC	CB	CA
		Write:								

$02C0 - $02DF   **Analog to Digital Converter 10 Bit 8 Channel (ATD0) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$02C6	ATD0STAT0	Read:	SCF	0	ETORF	FIFOR	0	CC2	CC1	CC0
		Write:								
$02C7	Reserved	Read:	U	U	U	U	U	U	U	U
		Write:								
$02C8	ATD0TEST0	Read:	U	U	U	U	U	U	U	U
		Write:								
$02C9	ATD0TEST1	Read:	U	U	0	0	0	0	0	SC
		Write:								
$02CA	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$02CB	ATD0STAT1	Read:	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		Write:								
$02CC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$02CD	ATD0DIEN	Read:	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
		Write:								
$02CE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$02CF	PORTAD0	Read:	Bit7	6	5	4	3	2	1	BIT 0
		Write:								
$02D0	ATD0DR0H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$02D1	ATD0DR0L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$02D2	ATD0DR1H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$02D3	ATD0DR1L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$02D4	ATD0DR2H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$02D5	ATD0DR2L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$02D6	ATD0DR3H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$02D7	ATD0DR3L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$02D8	ATD0DR4H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$02D9	ATD0DR4L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$02DA	ATD0DR5H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$02DB	ATD0DR5L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$02DC	ATD0DR6H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								

$02C0 - $02DF　　　　**Analog to Digital Converter 10 Bit 8 Channel (ATD0) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$02DD	ATD0DR6L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$02DE	ATD0DR7H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$02DF	ATD0DR7L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								

$02E0 - $02EF　　　　**Reserved**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$02E0 - $02EF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$02F0 - $02F7　　　　**Voltage Regulator (VREG_3V3) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$02F0	VREGHTCL	Read:				Reserved for Factory Test				
		Write:								
$02F1	VREGCTRL	Read:	0	0	0	0	0	LVDS	LVIE	LVIF
		Write:								
$02F2	VREGAPICL	Read:	APICLK	APIR3	APIR2	APIR1	APIR0	APIFE	APIE	APIF
		Write:								
$02F3	VREGAPITR	Read:	APITR5	APITR4	APITR3	APITR2	APITR1	APITR0	0	0
		Write:								
$02F4	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$02F5	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$02F6	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$02F7	Reserved	Read	0	0	0	0	0	0	0	0
		Write:								

$02F8 - $02FF　　　　**Reserved**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$02F8 - $02FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0300 - $0327   Pulse Width Modulator 8 Bit 8 Channel (PWM) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0300	PWME	Read: Write:	PWME7	PWME6	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
$0301	PWMPOL	Read: Write:	PPOL7	PPOL6	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
$0302	PWMCLK	Read: Write:	PCLK7	PCLK6	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
$0303	PWMPRCLK	Read: Write:	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
$0304	PWMCAE	Read: Write:	CAE7	CAE6	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
$0305	PWMCTL	Read: Write:	CON67	CON45	CON23	CON01	PSWAI	PFRZ	0	0
$0306	PWMTST Test Only	Read: Write:	0	0	0	0	0	0	0	0
$0307	PWMPRSC	Read: Write:	0	0	0	0	0	0	0	0
$0308	PWMSCLA	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0309	PWMSCLB	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$030A	PWMSCNTA	Read: Write:	0	0	0	0	0	0	0	0
$030B	PWMSCNTB	Read: Write:	0	0	0	0	0	0	0	0
$030C	PWMCNT0	Read: Write:	Bit 7 0	6 0	5 0	4 0	3 0	2 0	1 0	Bit 0 0
$030D	PWMCNT1	Read: Write:	Bit 7 0	6 0	5 0	4 0	3 0	2 0	1 0	Bit 0 0
$030E	PWMCNT2	Read: Write:	Bit 7 0	6 0	5 0	4 0	3 0	2 0	1 0	Bit 0 0
$030F	PWMCNT3	Read: Write:	Bit 7 0	6 0	5 0	4 0	3 0	2 0	1 0	Bit 0 0
$0310	PWMCNT4	Read: Write:	Bit 7 0	6 0	5 0	4 0	3 0	2 0	1 0	Bit 0 0
$0311	PWMCNT5	Read: Write:	Bit 7 0	6 0	5 0	4 0	3 0	2 0	1 0	Bit 0 0
$0312	PWMCNT6	Read: Write:	Bit 7 0	6 0	5 0	4 0	3 0	2 0	1 0	Bit 0 0
$0313	PWMCNT7	Read: Write:	Bit 7 0	6 0	5 0	4 0	3 0	2 0	1 0	Bit 0 0
$0314	PWMPER0	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0315	PWMPER1	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0316	PWMPER2	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0317	PWMPER3	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0318	PWMPER4	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

$0300 - $0327   Pulse Width Modulator 8 Bit 8 Channel (PWM) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0319	PWMPER5	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$031A	PWMPER6	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$031B	PWMPER7	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$031C	PWMDTY0	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$031D	PWMDTY1	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$031E	PWMDTY2	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$031F	PWMDTY3	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0320	PWMDTY4	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0321	PWMDTY5	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0322	PWMDTY6	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0323	PWMDTY7	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0324	PWMSDN	Read: Write:	PWMIF	PWMIE	0 PWM RSTRT	PWMLVL	0	PWM7IN	PWM7IN L	PWM7E NA
$0325	Reserved	Read: Write:	0	0	0	0	0	0	0	0
$0326	Reserved	Read: Write:	0	0	0	0	0	0	0	0
$0327	Reserved	Read: Write:	0	0	0	0	0	0	0	0

$0328 - $033F

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0328 - $033F	Reserved	Read: Write:	0	0	0	0	0	0	0	0

$0340 - $0367   Periodic Interrupt Timer (PIT) Map

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0340	PITCFLMT	Read: Write:	PITE	PITSWAI	PITFRZ	0	0	0	0 PFLMT1	0 PFLMT0
$0341	PITFLT	Read: Write:	0	0	0	0	0 PFLT3	0 PFLT2	0 PFLT1	0 PFLT0
$0342	PITCE	Read: Write:	0	0	0	0	PCE3	PCE2	PCE1	PCE0
$0343	PITMUX	Read: Write:	0	0	0	0	PMUX3	PMUX2	PMUX1	PMUX0

$0340 - $0367   **Periodic Interrupt Timer (PIT) Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0344	PITINTE	Read:	0	0	0		PINTE3	PINTE2	PINTE1	PINTE0
		Write:								
$0345	PITTF	Read:	0	0	0	0	PTF3	PTF2	PTF1	PTF0
		Write:								
$0346	PITMTLD0	Read:/Write:	PMTLD7	PMTLD6	PMTLD5	PMTLD4	PMTLD3	PMTLD2	PMTLD1	PMTLD0
$0347	PITMTLD1	Read:/Write:	PMTLD7	PMTLD6	PMTLD5	PMTLD4	PMTLD3	PMTLD2	PMTLD1	PMTLD0
$0348	PITLD0 (hi)	Read:/Write:	PLD15	PLD14	PLD13	PLD12	PLD11	PLD10	PLD9	PLD8
$0349	PITLD0 (lo)	Read:/Write:	PLD7	PLD6	PLD5	PLD4	PLD3	PLD2	PLD1	PLD0
$034A	PITCNT0 (hi)	Read:/Write:	PCNT15	PCNT14	PCNT13	PCNT12	PCNT11	PCNT10	PCNT9	PCNT8
$034B	PITCNT0 (lo)	Read:/Write:	PCNT7	PCNT6	PCNT5	PCNT4	PCNT3	PCNT2	PCNT1	PCNT0
$034C	PITLD1 (hi)	Read:/Write:	PLD15	PLD14	PLD13	PLD12	PLD11	PLD10	PLD9	PLD8
$034D	PITLD1 (lo)	Read:/Write:	PLD7	PLD6	PLD5	PLD4	PLD3	PLD2	PLD1	PLD0
$034E	PITCNT1 (hi)	Read:/Write:	PCNT15	PCNT14	PCNT13	PCNT12	PCNT11	PCNT10	PCNT9	PCNT8
$034F	PITCNT1 (lo)	Read:/Write:	PCNT7	PCNT6	PCNT5	PCNT4	PCNT3	PCNT2	PCNT1	PCNT0
$0350	PITLD2 (hi)	Read:/Write:	PLD15	PLD14	PLD13	PLD12	PLD11	PLD10	PLD9	PLD8
$0351	PITLD2 (lo)	Read:/Write:	PLD7	PLD6	PLD5	PLD4	PLD3	PLD2	PLD1	PLD0
$0352	PITCNT2 (hi)	Read:/Write:	PCNT15	PCNT14	PCNT13	PCNT12	PCNT11	PCNT10	PCNT9	PCNT8
$0353	PITCNT2 (lo)	Read:/Write:	PCNT7	PCNT6	PCNT5	PCNT4	PCNT3	PCNT2	PCNT1	PCNT0
$0354	PITLD3 (hi)	Read:/Write:	PLD15	PLD14	PLD13	PLD12	PLD11	PLD10	PLD9	PLD8
$0355	PITLD3 (lo)	Read:/Write:	PLD7	PLD6	PLD5	PLD4	PLD3	PLD2	PLD1	PLD0
$0356	PITCNT3 (hi)	Read:/Write:	PCNT15	PCNT14	PCNT13	PCNT12	PCNT11	PCNT10	PCNT9	PCNT8
$0357	PITCNT3 (lo)	Read:/Write:	PCNT7	PCNT6	PCNT5	PCNT4	PCNT3	PCNT2	PCNT1	PCNT0
$0358 - $0367	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0368 - $037F   **Reserved**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0368 - $037F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0380 - $03BF   XGATE Map

Address	Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0380	XGMCTL	Read:	XGE	XGFRZ	0	XGDBG	0	0	XGSWEIF	XGIE
		Write:			XGDBGM		XGSS			
$0381	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0382	XGCHID	Read:	0	XGCHID[6:0]						
		Write:								
$0383	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0384	XGVBR	Read:	0	0	0	0	0	0	0	0
		Write:								
$0385	XGVBR	Read:	0	0	0	0	XGVBR[19:16]			
		Write:								
$0386	XGVBR	Read:	XGVBR[15:8]							
		Write:								
$0387	XGVBR	Read:	XGVBR[7:1]							0
		Write:								
$0388	XGIF	Read:	0	0	0	0	0	0	0	XGIF_78
		Write:								
$0389	XGIF	Read:	XGIF_77	XGIF_76	XGIF_75	XGIF_74	XGIF_73	XGIF_72	XGIF_71	XGIF_70
		Write:								
$038A	XGIF	Read:	XGIF_6F	XGIF_6E	XGIF_6D	XGIF_6C	XGIF_6B	XGIF_6A	XGIF_69	XGIF_68
		Write:								
$023B	XGIF	Read:	XGIF_67	XGIF_66	XGIF_65	XGIF_64	XGIF_63	XGIF_62	XGIF_61	XGIF_60
		Write:								
$023C	XGIF	Read:	XGIF_5F	XGIF_5E	XGIF_5D	XGIF_5C	XGIF_5B	XGIF_5A	XGIF_59	XGIF_58
		Write:								
$038D	XGIF	Read:	XGIF_57	XGIF_56	XGIF_55	XGIF_54	XGIF_53	XGIF_52	XGIF_51	XGIF_50
		Write:								
$038E	XGIF	Read:	XGIF_4F	XGIF_4E	XGIF_4D	XGIF_4C	XGIF_4B	XGIF_4A	XGIF_49	XGIF_48
		Write:								
$038F	XGIF	Read:	XGIF_47	XGIF_46	XGIF_45	XGIF_44	XGIF_43	XGIF_42	XGIF_41	XGIF_40
		Write:								
$0390	XGIF	Read:	XGIF_3F	XGIF_3E	XGIF_3D	XGIF_3C	XGIF_3B	XGIF_3A	XGIF_39	XGIF_38
		Write:								
$0391	XGIF	Read:	XGIF_37	XGIF_36	XGIF_35	XGIF_34	XGIF_33	XGIF_32	XGIF_31	XGIF_30
		Write:								
$0392	XGIF	Read:	XGIF_2F	XGIF_2E	XGIF_2D	XGIF_2C	XGIF_2B	XGIF_2A	XGIF_29	XGIF_28
		Write:								
$0393	XGIF	Read:	XGIF_27	XGIF_26	XGIF_25	XGIF_24	XGIF_23	XGIF_22	XGIF_21	XGIF_20
		Write:								
$0394	XGIF	Read:	XGIF_1F	XGIF_1E	XGIF_1D	XGIF_1C	XGIF_1B	XGIF_1A	XGIF_19	XGIF_18
		Write:								
$0395	XGIF	Read:	XGIF_17	XGIF_16	XGIF_15	XGIF_14	XGIF_13	XGIF_12	XGIF_11	XGIF_10
		Write:								
$0396	XGIF	Read:	XGIF_0F	XGIF_0E	XGIF_0D	XGIF_0C	XGIF_0B	XGIF_0A	XGIF_09	0
		Write:								
$0397	XGIF	Read:	0	0	0	0	0	0	0	0
		Write:								

$0380 - $03BF　　　　　**XGATE Map**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0398	XGSWT (hi)	Read:	0	0	0	0	0	0	0	0
		Write:	XGSWTM[7:0]							
$0399	XGSWT (lo)	Read:	XGSWT[7:0]							
		Write:								
$039A	XGSEM (hi)	Read:	0	0	0	0	0	0	0	0
		Write:	XGSEMM[7:0]							
$039B	XGSEM (lo)	Read:	XGSEM[7:0]							
		Write:								
$039C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$039D	XGCCR	Read:	0	0	0	0	XGN	XGZ	XGV	XGC
		Write:								
$039E	XGPC (hi)	Read:	XGPC[15:8]							
		Write:								
$039F	XGPC (lo)	Read:	XGPC[7:0]							
		Write:								
$03A0	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$03A1	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$03A2	XGR1 (hi)	Read:	XGR1[15:8]							
		Write:								
$03A3	XGR1 (lo)	Read:	XGR1[7:0]							
		Write:								
$03A4	XGR2 (hi)	Read:	XGR2[15:8]							
		Write:								
$03A5	XGR2 (lo)	Read:	XGR2[7:0]							
		Write:								
$03A6	XGR3 (hi)	Read:	XGR3[15:8]							
		Write:								
$03A7	XGR3 (lo)	Read:	XGR3[7:0]							
		Write:								
$03A8	XGR4 (hi)	Read:	XGR4[15:8]							
		Write:								
$03A9	XGR4 (lo)	Read:	XGR4[7:0]							
		Write:								
$03AA	XGR5 (hi)	Read:	XGR5[15:8]							
		Write:								
$03AB	XGR5(lo)	Read:	XGR5[7:0]							
		Write:								
$03AC	XGR6 (hi)	Read:	XGR6[15:8]							
		Write:								
$03AD	XGR6 (lo)	Read:	XGR6[7:0]							
		Write:								
$03AE	XGR7 (hi)	Read:	XGR7[15:8]							
		Write:								
$03AF	XGR7 (lo)	Read:	XGR7[7:0]							
		Write:								
$03B0 - $03BF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$03C0 - $07FF   **Reserved**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$03C0 - $07FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

1.7 Part ID Assignments

The part ID is located in two 8-bit registers PARTIDH and PARTIDL (addresses $001A and $001B). The read-only value is a unique part ID for each revision of the chip. **Table 1-2** shows the assigned part ID number and Mask Set number.

Table 1-2 Assigned Part ID Numbers

Device	Mask Set Number	Part ID[1]
MC9S12XDP512	L40V	$C400

NOTES:

1. The coding is as follows:
Bit 15-12: Major family identifier
Bit 11-8: Minor family identifier
Bit 7-4: Major mask set revision number including FAB transfers
Bit 3-0: Minor - non full - mask set revision

Section 2 Signal Description

This section describes signals that connect off-chip. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals. It is built from the signal description sections of the Block User Guides of the individual IP blocks on the device.

2.1 Device Pinout

The MC9S12XDP512 is available in a 144-pin Low Profile Flat Quad Package (LQFP),112-pin Low Profile Flat Quad Package (LQFP) and in a 80-pin Quad Flat Package (QFP). The XD-Family of devices offers pin-compatible packaged devices to assist with system development and accommodate expansion of the application.

The MC9S12XDP512 device is offered in the following options:

- 144-pin LQFP package with an external bus interface (address/data bus)
- 112-pin LQFP without external bus interface
- 80-pin QFP without external bus interface

Most pins perform two or more functions, as described in more detail in **Section 2.2 Signal Properties Summary**. **Figure 2-1**, **Figure 2-2** and **Figure 2-3** show the pin assignments for the various packages.

Figure 2-1 MC9S12XD-Family Pin Assignment 144 LQFP Package

MC9S12XD-Family
144 LQFP

Pins shown in *BOLD-ITALICS* neither available on the 112 LQFP
nor on the 80 QFP Package Option

Pins shown in **BOLD** are not available on the 80 QFP package

Left side pins (1–36):

1 — $\overline{SS1}$/PWM3/KWP3/PP3
2 — SCK1/PWM2/KWP2/PP2
3 — MOSI1/PWM1/KWP1/PP1
4 — MISO1/PWM0/KWP0/PP0
5 — $\overline{CS1}$/KWJ2/PJ2
6 — NOACC/ADDR22/PK6
7 — IQSTAT3/ADDR19/PK3
8 — IQSTAT2/ADDR18/PK2
9 — IQSTAT1/ADDR17/PK1
10 — IQSTAT0/ADDR16/PK0
11 — IOC0/PT0
12 — IOC1/PT1
13 — IOC2/PT2
14 — IOC3/PT3
15 — VDD1
16 — VSS1
17 — IOC4/PT4
18 — IOC5/PT5
19 — IOC6/PT6
20 — IOC7/PT7
21 — ADDR21/PK5
22 — ADDR20/PK4
23 — TXD2/KWJ1/PJ1
24 — RXD2/KWJ0/PJ0
25 — MODC/BKGD
26 — VDDX2
27 — VSSX2
28 — DATA8/PC0
29 — DATA9/PC1
30 — DATA10/PC2
31 — DATA11/PC3
32 — $\overline{UDS}$/ADDR0/PB0
33 — ADDR1/PB1
34 — ADDR2/PB2
35 — ADDR3/PB3
36 — ADDR4/PB4

Bottom side pins (37–72):

37 — ADDR5/PB5
38 — ADDR6/PB6
39 — ADDR7/PB7
40 — DATA12/PC4
41 — DATA13/PC5
42 — DATA14/PC6
43 — DATA15/PC7
44 — TXD5/$\overline{SS2}$/KWH7/PH7
45 — RXD5/SCK2/KWH6/PH6
46 — TXD4/MOSI2/KWH5/PH5
47 — RXD4/MISO2/KWH4/PH4
48 — XCLKS/ECLKX2/PE7
49 — $\overline{TAGHI}$/MODB/PE6
50 — RE/$\overline{TAGLO}$/MODA/PE5
51 — ECLK/PE4
52 — VSSR1
53 — VDDR1
54 — RESET
55 — VDDPLL
56 — XFC
57 — VSSPLL
58 — EXTAL
59 — XTAL
60 — TEST
61 — $\overline{SS1}$/KWH3/PH3
62 — SCK1/KWH2/PH2
63 — MOSI1/KWH1/PH1
64 — MISO1/KWH0/PH0
65 — PD0/DATA0
66 — PD1/DATA1
67 — PD2/DATA2
68 — PD3/DATA3
69 — $\overline{LDS}$/$\overline{LSTRB}$/PE3/EROMCTL
70 — WE/R/$\overline{W}$/PE2
71 — $\overline{IRQ}$/PE1
72 — $\overline{XIRQ}$/PE0

Top side pins (109–144):

144 — PP4/KWP4/PWM4/MISO2
143 — PP5/KPW5/PWM5/MOSI2
142 — PP6/KWP6/PWM6/$\overline{SS2}$
141 — PP7/KWP7/PWM7/SCK2
140 — PK7/ROMCTL/EWAIT
139 — VDDX1
138 — VSSX1
137 — PM0/RXCAN0
136 — PM1/TXCAN0
135 — PM2/RXCAN1/RXCAN0/MISO0
134 — PM3/TXCAN1/TXCAN0/$\overline{SS0}$
133 — PM4/RXCAN2/RXCAN0/RXCAN4/MOSI0
132 — PM5/TXCAN2/TXCAN0/RXCAN4/SCK0
131 — PJ4/KWJ4/SDA1/$\overline{CS0}$
130 — PJ5/KWJ5/SCL1/$\overline{CS2}$
129 — PJ6/KWJ6/RXCAN4/SDA0
128 — PJ7/KWJ7/TXCAN4/SCL0
127 — VREGEN
126 — PS7/$\overline{SS0}$
125 — PS6/SCK0
124 — PS5/MOSI0
123 — PS4/MISO0
122 — PS3/TXD1
121 — PS2/RXD1
120 — PS1/TXD0
119 — PS0/RXD0
118 — PM6/RXCAN3/RXCAN4/RXD3
117 — PM7/TXCAN3/TXCAN4/TXD3
116 — PAD23/AN23
115 — PAD22/AN22
114 — PAD21/AN21
113 — PAD20/AN20
112 — PAD19/AN19
111 — PAD18/AN18
110 — VSSA
109 — VRL

Right side pins (73–108):

108 — VRH
107 — VDDA
106 — PAD17/AN17
105 — PAD16/AN16
104 — PAD15/AN15
103 — PAD07/AN07
102 — PAD14/AN14
101 — PAD06/AN06
100 — PAD13/AN13
99 — PAD05/AN05
98 — PAD12/AN12
97 — PAD04/AN04
96 — PAD11/AN11
95 — PAD03/AN03
94 — PAD10/AN10
93 — PAD02/AN02
92 — PAD09/AN09
91 — PAD01/AN01
90 — PAD08/AN08
89 — PAD00/AN00
88 — VSS2
87 — VDD2
86 — PD7/DATA7
85 — PD6/DATA6
84 — PD5/DATA5
83 — PD4/DATA4
82 — VDDR2
81 — VSSR2
80 — PA7/ADDR15
79 — PA6/ADDR14
78 — PA5/ADDR13
77 — PA4/ADDR12
76 — PA3/ADDR11
75 — PA2/ADDR10
74 — PA1/ADDR9
73 — PA0/ADDR8

Figure 2-2 MC9S12XDP512 Pin assignments 112 LQFP Package

Figure 2-3 MC9S12XDP512 Pin assignments 80 QFP Package

2.2 Signal Properties Summary

Table 2-1 summarizes the pin functionality.

Table 2-1 Signal Properties Summary

Pin Name Funct. 1	Pin Name Funct. 2	Pin Name Funct. 3	Pin Name Funct. 4	Pin Name Funct. 5	Power Supply	Internal Pull Resistor		Description
						CTRL	Reset State	
EXTAL	—	—	—	—	VDDPLL	NA	NA	Oscillator Pins
XTAL	—	—	—	—	VDDPLL	NA	NA	
$\overline{\text{RESET}}$	—	—	—	—	VDDR	PULLUP		External Reset
TEST	—	—	—	—	N.A.	RESET PIN	DOWN	Test Input
VREGEN	—	—	—	—	VDDX	Always on	Up	Voltage Regulator Enable Input
XFC	—	—	—	—	VDDPLL	NA	NA	PLL Loop Filter
BKGD	MODC	—	—	—	VDDR	Always on	Up	Background Debug
PAD[23:08]	AN[15:0]	—	—	—	VDDA	PER0 AD1/ PER1 AD1	Disabled	Port AD Inputs of ATD1, Analog Inputs of ATD1
PAD[07:00]	AN[7:0]	—	—	—	VDDA	PER1 AD0	Disabled	Port AD Inputs of ATD0, Analog Inputs of ATD0
PA[7:0]	ADDR[15:8]	IVD[15:8]	—	—	VDDR	PUCR	Disabled	Port A I/O, Address Bus, Internal Visibility Data
PB[7:1]	ADDR[7:1]	IVD[7:0]	—	—	VDDR	PUCR	Disabled	Port B I/O, Address Bus, Internal Visibility Data
PB0	ADDR0	$\overline{\text{UDS}}$			VDDR	PUCR	Disabled	Port B I/O, Address Bus, Upper Data Strobe
PC[7:0]	DATA[15:8]	—	—	—	VDDR	PUCR	Disabled	Port C I/O, Data Bus
PD[7:0]	DATA[7:0]	—	—	—	VDDR	PUCR	Disabled	Port D I/O, Data Bus
PE7	ECLKX2	$\overline{\text{XCLKS}}$	—	—	VDDR	PUCR	Up	Port E I/O, System clock output, Clock Select
PE6	$\overline{\text{TAGHI}}$	MODB	—	—	VDDR	While $\overline{\text{RESET}}$ pin is low: Down		Port E I/O, Tag High, Mode Input
PE5	$\overline{\text{RE}}$	MODA	$\overline{\text{TAGLO}}$	—	VDDR	While RESET pin is low: Down		Port E I/O, Read Enable, Mode Input, Tag Low Input
PE4	ECLK	—	—	—	VDDR	PUCR	Up	Port E I/O, Bus Clock Output
PE3	$\overline{\text{LSTRB}}$	$\overline{\text{LDS}}$	EROMCTL	—	VDDR	PUCR	Up	Port E I/O, Low Byte Data strobe, EROMON control
PE2	R/$\overline{\text{W}}$	$\overline{\text{WE}}$	—	—	VDDR	PUCR	Up	Port E I/O, Read/Write
PE1	$\overline{\text{IRQ}}$	—	—	—	VDDR	PUCR	Up	Port E Input, Maskable Interrupt
PE0	$\overline{\text{XIRQ}}$	—	—	—	VDDR	PUCR	Up	Port E Input, Non Maskable Interrupt
PH7	KWH7	SS2	TXD5	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, SS of SPI2, TXD of SCI5

Pin Name Funct. 1	Pin Name Funct. 2	Pin Name Funct. 3	Pin Name Funct. 4	Pin Name Funct. 5	Power Supply	Internal Pull Resistor		Description
						CTRL	Reset State	
PH6	KWH6	SCK2	RXD5	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, SCK of SPI2, RXD of SCI5
PH5	KWH5	MOSI2	TXD4	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, MOSI of SPI2, TXD of SCI4
PH4	KWH4	MISO2	RXD4	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, MISO of SPI2, RXD of SCI4
PH3	KWH3	SS1	—	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, SS of SPI1
PH2	KWH2	SCK1	—	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, SCK of SPI1
PH1	KWH1	MOSI1	—	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, MOSI of SPI1
PH0	KWH0	MISO1	—	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, MISO of SPI1
PJ7	KWJ7	TXCAN4	SCL0	TXCAN0	VDDX	PERJ/ PPSJ	Up	Port J I/O, Interrupt, TX of CAN4, SCL of IIC0, TX of CAN0
PJ6	KWJ6	RXCAN4	SDA0	RXCAN0	VDDX	PERJ/ PPSJ	Up	Port J I/O, Interrupt, RX of CAN4, SDA of IIC0, RX of CAN0
PJ5	KWJ5	SCL1	$\overline{CS2}$	—	VDDX	PERJ/ PPSJ	Up	Port J I/O, Interrupt, SCL of IIC1, Chip Select 2
PJ4	KWJ4	SDA1	$\overline{CS0}$	—	VDDX	PERJ/ PPSJ	Up	Port J I/O, Interrupt, SDA of IIC1, Chip Select 0
PJ2	KWJ2	$\overline{CS1}$	—	—	VDDX	PERJ/ PPSJ	Up	Port J I/O, Interrupts, Chip Select 1
PJ1	KWJ1	TXD2	—	—	VDDX	PERJ/ PPSJ	Up	Port J I/O, Interrupts, TXD of SCI2
PJ0	KWJ0	RXD2	—	—	VDDX	PERJ/ PPSJ	Up	Port J I/O, Interrupts, RXD of SCI2
PK7	$\overline{EWAIT}$	ROMCTL	—	—	VDDX	PUCR	Up	Port K I/O, EWAIT input, ROM On Control
PK6	NOACC	ADDR22	—	—	VDDX	PUCR	Up	Port K I/O, Extended Address, No Access
PK[5:4]	ADDR [21:20]	—	—	—	VDDX	PUCR	Up	Port K I/O, Extended Addresses
PK3	ADDR19	IQSTAT3	—	—	VDDX	PUCR	Up	Extended Address, PIPE status
PK2	ADDR18	IQSTAT2	—	—	VDDX	PUCR	Up	Extended Address, PIPE status
PK1	ADDR17	IQSTAT1	—	—	VDDX	PUCR	Up	Extended Address, PIPE status
PK0	ADDR16	IQSTAT0	—	—	VDDX	PUCR	Up	Extended Address, PIPE status
PM7	TXCAN4	TXD3	TXCAN3	—	VDDX	PERM/ PPSM	Disabled	Port M I/O, TX of CAN3&4, TXD of SCI3
PM6	RXCAN4	RXD3	RXCAN3	—	VDDX	PERM/ PPSM	Disabled	Port M I/O RX of CAN3&4, RXD of SCI3
PM5	TXCAN2	TXCAN0	TXCAN4	SCK0	VDDX	PERM/ PPSM	Disabled	Port M I/OCAN0, CAN2, CAN4, SCK of SPI0

Pin Name Funct. 1	Pin Name Funct. 2	Pin Name Funct. 3	Pin Name Funct. 4	Pin Name Funct. 5	Power Supply	Internal Pull Resistor		Description
						CTRL	Reset State	
PM4	RXCAN2	RXCAN0	RXCAN4	MOSI0	VDDX	PERM/ PPSM	Disabled	Port M I/O, CAN0, CAN2, CAN4, MOSI of SPI0
PM3	TXCAN1	TXCAN0	—	$\overline{SS0}$	VDDX	PERM/ PPSM	Disabled	Port M I/O TX of CAN1, CAN0, $\overline{SS}$ of SPI0
PM2	RXCAN1	RXCAN0	—	MISO0	VDDX	PERM/ PPSM	Disabled	Port M I/O, RX of CAN1, CAN0, MISO of SPI0
PM1	TXCAN0		—	—	VDDX	PERM/ PPSM	Disabled	Port M I/O, TX of CAN0
PM0	RXCAN0		—	—	VDDX	PERM/ PPSM	Disabled	Port M I/O, RX of CAN0
PP7	KWP7	PWM7	SCK2	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 7 of PWM, SCK of SPI2
PP6	KWP6	PWM6	SS2	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 6 of PWM, SS of SPI2
PP5	KWP5	PWM5	MOSI2	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 5 of PWM, MOSI of SPI2
PP4	KWP4	PWM4	MISO2	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 4 of PWM, MISO2 of SPI2
PP3	KWP3	PWM3	$\overline{SS1}$	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 3 of PWM, $\overline{SS}$ of SPI1
PP2	KWP2	PWM2	SCK1	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 2 of PWM, SCK of SPI1
PP1	KWP1	PWM1	MOSI1	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 1 of PWM, MOSI of SPI1
PP0	KWP0	PWM0	MISO1	—	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, Channel 0 of PWM, MISO2 of SPI1
PS7	SS0	—	—	—	VDDX	PERS/ PPSS	Up	Port S I/O, SS of SPI0
PS6	SCK0	—	—	—	VDDX	PERS/ PPSS	Up	Port S I/O, SCK of SPI0
PS5	MOSI0	—	—	—	VDDX	PERS/ PPSS	Up	Port S I/O, MOSI of SPI0
PS4	MISO0	—	—	—	VDDX	PERS/ PPSS	Up	Port S I/O, MISO of SPI0
PS3	TXD1	—	—	—	VDDX	PERS/ PPSS	Up	Port S I/O, TXD of SCI1
PS2	RXD1	—	—	—	VDDX	PERS/ PPSS	Up	Port S I/O, RXD of SCI1
PS1	TXD0	—	—	—	VDDX	PERS/ PPSS	Up	Port S I/O, TXD of SCI0
PS0	RXD0	—	—	—	VDDX	PERS/ PPSS	Up	Port S I/O, RXD of SCI0

Pin Name Funct. 1	Pin Name Funct. 2	Pin Name Funct. 3	Pin Name Funct. 4	Pin Name Funct. 5	Power Supply	Internal Pull Resistor		Description
						CTRL	Reset State	
PT[7:0]	IOC[7:0]	—	—	—	VDDX	PERT/ PPST	Disabled	Port T I/O, Timer channels

2.3 Detailed Signal Descriptions

2.3.1 EXTAL, XTAL — Oscillator Pins

EXTAL and XTAL are the crystal driver and external clock pins. On reset all the device clocks are derived from the EXTAL input frequency. XTAL is the crystal output.

2.3.2 $\overline{\text{RESET}}$ — External Reset Pin

An active low bidirectional control signal, it acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset. The $\overline{\text{RESET}}$ pin has an internal pullup device.

2.3.3 TEST — Test Pin

This input only pin is reserved for test. This pin has a pulldown device.

> *NOTE:* *The TEST pin must be tied to VSS in all applications.*

2.3.4 VREGEN — Voltage Regulator Enable Pin

This input only pin enables or disables the on-chip voltage regulator. The input has a pullup device.

2.3.5 XFC — PLL Loop Filter Pin

Please ask your Motorola representative for the interactive application note to compute PLL loop filter elements. Any current leakage on this pin must be avoided.

XFC

MCU

R$_0$

C$_P$

C$_S$

VDDPLL   VDDPLL
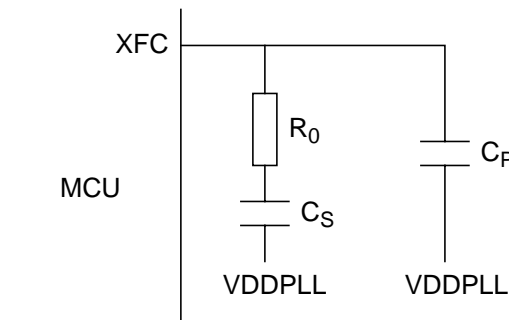
Figure 2-4 PLL Loop Filter Connections

2.3.6 BKGD / MODC — Background Debug and Mode Pin

The BKGD/MODC pin is used as a pseudo-open-drain pin for the background debug communication. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. The BKGD pin has a pullup device.

2.3.7 PAD[23:08] / AN[15:0] — Port AD Input Pin of ATD1

PAD[23:08] are general purpose input or output pins and analog inputs AN[15:0] of the analog to digital converter ATD1.

2.3.8 PAD[07:00] / AN[7:0] — Port AD Input Pins of ATD0

PAD[07:00] are general purpose input or output pins and analog inputs AN[7:0] of the analog to digital converter ATD0.

2.3.9 PA[7:0] / ADDR[15:8] / IVD[15:8] — Port A I/O Pins

PA7-PA0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the external address bus. In MCU emulation modes of operation, these pins are used for external address bus and internal visibility read data.

2.3.10 PB[7:1] / ADDR[7:1] / IVD[7:1] — Port B I/O Pins

PB7-PB1 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the external address bus. In MCU emulation modes of operation, these pins are used for external address bus and internal visibility read data.

2.3.11 PB0 / ADDR0 / $\overline{\text{UDS}}$ / IVD[0] — Port B I/O Pin

PB0 is a general purpose input or output pin. In MCU expanded modes of operation, this pin is used for the external address bus ADDR0 or as upper data strobe signal. In MCU emulation modes of operation, this pin is used for external address bus ADDR0 and internal visibility read data IVD0.

2.3.12 PC[7:0] / DATA [15:8] — Port C I/O Pins

PC7-PC0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the external data bus.

The input voltage thresholds for PC[7:0] can be configured to reduced levels, to allow data from an external 3.3V peripheral to be read by the MCU operating at 5.0V. The input voltage thresholds for PC[7:0] are configured to reduced levels out of reset in expanded and emulation modes.

2.3.13 PD[7:0] / DATA [7:0] — Port D I/O Pins

PD7-PD0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the external data bus.

The input voltage thresholds for PD[7:0] can be configured to reduced levels, to allow data from an external 3.3V peripheral to be read by the MCU operating at 5.0V. The input voltage thresholds for PD[7:0] are configured to reduced levels out of reset in expanded and emulation modes.

2.3.14 PE7 / ECLKX2 / $\overline{\text{XCLKS}}$ — Port E I/O Pin 7

PE7 is a general purpose input or output pin. The $\overline{\text{XCLKS}}$ is an input signal which controls whether a crystal in combination with the internal loop controlled (low power) Pierce oscillator is used or whether full swing Pierce oscillator/external clock circuitry is used.

The XCLKS pin selects the oscillator configuration during RESET low phase while a clock quality check is ongoing. This is the case for:

- Power on Reset or Low Voltage Reset
- Clock Monitor Reset
- Any Reset while in Self Clock Mode or Full Stop Mode

The selected oscillator configuration is frozen with the rising edge of RESET.

The pin can be configured to drive the internal system clock ECLKX2.

Figure 2-5 Loop Controlled Pierce Oscillator Connections (PE7=1)
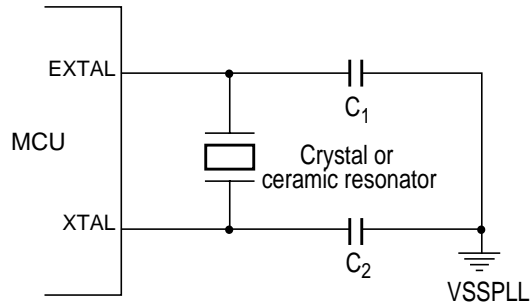
Figure 2-6 Full Swing Pierce Oscillator Connections (PE7=0)
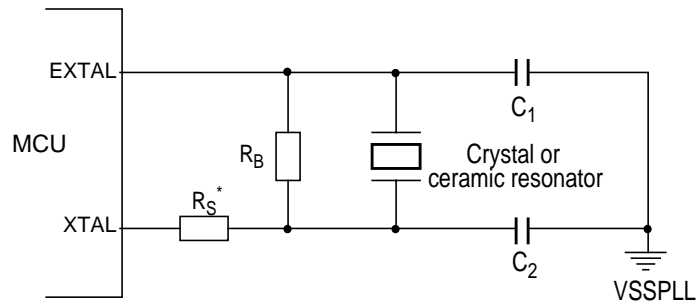
Figure 2-7 External Clock Connections (PE7=0)
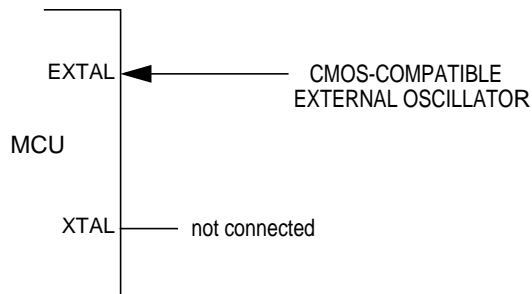
2.3.15 PE6 / MODB / $\overline{\text{TAGHI}}$ — Port E I/O Pin 6

PE6 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODB bit at the rising edge of $\overline{\text{RESET}}$. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low. $\overline{\text{TAGHI}}$ is used to tag the high half of the instruction word being read into the instruction queue.

The input voltage threshold for PE6 can be configured to reduced levels, to allow data from an external 3.3V peripheral to be read by the MCU operating at 5.0V. The input voltage threshold for PE6 is configured to reduced levels out of reset in expanded and emulation modes.

2.3.16 PE5 / MODA / $\overline{\text{TAGLO}}$ / $\overline{\text{RE}}$ — Port E I/O Pin 5

PE5 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODA bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the Read Enable $\overline{\text{RE}}$ output. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low. $\overline{\text{TAGLO}}$ is used to tag the low half of the instruction word being read into the instruction queue.

The input voltage threshold for PE5 can be configured to reduced levels, to allow data from an external 3.3V peripheral to be read by the MCU operating at 5.0V. The input voltage threshold for PE5 is configured to reduced levels out of reset in expanded and emulation modes.

2.3.17 PE4 / ECLK — Port E I/O Pin 4

PE4 is a general purpose input or output pin. It can be configured to drive the internal bus clock ECLK. ECLK can be used as a timing reference.

2.3.18 PE3 / $\overline{\text{LSTRB}}$ / $\overline{\text{LDS}}$ / EROMCTL— Port E I/O Pin 3

PE3 is a general purpose input or output pin. In MCU expanded modes of operation, $\overline{\text{LSTRB}}$ or $\overline{\text{LDS}}$ can be used for the low byte strobe function to indicate the type of bus access. At the rising edge of $\overline{\text{RESET}}$ the state of this pin is latched to the EROMON bit.

2.3.19 PE2 / R/$\overline{\text{W}}$ / $\overline{\text{WE}}$— Port E I/O Pin 2

PE2 is a general purpose input or output pin. In MCU expanded modes of operations, this pin drives the read/write output signal or write enable output signal for the external bus. It indicates the direction of data on the external bus.

2.3.20 PE1 / $\overline{\text{IRQ}}$ — Port E Input Pin 1

PE1 is a general purpose input pin and the maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

2.3.21 PE0 / $\overline{\text{XIRQ}}$ — Port E Input Pin 0

PE0 is a general purpose input pin and the non-maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

2.3.22 PH7 / KWH7 / $\overline{\text{SS2}}$ / TXD5 — Port H I/O Pin 7

PH7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as slave select pin $\overline{\text{SS}}$ of the Serial Peripheral Interface 2 (SPI2). It can be configured as the transmit pin TXD of Serial Communication Interface 5 (SCI5).

2.3.23 PH6 / KWH6 / SCK2 / RXD5 — Port H I/O Pin 6

PH6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 2 (SPI2). It can be configured as the receive pin RXD of Serial Communication Interface 5 (SCI5).

2.3.24 PH5 / KWH5 / MOSI2 / TXD4 — Port H I/O Pin 5

PH5 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 2 (SPI2). It can be configured as the transmit pin TXD of Serial Communication Interface 4 (SCI4).

2.3.25 PH4 / KWH4 / MISO2 / RXD4 — Port H I/O Pin 2

PH4 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 2 (SPI2). It can be configured as the receive pin RXD of Serial Communication Interface 4 (SCI4).

2.3.26 PH3 / KWH3 / $\overline{\text{SS1}}$ — Port H I/O Pin 3

PH3 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as slave select pin $\overline{\text{SS}}$ of the Serial Peripheral Interface 1 (SPI1).

2.3.27 PH2 / KWH2 / SCK1 — Port H I/O Pin 2

PH2 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 1 (SPI1).

2.3.28 PH1 / KWH1 / MOSI1 — Port H I/O Pin 1

PH1 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 1 (SPI1).

2.3.29 PH0 / KWH0 / MISO1 — Port H I/O Pin 0

PH0 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 1 (SPI1).

2.3.30 PJ7 / KWJ7 / TXCAN4 / SCL0 / TXCAN0— PORT J I/O Pin 7

PJ7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the transmit pin TXCAN for the Motorola Scalable Controller Area Network controller 0 or 4 (CAN0 or CAN4) or as the serial clock pin SCL of the IIC0 module.

2.3.31 PJ6 / KWJ6 / RXCAN4 / SDA0 / RXCAN0 — PORT J I/O Pin 6

PJ6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the receive pin RXCAN for the Motorola Scalable Controller Area Network controller 0 or 4 (CAN0 or CAN4) or as the serial data pin SDA of the IIC0 module.

2.3.32 PJ5 / KWJ5 / SCL1 / $\overline{\text{CS2}}$ — PORT J I/O Pin 5

PJ5 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the serial clock pin SCL of the IIC1 module. It can be configured to provide a chip select output.

2.3.33 PJ4 / KWJ4 / SDA1 / $\overline{\text{CS0}}$ — PORT J I/O Pin 4

PJ4 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the serial data pin SDA of the IIC1 module. It can be configured to provide a chip select output.

2.3.34 PJ2 / KWJ2 / $\overline{\text{CS1}}$ — PORT J I/O Pin 2

PJ2 is a general purpose input or output pins. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured to provide a chip select output.

2.3.35 PJ1 / KWJ1 / TXD2 — PORT J I/O Pin 1

PJ1 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the transmit pin TXD of the Serial Communication Interface 2 (SCI2).

2.3.36 PJ0 / KWJ0 / RXD2 — PORT J I/O Pin 0

PJ0 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the receive pin RXD of the Serial Communication Interface 2 (SCI2).

2.3.37 PK7 / $\overline{\text{EWAIT}}$ / ROMCTL — Port K I/O Pin 7

PK7 is a general purpose input or output pin. During MCU emulation modes and normal expanded modes of operation, this pin is used to enable the Flash EEPROM memory in the memory map (ROMCTL). At the rising edge of $\overline{\text{RESET}}$, the state of this pin is latched to the ROMON bit. The $\overline{\text{EWAIT}}$ input signal maintains the external bus access until the external device is ready to capture data (write) or provide data (read).

2.3.38 PK6 / NOACC / ADDR22 — Port K I/O Pin 6

PK6 is a general purpose input or output pin. During MCU expanded modes of operation, the NOACC signal is used to indicate that the current bus cycle is an unused or "free" cycle. This signal will assert when the CPU is not using the bus. This pin also provides the expanded address ADDR22 for the external bus. In Emulation modes NOACC is available and is time multiplexed with the high address.

2.3.39 PK[5:4] / ADDR[21:20] — Port K I/O Pins [5:4]

PK5-PK4 are general purpose input or output pins. In MCU expanded modes of operation, these pins provide the expanded address ADDR[21:20] for the external bus.

2.3.40 PK[3:0] / ADDR[19:16] / IQSTAT[3:0] — Port K I/O Pins [3:0]

PK3-PK0 are general purpose input or output pins. In MCU expanded modes of operation, these pins provide the expanded address ADDR[19:16] for the external bus and carry instruction pipe information.

2.3.41 PM7 / TXCAN3 / TXCAN4 / TXD3 — Port M I/O Pin 7

PM7 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Motorola Scalable Controller Area Network controller 3 or 4 (CAN3 or CAN4). PM7 can be configured as the transmit pin TXD3 of the Serial Communication Interface 3 (SCI3).

2.3.42 PM6 / RXCAN3 / RXCAN4 / RXD3 — Port M I/O Pin 6

PM6 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Motorola Scalable Controller Area Network controller 3 or 4 (CAN3 or CAN4). PM6 can be configured as the receive pin RXD3 of the Serial Communication Interface 3 (SCI3).

2.3.43 PM5 / TXCAN0 / TXCAN2 / TXCAN4 / SCK0 — Port M I/O Pin 5

PM5 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Motorola Scalable Controller Area Network controllers 0, 2 or 4 (CAN0, CAN2 or CAN4). It can be configured as the serial clock pin SCK of the Serial Peripheral Interface 0 (SPI0).

2.3.44 PM4 / RXCAN0 / RXCAN2 / RXCAN4 / MOSI0 — Port M I/O Pin 4

PM4 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Motorola Scalable Controller Area Network controllers 0,2 or 4 (CAN0, CAN2 or CAN4). It can be configured as the master output (during master mode) or slave input pin (during slave mode) MOSI for the Serial Peripheral Interface 0 (SPI0).

2.3.45 PM3 / TXCAN1 / TXCAN0 / $\overline{SS0}$ — Port M I/O Pin 3

PM3 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Motorola Scalable Controller Area Network controllers 1 or 0 (CAN1 or CAN0). It can be configured as the slave select pin $\overline{SS}$ of the Serial Peripheral Interface 0 (SPI0).

2.3.46 PM2 / RXCAN1 / RXCAN0 / MISO0 — Port M I/O Pin 2

PM2 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Motorola Scalable Controller Area Network controllers 1 or 0 (CAN1 or CAN0). It can be configured as the master input (during master mode) or slave output pin (during slave mode) MISO for the Serial Peripheral Interface 0 (SPI0).

2.3.47 PM1 / TXCAN0 — Port M I/O Pin 1

PM1 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the Motorola Scalable Controller Area Network controller 0 (CAN0).

2.3.48 PM0 / RXCAN0 — Port M I/O Pin 0

PM0 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the Motorola Scalable Controller Area Network controller 0 (CAN0).

2.3.49 PP7 / KWP7 / PWM7 / SCK2 — Port P I/O Pin 7

PP7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 7 output. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 2 (SPI2).

2.3.50 PP6 / KWP6 / PWM6 / $\overline{SS2}$ — Port P I/O Pin 6

PP6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 6 output. It can be configured as slave select pin $\overline{SS}$ of the Serial Peripheral Interface 2 (SPI2).

2.3.51 PP5 / KWP5 / PWM5 / MOSI2 — Port P I/O Pin 5

PP5 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 5 output. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 2 (SPI2).

2.3.52 PP4 / KWP4 / PWM4 / MISO2 — Port P I/O Pin 4

PP4 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 4 output. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 2 (SPI2).

2.3.53 PP3 / KWP3 / PWM3 / $\overline{SS1}$ — Port P I/O Pin 3

PP3 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 3 output. It can be configured as slave select pin $\overline{SS}$ of the Serial Peripheral Interface 1 (SPI1).

2.3.54 PP2 / KWP2 / PWM2 / SCK1 — Port P I/O Pin 2

PP2 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 2 output. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 1 (SPI1).

2.3.55 PP1 / KWP1 / PWM1 / MOSI1 — Port P I/O Pin 1

PP1 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 1 output. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 1 (SPI1).

2.3.56 PP0 / KWP0 / PWM0 / MISO1 — Port P I/O Pin 0

PP0 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 0 output. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 1 (SPI1).

2.3.57 PS7 / $\overline{SS0}$ — Port S I/O Pin 7

PS7 is a general purpose input or output pin. It can be configured as the slave select pin $\overline{SS}$ of the Serial Peripheral Interface 0 (SPI0).

2.3.58 PS6 / SCK0 — Port S I/O Pin 6

PS6 is a general purpose input or output pin. It can be configured as the serial clock pin SCK of the Serial Peripheral Interface 0 (SPI0).

2.3.59 PS5 / MOSI0 — Port S I/O Pin 5

PS5 is a general purpose input or output pin. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 0 (SPI0).

2.3.60 PS4 / MISO0 — Port S I/O Pin 4

PS4 is a general purpose input or output pin. It can be configured as master input (during master mode) or slave output pin (during slave mode) MOSI of the Serial Peripheral Interface 0 (SPI0).

2.3.61 PS3 / TXD1 — Port S I/O Pin 3

PS3 is a general purpose input or output pin. It can be configured as the transmit pin TXD of Serial Communication Interface 1 (SCI1).

2.3.62 PS2 / RXD1 — Port S I/O Pin 2

PS2 is a general purpose input or output pin. It can be configured as the receive pin RXD of Serial Communication Interface 1 (SCI1).

2.3.63 PS1 / TXD0 — Port S I/O Pin 1

PS1 is a general purpose input or output pin. It can be configured as the transmit pin TXD of Serial Communication Interface 0 (SCI0).

2.3.64 PS0 / RXD0 — Port S I/O Pin 0

PS0 is a general purpose input or output pin. It can be configured as the receive pin RXD of Serial Communication Interface 0 (SCI0).

2.3.65 PT[7:0] / IOC[7:0] — Port T I/O Pins [7:0]

PT7-PT0 are general purpose input or output pins. They can be configured as input capture or output compare pins IOC7-IOC0 of the Enhanced Capture Timer (ECT).

2.4 Power Supply Pins

MC9S12XDP512 power and ground pins are described below.

> **NOTE:** *All VSS pins must be connected together in the application.*

2.4.1 VDDX1, VDDX2, VSSX1,VSSX2 — Power & Ground Pins for I/O Drivers

External power and ground for I/O drivers. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.2 VDDR1, VDDR2, VSSR1, VSSR2 — Power & Ground Pins for I/O Drivers & for Internal Voltage Regulator

External power and ground for I/O drivers and input to the internal voltage regulator. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.3 VDD1, VDD2, VSS1, VSS2 — Core Power Pins

Power is supplied to the MCU through VDD and VSS. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VREGEN is tied to ground.

> **NOTE:** *No load allowed except for bypass capacitors.*

2.4.4 VDDA, VSSA — Power Supply Pins for ATD and VREG

VDDA, VSSA are the power supply and ground input pins for the voltage regulator and the analog to digital converters.

2.4.5 VRH, VRL — ATD Reference Voltage Input Pins

VRH and VRL are the reference voltage input pins for the analog to digital converter.

2.4.6 VDDPLL, VSSPLL — Power Supply Pins for PLL

Provides operating voltage and ground for the Oscillator and the Phased-Locked Loop. This allows the supply voltage to the Oscillator and PLL to be bypassed independently.This 2.5V voltage is generated by the internal voltage regulator.

> **NOTE:** *No load allowed except for bypass capacitors.*

Table 2-2 MC9S12XDP512 Power and Ground Connection Summary

Mnemonic	Pin Number			Nominal Voltage	Description
	144-pin LQFP	112-pin LQFP	80-pin QFP		
VDD1, 2	15, 87	13, 65	9, 49	2.5 V	Internal power and ground generated by internal regulator
VSS1, 2	16, 88	14, 66	10, 50	0V	
VDDR1	53	41	29	5.0 V	External power and ground, supply to pin drivers and internal voltage regulator
VSSR1	52	40	28	0 V	
VDDX1	139	107	77	5.0 V	External power and ground, supply to pin drivers
VSSX1	138	106	76	0 V	
VDDX2	26	N.A.	N.A.	5.0 V	External power and ground, supply to pin drivers
VSSX2	27	N.A.	N.A.	0 V	
VDDR2	82	N.A.	N.A.	5.0 V	External power and ground, supply to pin drivers
VSSR2	81	N.A.	N.A.	0 V	
VDDA	107	83	59	5.0 V	Operating voltage and ground for the analog-to-digital converters and the reference for the internal voltage regulator, allows the supply voltage to the A/D to be bypassed independently.
VSSA	110	86	62	0 V	
VRL	109	85	61	0 V	Reference voltages for the analog-to-digital converter.
VRH	108	84	60	5.0 V	
VDDPLL	55	43	31	2.5 V	Provides operating voltage and ground for the Phased-Locked Loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator.
VSSPLL	57	45	33	0 V	
VREGEN	127	97	N.A.	5V	Internal Voltage Regulator enable/disable

2.4.7 VREGEN — On Chip Voltage Regulator Enable

Enables the internal 5V to 2.5V voltage regulator. If this pin is tied low, VDD1,2 and VDDPLL must be supplied externally.

Section 3 System Clock Description

3.1 Overview

The Clock and Reset Generator module (CRG) provides the internal clock signals for the core and all peripheral modules. **Figure 3-1** shows the clock connections from the CRG to all modules.

Consult the CRG Block User Guide for details on clock generation.
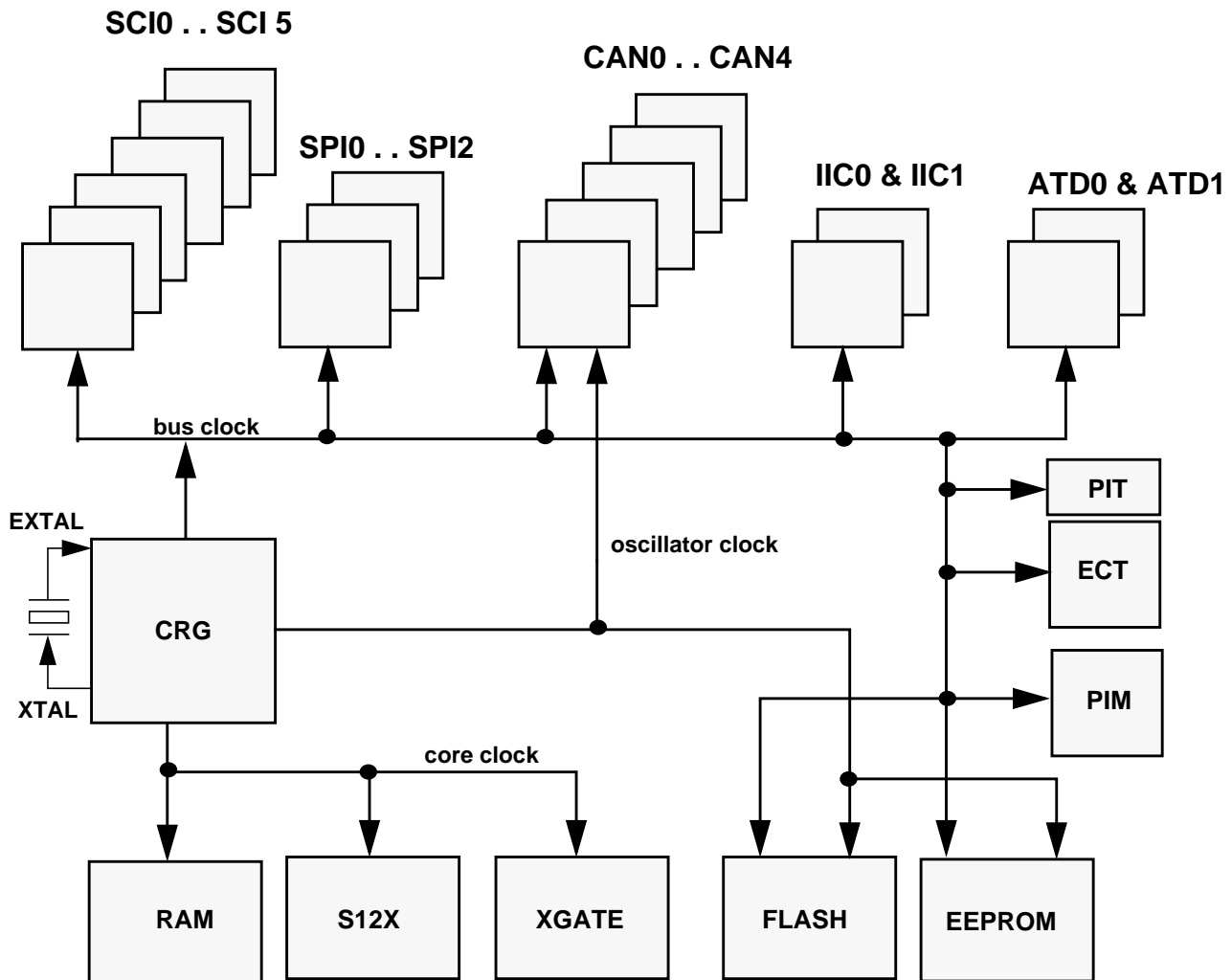
Figure 3-1 Clock Connections

The MCU's system clock can be supplied in several ways enabling a range of system operating frequencies to be supported:

- the on chip phase Locked Loop (PLL)

- the pll self clocking

- the Oscillator

The clock generated by the PLL or Oscillator provides the main system clock frequencies Core Clock and Bus Clock. As shown in **Figure 3-1** this system clocks are used throughout the MCU to drive the Core, the memories and the peripherals.

The Program Flash memory and the EEPROM are supplied by the Bus Clock and the Oscillator clock.The Oscillator clock is used as a time base to derive the program and erase times for the NVM's. Consult the FTX512k4 block guide and the EETX4K block guide for more details on the operation of the NVM's.

The CAN modules may be configured to have their clock sources derived either from the bus clock or directly from the Oscillator clock. This allows the user to select its clock based on the required jitter performance. Consult MSCAN block description for more details on the operation and configuration of the CAN blocks.

The frequency generated by the PLL is determined by the two registers REFDIV and SYNR.

> *Please note that it is possible to configure the PLL to generate a system frequency higher than that supported by the design of the device. It is the responsibility of the user to insure that the device is operated within it's specified limits at all time.*

In order to ensure the presence of the clock the MCU includes an on-chip Clock Monitor connected to the output of the Oscillator. The Clock Monitor can be configured to invoke the PLL self clocking mode or to generate a system reset if it is allowed to time out as a result of no oscillator clock being present.

In addition to the clock monitor the MCU also provides a clock quality checker which performs a more accurate check of the clock. The clock quality checker counts a predetermined number of clock edges within a defined time window to insure that the clock is running. The checker can be invoked following specific events such as on wake-up or clock monitor failure.

Section 4 Modes of Operation

4.1 Overview

The MCU can operate in six different modes. The different modes, the state of ROMCTL and EROMCTL pin on rising edge of $\overline{\text{RESET}}$ and the security state of the on chip Flash memory affects the following device characteristics:

- External bus interface configuration

- Access to Flash area and to unimplemented area

- Register visibility in Emulation and Expanded Mode

- Debug features enabled or disabled

The $\overline{\text{XCLKS}}$ pin defines the configuration of the on chip oscillator and the **VREGEN** pin defines whether the on chip voltage regulator is enabled or disabled.

4.2 Chip Configuration Summary

4.2.1 Mode Selection

The operating mode out of reset is determined by the states of the MODC, MODB, and MODA pins during reset (**Table 4-1**). The MODC, MODB, and MODA bits in the MODE register show the current operating mode and provide limited mode switching during operation. The states of the MODC, MODB, and MODA pins are latched into these bits on the rising edge of the reset signal.

Table 4-1 Mode selection

BKGD = MODC	PE6 = MODB	PE5 = MODA	Mode Description
0	0	0	Special Single Chip Mode
0	1	1	Emulation Expanded Mode
0	1	0	Special Test Mode
0	0	1	Emulation Single Chip Mode
1	0	0	Normal Single Chip Mode
1	0	1	Normal Expanded Mode
1	1	X	Reserved

4.2.2 ROMON and EROMON Pin Control Function

In Normal Expanded Modes and in Emulation Modes the ROMON bit and the EROMON bit in the MISC register defines if the on chip Flash memory is the memory map or not. For a detailed description of the ROMON and EROMON bits refer to the S12XMMC Block Guide.

The ROMCTL signal (PK7) allows the setting of the ROMON bit and EROMCTL signal (PE3) allows the setting of the EROMON bit in the MISC register.

 The state of the ROMCTL pin is latched into the ROMON bit in the MISC register on the rising edge of the $\overline{\text{RESET}}$ signal in Emulation Expanded Mode, Emulation Single Chip Mode and Normal Expanded Mode.(**Table 4-2**) The state of the EROMCTL pin is latched into the EROMON bit in the MISC register on the rising edge of the $\overline{\text{RESET}}$ signal in Emulation Expanded Mode or Emulation Single Chip Mode(**Table 4-4**).

Table 4-2 ROMON Pin Control Function

Mode	PK7 = ROMCTL	ROMON Bit
Special Single Chip Mode	X	1
Emulation Expanded Mode	0	0
	1	1
Special Test Mode	X	0
Emulation Single Chip Mode	0	0
	1	1
Normal Single Chip Mode	X	1
Normal Expanded Mode	0	0
	1	1

Table 4-3 EROMON Pin Control Function

Mode	PE3 = EROMCTL	EROMON Bit
Special Single Chip Mode	X	0
Emulation Expanded Mode	0	0
	1	1
Special Test Mode	X	0
Emulation Single Chip Mode	0	0
	1	1
Normal Single Chip Mode	X	0
Normal Expanded Mode	0	0
	1	1

4.2.3 Oscillator Configuration Pin Control

At reset the configuration of the Oscillator can be selected using the $\overline{\text{XCLKS}}$ pin. The state of this pin on the rising edge of the $\overline{\text{RESET}}$ pin determines which oscillator will be used.

Table 4-4 Clock Selection Based on PE7

PE7 = $\overline{\text{XCLKS}}$	Description
0	Full swing pierce oscillator or external clock source selected
1	Loop controlled pierce oscillator selected

4.2.4 Voltage Regulator Pin Control

The logic level on the voltage regulator enable VREGEN pin determines whether the on chip voltage regulator is used or not.

Table 4-5 Voltage Regulator VREGEN

VREGEN	Description
1	Internal Voltage Regulator enabled
0	Internal Voltage Regulator disabled, VDD1,2 and VDDPLL must be supplied externally with 2.5V

4.2.5 Register visibility in Emulation and Expanded modes

Table 4-6 shows a list of registers which may need to be "re-built" externally when using the MC9S12XDP512 in emulation modes. The notation "RE" and "RI" in the table refers to the source of the read data for the registers in each mode. In some cases the write data should update both the internal register and the external bus "WG". The change to the internal registers should have the same effect on the device operation when it is external.

RI: Read internal only, RE: Read external only, R0: Ready always 0

WI: write internal only, WG: Write int & ext, NW: No write

Table 4-6 Register Accessibility of Port Replacement Registers (PRR)

Port/Address	Module	Single Chip modes		Expanded Modes			
		Special Single Chip	Normal Single Chip	Emulation Single Chip	Normal Expanded Mode	Emulation Expanded Mode	Special Test Mode
PORTA/$0000	PIM	RI/WI	RI/WI	RE/WG	RI/WI	RE/WG	RI/WI
PORTB/$0001	PIM	RI/WI	RI/WI	RE/WG	RI/WI	RE/WG	RI/WI
DDRA/$0002	PIM	RI/WI	RI/WI	RE/WG	RI/WI	RE/WG	RI/WI
DDRB/$0003	PIM	RI/WI	RI/WI	RE/WG	RI/WI	RE/WG	RI/WI
PORTC/$0004	PIM	RI/WI	RI/WI	RE/WG	RI/WI	RE/WG	RI/WI
PORTD/$0005	PIM	RI/WI	RI/WI	RE/WG	RI/WI	RE/WG	RI/WI
DDRC/$0006	PIM	RI/WI	RI/WI	RE/WG	RI/WI	RE/WG	RI/WI
DDRD/$0007	PIM	RI/WI	RI/WI	RE/WG	RI/WI	RE/WG	RI/WI
PORTE/$0008	PIM	RI/WI	RI/WI	RE/WG	RI/WI	RE/WG	RI/WI
DDRE/$0009	PIM	RI/WI	RI/WI	RE/WG	RI/WI	RE/WG	RI/WI
EIFCTL/$000A	EBI	RI/WI	RI/WI	RE/WG	RI/WI	RE/WG	RI/WI
MODE/$000B	EBI	RI/WI	RI/WI	RE/WG	RI/WI	RE/WG	RI/WI
PUCR/$000C	PIM	RI/WI	RI/WI	RE/WG	RI/WI	RE/WG	RI/WI
RDRIV/$000D	PIM	RI/WI	RI/WI	RE/WG	RI/WI	RE/WG	RI/WI
RSVD/$000E	EBI	R0/NW	R0/NW	R0/NW	R0/NW	R0/NW	R0/NW
RSVD/$000F	EBI	R0/NW	R0/NW	R0/NW	R0/NW	R0/NW	R0/NW

Table 4-6 Register Accessibility of Port Replacement Registers (PRR)

		Single Chip modes		Expanded Modes			
MISC/$0013	MMC	RI/WI	RI/WI	RE/WG	RI/WI	RE/WG	RI/WI
PORTK/$0032	PIM	RI/WI	RI/WI	RE/WG	RI/WI	RE/WG	RI/WI
DDRK/$0033	PIM	RI/WI	RI/WI	RE/WG	RI/WI	RE/WG	RI/WI

4.3 Security

The MCU security feature allows the the protection of the on chip Flash and EEPROM memory. For a detailed description of the security features refer to the S12X9SEC block guide.

4.4 Low Power Modes

The microcontroller features three main low power modes. Consult the respective Block Guide for information on the module behavior in Stop, Pseudo Stop, and Wait Mode. An important source of information about the clock system is the Clock and Reset Generator Block Guide (CRG).

4.4.1 Stop Mode

Executing the CPU STOP instruction stops all clocks and the oscillator thus putting the chip in fully static mode. Wake up from this mode can be done via reset or external interrupts.

4.4.2 Pseudo Stop Mode

This mode is entered by executing the CPU STOP instruction. In this mode the oscillator is still running and the Real Time Interrupt (RTI) or Watchdog (COP) sub module can stay active. Other peripherals are turned off. This mode consumes more current than the full STOP mode, but the wake up time from this mode is significantly shorter.

4.4.3 Wait Mode

This mode is entered by executing the CPU WAI instruction. In this mode the CPU will not execute instructions. The internal CPU signals (address and databus) will be fully static. All peripherals stay active. For further power consumption the peripherals can individually turn off their local clocks.

4.4.4 Run Mode

Although this is not a low power mode, unused peripheral modules should not be enabled in order to save power.

4.5 Freeze Mode

The Enhanced Capture Timer, Pulse Width Modulator, Analog Digital Converters and the Periodic Interrupt Timer provide a software programmable option to freeze the module status during the Background Debug Module is active. This is useful when debugging application software. For detailed description of the behavior of the ATD0, ATD1, ECT, PWM and PIT during Background Debug Module block is active consult the corresponding Block Guides.

Section 5 Resets and Interrupts

5.1 Overview

Consult the S12XCPU Block Guide for information on Exception Processing.

5.2 Vectors

5.2.1 Vector Table

Table 5-1 lists interrupt sources and vectors in default order of priority. The Interrupt module (S12XINT) provides an Interrupt Vector Base Register (IVBR) to relocate the vectors. Associated with each I-bit maskable service request is a configuration register selecting if the service request is enabled, the service request priority level and whether the service request is handled either by the S12X CPU or by the XGATE DMA module.

The HPRIO register and functionality is no longer supported on the S12X devices. This functionality is superseded by a 7 level service request priority scheme. Please refer to the S12XINT Block Guide for detailed information.

Table 5-1 Interrupt Vector Locations

Vector Address[1]	XGATE Channel ID[2]	Interrupt Source	CCR Mask	Local Enable
$FFFE,	-	System Reset	None	None
$FFFC	-	Clock Monitor Reset	None	PLLCTL (CME, SCME)
$FFFA	-	COP Watchdog Reset	None	COP rate select
Vector Base + $F8	-	Unimplemented instruction trap	None	None
Vector Base+ $F6	-	SWI	None	None
Vector Base+ $F4	-	XIRQ	X-Bit	None
Vector Base+ $F2	-	IRQ	I-Bit	IRQCR (IRQEN)
Vector Base+ $F0	$78	Real Time Interrupt	I-Bit	CRGINT (RTIE)
Vector Base+ $EE	$77	Enhanced Capture Timer channel 0	I-Bit	TIE (C0I)
Vector Base + $EC	$76	Enhanced Capture Timer channel 1	I-Bit	TIE (C1I)
Vector Base+ $EA	$75	Enhanced Capture Timer channel 2	I-Bit	TIE (C2I)
Vector Base+ $E8	$74	Enhanced Capture Timer channel 3	I-Bit	TIE (C3I)
Vector Base+ $E6	$73	Enhanced Capture Timer channel 4	I-Bit	TIE (C4I)
Vector Base+ $E4	$72	Enhanced Capture Timer channel 5	I-Bit	TIE (C5I)
Vector Base + $E2	$71	Enhanced Capture Timer channel 6	I-Bit	TIE (C6I)
Vector Base+ $E0	$70	Enhanced Capture Timer channel 7	I-Bit	TIE (C7I)
Vector Base+ $DE	$6F	Enhanced Capture Timer overflow	I-Bit	TSRC2 (TOF)
Vector Base+ $DC	$6E	Pulse accumulator A overflow	I-Bit	PACTL (PAOVI)

Vector Base + $DA	$6D	Pulse accumulator input edge	I-Bit	PACTL (PAI)
Vector Base + $D8	$6C	SPI0	I-Bit	SPI0CR1 (SPIE, SPTIE)
Vector Base+ $D6	$6B	SCI0	I-Bit	SCI0CR2 (TIE, TCIE, RIE, ILIE)
Vector Base + $D4	$6A	SCI1	I-Bit	SCI1CR2 (TIE, TCIE, RIE, ILIE)
Vector Base + $D2	$69	ATD0	I-Bit	ATD0CTL2 (ASCIE)
Vector Base + $D0	$68	ATD1	I-Bit	ATD1CTL2 (ASCIE)
Vector Base + $CE	$67	Port J	I-Bit	PIEJ (PIEJ7-PIEJ0)
Vector Base + $CC	$66	Port H	I-Bit	PIEH (PIEH7-PIEH0)
Vector Base + $CA	$65	Modulus Down Counter underflow	I-Bit	MCCTL(MCZI)
Vector Base + $C8	$64	Pulse Accumulator B Overflow	I-Bit	PBCTL(PBOVI)
Vector Base + $C6	$63	CRG PLL lock	I-Bit	CRGINT(LOCKIE)
Vector Base + $C4	$62	CRG Self Clock Mode	I-Bit	CRGINT (SCMIE)
Vector Base + $C2	$61	Reserved		
Vector Base + $C0	$60	IIC0 Bus	I-Bit	IBCR0 (IBIE)
Vector Base + $BE	$5F	SPI1	I-Bit	SPI1CR1 (SPIE, SPTIE)
Vector Base + $BC	$5E	SPI2	I-Bit	SPI2CR1 (SPIE, SPTIE)
Vector Base + $BA	$5D	EEPROM	I-Bit	ECNFG (CCIE, CBEIE)
Vector Base + $B8	$5C	FLASH	I-Bit	FCNFG (CCIE, CBEIE)
Vector Base + $B6	$5B	CAN0 wake-up	I-Bit	CAN0RIER (WUPIE)
Vector Base + $B4	$5A	CAN0 errors	I-Bit	CAN0RIER (CSCIE, OVRIE)
Vector Base + $B2	$59	CAN0 receive	I-Bit	CAN0RIER (RXFIE)
Vector Base + $B0	$58	CAN0 transmit	I-Bit	CAN0TIER (TXEIE2-TXEIE0)
Vector Base + $AE	$57	CAN1 wake-up	I-Bit	CAN1RIER (WUPIE)
Vector Base + $AC	$56	CAN1 errors	I-Bit	CAN1RIER (CSCIE, OVRIE)
Vector Base + $AA	$55	CAN1 receive	I-Bit	CAN1RIER (RXFIE)
Vector Base + $A8	$54	CAN1 transmit	I-Bit	CAN1TIER (TXEIE2-TXEIE0)
Vector Base + $A6	$53	CAN2 wake-up	I-Bit	CAN2RIER (WUPIE)
Vector Base + $A4	$52	CAN2 errors	I-Bit	CAN2RIER (CSCIE, OVRIE)
Vector Base + $A2	$51	CAN2 receive	I-Bit	CAN2RIER (RXFIE)
Vector Base + $A0	$50	CAN2 transmit	I-Bit	CAN2TIER (TXEIE2-TXEIE0)
Vector Base + $9E	$4F	CAN3 wake-up	I-Bit	CAN3RIER (WUPIE)
Vector Base+ $9C	$4E	CAN3 errors	I-Bit	CAN3RIER (CSCIE, OVRIE)
Vector Base+ $9A	$4D	CAN3 receive	I-Bit	CAN3RIER (RXFIE)
Vector Base + $98	$4C	CAN3 transmit	I-Bit	CAN3TIER (TXEIE2-TXEIE0)
Vector Base + $96	$4B	CAN4 wake-up	I-Bit	CAN4RIER (WUPIE)
Vector Base + $94	$4A	CAN4 errors	I-Bit	CAN4RIER (CSCIE, OVRIE)

Vector Base + $92	$49	CAN4 receive	I-Bit	CAN4RIER (RXFIE)
Vector Base + $90	$48	CAN4 transmit	I-Bit	CAN4TIER (TXEIE2-TXEIE0)
Vector Base + $8E	$47	Port P Interrupt	I-Bit	PIEP (PIEP7-PIEP0)
Vector Base+ $8C	$46	PWM Emergency Shutdown	I-Bit	PWMSDN (PWMIE)
Vector Base + $8A	$45	SCI2	I-Bit	SCI2CR2 (TIE, TCIE, RIE, ILIE)
Vector Base + $88	$44	SCI3	I-Bit	SCI3CR2 (TIE, TCIE, RIE, ILIE)
Vector Base + $86	$43	SCI4	I-Bit	SCI4CR2 (TIE, TCIE, RIE, ILIE)
Vector Base + $84	$42	SCI5	I-Bit	SCI5CR2 (TIE, TCIE, RIE, ILIE)
Vector Base + $82	$41	IIC1 Bus	I-Bit	IBCR (IBIE)
Vector Base + $80	$40	Low Voltage interrupt LVI	I-Bit	VREGCTRL (LVIE)
Vector Base + $7E	$3F	Autonomous Periodical interrupt API	I-Bit	VREGAPICTRL (APIE)
Vector Base + $7C	$3E	Reserved		
Vector Base + $7A	$3D	Periodic Interrupt Timer	I-Bit	PITINTE (PINTE0)
Vector Base + $78	$3C	Periodic Interrupt Timer	I-Bit	PITINTE (PINTE1)
Vector Base + $76	$3B	Periodic Interrupt Timer	I-Bit	PITINTE (PINTE2)
Vector Base + $74	$3A	Periodic Interrupt Timer	I-Bit	PITINTE (PINTE3)
Vector Base + $72	$39	XGATE Software Trigger 0	I-Bit	XGMCTL (XGIE)
Vector Base + $70	$38	XGATE Software Trigger 1	I-Bit	XGMCTL (XGIE)
Vector Base + $6E	$37	XGATE Software Trigger 2	I-Bit	XGMCTL (XGIE)
Vector Base + $6C	$36	XGATE Software Trigger 3	I-Bit	XGMCTL (XGIE)
Vector Base + $6A	$35	XGATE Software Trigger 4	I-Bit	XGMCTL (XGIE)
Vector Base + $68	$34	XGATE Software Trigger 5	I-Bit	XGMCTL (XGIE)
Vector Base + $66	$33	XGATE Software Trigger 6	I-Bit	XGMCTL (XGIE)
Vector Base + $64	$32	XGATE Software Trigger 7	I-Bit	XGMCTL (XGIE)
Vector Base + $62	-	XGATE Software Error Interrupt	I-Bit	XGMCTL (XGIE)
Vector Base + $60	-	XSRAM20K Access Violation	I-Bit	XSCTRL (XSAVIE)
Vector Base+ $12 to Vector Base + $5E	Reserved			
Vector Base + $10	-	Spurious Interrupt	-	None

NOTES:
1. 16 bits Vector Address based
2. For detailed description of XGATE Channel ID refer to XGATE Block Guide

5.3 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module Block Guides for register reset states.

5.3.1 I/O pins

Refer to the PIM Block Guide for reset configurations of all peripheral module ports.

> **NOTE:** *For devices assembled in 80-pin and 112-pin QFP packages all non-bonded out pins should be configured as outputs after reset in order to avoid current drawn from floating inputs. Refer to **Table 2-1** for affected pins.*

5.3.2 Memory

Refer to **Table 1-1** for locations of the memories depending on the operating mode after reset.

The RAM array is not automatically initialized out of reset.

Section 6 S12XCPU Block Description

Consult the S12XCPU Block Guide for information about the S12XCPU module.

Section 7 S12XMMC Block Description

Consult the S12XMMC Block Guide for information about the S12XMMC module.

Section 8 S12XEBI Block Description

Consult the S12XEBI Block Guide for information about the S12XEBI module.

Section 9 S12XINT Block Description

Consult the S12XINT Block Guide for information about the S12XINT module.

Section 10 S12XDBG Block Description

Consult the S12XDBG Block Guide for information about the S12XDBG module.

Section 11 S12XBDM Block Description

Consult the S12XBDM Block Guide for information about the S12XBDM module.

Section 12 XGATE Block Description

Consult the XGATE Block Guide for information about the co-processor.

Section 13 Periodic Interrupt Timer (PIT) Block Description

The Periodic Interrupt Timer Module contains four hardware trigger signal lines PITTRIG0, PITTRIG1, PITTRIG2 and PITTRIG3. One for each timer channel. **Table 17-1** and **Table 18-1** show the connection of these trigger outputs on MC9S12DP256 device. The trigger signal lines PITTRIG2 and PITTRIG3 are not used on MC9S12XDP512. Consult the PIT Block Guide for information about the Periodic Interrupt Timer module.When the PIT Block Guide refers to freeze mode this is equivalent to active BDM mode.

Section 14 Oscillator (OSC_LCP) Block

Consult the OSC_LCP Block Guide for information about the Oscillator Module.

Section 15 Clock and Reset Generator (CRG) Block Description

The COP timeout rate bits CR[2:0] in the COPCTL register are loaded on rising edge of $\overline{\text{RESET}}$ from the Flash Control Register FCTL ($0107) located in the Flash EEPROM block.See **Table 15-1**. On $\overline{\text{RESET}}$ into special modes the COP timeout rate bits are always set to the highest watchdog rate. (CR[2:0] = 111, 2^{24} oscillator cycles to time-out) **Table 15-1** shows also the write restrictions of the COP rate bits CR[2:0] in the COPCTL register. Writing to the MODE Register in the S12XEBI has no effect on the COP rate bits in the COPCTL register.

The FCTL register is loaded from the Flash Configuration Field byte at global address $7F_FF0E during the reset sequence. For more information on FCTL register refer to the FTX512K4 Block Guide.

Table 15-1 Initial COP Configuration

NV[2:0] in FCTL Register	CR[2:0] in COPCTL Register		Write of CR[2:0] (after reset initializiation from FCTL)	
	Normal & Emulation Modes	Special Modes	Normal & Emulatin Modes	Special Modes
000	111	111	never	always
001	110			
010	101			
011	100			
100	011			
101	010			
110	001			
111	000	000	once	

Consult the CRG Block Guide for information about the Clock and Reset Generator module.

Section 16 Enhanced Capture Timer (ECT) Block

Description

Consult the ECT_16B8C Block Guide for information about the Enhanced Capture Timer module When the ECT_16B8C Block Guide refers to freeze mode this is equivalent to active BDM mode.

Section 17 10 Bit 8 channel Analog to Digital Converter (ATD0) Block Description

The ATD_10B8C module includes four external trigger inputs ETRIG0, ETRIG1, ETRIG and ETRIG3. The external trigger allows the user to synchronize ATD conversion to external trigger events. **Table 17-1** shows the connection of the external trigger inputs on MC9S12XDP512.

Table 17-1 ATD0 External Trigger Sources

External Trigger Input	Connectivity
ETRIG0	Pulse Width Modulator Channel 1
ETRIG1	Pulse Width Modulator Channel 3
ETRIG2	Periodic Interrupt Timer Hardware Trigger 0
ETRIG3	Periodic Interrupt Timer Hardware Trigger 1

Consult the ATD_10B8C Block Guide for information about the Analog to Digital Converter module. When the ATD_10B8C Block Guide refers to freeze mode this is equivalent to active BDM mode.

Section 18 10 Bit 16 Channel Analog to Digital Converter (ATD1) Block Description

The ATD_10B16C module includes four external trigger inputs ETRIG0, ETRIG1, ETRIG and ETRIG3. The external trigger feature allows the user to synchronize ATD conversion to external trigger events. **Table 18-1** shows the connection of the external trigger inputs on MC9S12XDP512.

Table 18-1 ATD1 External Trigger Sources

External Trigger Input	Connectivity
ETRIG0	Pulse Width Modulator Channel 1
ETRIG1	Pulse Width Modulator Channel 3
ETRIG2	Periodic Interrupt Timer Hardware Trigger 0
ETRIG3	Periodic Interrupt Timer Hardware Trigger 1

Consult the ATD_10B16C Block Guide for information about the Analog to Digital Converter module. When the ATD_10B16C Block Guide refers to freeze mode this is equivalent to active BDM mode.

Section 19 Inter-IC Bus (IIC) Block Description

There are two Inter-IC Bus blocks implemented (IIC0, IIC1) on the MC9S12DP256 device. Consult the IIC Block Guide for information about each Inter-IC Bus module.

Section 20 Serial Communications Interface (SCI) Block Description

There are six Serial Communications Interfaces (SCI0, SCI1, SCI2, SCI3, SCI4 and SCI5) implemented on the MC9S12XDP512 device. Consult the SCI Block Guide for information about each Serial Communications Interface module.

Section 21 Serial Peripheral Interface (SPI) Block Description

There are three Serial Peripheral Interfaces(SPI0, SPI1 and SPI2) implemented on MC9S12XDP512. Consult the SPI Block Guide for information about each Serial Peripheral Interface module.

Section 22 Pulse Width Modulator (PWM) Block Description

Consult the PWM_8B8C Block Guide for information about the Pulse Width Modulator module. When the PWM _8B8CBlock Guide refers to freeze mode this is equivalent to active BDM mode.

Section 23 Flash EEPROM 512K Block Description

Consult the FTX512K4 Block Guide for information about the flash module.

> *The "S12 LRAE" is a generic Load RAM and Execute (LRAE) program which will be programmed into the flash memory of this device during manufacture. This LRAE program will provide greater programming flexibility to the end users by allowing the device to be programmed directly using CAN or SCI after it is assembled on the PCB. Use of the LRAE program is at the discretion of the end user and, if not required, it must simply be erased prior to flash programming. For more*

*details of the S12 LRAE and its implementation, please see the S12 LREA
Application Note (AN2546/D).*

Section 24 EEPROM 4K Block Description

Consult the EETX4K Block Guide for information about the EEPROM module.

Section 25 XSRAM20K Block description

Consult the XSRAM20K Block Guide for information about the XSRAM20K module.

Section 26 MSCAN Block Description

There are five MSCAN modules (CAN4, CAN3, CAN2, CAN1 and CAN0) implemented on the
MC9S12XDP512. Consult the MSCAN Block Guide for information about the Motorola Scalable CAN
Module.

Section 27 Port Integration Module (PIM) Block Description

Consult the PIM_9XD Family Block Guide for information about the Port Integration Module.

Section 28 Voltage Regulator (VREG_3V3) Block Description

Consult the VREG3V3 Block Guide for information about the dual output linear voltage regulator.

- VREGEN is accessible externally
- The API Trimming bits APITR[5:0] need to be set by the customer if accurate period is wanted.

28.1 Recommended PCB Layout

The PCB must be carefully laid out to ensure proper operation of the voltage regulator as well as of the
MCU itself. The following rules must be observed:

- Every supply pair must be decoupled by a ceramic capacitor connected as near as possible to the
corresponding pins (C1 - C6).
- Central point of the ground star for LQFP112/QFP80   should be the VSSR pin.
- Central point of the ground star for LQFP144   should be the VSSA pin.

- Use low ohmic low inductance connections between VSS1, VSS2 and VSSR.

- VSSPLL must be directly connected to VSSR.

- Keep traces of VSSPLL, EXTAL and XTAL as short as possible and occupied board area for C7, C8 and Q1 as small as possible.

- Do not place other signals or supplies underneath area occupied by C7, C8 and Q1 and the connection area to the MCU.

- Central power input should be fed in at the VDDA/VSSA pins.

Table 28-1 Recommended decoupling capacitor choice

Component	Purpose	Type	Value
C1	VDD1 filter cap	ceramic X7R	400nF
C2	VDD2 filter cap (not 80 QFP)	ceramic X7R	400nF
C3	VDDA filter cap	ceramic X7R	100nF
C4	VDDR filter cap	X7R/tantalum	>=100nF
C5	VDDPLL filter cap	ceramic X7R	200nF
C6	VDDX filter cap	X7R/tantalum	>=100nF
C7	OSC load cap		
C8	OSC load cap		
C9	PLL loop filter cap	See PLL specification chapter	
C10	PLL loop filter cap		
C11	VDDX filter cap	X7R/tantalum	>=100nF
C12	VDDX filter cap	X7R/tantalum	>=100nF
R1	PLL loop filter res	See PLL specification chapter	
Q1	Quartz		

Figure 28-1 LQFP144 recommended PCB layout
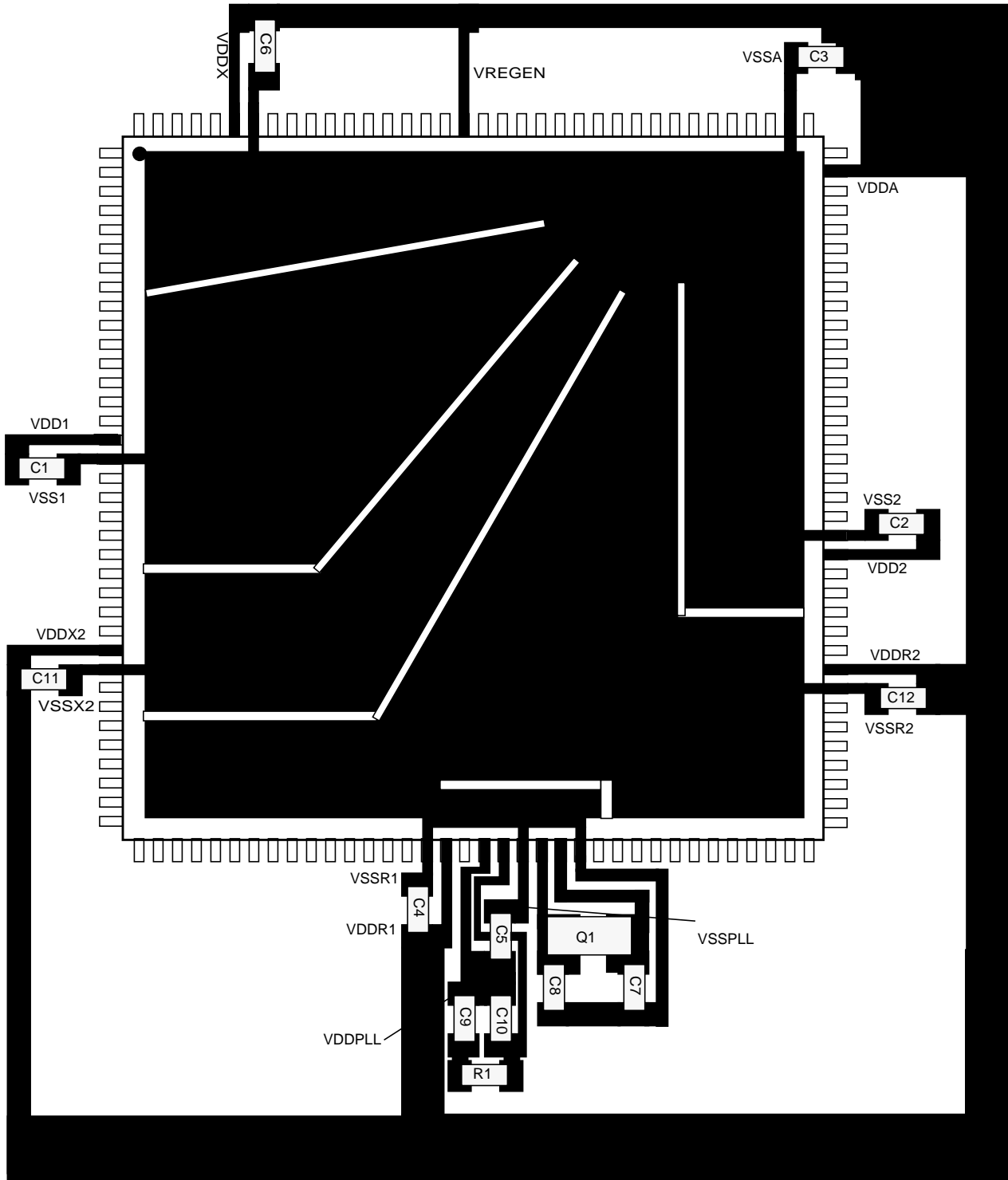
Figure 28-2 LQFP112 recommended PCB layout
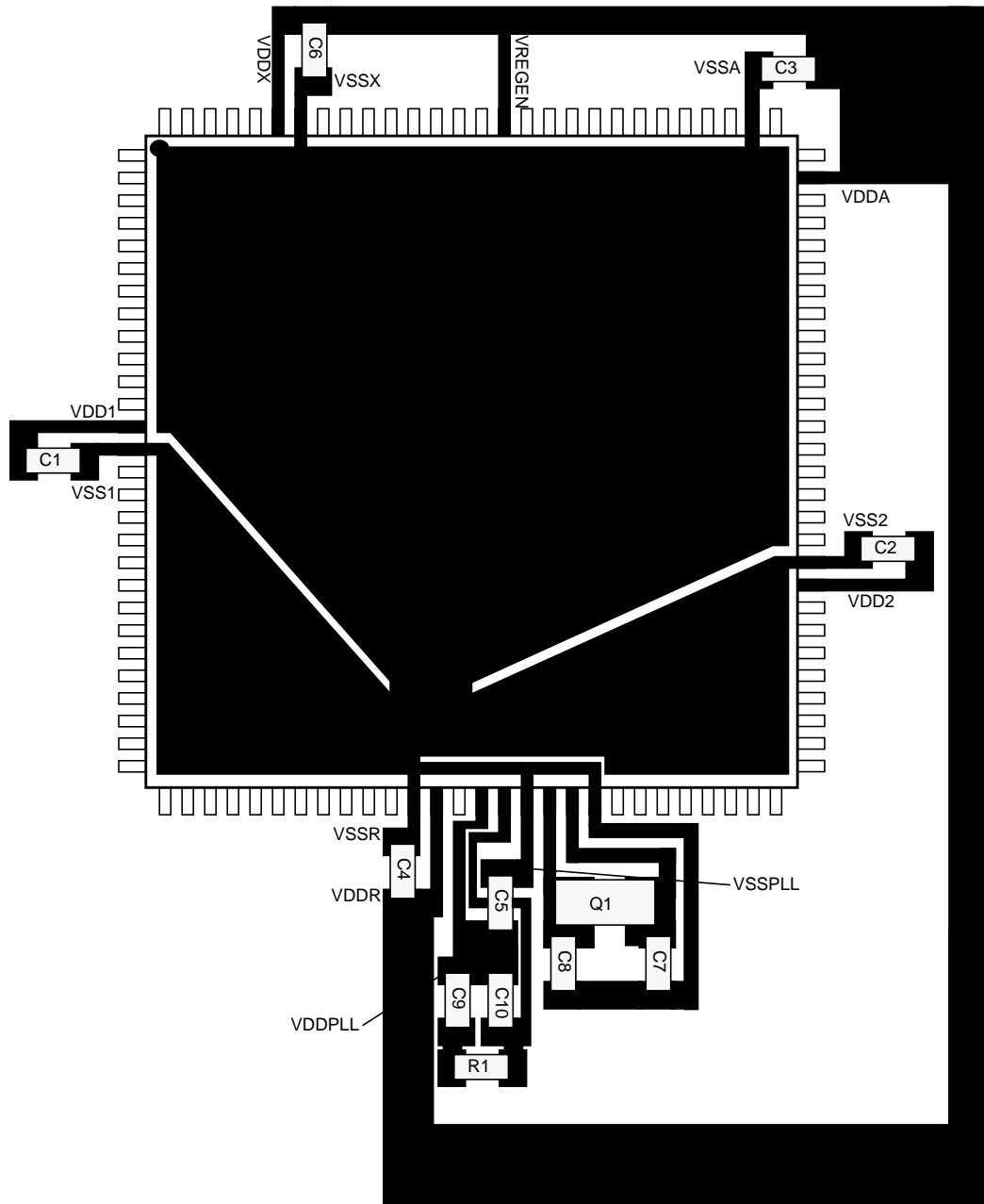
Figure 28-3 QFP80 recommended PCB layout
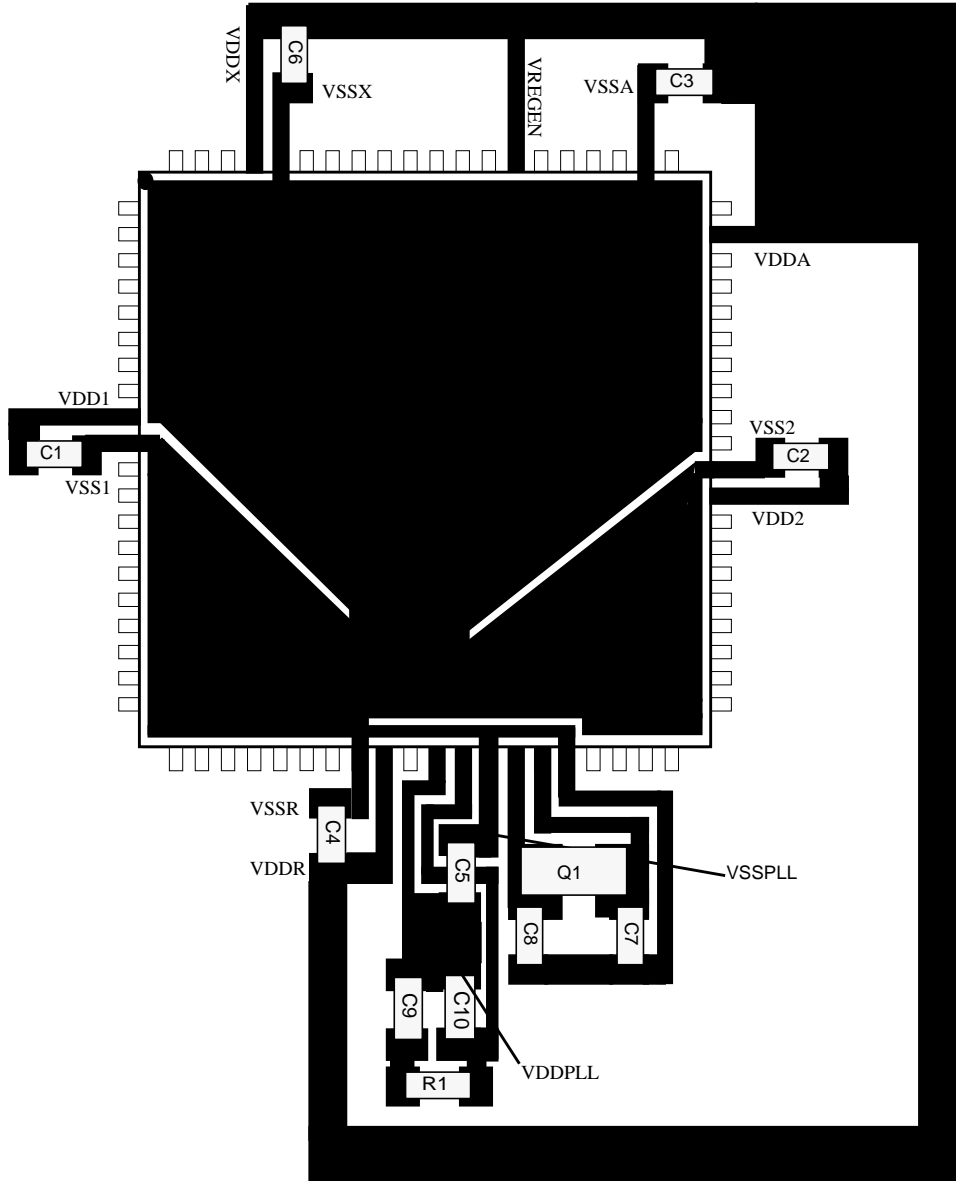
Appendix A Electrical Characteristics

A.1 General

> **NOTE:** *The electrical characteristics given in this section are preliminary and should be used as a guide only. Values cannot be guaranteed by Motorola and are subject to change without notice.*

This supplement contains the most accurate electrical information for the MC9S12XDP512 microcontroller available at the time of publication. The information should be considered **PRELIMINARY** and is subject to change.

This introduction is intended to give an overview on several common topics like power supply, current injection etc.

A.1.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

> **NOTE:** *This classification is shown in the column labeled "C" in the parameter tables where appropriate.*

P:

Those parameters are guaranteed during production testing on each individual device.

C:

Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.

T:

Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.

D:

Those parameters are derived mainly from simulations.

A.1.2 Power Supply

The MC9S12XDP512 utilizes several pins to supply power to the I/O ports, A/D converter, oscillator and PLL as well as the digital core.

The VDDA, VSSA pair supplies the A/D converter and the resistor ladder of the internal voltage regulator.

The VDDX, VSSX, VDDR and VSSR pairs supply the I/O pins, VDDR supplies also the internal voltage regulator.

VDD1, VSS1, VDD2 and VSS2 are the supply pins for the digital logic, VDDPLL, VSSPLL supply the oscillator and the PLL.

VSS1 and VSS2 are internally connected by metal.

VDDA, VDDX, VDDR as well as VSSA, VSSX, VSSR are connected by anti-parallel diodes for ESD protection.

> **NOTE:** *In the following context VDD5 is used for either VDDA, VDDR and VDDX; VSS5 is used for either VSSA, VSSR and VSSX unless otherwise noted.*
> *IDD5 denotes the sum of the currents flowing into the VDDA, VDDX and VDDR pins.*
> *VDD is used for VDD1, VDD2 and VDDPLL, VSS is used for VSS1, VSS2 and VSSPLL.*
> *IDD is used for the sum of the currents flowing into VDD1 and VDD2.*

A.1.3 Pins

There are four groups of functional pins.

A.1.3.1 5V I/O pins

Those I/O pins have a nominal level of 5V. This class of pins is comprised of all port I/O pins, the analog inputs, BKGD and the RESET pins.The internal structure of all those pins is identical, however some of the functionality may be disabled. E.g. for the analog inputs the output drivers, pull-up and pull-down resistors are disabled permanently.

A.1.3.2 Analog Reference

This group is made up by the VRH and VRL pins.

A.1.3.3 Oscillator

The pins XFC, EXTAL, XTAL dedicated to the oscillator have a nominal 2.5V level. They are supplied by VDDPLL.

A.1.3.4 TEST

This pin is used for production testing only.

A.1.3.5 VREGEN

This pin is used to enable the on chip voltage regulator.

A.1.4 Current Injection

Power supply must maintain regulation within operating V_{DD5} or V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD5}$) is greater than I_{DD5}, the injection current may flow out of VDD5 and could result in external power supply going out of regulation. Ensure external VDD5 load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power; e.g. if no system clock is present, or if clock rate is very low which would reduce overall power consumption.

A.1.5 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation under or outside those maxima is not guaranteed. Stress beyond those limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS5} or V_{DD5}).

Table A-1 Absolute Maximum Ratings[1]

Num	Rating	Symbol	Min	Max	Unit
1	I/O, Regulator and Analog Supply Voltage	V_{DD5}	-0.3	6.0	V
2	Digital Logic Supply Voltage [2]	V_{DD}	-0.3	3.0	V
3	PLL Supply Voltage [2]	V_{DDPLL}	-0.3	3.0	V
4	Voltage difference VDDX to VDDR and VDDA	Δ_{VDDX}	-0.3	0.3	V
5	Voltage difference VSSX to VSSR and VSSA	Δ_{VSSX}	-0.3	0.3	V
6	Digital I/O Input Voltage	V_{IN}	-0.3	6.0	V
7	Analog Reference	V_{RH}, V_{RL}	-0.3	6.0	V
8	XFC, EXTAL, XTAL inputs	V_{ILV}	-0.3	3.0	V
9	TEST input	V_{TEST}	-0.3	10.0	V
10	Instantaneous Maximum Current Single pin limit for all digital I/O pins [3]	I_D	-25	+25	mA
11	Instantaneous Maximum Current Single pin limit for XFC, EXTAL, XTAL[4]	I_{DL}	-25	+25	mA
12	Instantaneous Maximum Current Single pin limit for TEST [5]	I_{DT}	-0.25	0	mA
13	Storage Temperature Range	T_{stg}	– 65	155	°C

NOTES:
1. Beyond absolute maximum ratings device might be damaged.

2. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when the device is powered from an external source.
3. All digital I/O pins are internally clamped to V_{SSX} and V_{DDX}, V_{SSR} and V_{DDR} or V_{SSA} and V_{DDA}.
4. Those pins are internally clamped to V_{SSPLL} and V_{DDPLL}.
5. This pin is clamped low to V_{SSPLL}, but not clamped high. This pin must be tied low in applications.

A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 Stress test qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table A-2 ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ohm
	Storage Capacitance	C	100	pF
	Number of Pulse per pin positive negative	-	- 3 3	
Machine	Series Resistance	R1	0	Ohm
	Storage Capacitance	C	200	pF
	Number of Pulse per pin positive negative	-	- 3 3	
Latch-up	Minimum input voltage limit		-2.5	V
	Maximum input voltage limit		7.5	V

Table A-3 ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1	C	Human Body Model (HBM)	V_{HBM}	2000	-	V
2	C	Machine Model (MM)	V_{MM}	200	-	V
3	C	Charge Device Model (CDM)	V_{CDM}	500	-	V
4	C	Latch-up Current at $T_A = 125°C$ positive negative	I_{LAT}	+100 -100	-	mA
5	C	Latch-up Current at $T_A = 27°C$ positive negative	I_{LAT}	+200 -200	-	mA

A.1.7 Operating Conditions

This chapter describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

> **NOTE:**   *Please refer to the temperature rating of the device (C, V, M) with regards to the ambient temperature T_A and the junction temperature T_J. For power dissipation calculations refer to **Section A.1.8 Power Dissipation and Thermal Characteristics**.*

Table A-4 Operating Conditions

Rating	Symbol	Min	Typ	Max	Unit
I/O, Regulator and Analog Supply Voltage	V_{DD5}	3	5	5.5	V
Digital Logic Supply Voltage [1]	V_{DD}	2.35	2.5	2.75	V
PLL Supply Voltage [2]	V_{DDPLL}	2.35	2.5	2.75	V
Voltage Difference VDDX to VDDR and VDDA	Δ_{VDDX}	-0.1	0	0.1	V
Voltage Difference VSSX to VSSR and VSSA	Δ_{VSSX}	-0.1	0	0.1	V
Oscillator	f_{osc}	0.5	-	16	MHz
Bus Frequency	f_{bus}	0.5	-	40	MHz
MC9S12XDP512**C**					
Operating Junction Temperature Range	T_J	-40	-	100	°C
Operating Ambient Temperature Range [2]	T_A	-40	27	85	°C
MC9S12XDP512**V**					
Operating Junction Temperature Range	T_J	-40	-	120	°C
Operating Ambient Temperature Range [2]	T_A	-40	27	105	°C
MC9S12XDP512**M**					
Operating Junction Temperature Range	T_J	-40	-	140	°C
Operating Ambient Temperature Range [2]	T_A	-40	27	125	°C

NOTES:
1. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when this regulator is disabled and the device is powered from an external source.
2. Please refer to **Section A.1.8 Power Dissipation and Thermal Characteristics** for more details about the relation between ambient temperature T_A and device junction temperature T_J.

A.1.8 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \Theta_{JA})$$

T_J = Junction Temperature, $[°C]$

T_A = Ambient Temperature, $[°C]$

P_D = Total Chip Power Dissipation, $[W]$

Θ_{JA} = Package Thermal Resistance, $[°C/W]$

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation, $[W]$

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}{}^2$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX and VDDR.
For R_{DSON} is valid:

$$R_{DSON} = \frac{V_{OL}}{I_{OL}}; \text{for outputs driven low}$$

respectively

$$R_{DSON} = \frac{V_{DD5} - V_{OH}}{I_{OH}}; \text{for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

I_{DDR} is the current shown in **Table A-9** and not the overall current flowing into VDDR, which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}{}^2$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX and VDDR.

Table A-5 Thermal Package Characteristics[1]

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	Thermal Resistance LQFP144, single sided PCB	θ_{JA}	-	-	TBD	^{o}C/W
2	T	Thermal Resistance LQFP144, double sided PCB with 2 internal planes	θ_{JA}	-	-	TBD	^{o}C/W
3	T	Thermal Resistance LQFP112, single sided PCB	θ_{JA}	-	-	TBD	^{o}C/W
4	T	Thermal Resistance LQFP112, double sided PCB with 2 internal planes	θ_{JA}	-	-	TBD	^{o}C/W
5	T	Thermal Resistance LQFP112, single sided PCB[2]	θ_{JA}	-	-	TBD	^{o}C/W
6	T	Thermal Resistance LQFP112, double sided PCB with 2 internal planes[3]	θ_{JA}	-	-	TBD	^{o}C/W
7	T	Thermal Resistance QFP 80, single sided PCB	θ_{JA}	-	-	TBD	^{o}C/W
8	T	Thermal Resistance QFP 80, double sided PCB with 2 internal planes	θ_{JA}	-	-	TBD	^{o}C/W

NOTES:

1. The values for thermal resistance are achieved by package simulations
2. PC Board according to EIA/JEDEC Standard 51-2
3. PC Board according to EIA/JEDEC Standard 51-7

A.1.9 I/O Characteristics

This section describes the characteristics of all 5V I/O pins. All parameters are not always applicable, e.g. not all parameters are always applicable.

Table A-6 3.3V I/O Characteristics

Conditions are 3.0V < VDD5 <3.6V Temperature from -40C to +140C,unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Input High Voltage	V_{IH}	$0.65*V_{DD5}$	-	-	V
	T	Input High Voltage	V_{IH}	-	-	VDD5 + 0.3	V
2	P	Input Low Voltage	V_{IL}	-	-	$0.35*V_{DD5}$	V
	T	Input Low Voltage	V_{IL}	VSS5 - 0.3	-	-	V
3	C	Input Hysteresis	V_{HYS}		250		mV
4	P	Input Leakage Current (pins in high impedance input mode)[1] V_{in} = V_{DD5} or V_{SS5}	I_{in}	−2.5	-	2.5	μA
5	C	Output High Voltage (pins in output mode) Partial Drive I_{OH} = −2mA	V_{OH}	$V_{DD5} - 0.4$	-	-	V

Table A-6 3.3V I/O Characteristics

		Conditions are 3.0V < VDD5 <3.6V Temperature from -40C to +140C,unless otherwise noted					
6	P	Output High Voltage (pins in output mode) Full Drive IOH = −5.5mA	V_{OH}	$V_{DD5}-0.4$	-	-	V
7	C	Output Low Voltage (pins in output mode) Partial Drive IOL = +2mA	V_{OL}	-	-	0.4	V
8	P	Output Low Voltage (pins in output mode) Full Drive I_{OL} = +5.5mA	V_{OL}	-	-	0.4	V
9	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	-	-	TBD	µA
10	C	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	TBD	-	-	µA
11	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	-	-	TBD	µA
12	C	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	TBD	-	-	µA
13	D	Input Capacitance	C_{in}		6	-	pF
14	T	Injection current[2] Single Pin limit Total Device Limit. Sum of all injected currents	I_{ICS} I_{ICP}	-2.5 -25	-	2.5 25	mA
15	P	Port H, J, P Interrupt Input Pulse filtered[3]	t_{PULSE}			3	µs
16	P	Port H, J, P Interrupt Input Pulse passed[3]	t_{PULSE}	10			µs

NOTES:
1. Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8 C to 12 C in the temperature range from 50 C to 125 C.
2. Refer to **Section A.1.4 Current Injection**, for more details
3. Parameter only applies in STOP or Pseudo STOP mode.

Table A-7 5V I/O Characteristics

Conditions are 4.5V < VDD5 <5.5V Temperature from -40C to +140C,unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Input High Voltage	V_{IH}	$0.65*V_{DD5}$	-	-	V
	T	Input High Voltage	V_{IH}	-	-	VDD5 + 0.3	V
2	P	Input Low Voltage	V_{IL}	-	-	$0.35*V_{DD5}$	V
	T	Input Low Voltage	V_{IL}	VSS5 - 0.3	-	-	V
3	C	Input Hysteresis	V_{HYS}		250		mV
4	P	Input Leakage Current (pins in high impedance input mode)[1] $V_{in} = V_{DD5}$ or V_{SS5}	I_{in}	−2.5	-	2.5	µA
5	C	Output High Voltage (pins in output mode) Partial Drive $I_{OH} = -2mA$	V_{OH}	$V_{DD5} - 0.8$	-	-	V
6	P	Output High Voltage (pins in output mode) Full Drive IOH = −10mA	V_{OH}	$V_{DD5} - 0.8$	-	-	V
7	C	Output Low Voltage (pins in output mode) Partial Drive IOL = +2mA	V_{OL}	-	-	0.8	V
8	P	Output Low Voltage (pins in output mode) Full Drive $I_{OL} = +10mA$	V_{OL}	-	-	0.8	V
9	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	-	-	-130	µA
10	C	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	-10	-	-	µA
11	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	-	-	130	µA
12	C	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	10	-	-	µA
13	D	Input Capacitance	C_{in}		6	-	pF
14	T	Injection current[2] Single Pin limit Total Device Limit. Sum of all injected currents	I_{ICS} I_{ICP}	-2.5 -25	-	2.5 25	mA
15	P	Port H, J, P Interrupt Input Pulse filtered[3]	t_{PULSE}			3	µs
16	P	Port H, J, P Interrupt Input Pulse passed[3]	t_{PULSE}	10			µs

NOTES:
1. Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8 C to 12 C in the temperature range from 50 C to 125 C.
2. Refer to **Section A.1.4 Current Injection**, for more details
3. Parameter only applies in STOP or Pseudo STOP mode.

Table A-8 I/O Characteristics for Port C, D, PE5 and PE6 for reduced input voltage thresholds (ITHRS set in MODE register)

Num	C	Rating	Symbol	Min	Typ	Max	Unit
		Conditions are 4.5V < VDD5 <5.5V Temperature from -40C to +140C,unless otherwise noted					
1	P	Input High Voltage	V_{IH}	TBD	-	-	V
	T	Input High Voltage	V_{IH}	-	-	TBD	V
2	P	Input Low Voltage	V_{IL}	-	-	TBD	V
	T	Input Low Voltage	V_{IL}	TBD	-	-	V
3	C	Input Hysteresis	V_{HYS}		TBD		mV

A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

A.1.10.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted the currents are measured in single chip mode, internal voltage regulator enabled and at 40MHz bus frequency using a 4MHz oscillator in Colpitts mode. Production testing is performed using a square wave signal at the EXTAL input.

A.1.10.2 Additional Remarks

In expanded modes the currents flowing in the system are highly dependent on the load at the address, data and control signals as well as on the duty cycle of those signals. No generally applicable numbers can

given. A very good estimate is to take the single chip currents and add the currents due to the external loads.

Table A-9 Supply Current Characteristics

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Run supply currents Single Chip, Internal regulator enabled	I_{DD5}			TBD	mA
2	P P	Wait Supply current All modules enabled, PLL on only RTI enabled [1]	I_{DDW}			TBD TBD	mA
3	C P C C P C P C P	Pseudo Stop Current (API, RTI and COP disabled) [1, 2] -40°C 27°C 70°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C	I_{DDPS}		TBD TBD TBD TBD TBD TBD TBD TBD TBD	TBD TBD TBD TBD	μA
4	C C C C C C C	Pseudo Stop Current (API, RTI and COP enabled) [1, 2] -40°C 27°C 70°C 85°C 105°C 125°C 140°C	I_{DDPS}		TBD TBD TBD TBD TBD TBD TBD		μA
5	C P C C P C P C P	Stop Current [2] -40°C 27°C 70°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C	I_{DDS}		TBD TBD TBD TBD TBD TBD TBD TBD TBD	TBD TBD TBD TBD	μA

NOTES:
1. PLL off
2. At those low power dissipation levels $T_J = T_A$ can be assumed

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A.2 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

A.2.1 ATD Operating Characteristics

The **Table A-10** and **Table A-11** show conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:
$V_{SSA} \leq V_{RL} \leq V_{IN} \leq V_{RH} \leq V_{DDA}$. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table A-10 ATD Operating Characteristics 5V

Conditions are shown in **Table A-4** unless otherwise noted, Supply Voltage 4.5V < VDDA < 5.5V							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	D	Reference Potential <div align=right>Low</div><div align=right>High</div>	V_{RL} V_{RH}	V_{SSA} $V_{DDA}/2$		$V_{DDA}/2$ V_{DDA}	V V
2	C	Differential Reference Voltage[1]	V_{RH}-V_{RL}	4.50	5.00	5.5	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5		TBD	MHz
4	D	ATD 10-Bit Conversion Period <div align=right>Clock Cycles[2]</div><div align=right>Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}</div>	N_{CONV10} T_{CONV10}	14 TBD		28 14	Cycles μs
5	D	ATD 8-Bit Conversion Period <div align=right>Clock Cycles[2]</div><div align=right>Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}</div>	N_{CONV8} T_{CONV8}	12 TBD		26 13	Cycles μs
6	D	Recovery Time (V_{DDA}=5.0 Volts)	t_{REC}			20	μs
7	P	Reference Supply current 2 ATD blocks on	I_{REF}			0.750	mA
8	P	Reference Supply current 1 ATD block on	I_{REF}			0.375	mA

NOTES:

1. Full accuracy is not guaranteed when differential voltage is less than 4.50V
2. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

Table A-11 ATD Operating Characteristics 3.3V

Num	C	Rating		Symbol	Min	Typ	Max	Unit
1	D	Reference Potential	Low High	V_{RL} V_{RH}	V_{SSA} $V_{DDA}/2$		$V_{DDA}/2$ V_{DDA}	V V
2	C	Differential Reference Voltage[1]		V_{RH}-V_{RL}	3.0	3.3	3.6	V
3	D	ATD Clock Frequency		f_{ATDCLK}	0.5		TBD	MHz
4	D	ATD 10-Bit Conversion Period	Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	N_{CONV10} T_{CONV10}	14 TBD		28 14	Cycles µs
5	D	ATD 8-Bit Conversion Period	Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	N_{CONV8} T_{CONV8}	12 TBD		26 13	Cycles µs
6	D	Recovery Time (V_{DDA}=5.0 Volts)		t_{REC}			20	µs
7	P	Reference Supply current 2 ATD blocks on		I_{REF}			0.500	mA
8	P	Reference Supply current 1 ATD block on		I_{REF}			0.250	mA

NOTES:
1. Full accuracy is not guaranteed when differential voltage is less than 4.50V
2. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

A.2.2 Factors influencing accuracy

Three factors - source resistance, source capacitance and current injection - have an influence on the accuracy of the ATD.

A.2.2.1 Source Resistance:

Due to the input pin leakage current as specified in **Table A-7** in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance R_S specifies results in an error of less than 1/2 LSB (2.5mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance is allowed.

A.2.2.2 Source Capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage $\leq$ 1LSB, then the external filter capacitor, $C_f \geq 1024 * (C_{INS} - C_{INN})$.

A.2.2.3 Current Injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of $3FF ($FF in 8-bit mode) for analog inputs greater than V_{RH} and $000 for values less than V_{RL} unless the current is higher than specified as disruptive condition.

2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.

   The additional input voltage error on the converted channel can be calculated as $V_{ERR} = K * R_S * I_{INJ}$, with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

Table A-12 ATD Electrical Characteristics

Num	C	Rating	Symbol	Min	Typ	Max	Unit
Conditions are shown in **Table A-4** unless otherwise noted
1	C	Max input Source Resistance	R_S	-	-	1	KΩ
2	T	Total Input Capacitance Non Sampling Sampling	C_{INN} C_{INS}			10 22	pF
3	C	Disruptive Analog Input Current	I_{NA}	-2.5		2.5	mA
4	C	Coupling Ratio positive current injection	K_p			TBD	A/A
5	C	Coupling Ratio negative current injection	K_n			TBD	A/A

A.2.3 ATD accuracy

A.2.3.1 5V Range

Table A-13 specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table A-13 ATD Conversion Performance 5V

Num	C	Rating	Symbol	Min	Typ	Max	Unit
Conditions are shown in **Table A-4** unless otherwise noted
$V_{REF} = V_{RH} - V_{RL} = 5.12V$. Resulting to one 8 bit count = 20mV and one 10 bit count = 5mV
$f_{ATDCLK} = 2.0MHz$
1	P	10-Bit Resolution	LSB		5		mV
2	P	10-Bit Differential Nonlinearity	DNL	−1		1	Counts
3	P	10-Bit Integral Nonlinearity	INL	−2.5	±1.5	2.5	Counts
4	P	10-Bit Absolute Error[1]	AE	-3	±2.0	3	Counts
5	P	8-Bit Resolution	LSB		20		mV
6	P	8-Bit Differential Nonlinearity	DNL	−0.5		0.5	Counts
7	P	8-Bit Integral Nonlinearity	INL	−1.0	±0.5	1.0	Counts
8	P	8-Bit Absolute Error[1]	AE	-1.5	±1.0	1.5	Counts

NOTES:
1. These values include the quantization error which is inherently 1/2 count for any A/D converter.

A.2.3.2 3.3V Range

Table A-14 specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table A-14   ATD Conversion Performance 3.3V

Conditions are shown in **Table A-4** unless otherwise noted V_{REF} = V_{RH} - V_{RL} = 3.328V. Resulting to one 8 bit count = 13mV and one 10 bit count = 3.25mV f_{ATDCLK} = 2.0MHz							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	10-Bit Resolution	LSB		3.25		mV
2	P	10-Bit Differential Nonlinearity	DNL	−1.5		1.5	Counts
3	P	10-Bit Integral Nonlinearity	INL	−3.5	±1.5	3.5	Counts
4	P	10-Bit Absolute Error[1]	AE	-5	±2.5	5	Counts
5	P	8-Bit Resolution	LSB		13		mV
6	P	8-Bit Differential Nonlinearity	DNL	−0.5		0.5	Counts
7	P	8-Bit Integral Nonlinearity	INL	−1.5	±1.0	1.5	Counts
8	P	8-Bit Absolute Error[1]	AE	-2.0	±1.5	2.0	Counts

NOTES:
1. These values include the quantization error which is inherently 1/2 count for any A/D converter.

A.2.3.3 ATD Accuracy Definitions

For the following definitions see also **Figure A-1**.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) \ = \ \frac{V_i - V_{i-1}}{1LSB} - 1$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$INL(n) \ = \ \sum_{i=1}^{n} DNL(i) \ = \ \frac{V_n - V_0}{1LSB} - n$$
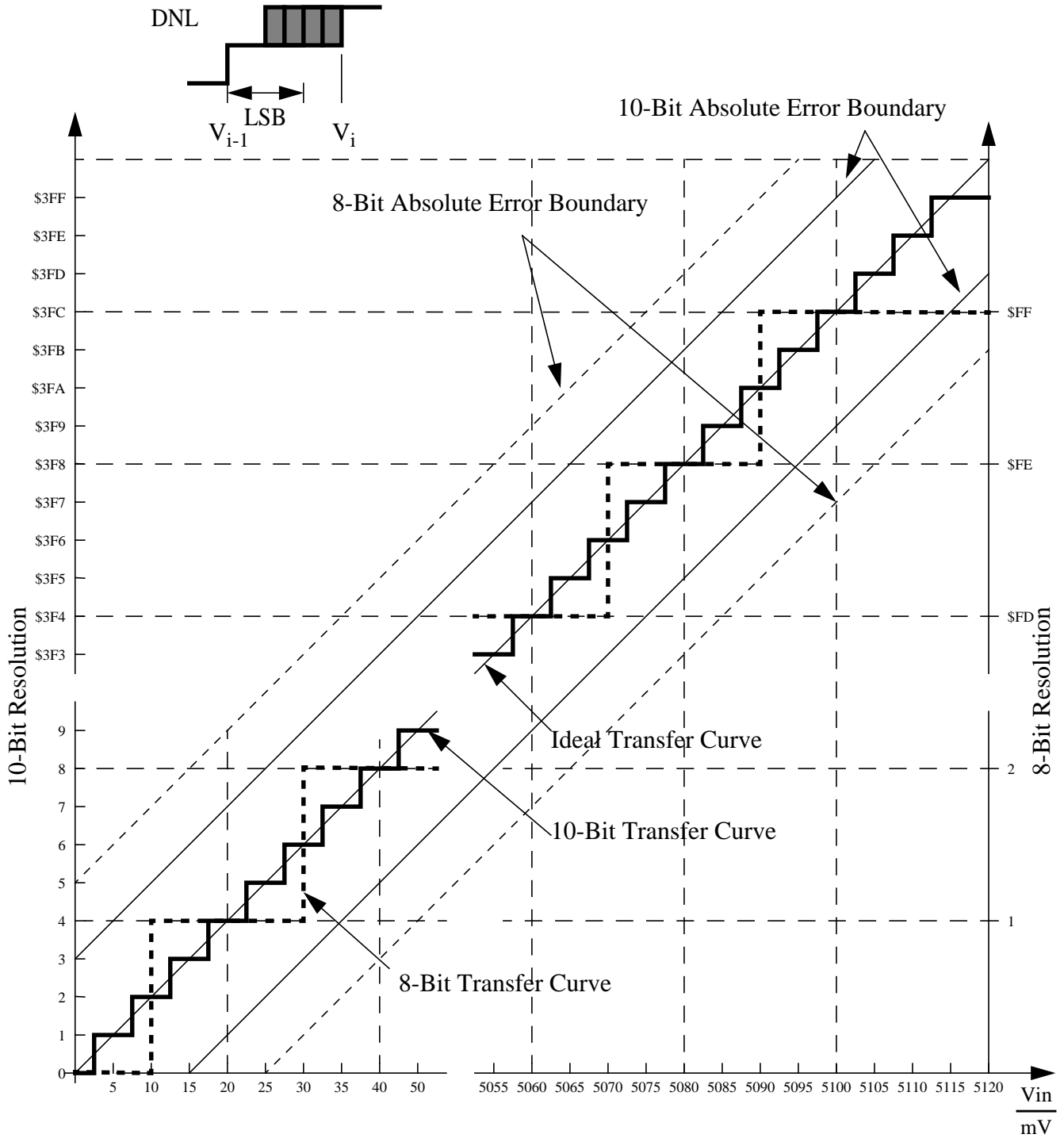
Figure A-1 ATD Accuracy Definitions

NOTE: **Figure A-1** *shows only definitions, for specification values refer to* **Table A-13**.

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A.3 NVM, Flash and EEPROM

NOTE: *Unless otherwise noted the abbreviation NVM (Non Volatile Memory) is used for both Flash and EEPROM.*

A.3.1 NVM timing

The time base for all NVM program or erase operations is derived from the oscillator. A minimum oscillator frequency f_{NVMOSC} is required for performing program or erase operations. The NVM modules do not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. Attempting to program or erase the NVM modules at a lower frequency a full program or erase transition is not assured.

The Flash and EEPROM program and erase operations are timed using a clock derived from the oscillator using the FCLKDIV and ECLKDIV registers respectively. The frequency of this clock must be set within the limits specified as f_{NVMOP}.

The minimum program and erase times shown in **Table A-15** are calculated for maximum f_{NVMOP} and maximum f_{bus}. The maximum times are calculated for minimum f_{NVMOP} and a f_{bus} of 2MHz.

A.3.1.1 Single Word Programming

The programming time for single word programming is dependant on the bus frequency as a well as on the frequency f_{NVMOP} and can be calculated according to the following formula.

$$t_{swpgm} = 9 \cdot \frac{1}{f_{NVMOP}} + 25 \cdot \frac{1}{f_{bus}}$$

A.3.1.2 Burst Programming

This applies only to the Flash where up to 64 words in a row can be programmed consecutively using burst programming by keeping the command pipeline filled. The time to program a consecutive word can be calculated as:

$$t_{bwpgm} = 4 \cdot \frac{1}{f_{NVMOP}} + 9 \cdot \frac{1}{f_{bus}}$$

The time to program a whole row is:

$$t_{brpgm} = t_{swpgm} + 63 \cdot t_{bwpgm}$$

Burst programming is more than 2 times faster than single word programming.

A.3.1.3 Sector Erase

Erasing a 1024 byte Flash sector or a 4 byte EEPROM sector takes:

$$t_{era} \approx 4000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.3.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{mass} \approx 20000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.3.1.5 Blank Check

The time it takes to perform a blank check on the Flash or EEPROM is dependant on the location of the first non-blank word starting at relative address zero. It takes one bus cycle per word to verify plus a setup of the command.

$$t_{check} \approx location \cdot t_{cyc} + 10 \cdot t_{cyc}$$

Table A-15   NVM Timing Characteristics

Num	C	Rating	Symbol	Min	Typ	Max	Unit
conditions		Conditions are shown in **Table A-4** unless otherwise noted					
1	D	External Oscillator Clock (MC9S12XDP512C< V, M)	f_{NVMOSC}	0.5		80 [1]	MHz
2	D	Bus frequency for Programming or Erase Operations	f_{NVMBUS}	1			MHz
3	D	Operating Frequency	f_{NVMOP}	150		200	kHz
4	P	Single Word Programming Time	t_{swpgm}	46 [2]		74.5 [3]	µs
5	D	Flash Burst Programming consecutive word [4]	t_{bwpgm}	20.4 [2]		31 [3]	µs
6	D	Flash Burst Programming Time for 32 Words [4]	t_{brpgm}	1331.2 [2]		2027.5 [3]	µs
7	P	Sector Erase Time	t_{era}	20 [5]		26.7 [3]	ms
8	P	Mass Erase Time	t_{mass}	100 [5]		133 [3]	ms
9	D	Blank Check Time Flash per block	t_{check}	11 [6]		65546 [7]	t_{cyc}
10	D	Blank Check Time EEPROM per block	t_{check}	11 [6]		2058[7]	t_{cyc}

NOTES:

1. Restrictions for oscillator in crystal mode apply!
2. Minimum Programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus}.

3. Maximum Erase and Programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f_{bus}. Refer to formulae in Sections **A.3.1.1 - A.3.1.4** for guidance.
4. Burst Programming operations are not applicable to EEPROM
5. Minimum Erase times are achieved under maximum NVM operating frequency f_{NVMOP}.
6. Minimum time, if first word in the array is not blank
7. Maximum time to complete check on an erased block

A.3.2 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures.

The failure rates for data retention and program/erase cycling are specified at the operating conditions noted.

The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

> **NOTE:** *All values shown in **Table A-16** are target values and subject to further extensive characterization.*

Table A-16   NVM Reliability Characteristics

Num	C	Rating	Symbol	Min	Typ	Max	Unit
Conditions are shown in **Table A-4** unless otherwise noted							
1	C	Data Retention at an average junction temperature of $T_{Javg} = 70°C$	t_{NVMRET}	15			Years
2	C	Flash number of Program/Erase cycles	n_{FLPE}	1000	10,000		Cycles
3	C	EEPROM number of Program/Erase cycles ($-40°C \leq T_J \leq 0°C$)	n_{EEPE}	10,000			Cycles
4	C	EEPROM number of Program/Erase cycles ($0°C < T_J \leq 140°C$)	n_{EEPE}	100,000			Cycles

A.4 Voltage Regulator

Table 28-2 Voltage Regulator Electrical Characteristics

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	P	Input Voltages	$V_{VDDR,A}$	3.15	—	5.5	V
2	P	Regulator Current Reduced Power Mode Shutdown Mode	I_{REG}	— —	20 12	50 40	μA μA
3	P	Output Voltage Core Full Performance Mode Reduced Power Mode Shutdown Mode	V_{DD}	2.35 1.6 —	2.5 2.5 —[1]	2.75 2.75 —	V V V
4	P	Output Voltage PLL Full Performance Mode Reduced Power Mode[2] Reduced Power Mode[3] Shutdown Mode	V_{DDPLL}	2.35 2.0 1.6 —	2.5 2.5 2.5 —[4]	2.75 2.75 2.75 —	V V V
7	P	Low Voltage Interrupt[5] Assert Level Deassert Level	V_{LVIA} V_{LVID}	4.1 4.25	4.37 4.52	4.66 4.77	V V
8	P	Low Voltage Reset[6] Assert Level	V_{LVRA}	2.25	—	—	V
9	C	Power-on Reset[7] Assert Level Deassert Level	V_{PORA} V_{PORD}	0.97 —	— —	— 2.05	V V
12	C	Trimmed API internal clock $\Delta f / f_{nominal}$	df_{API}	- 10%	—	+ 10%	—

NOTES:

1. High Impedance Output
2. Current IDDPLL = 1mA (Colpitts Oscillator)
3. Current IDDPLL = 3mA (Pierce Oscillator)
4. High Impedance Output
5. Monitors V_{DDA}, active only in Full Performance Mode. Indicates I/O & ADC performance degradation due to low supply voltage.
6. Monitors V_{DD}, active only in Full Performance Mode. MCU is monitored by the POR in RPM (see **Figure A-1**)
7. Monitors V_{DD}. Active in all modes.

NOTE: *The electrical characteristics given in this section are preliminary and should be used as a guide only. Values in this section cannot be guaranteed by Motorola and are subject to change without notice.*

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A.5 Reset, Oscillator and PLL

This section summarizes the electrical characteristics of the various startup scenarios for Oscillator and Phase-Locked-Loop (PLL).

A.5.1 Startup

Table A-17 summarizes several startup characteristics explained in this section. Detailed description of the startup behavior can be found in the Clock and Reset Generator (CRG) Block Guide.

Table A-17 Startup Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	D	Reset input pulse width, minimum input time	PW_{RSTL}	2			t_{osc}
2	D	Startup from Reset	n_{RST}	192		196	n_{osc}
3	D	Interrupt pulse width, $\overline{IRQ}$ edge-sensitive mode	PW_{IRQ}	20			ns
4	D	Wait recovery startup time	t_{WRS}			14	t_{cyc}

A.5.1.1 POR

The release level V_{PORR} and the assert level V_{PORA} are derived from the V_{DD} Supply. They are also valid if the device is powered externally. After releasing the POR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc}.

A.5.1.2 SRAM Data Retention

Provided an appropriate external reset signal is applied to the MCU, preventing the CPU from executing code when VDD5 is out of specification limits, the SRAM contents integrity is guaranteed if after the reset the PORF bit in the CRG Flags Register has not been set.

A.5.1.3 External Reset

When external reset is asserted for a time greater than PW_{RSTL} the CRG module generates an internal reset, and the CPU starts fetching the reset vector without doing a clock quality check, if there was an oscillation before reset.

A.5.1.4 Stop Recovery

Out of STOP the controller can be woken up by an external interrupt. A clock quality check as after POR is performed before releasing the clocks to the system.

A.5.1.5 Pseudo Stop and Wait Recovery

The recovery from Pseudo STOP and Wait are essentially the same since the oscillator was not stopped in both modes. The controller can be woken up by internal or external interrupts. After t_{wrs} the CPU starts fetching the interrupt vector.

A.5.2 Oscillator

The device features an internal low-power loop controlled Pierce oscillator and a full swing Pierce oscillator/external clock mode. The selection of loop controlled Pierce oscillator or full swing Pierce oscillator/external clock depends on the $\overline{XCLKS}$ signal which is sampled during reset. Before asserting the oscillator to the internal system clocks the quality of the oscillation is checked for each start from either power-on, STOP or oscillator fail. t_{CQOUT} specifies the maximum time before switching to the internal self clock mode after POR or STOP if a proper oscillation is not detected. The quality check also determines the minimum oscillator start-up time t_{UPOSC}. The device also features a clock monitor. A Clock Monitor Failure is asserted if the frequency of the incoming clock signal is below the Assert Frequency f_{CMFA}.

Table A-18 Oscillator Characteristics

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1a	C	Crystal oscillator range (loop controlled Pierce)	f_{OSC}	4.0		16	MHz
1b	C	Crystal oscillator range (full swing Pierce) [1,2]	f_{OSC}	0.5		40	MHz
2	P	Startup Current	i_{OSC}	100			μA
3	C	Oscillator start-up time (loop controlled Pierce)	t_{UPOSC}		TBD[3]	50[4]	ms
4	D	Clock Quality check time-out	t_{CQOUT}	0.45		2.5	s
5	P	Clock Monitor Failure Assert Frequency	f_{CMFA}	50	100	200	KHz
6	P	External square wave input frequency	f_{EXT}	0.5		TBD	MHz
7	D	External square wave pulse width low	t_{EXTL}	TBD			ns
8	D	External square wave pulse width high	t_{EXTH}	TBD			ns
9	D	External square wave rise time	t_{EXTR}			TBD	ns
10	D	External square wave fall time	t_{EXTF}			TBD	ns
11	D	Input Capacitance (EXTAL, XTAL inputs)	C_{IN}		TBD		pF

NOTES:
1. Depending on the crystal a damping series resistor might be necessary
2. $\overline{XCLKS}$ =0 during reset
3. f_{osc} = 4MHz, C = 22pF.
4. Maximum value is for extreme cases using high Q, low frequency crystals

A.5.3 Phase Locked Loop

The oscillator provides the reference clock for the PLL. The PLL´s Voltage Controlled Oscillator (VCO) is also the system clock source in self clock mode.

A.5.3.1 XFC Component Selection

This section describes the selection of the XFC components to achieve a good filter characteristics.
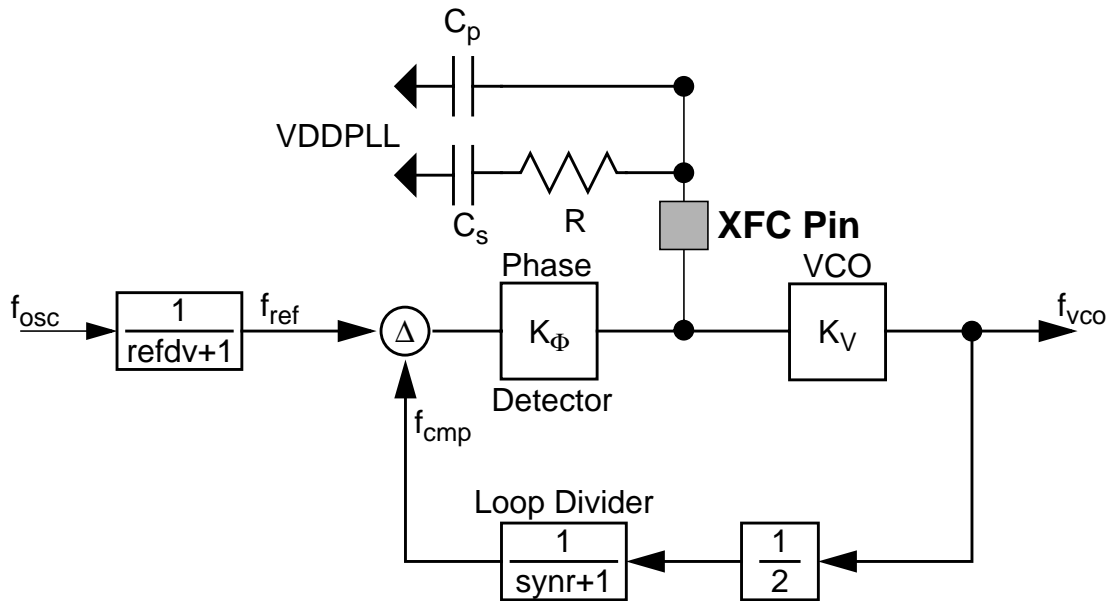
Figure A-2 Basic PLL functional diagram

The following procedure can be used to calculate the resistance and capacitance values using typical values for K_1, f_1 and i_{ch} from **Table A-19**.

The grey boxes show the calculation for $f_{VCO} = 80MHz$ and $f_{ref} = 4MHz$. E.g., these frequencies are used for $f_{OSC} = 4MHz$ and a 40MHz bus clock.

The VCO gain at the desired VCO frequency is approximated by:

$$K_V = K_1 \cdot e^{\frac{(f_1 - f_{vco})}{K_1 \cdot 1V}} = -195MHz/V \cdot e^{\frac{126 - 80}{-195}} = \text{-154.0MHz/V}$$

The phase detector relationship is given by:

$$K_\Phi = -\left|i_{ch}\right| \cdot K_V = -3.5\mu A \cdot (-154MHz/V) = 539.1Hz/\Omega$$

i_{ch} is the current in tracking mode.

The loop bandwidth f_C should be chosen to fulfill the Gardner's stability criteria by <u>at least</u> a factor of 10, typical values are 50. $\zeta = 0.9$ ensures a good transient response.

$$f_C < \frac{2 \cdot \zeta \cdot f_{ref}}{\pi \cdot \left(\zeta + \sqrt{1 + \zeta^2}\right)} \, \frac{1}{10} \rightarrow f_C < \frac{f_{ref}}{4 \cdot 10}; (\zeta = 0.9)$$

$$f_C < 100 \text{kHz}$$

And finally the frequency relationship is defined as

$$n = \frac{f_{VCO}}{f_{ref}} = 2 \cdot (synr + 1) \quad = 20$$

With the above values the resistance can be calculated. The example is shown for a loop bandwidth f_C=43kHz:

$$R = \frac{2 \cdot \pi \cdot n \cdot f_C}{K_\Phi} = \frac{2 \cdot \pi \cdot 20 \cdot 43 \text{kHz}}{(539.1 \text{Hz})/\Omega} = 10.0 \text{k}\Omega$$

The capacitance C_s can now be calculated as:

$$C_s = \frac{2 \cdot \zeta^2}{\pi \cdot f_C \cdot R} = \frac{0.516}{f_C \cdot R}; (\zeta = 0.9) \quad = 1.2 \text{nF} = \sim 1.0 \text{nF}$$

The capacitance C_p should be chosen in the range of:

$$\frac{C_s}{20} \le C_p \le \frac{C_s}{10} \quad C_P = 100 \text{pF}$$

A.5.3.2 Jitter Information

The basic functionality of the PLL is shown in **Figure A-2**. With each transition of the clock f_{cmp}, the deviation from the reference clock f_{ref} is measured and input voltage to the VCO is adjusted accordingly.The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in **Figure A-3**.
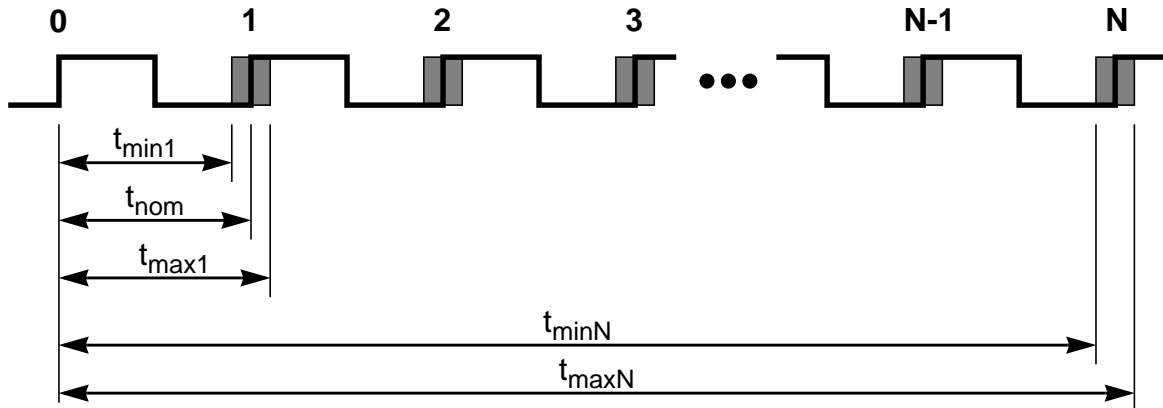
Figure A-3 Jitter Definitions

The relative deviation of t_{nom} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

For N < 100, the following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N}} + j_2$$
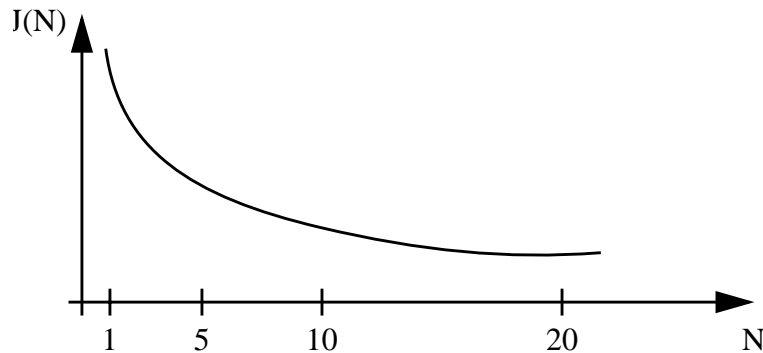
Figure A-4 Maximum bus clock jitter approximation

This is very important to notice with respect to timers, serial modules where a pre-scaler will eliminate the effect of the jitter to a large extent.

Table A-19 PLL Characteristics

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Self Clock Mode frequency	f_{SCM}	1		5.5	MHz
2	D	VCO locking range	f_{VCO}	8		80	MHz
3	D	Lock Detector transition from Acquisition to Tracking mode	$\lvert\Delta_{trk}\rvert$	3		4	%[1]
4	D	Lock Detection	$\lvert\Delta_{Lock}\rvert$	0		1.5	%[1]
5	D	Un-Lock Detection	$\lvert\Delta_{unl}\rvert$	0.5		2.5	%[1]
6	D	Lock Detector transition from Tracking to Acquisition mode	$\lvert\Delta_{unt}\rvert$	6		8	%[1]
7	C	PLLON Total Stabilization delay (Auto Mode) [2]	t_{stab}		TBD		ms
8	D	PLLON Acquisition mode stabilization delay [2]	t_{acq}		TBD		ms
9	D	PLLON Tracking mode stabilization delay [2]	t_{al}		TBD		ms
10	D	Fitting parameter VCO loop gain	K_1		-195		MHz/V
11	D	Fitting parameter VCO loop frequency	f_1		126		MHz
12	D	Charge pump current acquisition mode	$\lvert i_{ch}\rvert$		38.5		μA
13	D	Charge pump current tracking mode	$\lvert i_{ch}\rvert$		3.5		μA
14	C	Jitter fit parameter 1[2]	j_1			TBD	%
15	C	Jitter fit parameter 2[2]	j_2			TBD	%

Conditions are shown in **Table A-4** unless otherwise noted

NOTES:

1. % deviation from target frequency
2. f_{osc} = 4MHz, f_{BUS} = 40MHz equivalent f_{VCO} = 80MHz: REFDV = #$00, SYNR = #$09, Cs = 1.0nF, Cp = 100pF, Rs = 10kΩ

A.6 MSCAN

Table A-20 MSCAN Wake-up Pulse Characteristics

Num	C	Rating	Symbol	Min	Typ	Max	Unit
		Conditions are shown in **Table A-4** unless otherwise noted					
1	P	MSCAN Wake-up dominant pulse filtered	t_{WUP}			2	µs
2	P	MSCAN Wake-up dominant pulse pass	t_{WUP}	5			µs

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A.7 SPI

This section provides electrical parametrics and ratings for the SPI.

In **Table A-21** the measurement conditions are listed.

Table A-21 Measurement Conditions

Description	Value	Unit
Drive mode	full drive mode	—
Load capacitance C_{LOAD}, on all outputs	50	pF
Thresholds for delay measurement points	(20% / 80%) VDDX	V

A.7.1 Master Mode

In **Figure A-5** the timing diagram for master mode with transmission format CPHA=0 is depicted.
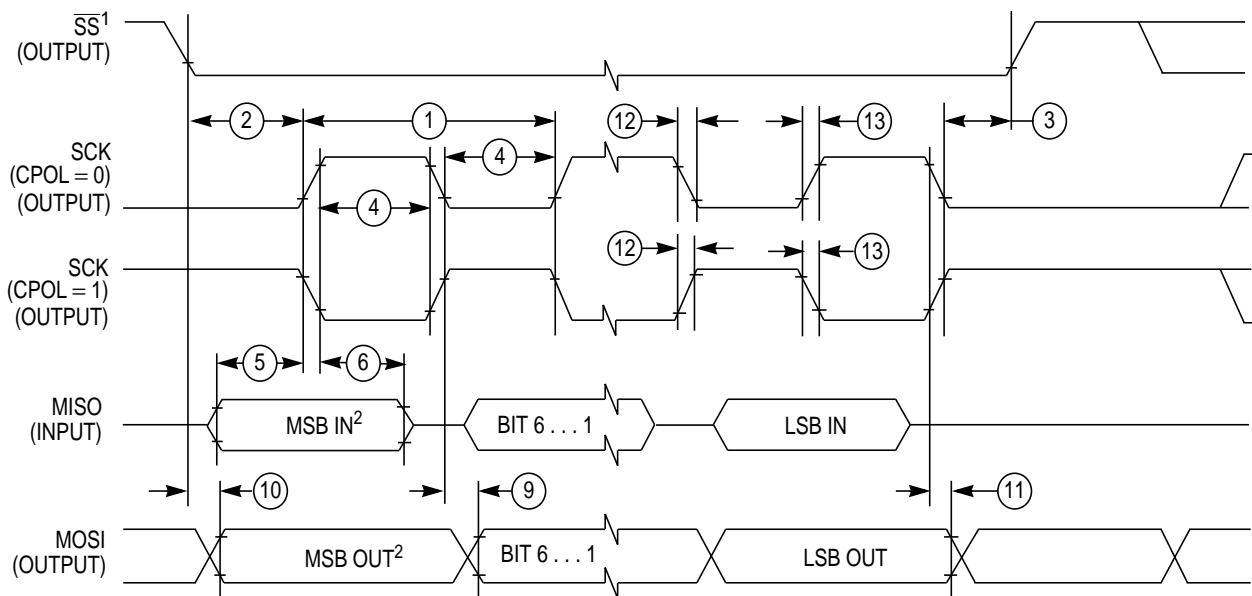
1.if configured as an output.

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-5 SPI Master Timing (CPHA=0)

In **Figure A-6** the timing diagram for master mode with transmission format CPHA=1 is depicted.
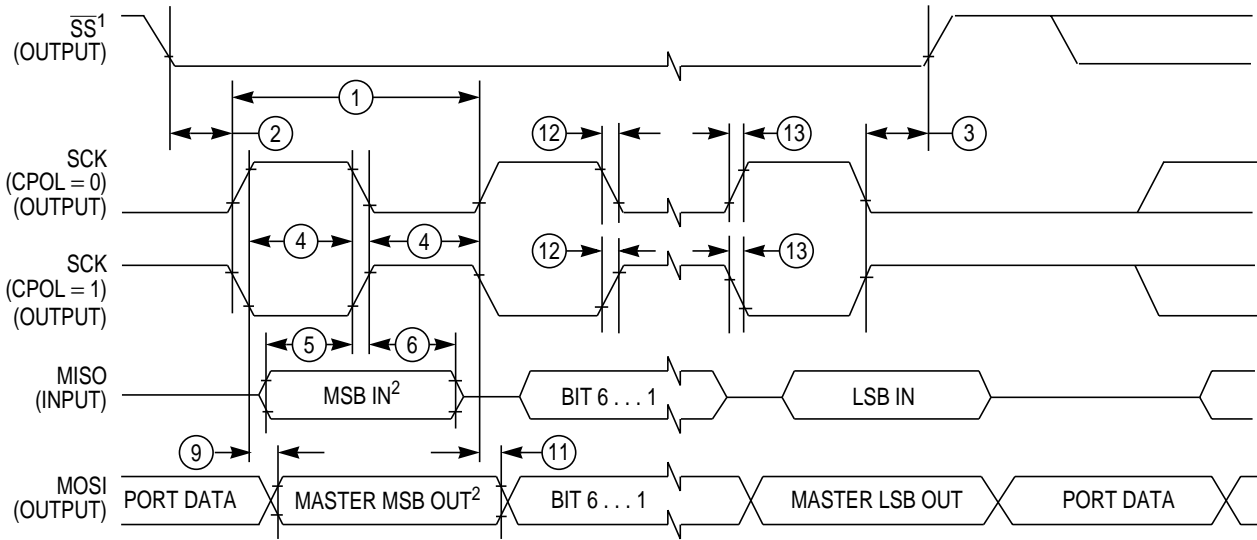
1. If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-6 SPI Master Timing (CPHA=1)

In **Table A-22** the timing characteristics for master mode are listed.

Table A-22 SPI Master Mode Timing Characteristics

Num	Characteristic	Symbol	Min	Typ	Max	Unit
1	SCK Frequency	f_{sck}	1/2048	—	1/2	f_{bus}
1	SCK Period	t_{sck}	2	—	2048	t_{bus}
2	Enable Lead Time	t_{lead}	—	1/2	—	t_{sck}
3	Enable Lag Time	t_{lag}	—	1/2	—	t_{sck}
4	Clock (SCK) High or Low Time	t_{wsck}	—	1/2	—	t_{sck}
5	Data Setup Time (Inputs)	t_{su}	8	—	—	ns
6	Data Hold Time (Inputs)	t_{hi}	8	—	—	ns
9	Data Valid after SCK Edge	t_{vsck}	—	—	29	ns
10	Data Valid after $\overline{SS}$ fall (CPHA=0)	t_{vss}	—	—	15	ns
11	Data Hold Time (Outputs)	t_{ho}	20	—	—	ns
12	Rise and Fall Time Inputs	t_{rfi}	—	—	8	ns
13	Rise and Fall Time Outputs	t_{rfo}	—	—	8	ns

A.7.2 Slave Mode

In **Figure A-7** the timing diagram for slave mode with transmission format CPHA=0 is depicted.
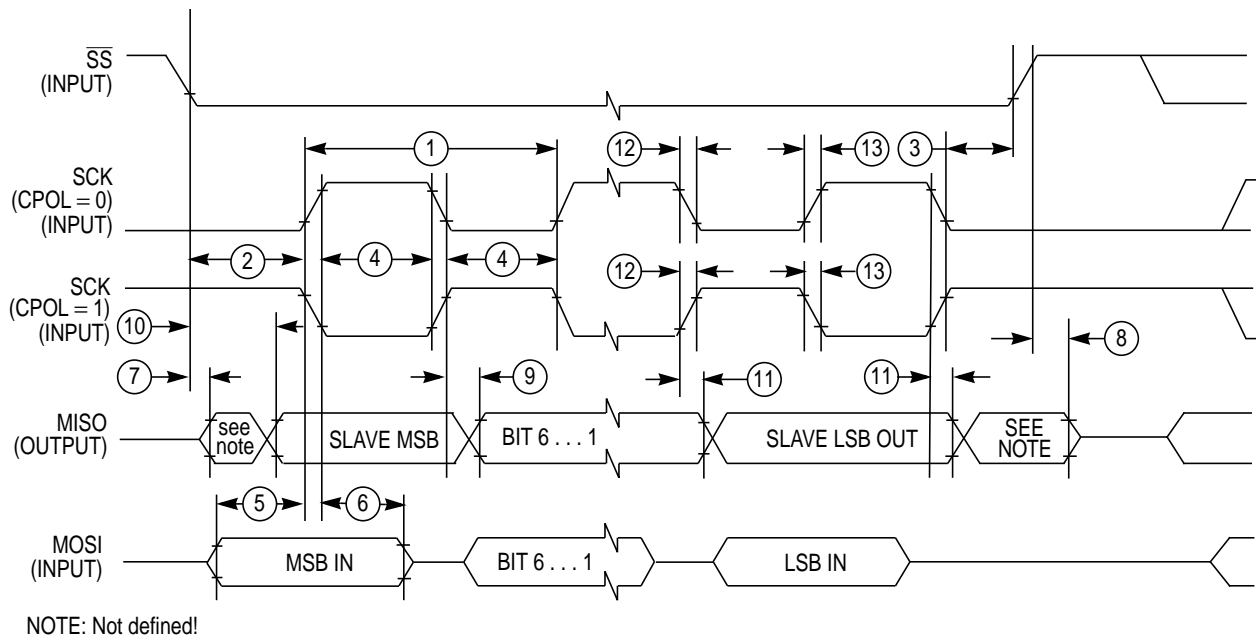
Figure A-7 SPI Slave Timing (CPHA=0)

In **Figure A-8** the timing diagram for slave mode with transmission format CPHA=1 is depicted.
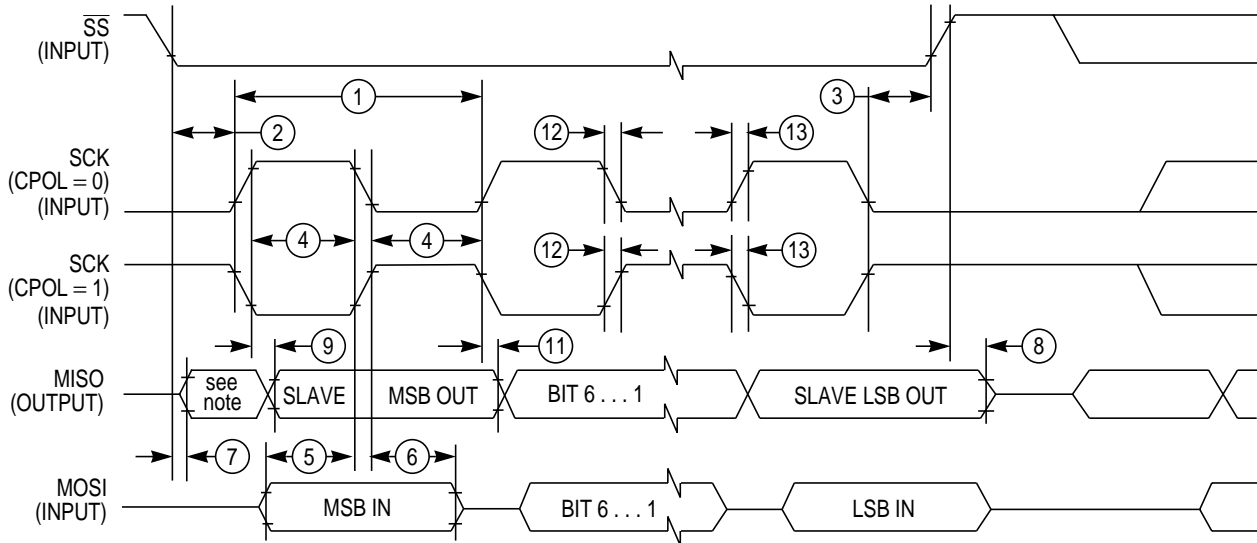
NOTE: Not defined!

Figure A-8 SPI Slave Timing (CPHA=1)

In **Table A-23** the timing characteristics for slave mode are listed.

Table A-23 SPI Slave Mode Timing Characteristics

Num	Characteristic	Symbol	Min	Typ	Max	Unit
1	SCK Frequency	f_{sck}	DC	—	1/4	f_{bus}
1	SCK Period	t_{sck}	4	—		t_{bus}
2	Enable Lead Time	t_{lead}	4	—	—	t_{bus}
3	Enable Lag Time	t_{lag}	4	—	—	t_{bus}
4	Clock (SCK) High or Low Time	t_{wsck}	4	—	—	t_{bus}
5	Data Setup Time (Inputs)	t_{su}	8	—	—	ns
6	Data Hold Time (Inputs)	t_{hi}	8	—	—	ns
7	Slave Access Time (time to data active)	t_{a}	—	—	20	ns
8	Slave MISO Disable Time	t_{dis}	—	—	22	ns
9	Data Valid after SCK Edge	t_{vsck}	—	—	$29 + 0.5 \cdot t_{bus}$	ns
10	Data Valid after $\overline{SS}$ fall	t_{vss}	—	—	$29 + 0.5 \cdot t_{bus}$	ns
11	Data Hold Time (Outputs)	t_{ho}	20	—	—	ns
12	Rise and Fall Time Inputs	t_{rfi}	—	—	8	ns
13	Rise and Fall Time Outputs	t_{rfo}	—	—	8	ns

A.8 External Bus Timing

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Appendix B Package Information

B.1 General

This section provides the physical dimensions of the MC9S12XDP512 packages.

B.2 144-pin LQFP

Figure 28-4 144-pin LQFP Mechanical Dimensions (case no. 918-03
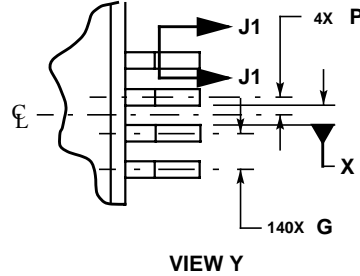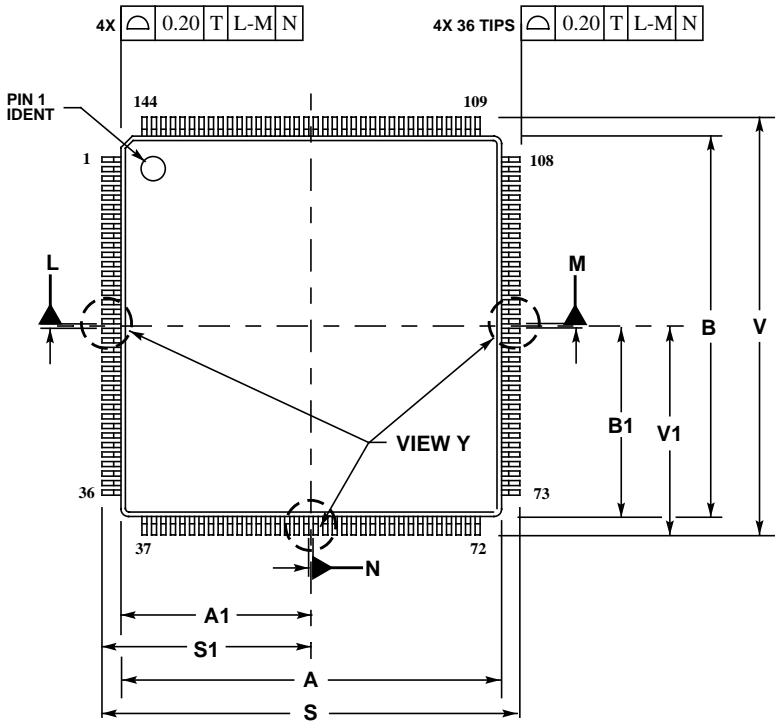
NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M, N TO BE DETERMINED AT THE SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.35.
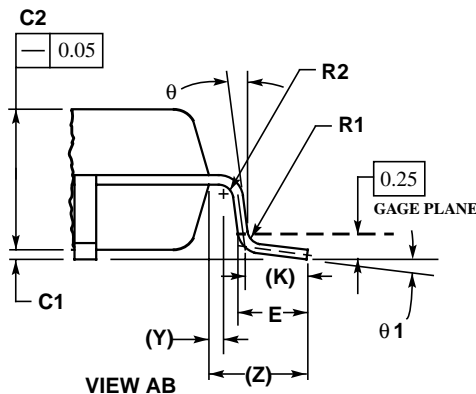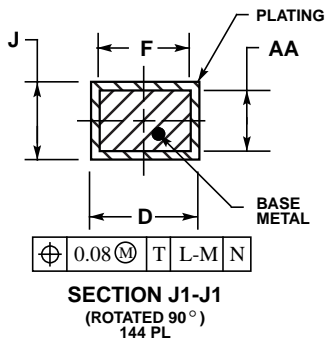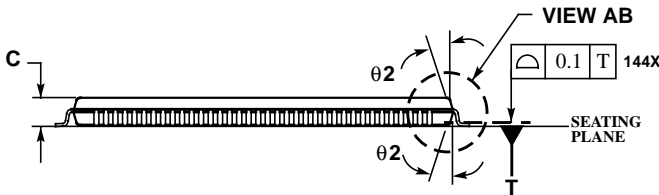
DIM	MILLIMETERS	
	MIN	MAX
A	20.00 BSC	
A1	10.00 BSC	
B	20.00 BSC	
B1	10.00 BSC	
C	1.40	1.60
C1	0.05	0.15
C2	1.35	1.45
D	0.17	0.27
E	0.45	0.75
F	0.17	0.23
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.13	0.20
R2	0.13	0.20
S	22.00 BSC	
S1	11.00 BSC	
V	22.00 BSC	
V1	11.00 BSC	
Y	0.25 REF	
Z	1.00 REF	
AA	0.09	0.16
θ	0 °	
θ1	0 °	7 °
θ2	11°	13°

B.3 112-pin LQFP package
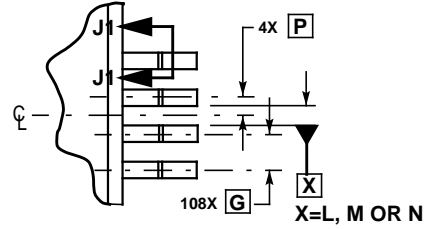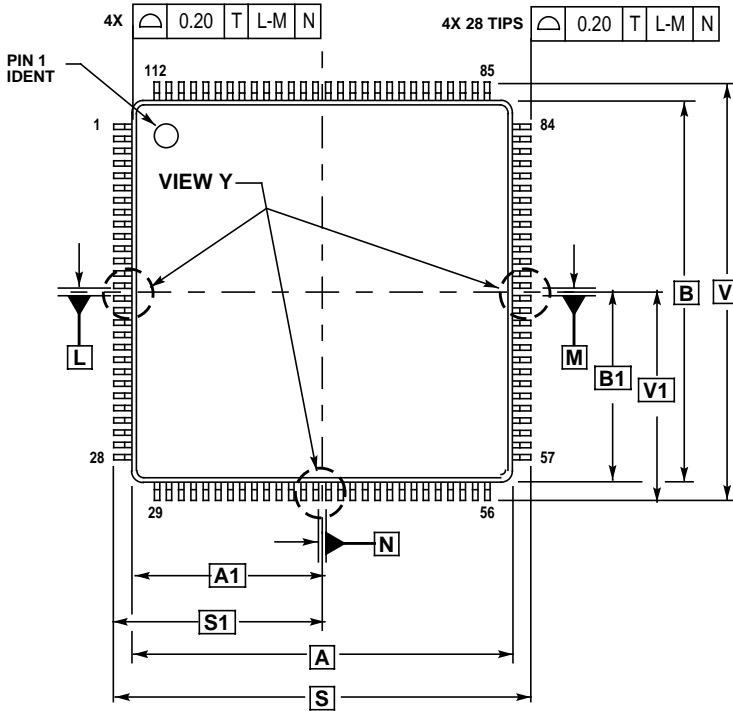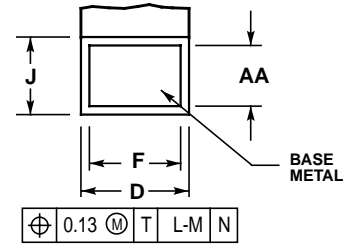
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.46.
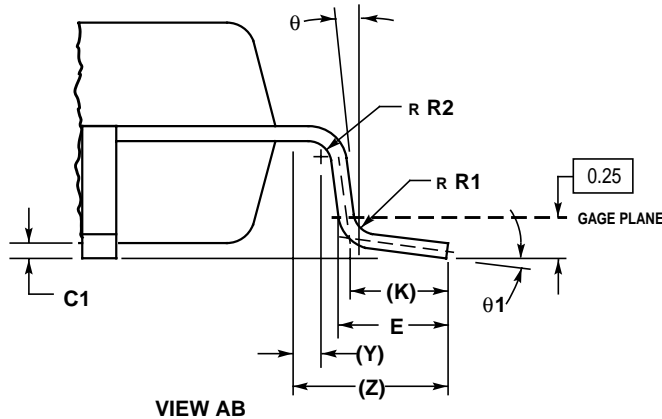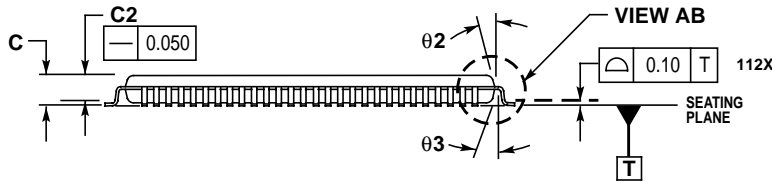
DIM	MILLIMETERS	
	MIN	MAX
A	20.000 BSC	
A1	10.000 BSC	
B	20.000 BSC	
B1	10.000 BSC	
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650 BSC	
J	0.090	0.170
K	0.500 REF	
P	0.325 BSC	
R1	0.100	0.200
R2	0.100	0.200
S	22.000 BSC	
S1	11.000 BSC	
V	22.000 BSC	
V1	11.000 BSC	
Y	0.250 REF	
Z	1.000 REF	
AA	0.090	0.160
θ	0°	8°
$\theta 1$	3°	7°
$\theta 2$	11°	13°
$\theta 3$	11°	13°

Figure B-1 112-pin LQFP mechanical dimensions (case no. 987)

B.4 80-pin QFP package

DETAIL A

DETAIL A

DETAIL C

SECTION B-B
VIEW ROTATED 90°

DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

DIM	MILLIMETERS	
---	MIN	MAX
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	---	0.25
J	0.13	0.23
K	0.65	0.95
L	12.35 REF	
M	5°	10°
N	0.13	0.17
P	0.325 BSC	
Q	0°	7°
R	0.13	0.30
S	16.95	17.45
T	0.13	---
U	0°	---
V	16.95	17.45
W	0.35	0.45
X	1.6 REF	

Figure B-2 80-pin QFP Mechanical Dimensions (case no. 841B)

User Guide End Sheet

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