



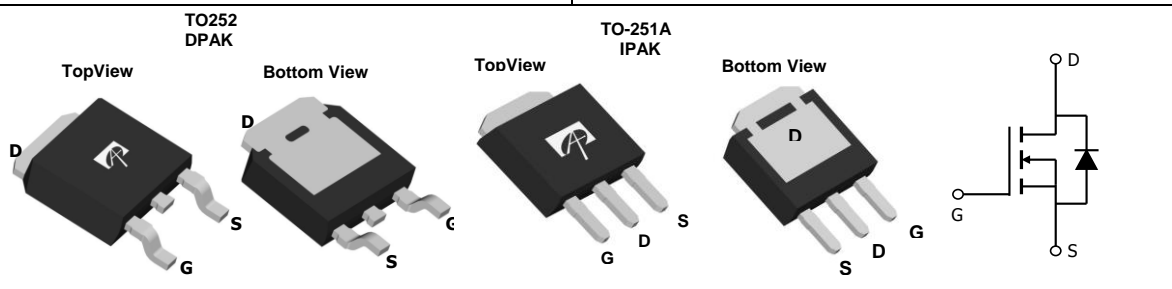
### General Description

The AOD444/AOI444 combine advanced trench MOSFET technology with a low resistance package to provide extremely low  $R_{DS(ON)}$ . Those devices are suitable for use in PWM, load switching and general purpose applications.

### Product Summary

$V_{DS}$	60V
$I_D$ (at $V_{GS}=10V$ )	12A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 60m $\Omega$
$R_{DS(ON)}$ (at $V_{GS} = 4.5V$ )	< 85m $\Omega$

100% UIS Tested  
100% Rg Tested



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>G</sup>	$I_D$	12	A
$T_C=25^\circ\text{C}$			
$T_C=100^\circ\text{C}$		9	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	30	
Continuous Drain Current	$I_{DSM}$	4	A
$T_A=25^\circ\text{C}$			
$T_A=70^\circ\text{C}$		3	
Avalanche Current <sup>C</sup>	$I_{AS}, I_{AR}$	19	A
Avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AS}, E_{AR}$	18	mJ
Power Dissipation <sup>B</sup>	$P_D$	20	W
$T_C=25^\circ\text{C}$			
$T_C=100^\circ\text{C}$		10	
Power Dissipation <sup>A</sup>	$P_{DSM}$	2.1	W
$T_A=25^\circ\text{C}$			
$T_A=70^\circ\text{C}$		1.3	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	17.4	30	$^\circ\text{C/W}$
$t \leq 10\text{s}$				
Maximum Junction-to-Ambient <sup>A D</sup>	$R_{\theta JC}$	50	60	$^\circ\text{C/W}$
Steady-State				
Maximum Junction-to-Case	$R_{\theta JC}$	4	7.5	$^\circ\text{C/W}$
Steady-State				

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =48V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =250μA	1	2.4	3	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	30			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =12A T <sub>J</sub> =125°C		47 85	60 100	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =6A		67	85	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		14		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.74	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				12	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =30V, f=1MHz	360	450	540	pF
C <sub>oss</sub>	Output Capacitance		40	61	80	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		16	27	40	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.6	1.4	2.0	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =12A		7.5	10	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge			3.8	5	nC
Q <sub>gs</sub>	Gate Source Charge			1.2		nC
Q <sub>gd</sub>	Gate Drain Charge			1.9		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, R <sub>L</sub> =2.5Ω, R <sub>GEN</sub> =3Ω		4.2		ns
t <sub>r</sub>	Turn-On Rise Time			3.4		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			16		ns
t <sub>f</sub>	Turn-Off Fall Time			2		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =12A, dI/dt=100A/μs		27	35	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =12A, dI/dt=100A/μs		30		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

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## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

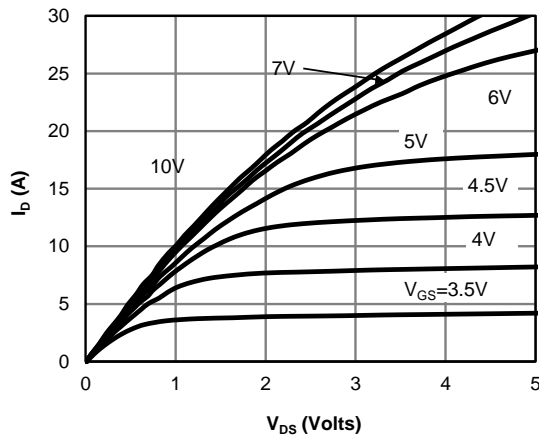


Fig 1: On-Region Characteristics (Note E)

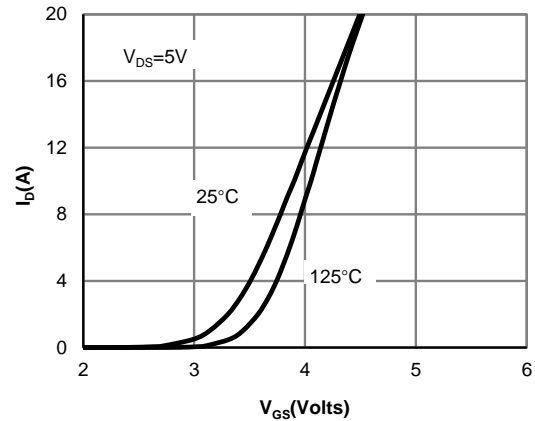


Figure 2: Transfer Characteristics (Note E)

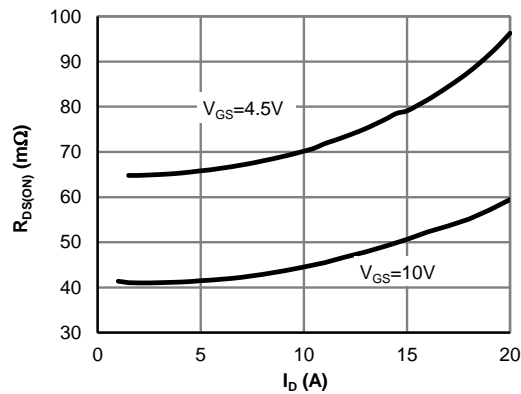


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

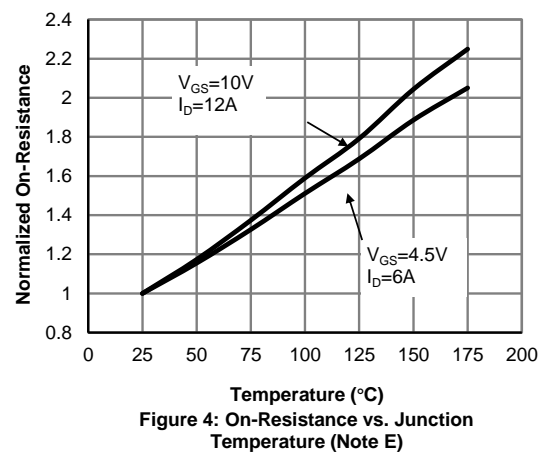


Figure 4: On-Resistance vs. Junction Temperature (Note E)

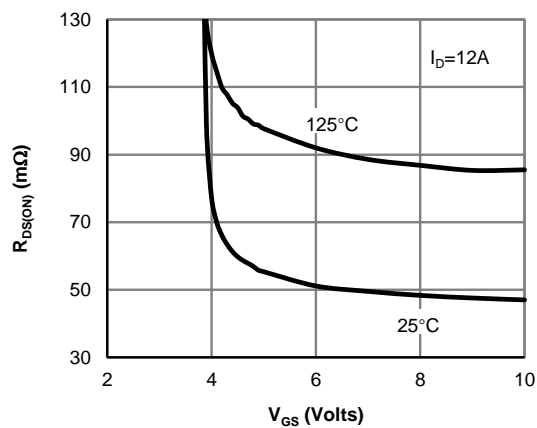


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

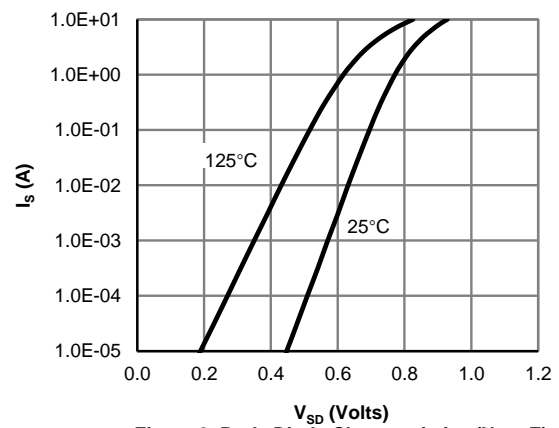
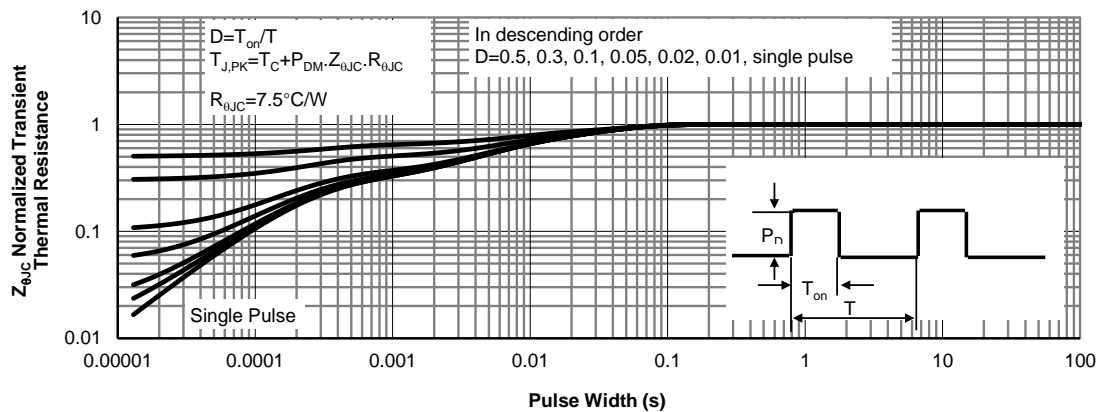
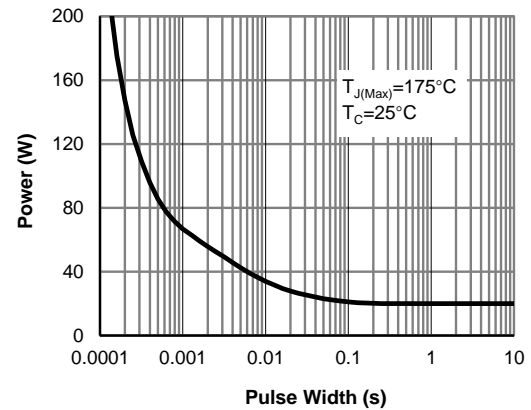
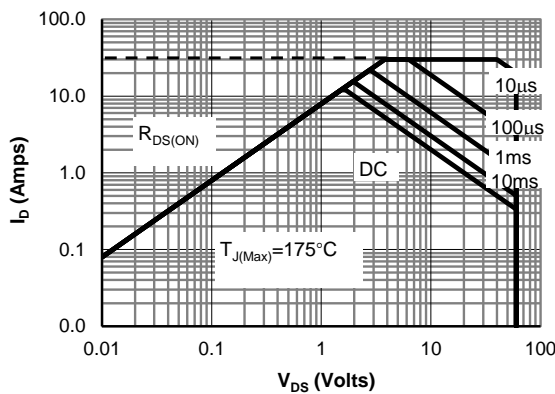
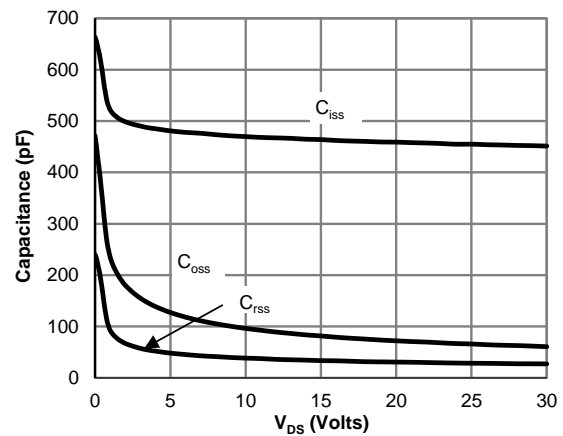
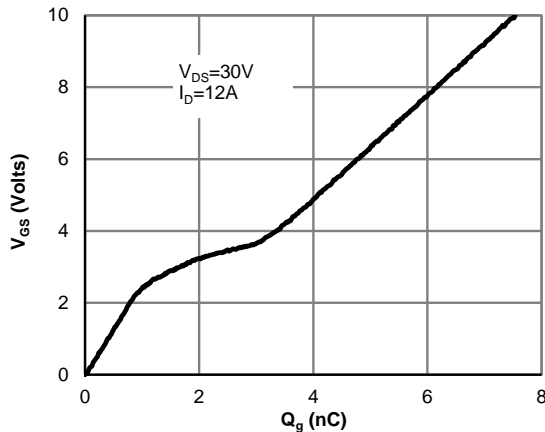
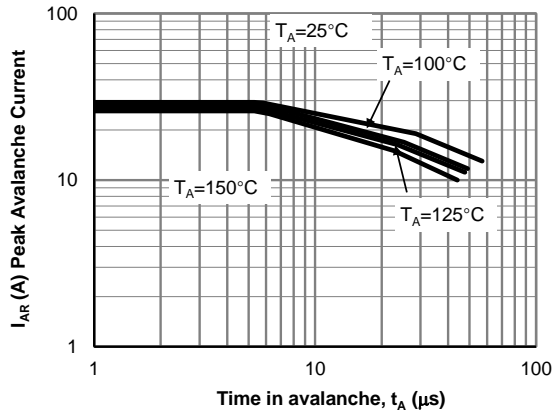


Figure 6: Body-Diode Characteristics (Note E)

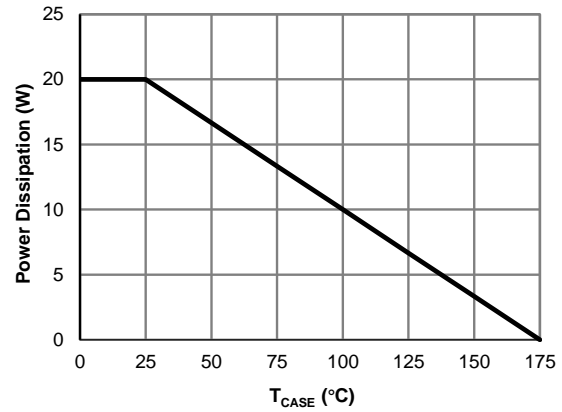
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



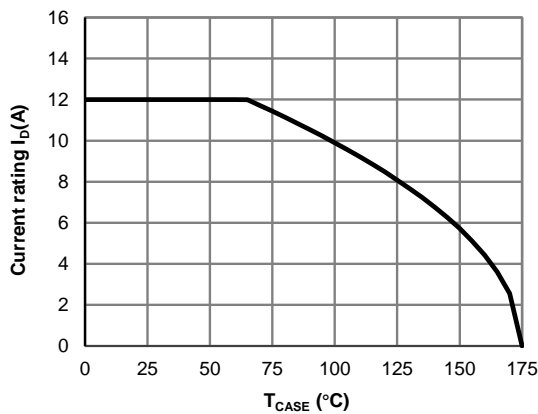
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



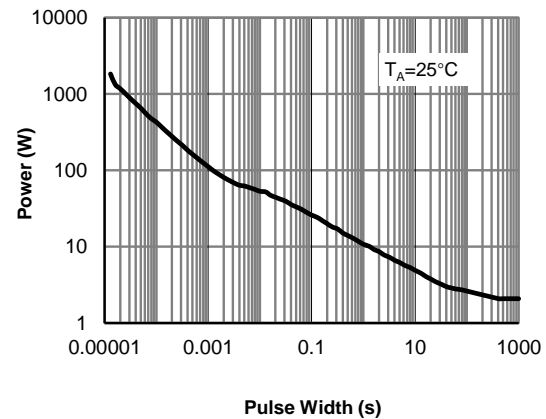
**Figure 12: Single Pulse Avalanche capability (Note C)**



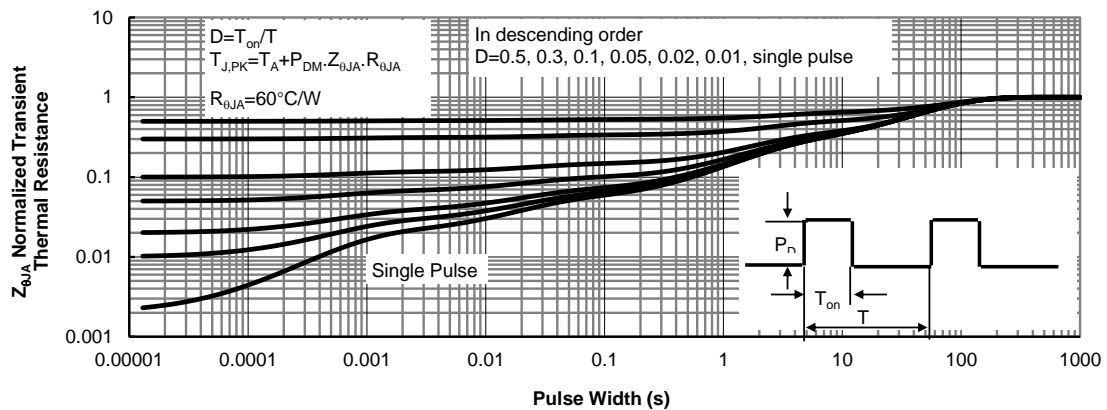
**Figure 13: Power De-rating (Note F)**



**Figure 14: Current De-rating (Note F)**

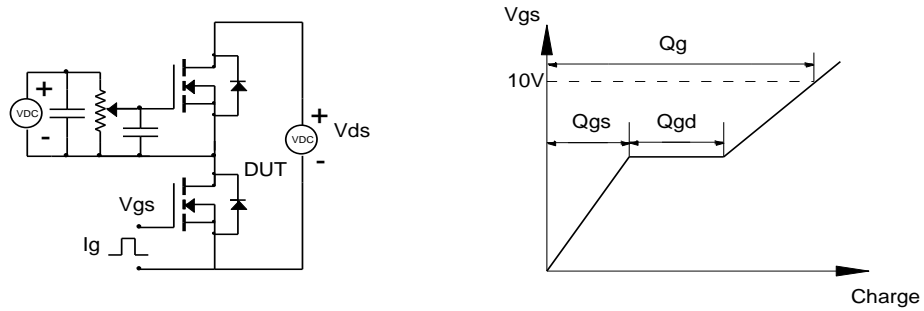


**Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)**

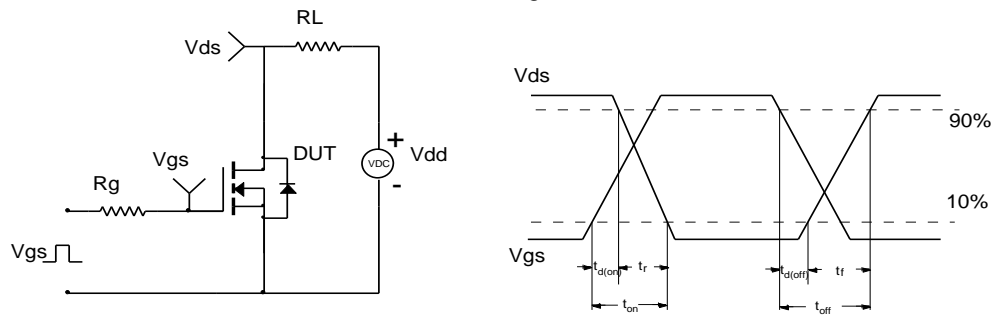


**Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)**

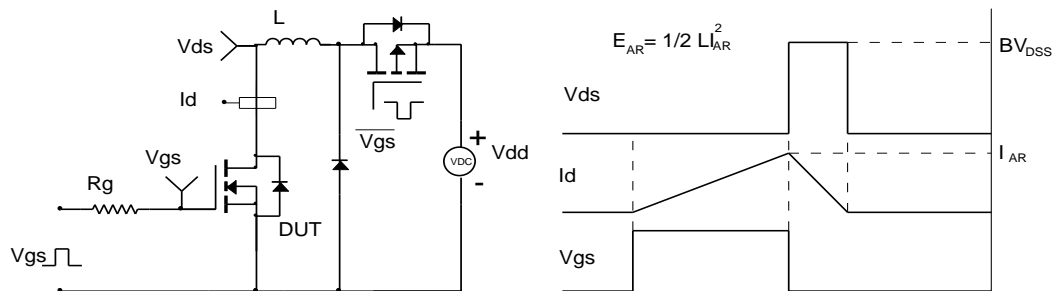
### Gate Charge Test Circuit & Waveform



### Resistive Switching Test Circuit & Waveforms



### Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



### Diode Recovery Test Circuit & Waveforms

