

Data Sheet

ADG824

FEATURES

- 0.5 Ω typical on resistance**
- 0.85 Ω maximum on resistance at 85°C**
- 1.65 V to 3.6 V operation**
- High current carrying capability: 300 mA continuous**
- Rail-to-rail switching operation**
- Fast switching times: <20 ns**
- Typical power consumption: (<0.1 μW)**
- 1.3 mm × 1.6 mm mini LFCSP package**

APPLICATIONS

- Cellular phones**
- PDAs**
- MP3 players**
- Power routing**
- Battery-powered systems**
- PCMCIA cards**
- Modems**
- Audio and video signal routing**
- Communication systems**

GENERAL DESCRIPTION

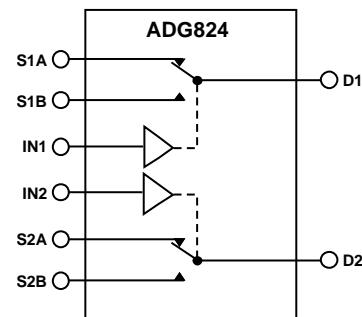
The ADG824 is a low voltage CMOS device containing two independently selectable single-pole, double throw (SPDT) switches. This device offers ultralow on resistance of less than 0.85 Ω over the full temperature range. The ADG824 is fully specified for 3.3 V, 2.5 V, and 1.8 V supply operation.

Each switch conducts equally well in both directions when on, and has an input signal range that extends to the supplies. The ADG824 exhibits break-before-make switching action.

The low on resistance of the ADG824 makes this device ideal for audio switching. In addition, a data rate of 180 Mbps makes the device suitable for USB low speed (1.5 Mbps) and full speed (12 Mbps) data switching.

The ADG824 is available in a 1.3 mm × 1.6 mm, 10-lead mini LFCSP package.

FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC 1 INPUT

Figure 1.
06693-001

PRODUCT HIGHLIGHTS

1. <0.85 Ω over the full temperature range of -40°C to +85°C.
2. Single 1.65 V to 3.6 V operation.
3. 1.8 V logic compatible.
4. High current carrying capability (300 mA continuous current at 3.3 V).
5. Low THD + N (0.06% typical).
6. 1.3 mm × 1.6 mm mini LFCSP package.

Rev. C

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

Features	1	ESD Caution.....	6
Applications.....	1	Pin Configuration and Function Descriptions.....	7
Functional Block Diagram	1	Typical Performance Characteristics	8
General Description	1	Test Circuits.....	11
Product Highlights	1	Terminology	13
Revision History	2	Outline Dimensions.....	14
Specifications.....	3	Ordering Guide	14
Absolute Maximum Ratings.....	6		

REVISION HISTORY

3/12—Rev. B to Rev. C

Changes to Features Section, General Description Section, and Product Highlights Section	1
Changes to On Resistance, R_{ON} Parameter and On Resistance Match Between Channels, ΔR_{ON} Parameter, Table 1.....	3
Changes to On Resistance, R_{ON} Parameter, On Resistance Match Between Channels, ΔR_{ON} Parameter, and On Resistance Flatness, $R_{FLAT(ON)}$, Table 2	4
Changes to On Resistance, R_{ON} Parameter, Table 3	5
Changes to Ordering Guide	14

1/09—Rev. A to Rev. B

Changes to On Resistance Match Between Channels, ΔR_{ON} Parameter, Table 1	3
Updated Outline Dimensions	14
Changes to Ordering Guide	14

7/08—Rev. 0 to Rev. A

Changes to Digital Inputs Parameter, Table 1.....	3
Changes to Digital Inputs Parameter, Table 2.....	4
Changes to Digital Inputs Parameter, Table 3.....	5

4/08—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 3.6 V, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	+25°C	-40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
On Resistance, R_{ON}	0.5 0.8	0.85	Ω typ Ω max	$V_{DD} = 2.7$ V, $V_S = 0$ V to V_{DD} , $I_{DS} = 100$ mA; see Figure 19
On Resistance Match Between Channels, ΔR_{ON}	0.003	0.04	Ω typ Ω max	$V_{DD} = 2.7$ V, $V_S = 0.65$ V, $I_{DS} = 100$ mA
On Resistance Flatness, $R_{FLAT(ON)}$	0.13	0.2	Ω typ Ω max	$V_{DD} = 2.7$ V, $V_S = 0$ V to V_{DD} , $I_{DS} = 100$ mA
LEAKAGE CURRENTS				
Source Off Leakage, I_S (Off)	± 0.2		nA typ	$V_{DD} = 3.6$ V
Channel On Leakage, I_D , I_S (On)	± 0.2		nA typ	$V_S = 0.6$ V/3.3 V, $V_D = 3.3$ V/0.6 V; see Figure 20
DIGITAL INPUTS				
Input High Voltage, V_{INH}		1.35	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005	± 0.1	μA typ μA max pF typ	$V_{IN} = V_{GND}$ or V_{DD} $V_{IN} = V_{GND}$ or V_{DD}
Digital Input Capacitance, C_{IN}	2.7			
DYNAMIC CHARACTERISTICS ¹				
t_{ON}	7 9.5	10.8	ns typ ns max	$R_L = 50 \Omega$, $C_L = 35$ pF $V_S = 2$ V/0 V; see Figure 22
t_{OFF}	6 7.7	8.6	ns typ ns max	$R_L = 50 \Omega$, $C_L = 35$ pF $V_S = 2$ V; see Figure 22
Break-Before-Make Time Delay, t_{BBM}	3.5	2	ns typ ns min pC typ	$R_L = 50 \Omega$, $C_L = 35$ pF $V_{S1} = V_{S2} = 2$ V; see Figure 23
Charge Injection, Q_{INJ}	27		dB typ	$V_S = 1.5$ V, $R_S = 0$ Ω , $C_L = 1$ nF; see Figure 24
Off Isolation	-71		dB typ	$R_L = 50 \Omega$, $C_L = 5$ pF, $f = 100$ kHz; see Figure 25
Channel-to-Channel Crosstalk	-90		dB typ	S1A to S2A/S1B to S2B, $R_L = 50 \Omega$, $C_L = 5$ pF, $f = 100$ kHz; see Figure 26
	-67		dB typ	S1A to S1B/S2A to S2B, $R_L = 50 \Omega$, $C_L = 5$ pF, $f = 100$ kHz; see Figure 27
Total Harmonic Distortion, THD + N	0.06		%	$R_L = 33 \Omega$, $f = 20$ Hz to 20 kHz, $V_S = 2$ V p-p
Insertion Loss	-0.05		dB typ	$R_L = 50 \Omega$, $C_L = 5$ pF; see Figure 28
-3 dB Bandwidth	90		MHz typ	$R_L = 50 \Omega$, $C_L = 5$ pF; see Figure 28
C_S (Off)	25		pF typ	
C_D , C_S (On)	58		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.003	1	μA typ μA max	$V_{DD} = 3.6$ V Digital inputs = 0 V or 3.6 V

¹ Guaranteed by design; not subject to production test.

$V_{DD} = 2.5 \text{ V} \pm 0.2 \text{ V}$, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	+25°C	-40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
On Resistance, R_{ON}	0.65 0.95	1.0	Ω typ Ω max	$V_{DD} = 2.3 \text{ V}$, $V_S = 0 \text{ V}$ to V_{DD} , $I_{DS} = 100 \text{ mA}$; see Figure 19
On Resistance Match Between Channels, ΔR_{ON}	0.005	0.04	Ω typ Ω max	$V_{DD} = 2.3 \text{ V}$, $V_S = 0.7 \text{ V}$, $I_{DS} = 100 \text{ mA}$
On Resistance Flatness, $R_{FLAT(ON)}$	0.2	0.35	Ω typ Ω max	$V_{DD} = 2.3 \text{ V}$, $V_S = 0 \text{ V}$ to V_{DD} , $I_{DS} = 100 \text{ mA}$
LEAKAGE CURRENTS				
Source Off Leakage, I_S (Off)	± 0.2		nA typ	$V_{DD} = 2.7 \text{ V}$
Channel On Leakage, I_D , I_S (On)	± 0.2		nA typ	$V_S = 0.6 \text{ V}/2.4 \text{ V}$, $V_D = 2.4 \text{ V}/0.6 \text{ V}$; see Figure 20
DIGITAL INPUTS				
Input High Voltage, V_{INH}		1.3	V min	
Input Low Voltage, V_{INL}		0.7	V max	
Input Current				
I_{INL} or I_{INH}	0.005	± 0.1	μA typ μA max	$V_{IN} = V_{GND}$ or V_{DD}
Digital Input Capacitance, C_{IN}	2.7		pF typ	$V_{IN} = V_{GND}$ or V_{DD}
DYNAMIC CHARACTERISTICS ¹				
t_{ON}	9 11.5	12.4	ns typ ns max	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$ $V_S = 1.5 \text{ V}/0 \text{ V}$; see Figure 22
t_{OFF}	6 7.4	8	ns typ ns max	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$ $V_S = 1.5 \text{ V}$; see Figure 22
Break-Before-Make Time Delay, t_{BBM}	5	3	ns typ ns min	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$ $V_{S1} = V_{S2} = 1.5 \text{ V}$; see Figure 23
Charge Injection, Q_{INJ}	21		pC typ	$V_S = 1.5 \text{ V}$, $R_S = 0 \Omega$, $C_L = 1 \text{ nF}$; see Figure 24
Off Isolation	-71		dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$; see Figure 25
Channel-to-Channel Crosstalk	-90		dB typ	S1A to S2A/S1B to S2B, $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$; see Figure 26
	-71		dB typ	S1A to S1B/S2A to S2B, $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$; see Figure 27
Total Harmonic Distortion, THD + N	0.1		%	$R_L = 33 \Omega$, $f = 20 \text{ Hz}$ to 20 kHz , $V_S = 1.5 \text{ V}$ p-p
Insertion Loss	-0.065		dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; see Figure 28
-3 dB Bandwidth	90		MHz typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; see Figure 28
C_S (Off)	25		pF typ	
C_D , C_S (On)	60		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.003	1	μA typ μA max	$V_{DD} = 2.7 \text{ V}$ Digital inputs = 0 V or 2.7 V

¹ Guaranteed by design; not subject to production test.

V_{DD} = 1.65 V to 1.95 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	+25°C	-40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range	0 to V_{DD}		V	
On Resistance, R_{ON}	1.3 2 3.1 0.01	2.4 3.6	Ω typ Ω max Ω max Ω typ	$V_{DD} = 1.8$ V, $V_S = 0$ V to V_{DD} , $I_{DS} = 100$ mA; see Figure 19 $V_{DD} = 1.65$ V, $V_S = 0$ V to V_{DD} , $I_{DS} = 100$ mA; see Figure 19 $V_{DD} = 1.65$ V, $V_S = 0.7$ V, $I_{DS} = 100$ mA
On Resistance Match Between Channels, ΔR_{ON}				
LEAKAGE CURRENTS				
Source Off Leakage, I_S (Off)	± 0.2		nA typ	$V_{DD} = 1.95$ V
Channel On Leakage, I_D , I_S (On)	± 0.2		nA typ	$V_S = 0.6$ V/1.65 V, $V_D = 1.65$ V/0.6 V; see Figure 20 $V_S = V_D = 0.6$ V or 1.65 V; see Figure 21
DIGITAL INPUTS				
Input High Voltage, V_{INH}		0.65 V_{DD}	V min	
Input Low Voltage, V_{INL}		0.35 V_{DD}	V max	
Input Current I_{INL} or I_{INH}	0.005	± 0.1	μA typ μA max pF typ	$V_{IN} = V_{GND}$ or V_{DD} $V_{IN} = V_{GND}$ or V_{DD}
Digital Input Capacitance, C_{IN}	2.7			
DYNAMIC CHARACTERISTICS¹				
t_{ON}	13 18.6	19.3	ns typ ns max	$R_L = 50 \Omega$, $C_L = 35$ pF $V_S = 1.2$ V/0 V; see Figure 22
t_{OFF}	7 9.8	10.2	ns typ ns max	$R_L = 50 \Omega$, $C_L = 35$ pF $V_S = 1.2$ V; see Figure 22
Break-Before-Make Time Delay, t_{BBM}	7.5 15 -71	5	ns typ ns min pC typ dB typ dB typ dB typ	$R_L = 50 \Omega$, $C_L = 35$ pF $V_{S1} = V_{S2} = 1.2$ V; see Figure 23 $V_S = 1$ V, $R_S = 0$ Ω , $C_L = 1$ nF; see Figure 24 $R_L = 50 \Omega$, $C_L = 5$ pF, $f = 100$ kHz; see Figure 25 S1A to S2A/S1B to S2B, $R_L = 50 \Omega$, $C_L = 5$ pF, $f = 100$ kHz; see Figure 26 S1A to S1B/S2A to S2B, $R_L = 50 \Omega$, $C_L = 5$ pF, $f = 100$ kHz; see Figure 27
Charge Injection, Q_{INJ}	-71		%	$R_L = 33 \Omega$, $f = 20$ Hz to 20 kHz, $V_S = 1.2$ V p-p
Off Isolation	-71		dB typ	$R_L = 50 \Omega$, $C_L = 5$ pF; see Figure 28
Channel-to-Channel Crosstalk	-90		MHz typ	$R_L = 50 \Omega$, $C_L = 5$ pF; see Figure 28
Total Harmonic Distortion, THD + N	0.4		pF typ	
Insertion Loss	-0.1		pF typ	
-3 dB Bandwidth	90			
C_S (Off)	26			
C_D , C_S (On)	61			
POWER REQUIREMENTS				
I_{DD}	0.003	1	μA typ μA max	$V_{DD} = 1.95$ V Digital inputs = 0 V or 1.95 V

¹ Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	-0.3 V to +4.6 V
Analog Inputs ¹	-0.3 V to $V_{DD} + 0.3$ V
Digital Inputs ¹	-0.3 V to +4.6 V or 10 mA, whichever occurs first
Peak Current, Sx or Dx Pins	Pulsed at 1 ms, 10% duty cycle max
3.3 V Operation	500 mA
2.5 V Operation	460 mA
1.8 V Operation	420 mA
Continuous Current, Sx or Dx Pins	
3.3 V Operation	300 mA
2.5 V Operation	275 mA
1.8 V Operation	250 mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Mini LFCSP Package	
θ_{JA} Thermal Impedance (4-Layer Board)	131.6°C/W
Reflow Soldering (Pb-Free)	
Peak Temperature	260°C
Time at Peak Temperature	10 sec to 40 sec

¹ Overvoltages at the INx, Sx, or Dx pins are clamped by internal diodes.
Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

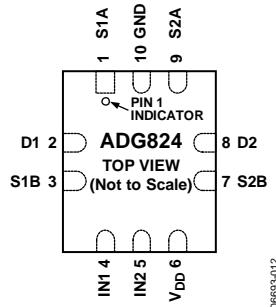


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	S1A	Source Terminal. This pin can be an input or an output.
2	D1	Drain Terminal. This pin can be an input or an output.
3	S1B	Source Terminal. This pin can be an input or an output.
4	IN1	Logic Control Input. This pin controls Switch S1A and Switch S1B to D1.
5	IN2	Logic Control Input. This pin controls Switch S2A and Switch S2B to D2.
6	V _{DD}	Most Positive Power Supply Potential.
7	S2B	Source Terminal. This pin can be an input or an output.
8	D2	Drain Terminal. This pin can be an input or an output.
9	S2A	Source Terminal. This pin can be an input or an output.
10	GND	Ground (0 V) Reference.

Table 6. ADG824 Truth Table

Logic (IN1/IN2)	Switch A (S1A or S2A)	Switch B (S1B or S2B)
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

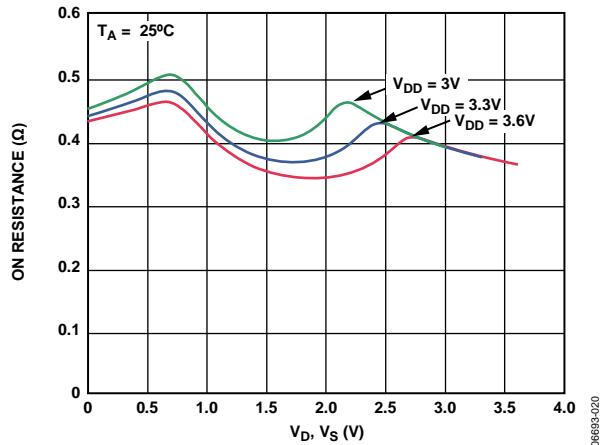


Figure 3. On Resistance vs. V_D (V_S), $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$

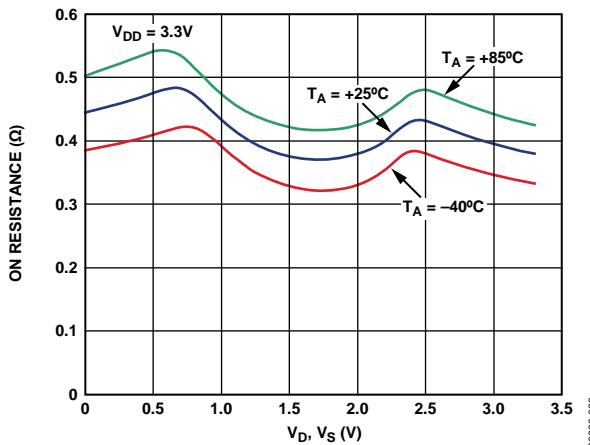


Figure 6. On Resistance vs. V_D (V_S) for Different Temperatures, $V_{DD} = 3.3\text{ V}$

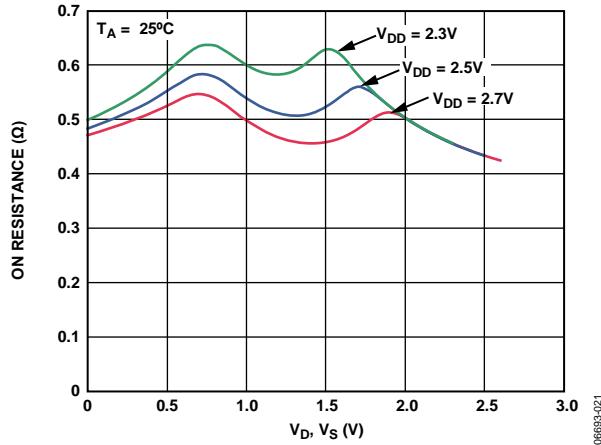


Figure 4. On Resistance vs. V_D (V_S), $V_{DD} = 2.5\text{ V} \pm 0.2\text{ V}$

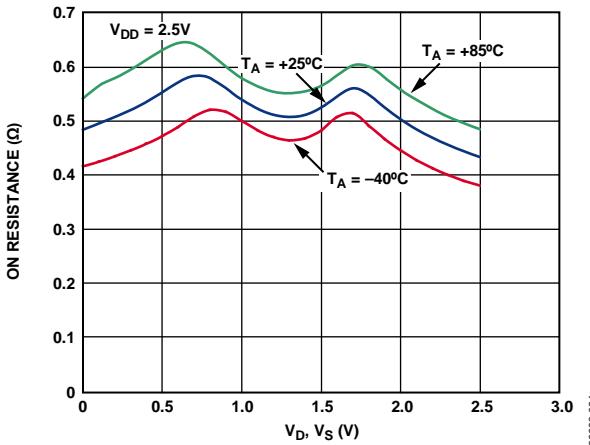


Figure 7. On Resistance vs. V_D (V_S) for Different Temperatures, $V_{DD} = 2.5\text{ V}$

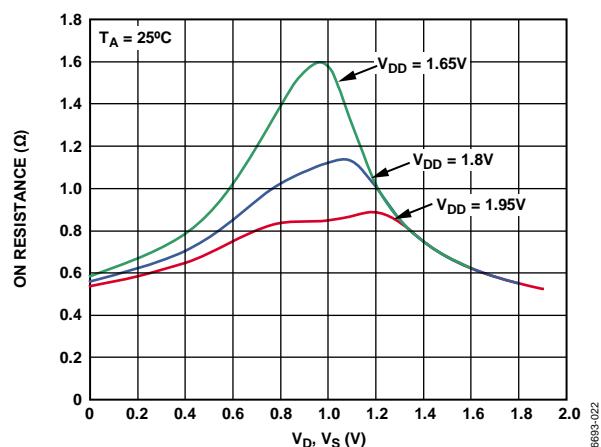


Figure 5. On Resistance vs. V_D (V_S), $V_{DD} = 1.8\text{ V} \pm 0.15\text{ V}$

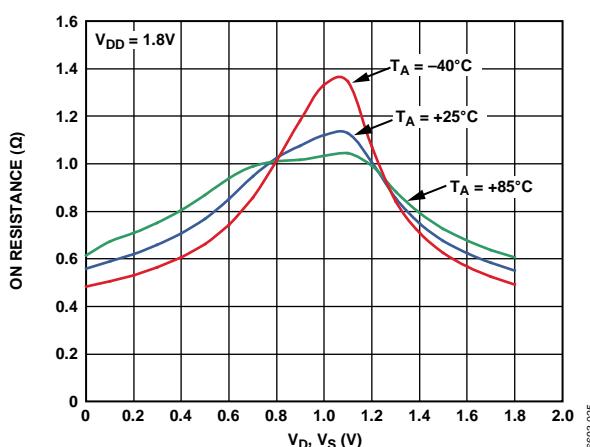
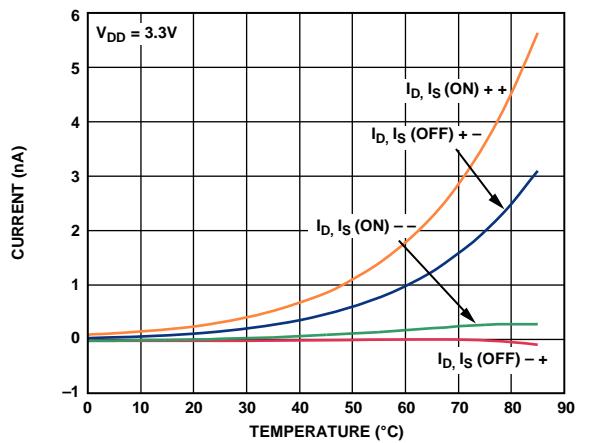
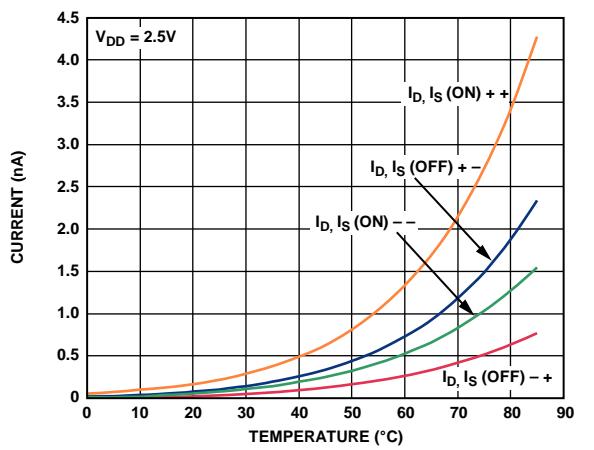


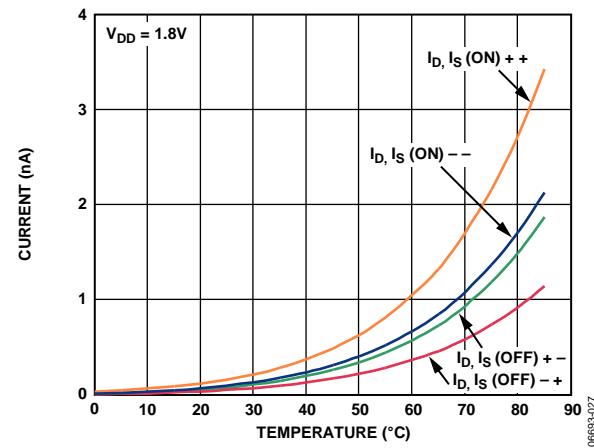
Figure 8. On Resistance vs. V_D (V_S) for Different Temperatures, $V_{DD} = 1.8\text{ V}$



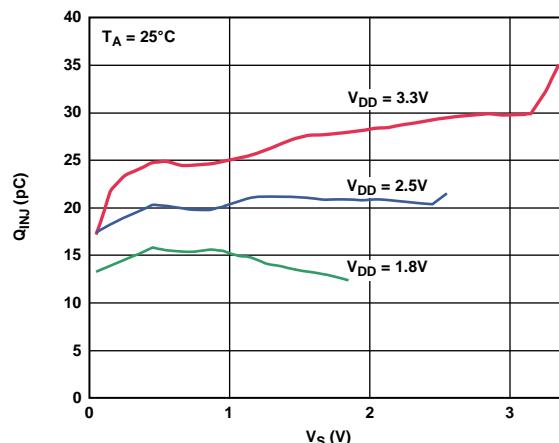
06693-028



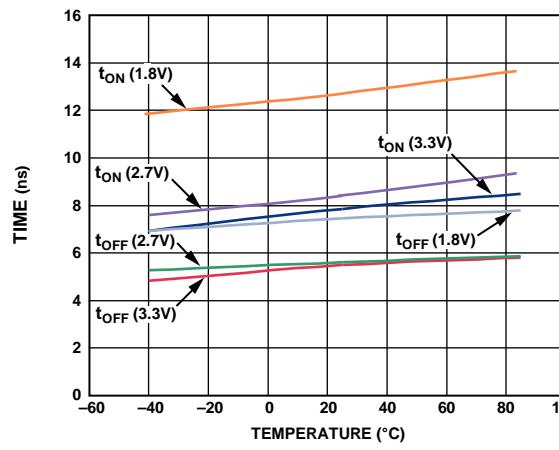
06693-017



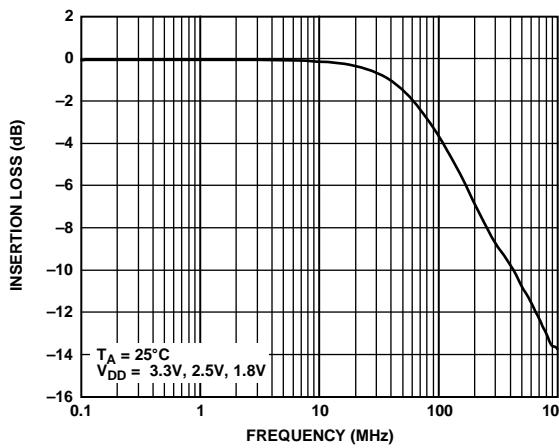
06693-027



06693-014



06693-019



06693-016

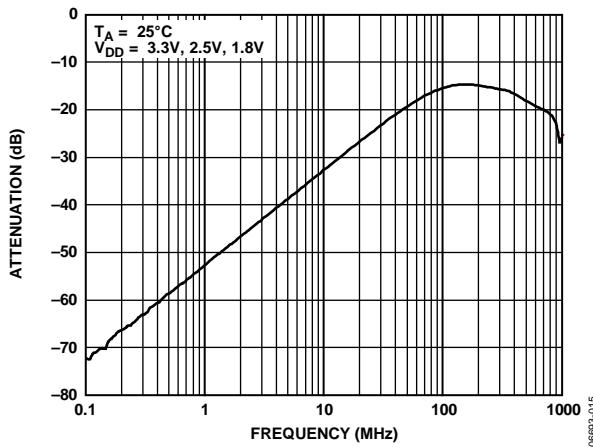


Figure 15. Off Isolation vs. Frequency

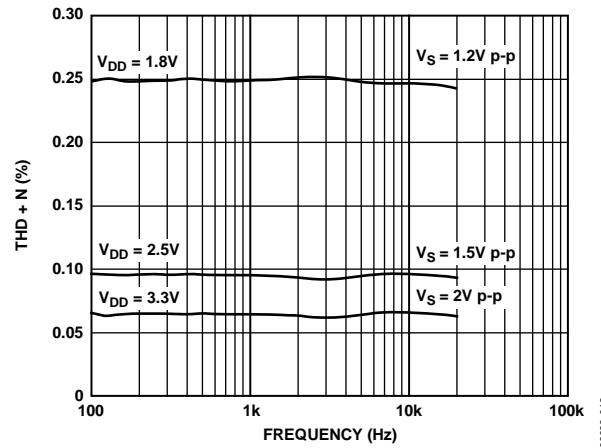


Figure 17. Total Harmonic Distortion + Noise vs. Frequency

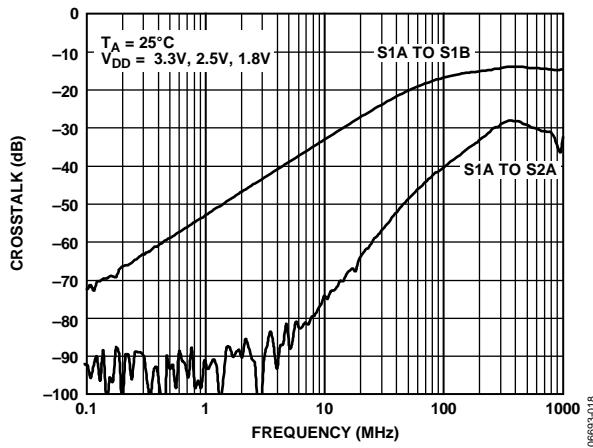


Figure 16. Crosstalk vs. Frequency

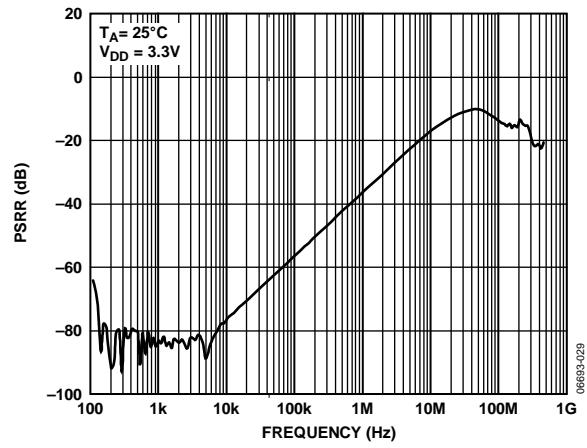


Figure 18. PSRR vs. Frequency

TEST CIRCUITS

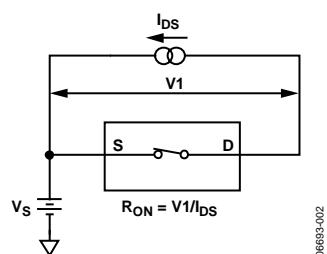


Figure 19. On Resistance

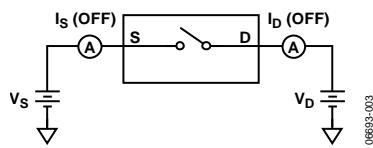


Figure 20. Off Leakage

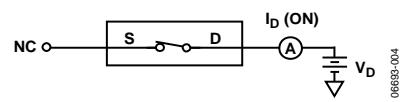
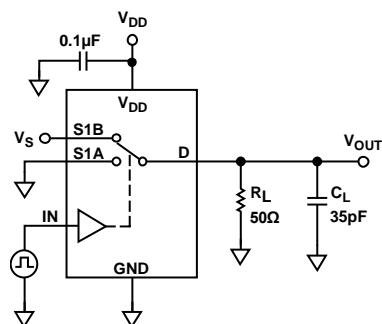
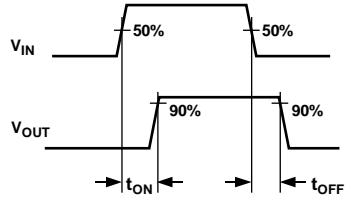
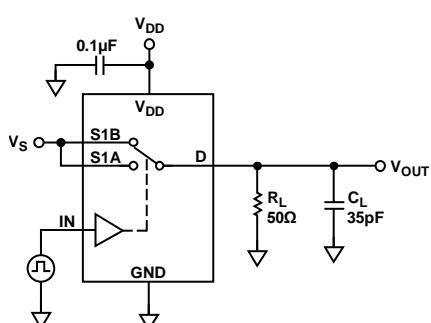
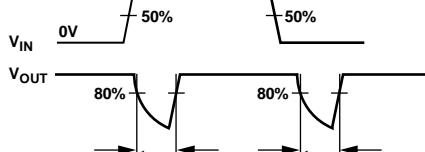


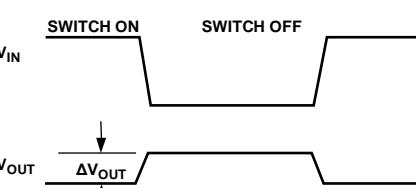
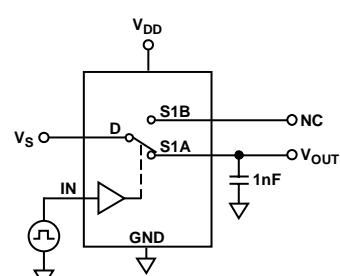
Figure 21. On Leakage

Figure 22. Switching Times, t_{ON} , t_{OFF} 

06693-005

Figure 23. Break-Before-Make Time Delay, t_{BBM} 

06693-006



06693-007

Figure 24. Charge Injection

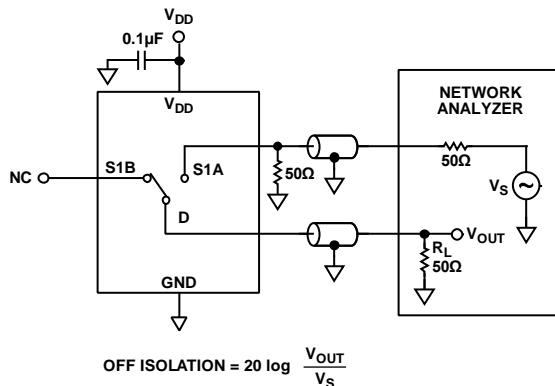


Figure 25. Off Isolation

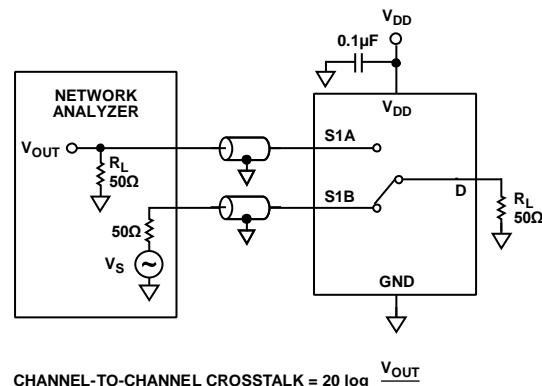


Figure 27. Channel-to-Channel Crosstalk (S1A to S1B/S2A to S2B)

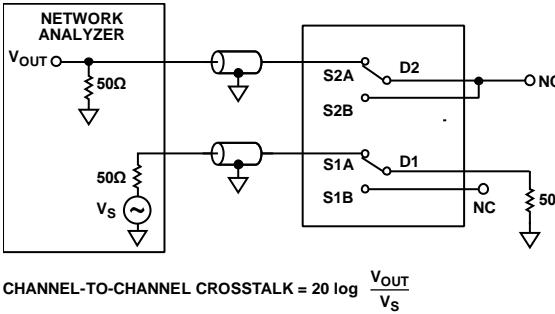


Figure 26. Channel-to-Channel Crosstalk (S1A to S2A/S1B to S2B)

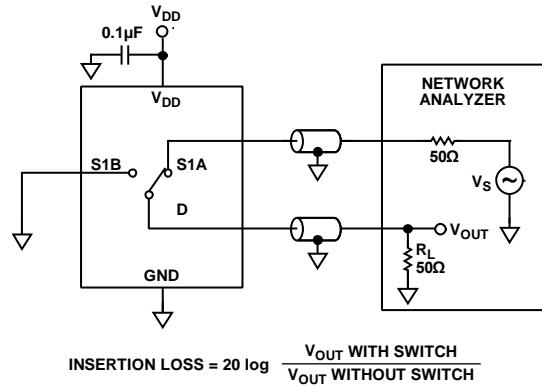


Figure 28. Bandwidth

TERMINOLOGY

I_{DD}

Positive supply current.

V_D (V_s)

Analog voltage on Terminal D and Terminal S.

R_{ON}

Ohmic resistance between Terminal D and Terminal S.

R_{FLAT} (On)

The difference between the maximum and minimum values of on resistance as measured on the switch.

ΔR_{ON}

On resistance match between any two channels.

I_s (Off)

Source leakage current with the switch off.

I_d (Off)

Drain leakage current with the switch off.

I_D, I_S (On)

Channel leakage current with the switch on.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL} (I_{INH})

Input current of the digital input.

C_s (Off)

Off switch source capacitance. Measured with reference to ground.

C_D, C_S (On)

On switch capacitance. Measured with reference to ground.

C_{IN}

Digital input capacitance.

t_{ON}

Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF}

Delay time between the 50% and 90% points of the digital input and switch off condition.

t_{BBM}

On or off time measured between the 80% points of both switches when switching from one to another.

Charge Injection

Measure of the glitch impulse transferred from the digital input to the analog output during on/off switching.

Off Isolation

Measure of unwanted signal coupling through an off switch.

Crosstalk

Measure of unwanted signal that is coupled from one channel to another as a result of parasitic capacitance.

-3 dB Bandwidth

Frequency at which the output is attenuated by 3 dB.

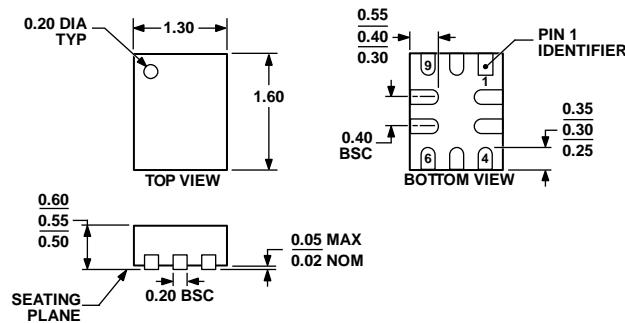
Insertion Loss

The loss due to the on resistance of the switch.

THD + N

Ratio of the harmonics amplitude plus noise of a signal to the fundamental.

OUTLINE DIMENSIONS



033007-A

Figure 29. 10-Lead Lead Frame Chip Scale Package (LFCSP_UQ)
 1.3 mm × 1.6 mm Body, Ultra Thin Quad
 (CP-10-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
ADG824BCPZ-REEL7	−40°C to +85°C	10-Lead Lead Frame Chip Scale Package (LFCSP_UQ)	CP-10-10	A
EVAL-ADG824EBZ	−40°C to +85°C	Evaluation Board		

¹ Z = RoHS Compliant Part.

NOTES

NOTES