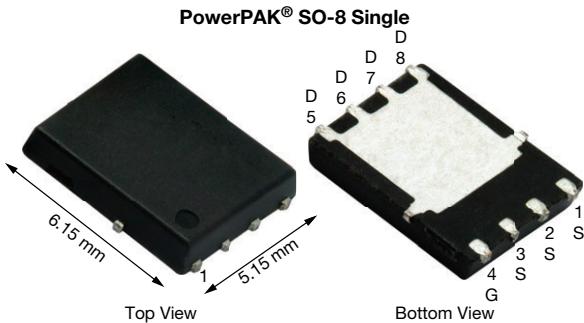


N-Channel 60 V (D-S) MOSFET



PRODUCT SUMMARY	
V _{DS} (V)	60
R _{DS(on)} max. (Ω) at V _{GS} = 10 V	0.0044
R _{DS(on)} max. (Ω) at V _{GS} = 4.5 V	0.0063
Q _g typ. (nC)	15.2
I _D (A)	80.3
Configuration	Single

FEATURES

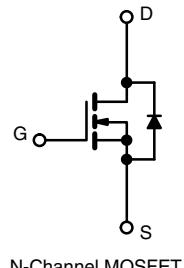
- TrenchFET® Gen IV power MOSFET
- Very low R_{DS} - Q_g figure-of-merit (FOM)
- Tuned for the lowest R_{DS} - Q_{oss} FOM
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- Primary side switch
- DC/DC converter
- Motor drive switch



N-Channel MOSFET

ORDERING INFORMATION

Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SiR186LDP-T1-RE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	60	V
Gate-source voltage	V _{GS}	± 20	
Continuous drain current (T _J = 150 °C)	T _C = 25 °C	80.3	A
	T _C = 70 °C	64.2	
	T _A = 25 °C	23.8 b, c	
	T _A = 70 °C	19 b, c	
Pulsed drain current (t = 100 µs)	I _{DM}	150	A
Continuous source-drain diode current	T _C = 25 °C	51.8	
	T _A = 25 °C	4.5 b, c	
Single pulse avalanche current	I _{AS}	25	mJ
Single pulse avalanche energy	E _{AS}	31.25	
Maximum power dissipation	T _C = 25 °C	57	W
	T _C = 70 °C	36	
	T _A = 25 °C	5 b, c	
	T _A = 70 °C	3.2 b, c	
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	t ≤ 10 s	R _{thJA}	20	°C/W
Maximum junction-to-case (drain)	Steady state	R _{thJC}	1.7	

Notes

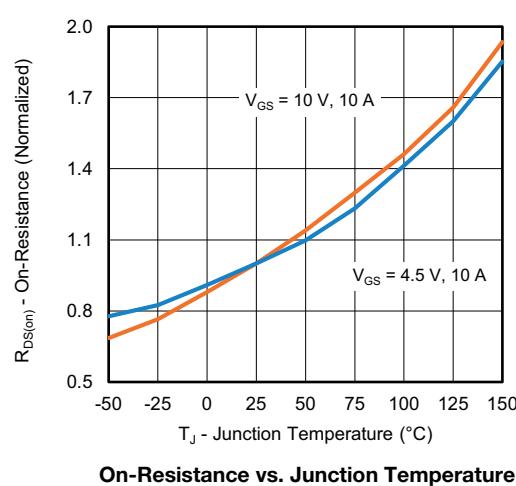
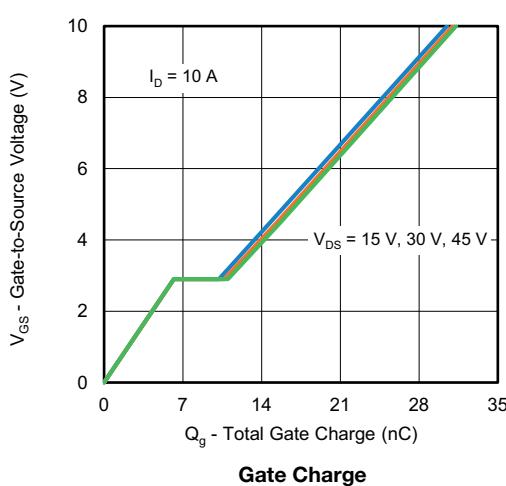
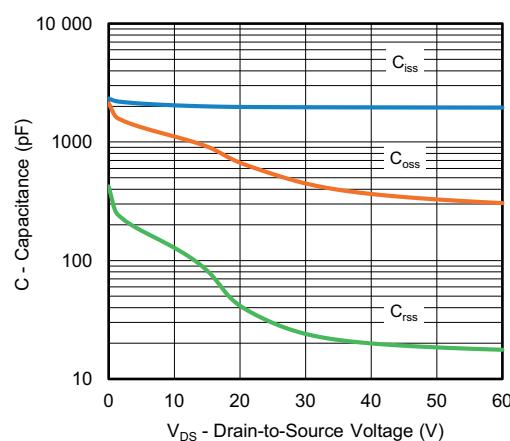
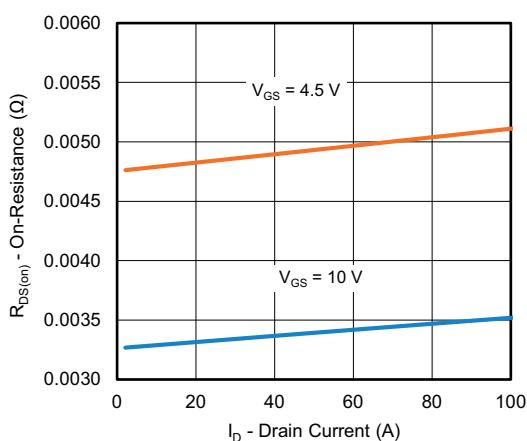
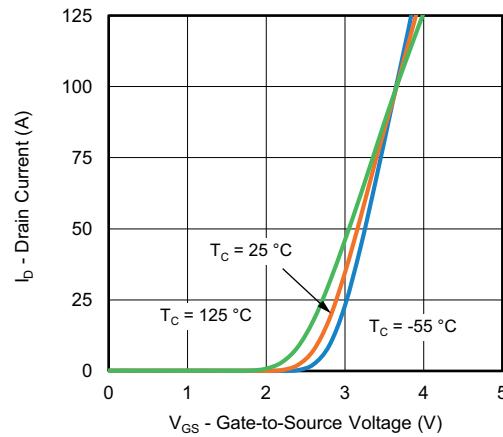
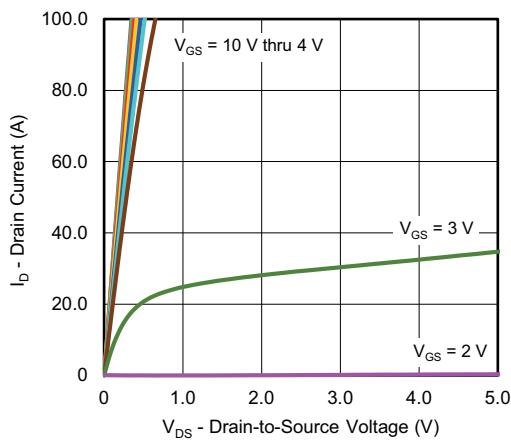
- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 10 s
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- f. Maximum under steady state conditions is 70 °C/W
- g. T_C = 25 °C

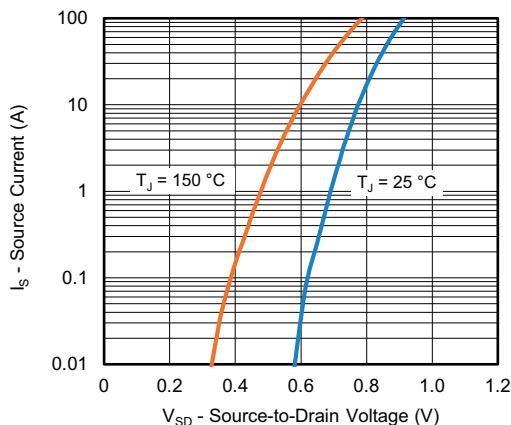
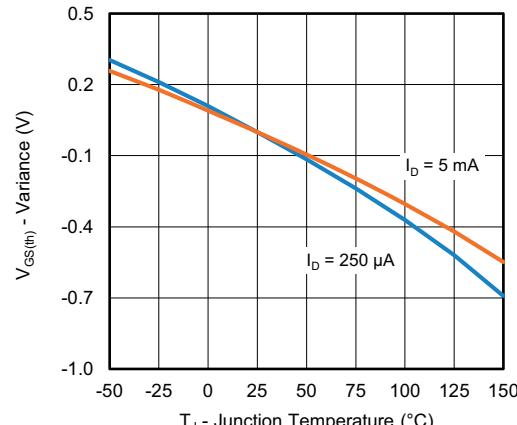
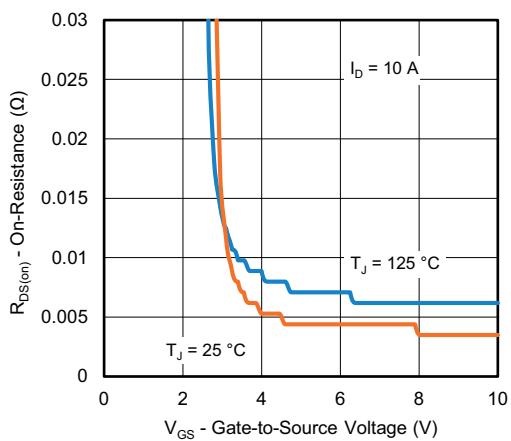
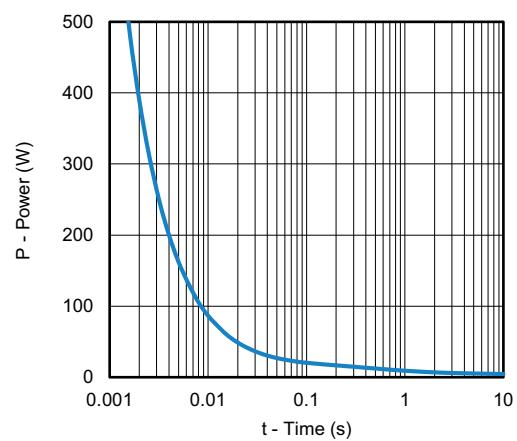
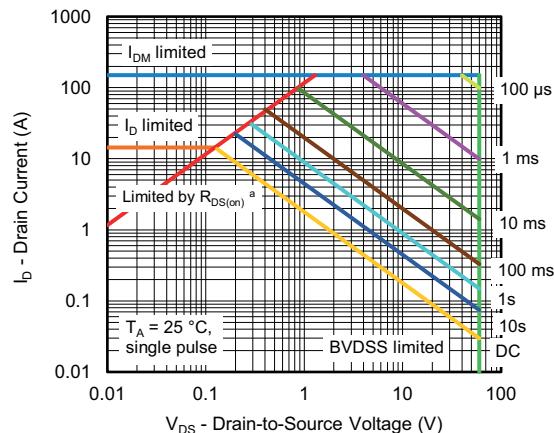
SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 10 \text{ mA}$	-	32	-	$\text{mV}/^\circ\text{C}$
$V_{GS(\text{th})}$ temperature coefficient	$\Delta V_{GS(\text{th})}/T_J$	$I_D = 250 \mu\text{A}$	-	-5	-	
Gate-source threshold voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1	-	2.5	V
Gate-source leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μA
		$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 70^\circ\text{C}$	-	-	15	
On-state drain current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 10 \text{ V}, V_{GS} = 10 \text{ V}$	40	-	-	A
Drain-source on-state resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}$	-	0.0035	0.0044	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	-	0.0049	0.0063	
Forward transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 15 \text{ A}$	-	54	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	1980	-	pF
Output capacitance	C_{oss}		-	447	-	
Reverse transfer capacitance	C_{rss}		-	24	-	
Total gate charge	Q_g	$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	-	31.5	48	nC
			-	15.2	23	
Gate-source charge	Q_{gs}	$V_{DS} = 30 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	-	6.2	-	
Gate-drain charge	Q_{gd}		-	4.5	-	
Output charge	Q_{oss}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$	-	28.3	-	
Gate resistance	R_g	$f = 1 \text{ MHz}$	0.3	0.85	1.5	Ω
Turn-on delay time	$t_{d(\text{on})}$	$V_{DD} = 30 \text{ V}, R_L = 3 \Omega, I_D \geq 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	11	22	ns
Rise time	t_r		-	6	12	
Turn-off delay time	$t_{d(\text{off})}$		-	26	52	
Fall time	t_f		-	6	12	
Turn-on delay time	$t_{d(\text{on})}$	$V_{DD} = 30 \text{ V}, R_L = 3 \Omega, I_D \geq 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	21	42	
Rise time	t_r		-	73	146	
Turn-off delay time	$t_{d(\text{off})}$		-	24	48	
Fall time	t_f		-	10	20	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_C = 25^\circ\text{C}$	-	-	51.8	A
Pulse diode forward current	I_{SM}		-	-	150	
Body diode voltage	V_{SD}	$I_S = 5 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.75	1.1	V
Body diode reverse recovery time	t_{rr}	$I_F = 10 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$	-	30	60	ns
Body diode reverse recovery charge	Q_{rr}		-	20	40	
Reverse recovery fall time	t_a		-	13	-	ns
Reverse recovery rise time	t_b		-	17	-	

Notes

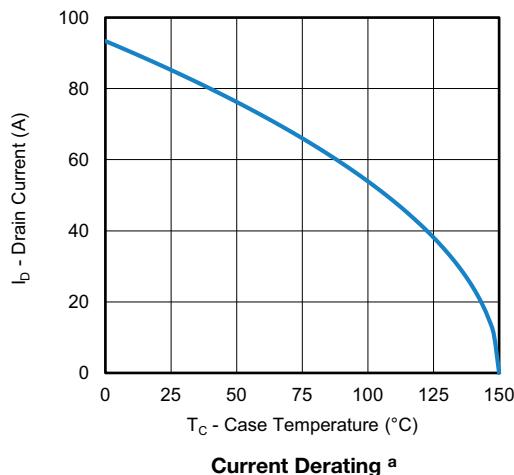
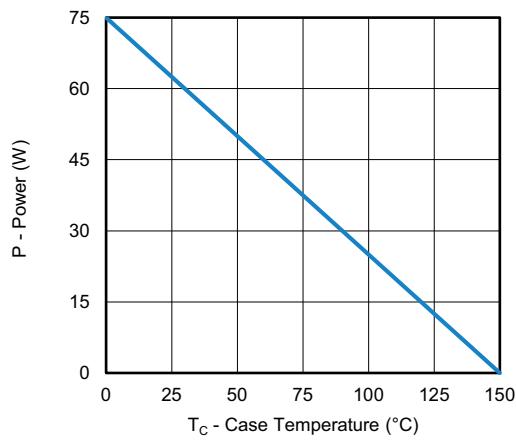
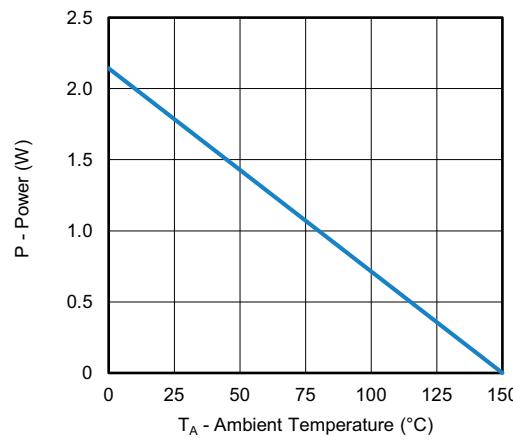
- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

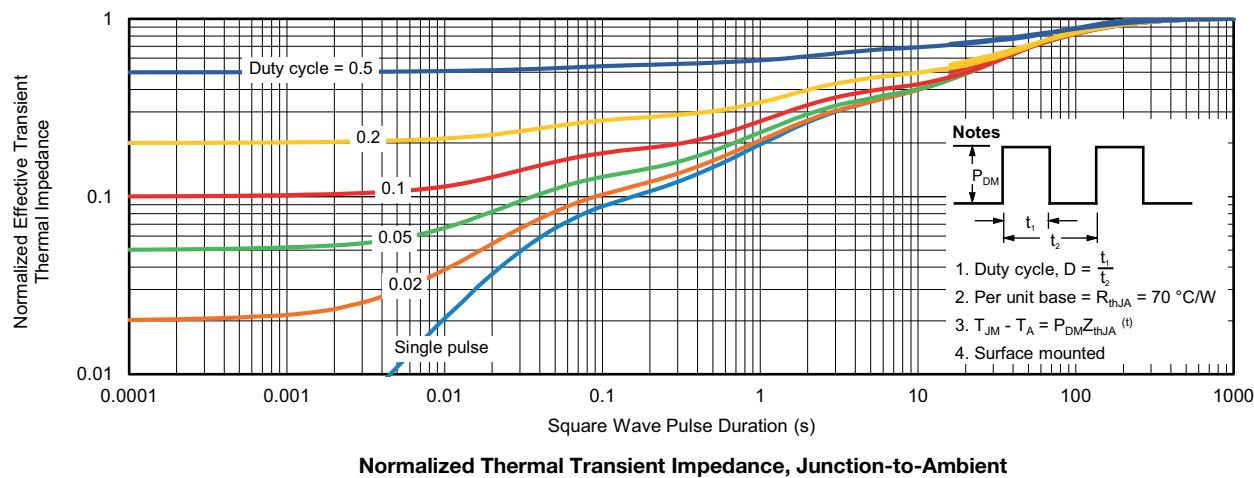
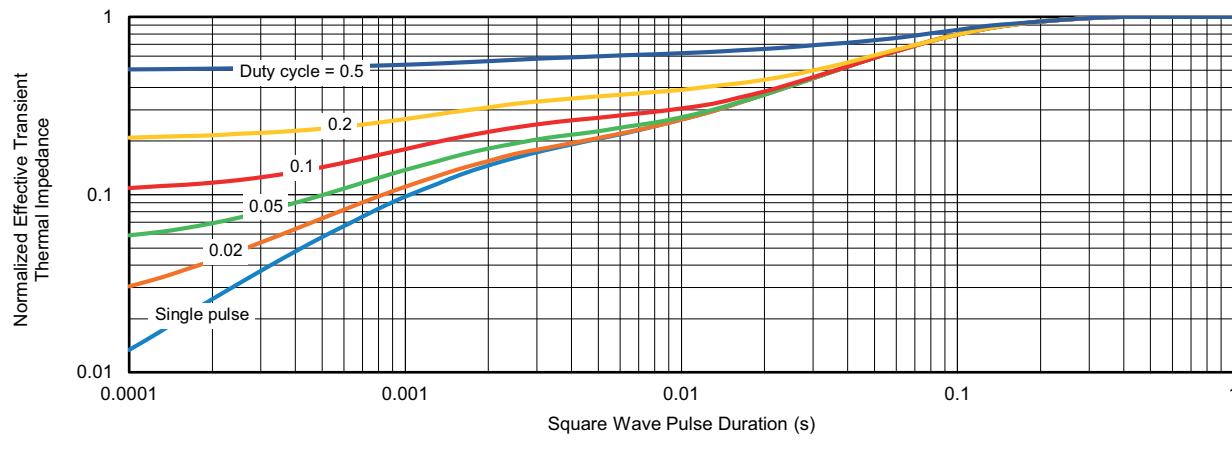
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

Threshold Voltage

On-Resistance vs. Gate-to-Source Voltage

Single Pulse Power, Junction-to-Ambient

Safe Operating Area, Junction-to-Ambient
Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

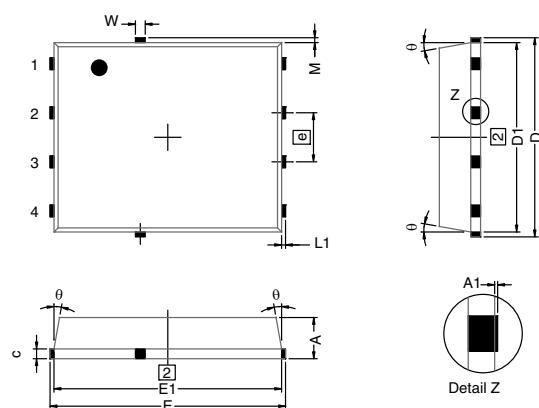
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power, Junction-to-Case

Power, Junction-to-Ambient
Note

- The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

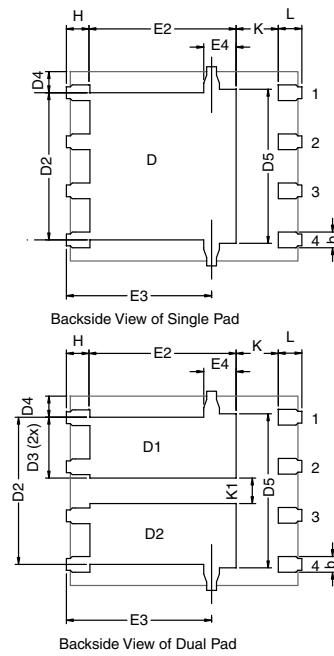
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case

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PowerPAK® SO-8, (Single/Dual)

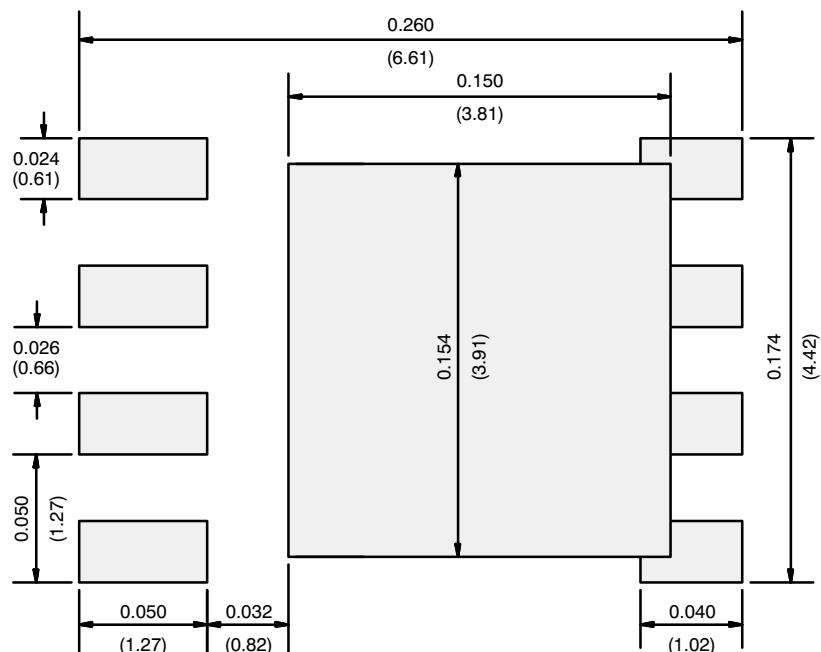

Notes

1. Inch will govern.
- 2 Dimensions exclusive of mold gate burrs.
3. Dimensions exclusive of mold flash and cutting burrs.



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 typ.			0.0225 typ.		
D5	3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4	0.75 typ.			0.030 typ.		
e	1.27 BSC			0.050 BSC		
K	1.27 typ.			0.050 typ.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		

ECN: S17-0173-Rev. L, 13-Feb-17
DWG: 5881

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single

Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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