Protection Devices

TVS (Transient Voltage Suppressor)

ESD102-U1-02ELS

Uni-directional, 3.3 V, 0.4 pF, 0201, RoHS

ESD102-U1-02ELS

Data Sheet

Revision 1.2, 2015-12-14
Final

Power Management & Multimarket

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1 Product Overview

1.1 Features

- ESD / transient protection of high speed data lines according to:
  - **IEC61000-4-2 (ESD): ±20 kV (air / contact)**
  - **IEC61000-4-4 (EFT): ±2.5 kV / 50 A (5/50 ns)**
  - **IEC61000-4-5 (surge): ±3 A (8/20 µs)**
- Uni-directional working voltage: **V_{RWM} = 3.3 V**
- Ultra low capacitance: **C_L = 0.4 pF (typical)**
- Very low clamping voltage: **V_{CL} = 8 V (typical) at I_{PP} = 16 A**
- Low reverse current: **I_R = 1 nA (typical)**
- Very low dynamic resistance: **R_{DYN} = 0.19 Ω (typical)**
- Pb-free (RoHS compliant) and halogen free package, very small form factor 0.62 x 0.32 x 0.31 mm^3

1.2 Application Examples

- USB 3.0, 10/100/1000 Ethernet, Firewire, DVI, HDMI, S-ATA, DisplayPort
- Mobile HDMI Link, MDDI, MIPI, SWP / NFC

1.3 Product Description

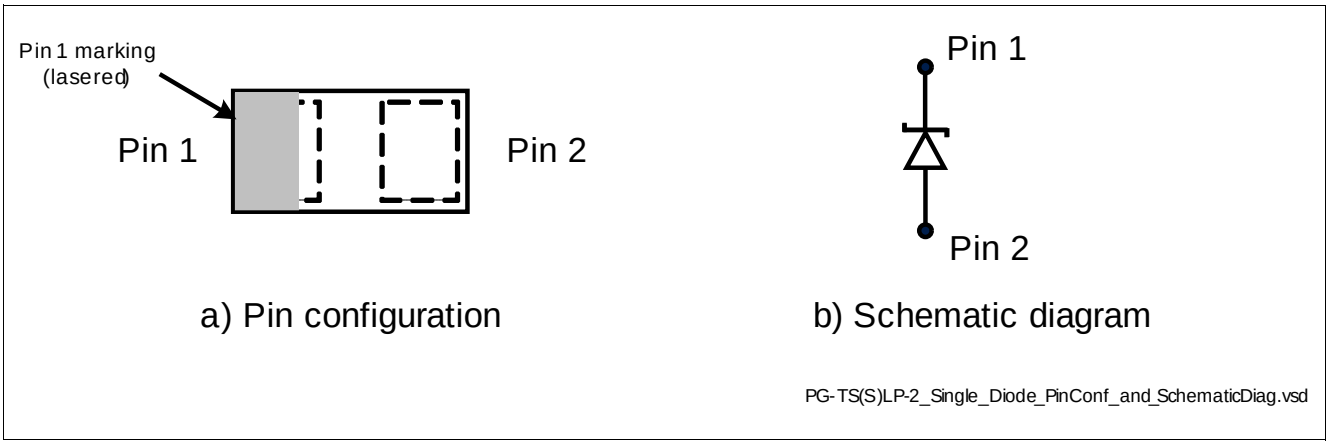

Figure 1 Pin Configuration and Schematic Diagram

Table 1 Part Information

Type	Package	Configuration	Marking code
ESD102-U1-02ELS	TSSLP-2-3	1 line, uni-directional	F

2 Maximum Ratings

Table 2 Maximum Rating *at T_A = 25 °C, unless otherwise specified*

Parameter	Symbol	Values	Unit
ESD air discharge[1)] ESD contact discharge[1)]	V_{ESD}	±20 ±20	kV
Peak pulse current[2)]	I_{PP}	±3	A
Operating temperature	T_{OP}	-55 to 125	°C
Storage temperature	T_{stg}	-65 to 150	°C

1) V_{ESD} according to IEC61000-4-2

2) Stress pulse: 8/20µs current waveform according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3 Electrical Characteristics at T_A = 25 °C, unless otherwise specified

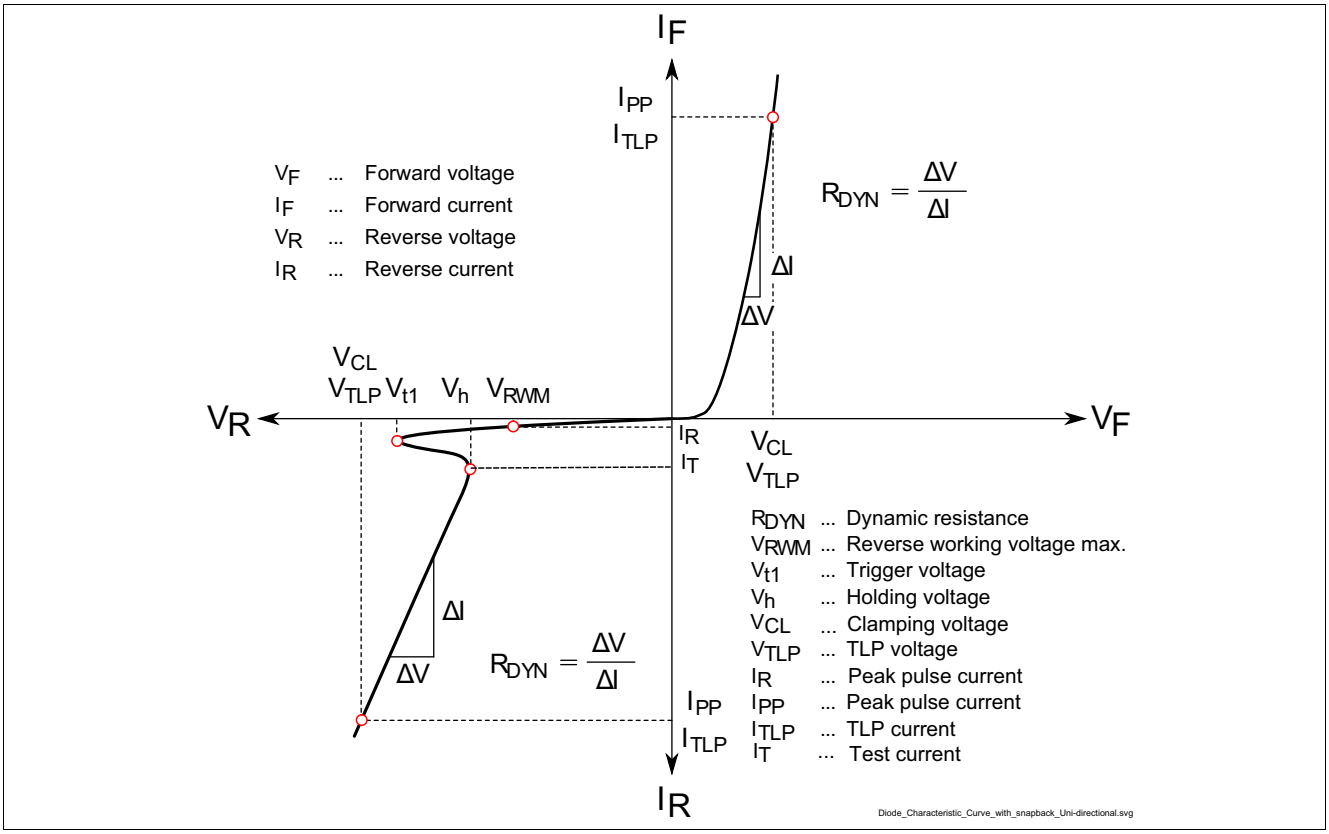

Figure 2 Definitions of Electrical Characteristics

Table 3 DC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	–	–	3.3	V	Pin 1 to Pin 2
Trigger voltage	V_{t1}	–	6.2	–		
Holding voltage	V_h	3.35	4	4.4		Pin 1 to Pin 2, I_R = 10 mA
Reverse current	I_R	–	1	50	nA	V_R = 3.3 V, from Pin 1 to Pin 2

Table 4 AC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	0.4	0.65	pF	V_R = 0 V, f = 1 MHz
		–	0.4	0.65	pF	V_R = 0 V, f = 1 GHz
Series inductance	L_S	–	0.2	–	nH	

Table 5 ESD and Surge Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage[1)]	V_{CL}	–	8	–	V	I_{TLP} = 16 A, t_p = 100 ns, from Pin 1 to Pin 2
		–	11	–		I_{TLP} = 30A, t_p = 100 ns from Pin 1 to Pin 2
Forward clamping voltage[1)]	V_{FC}	–	6	–		I_{TLP} = 16 A, t_p = 100 ns, from Pin 2 to Pin 1
		–	9	–		I_{TLP} = 30 A, t_p = 100 ns, from Pin 2 to Pin 1
Dynamic resistance[1)]	R_{DYN}	–	0.19	–	Ω	t_p = 100 ns from Pin 1 to Pin 2
		–	0.23	–	Ω	t_p = 100 ns from Pin 2 to Pin 1

1) Please refer to Application Note AN210[1]. TLP parameter: Z_0 = 50 Ω , t_p = 100ns, t_r = 0.6 ns.

4 Typical Characteristics at T_A=25°C, unless otherwise specified

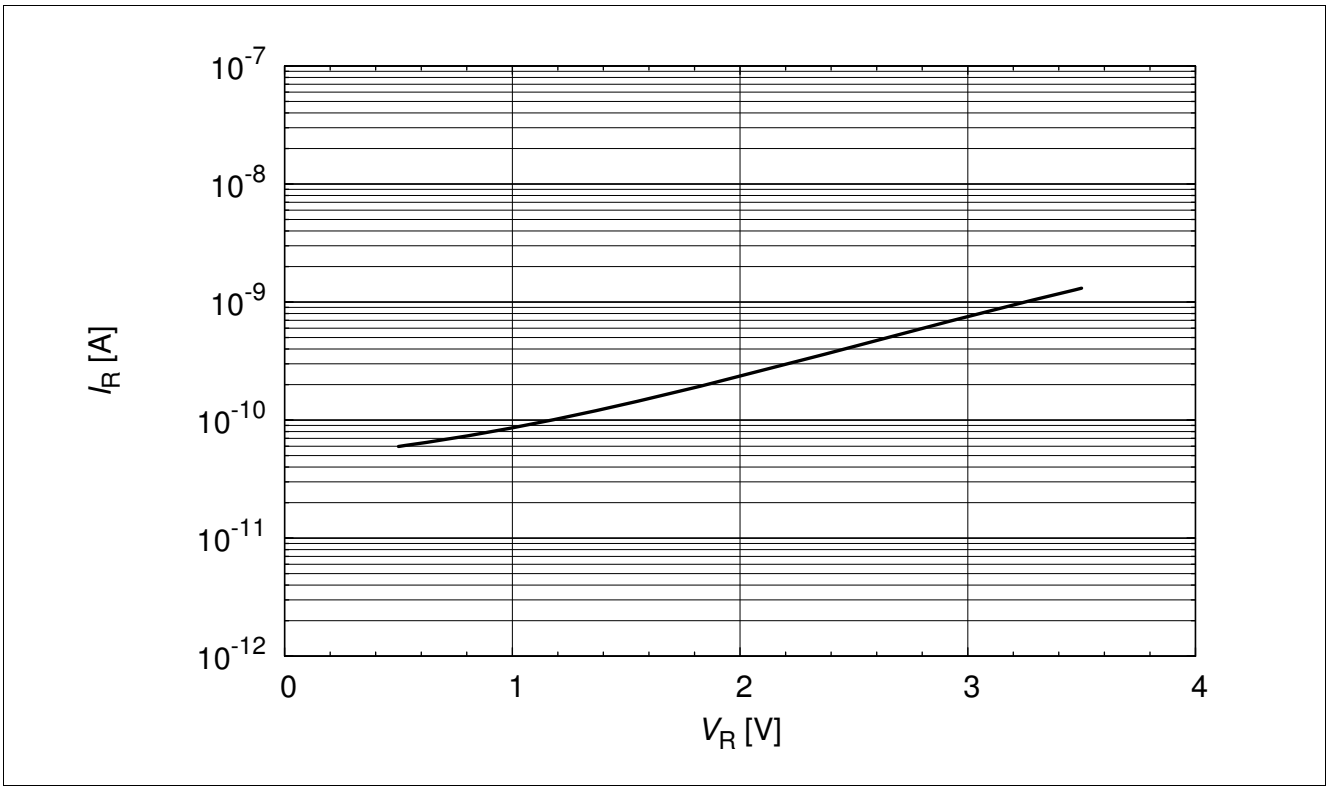

Figure 3 Reverse leakage current, $I_R = (V_R)$

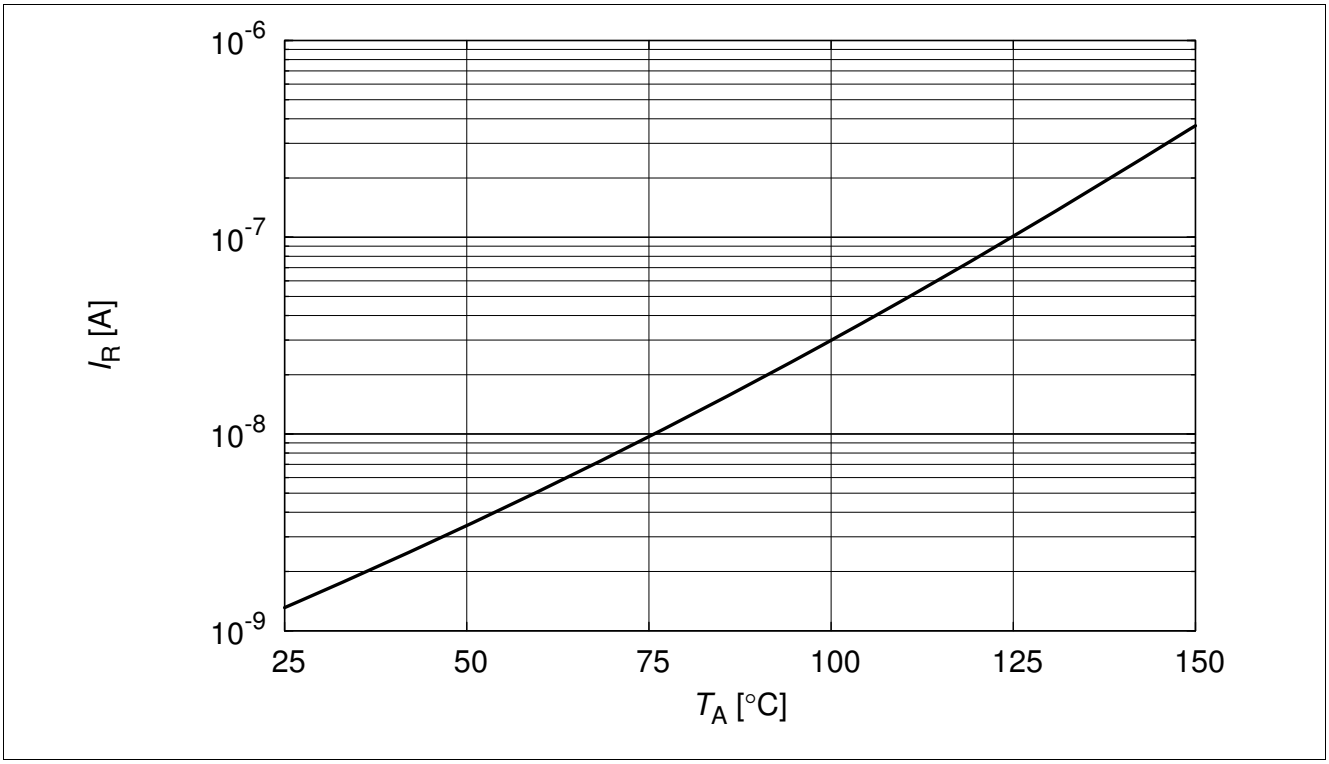

Figure 4 Reverse current $I_R = f(T_A)$, V_R = 3.3 V

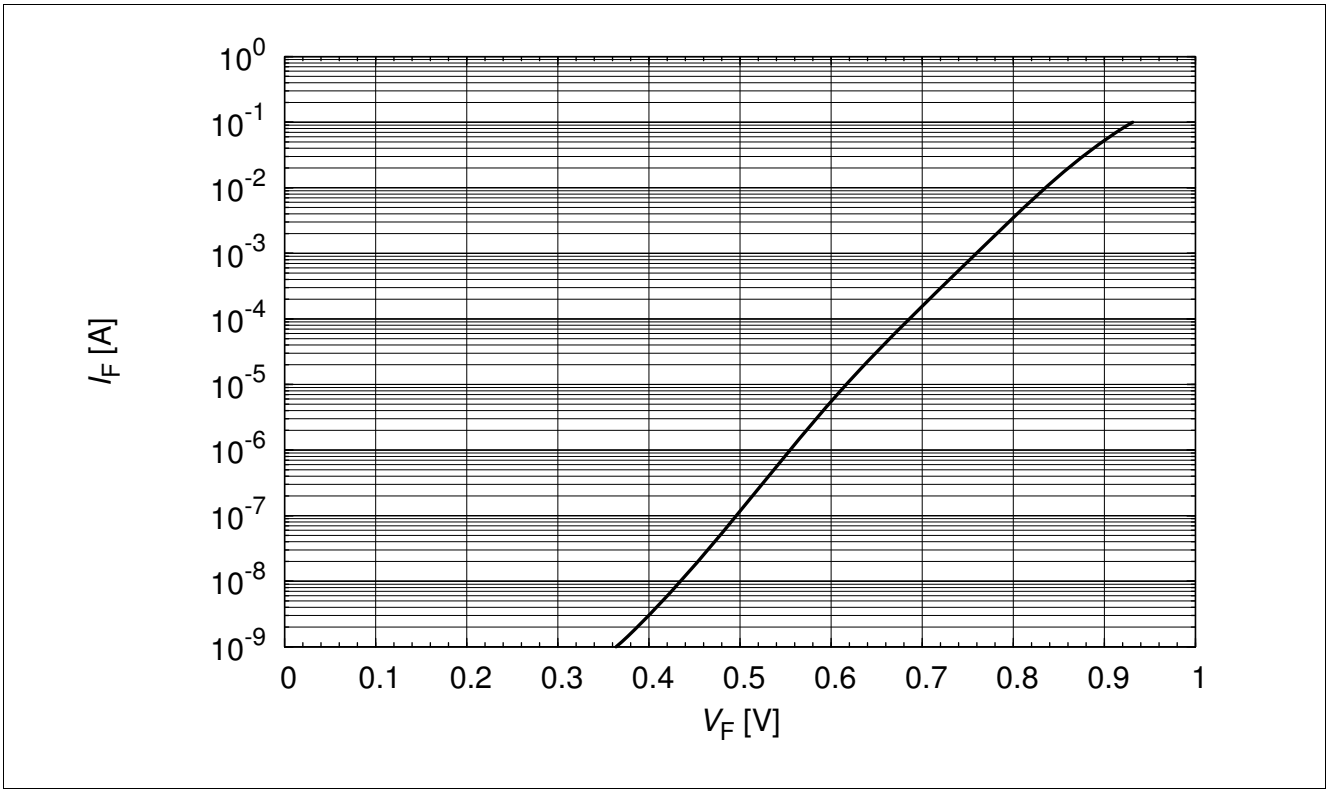

Figure 5 Forward current, $I_F = (V_F)$

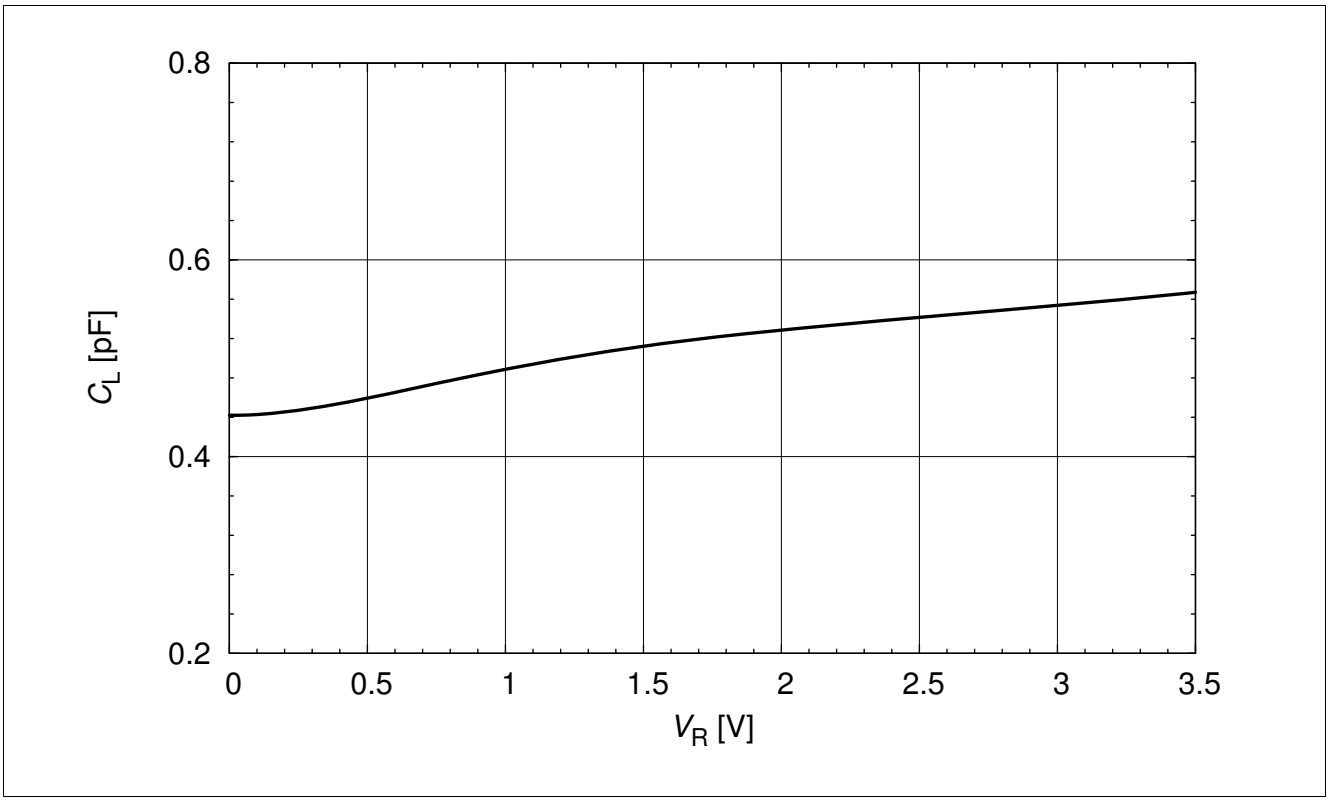

Figure 6 Line capacitance $C_L = f(V_R)$, f = 1MHz, from pin 1 to pin 2

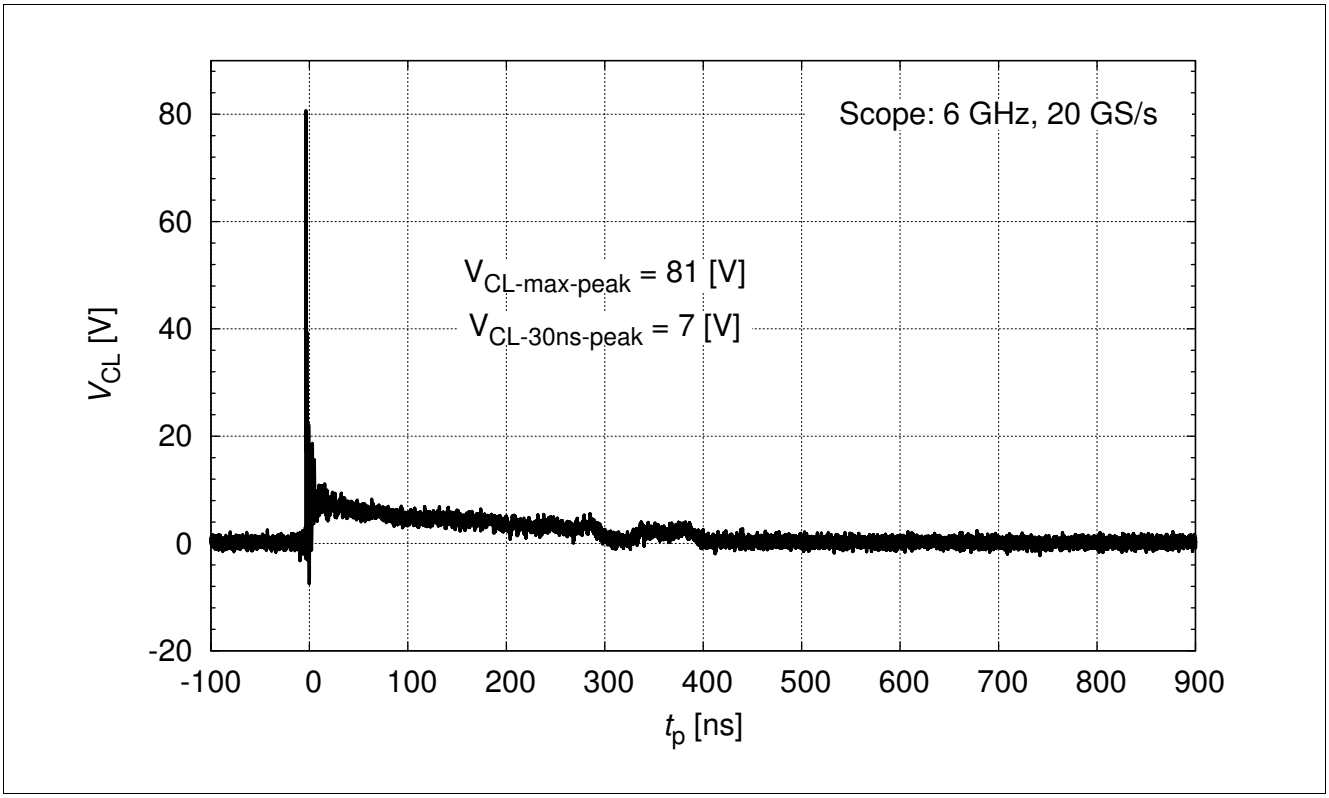

Figure 7 Clamping voltage (ESD): V_{CL} = $f(t)$, 8 kV positive pulse from pin 1 to pin 2

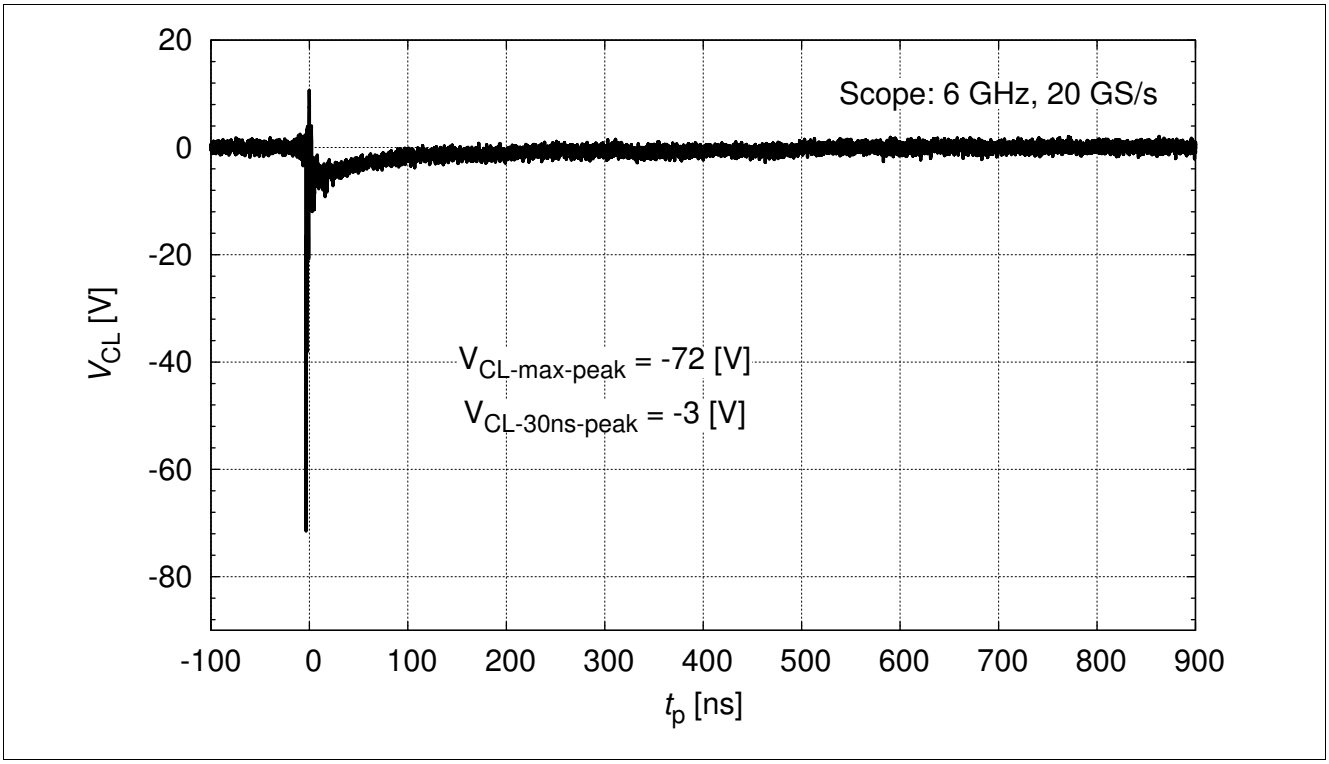

Figure 8 Clamping voltage (ESD): V_{CL} = $f(t)$, 8 kV negative pulse from pin 1 to pin 2

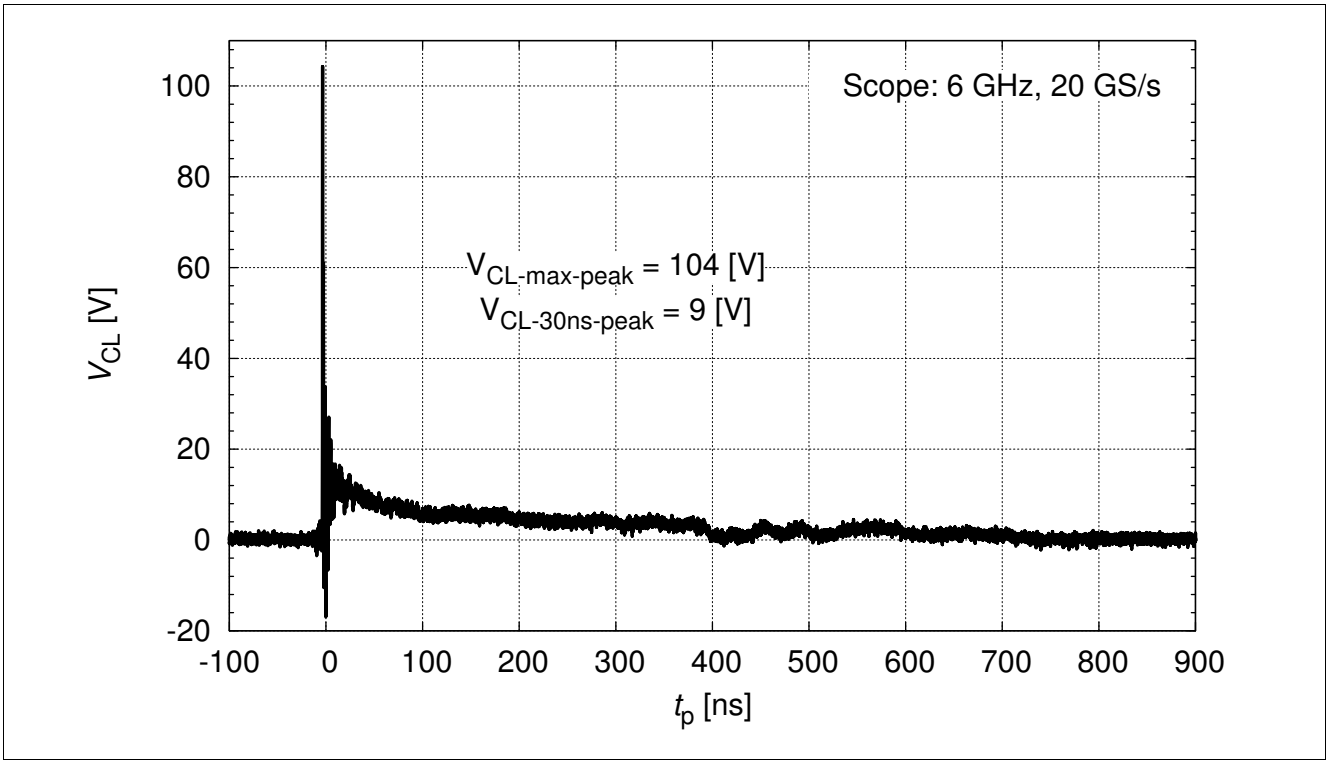

Figure 9 Clamping voltage (ESD): V_{CL} = *f*(*t*), 15 kV positive pulse from pin 1 to pin 2

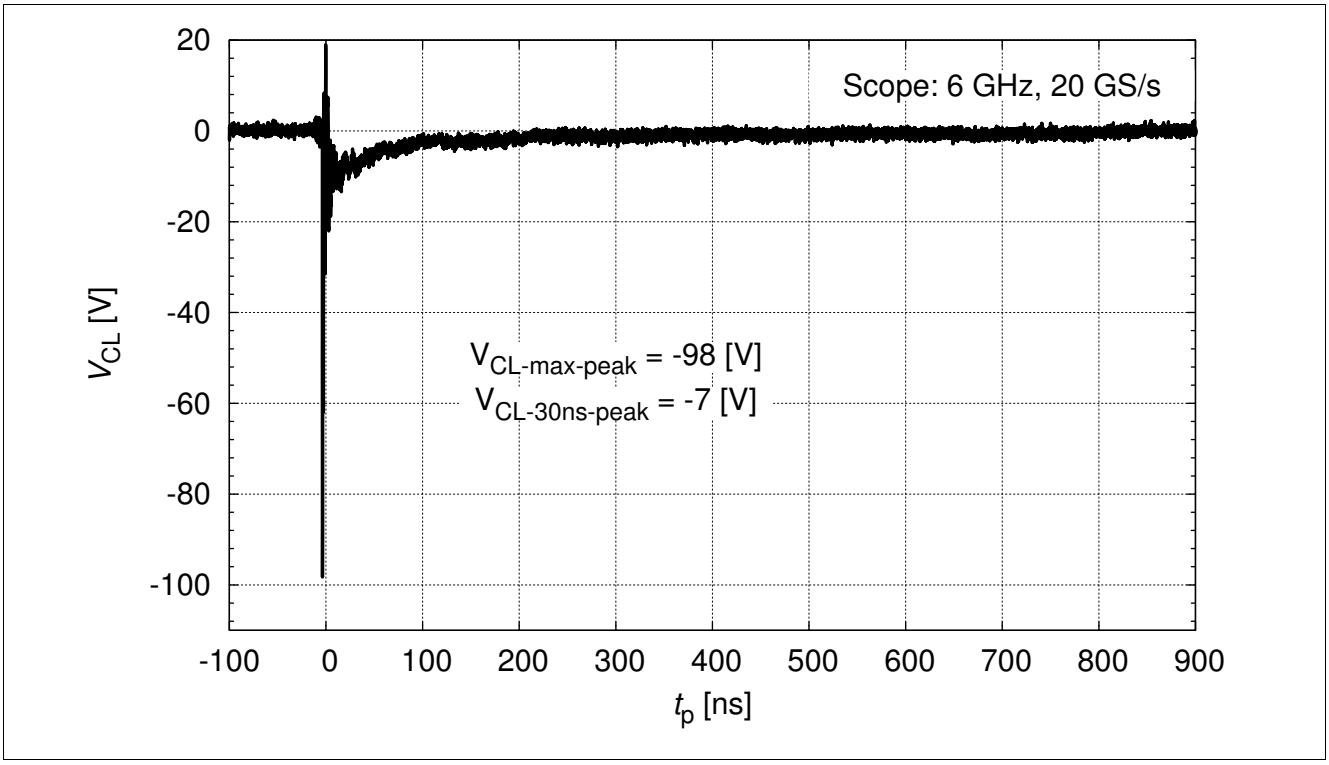

Figure 10 Clamping voltage (ESD): V_{CL} = *f*(*t*), 15 kV negative pulse from pin 1 to pin 2

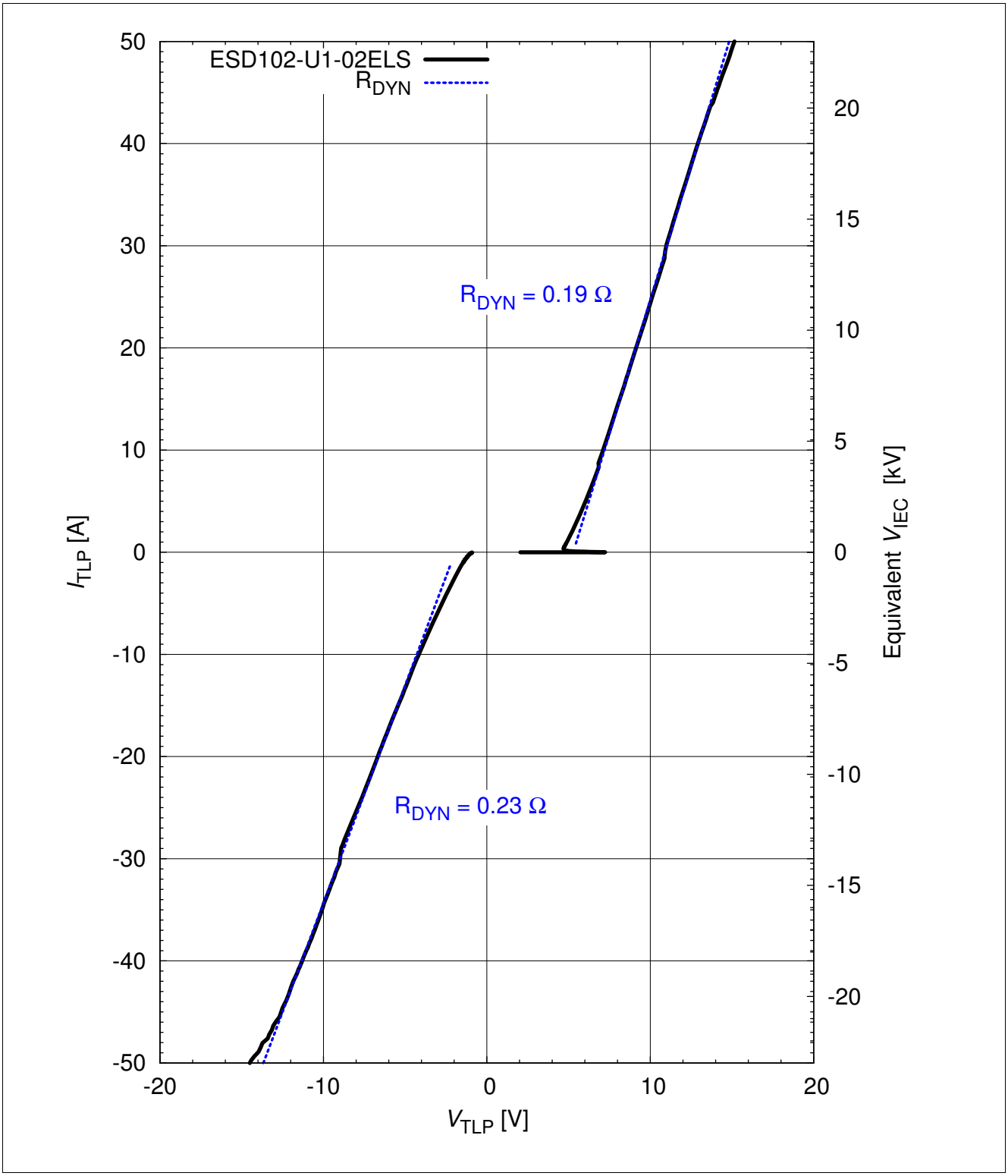

Figure 11 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ [1], pin 1 to pin 2

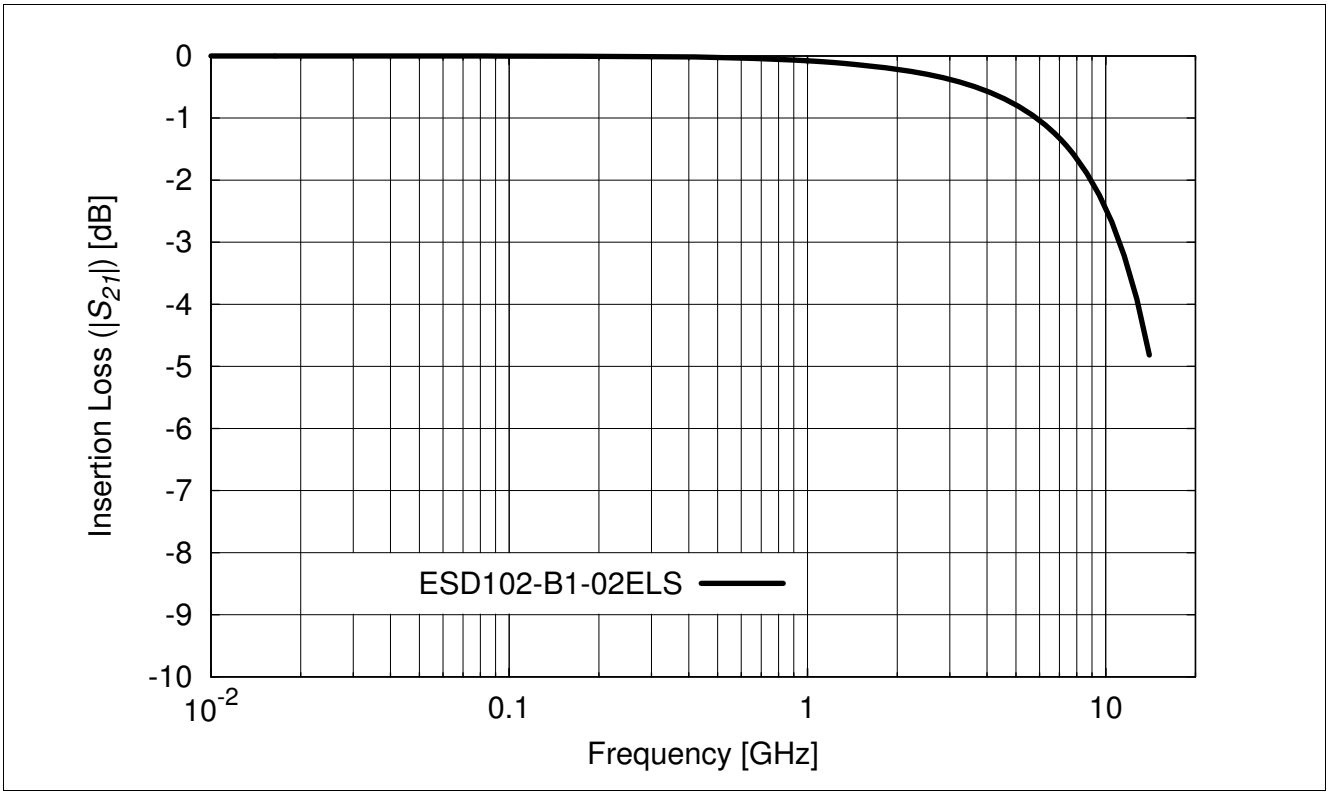

Figure 12 Insertion loss vs. frequency in a 50 Ω system

5 Application Information

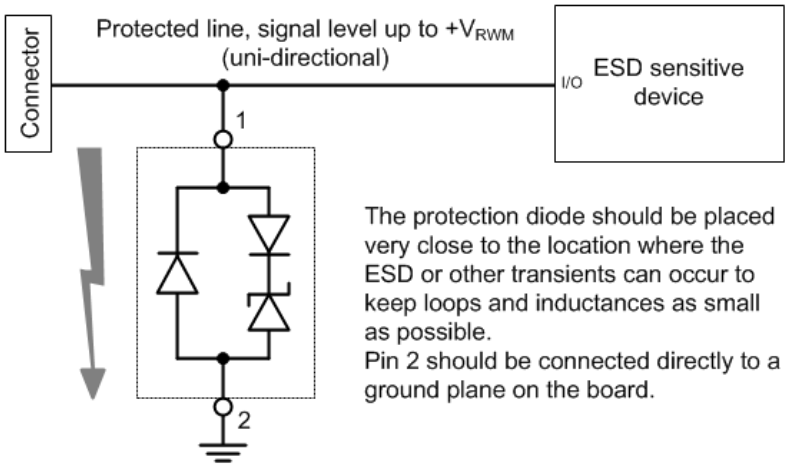

Figure 13 Single line, uni-directional ESD / Transient protection[2]

6 Package Information

6.1 TSSLP-2-3

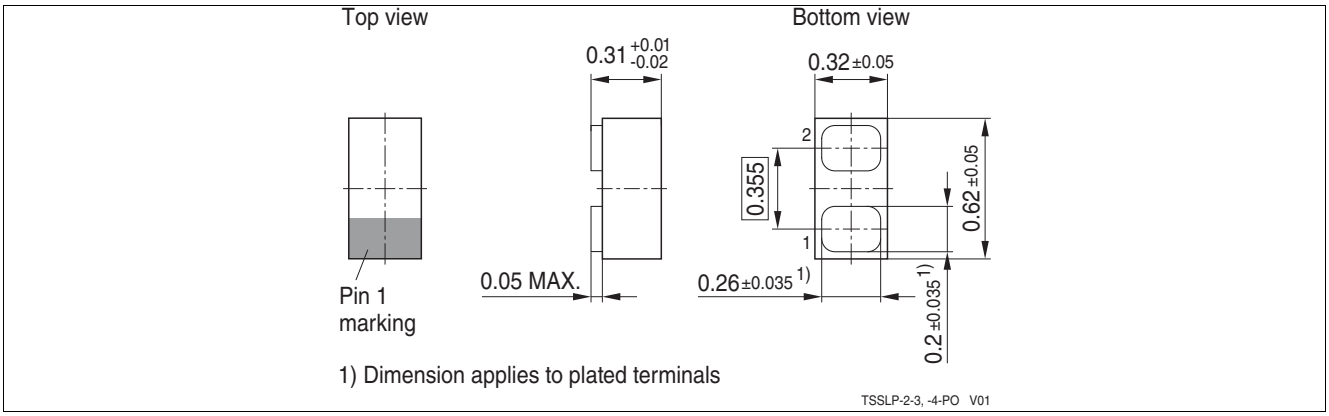

Figure 14 TSSLP-2-3 Package outline (dimension in mm)

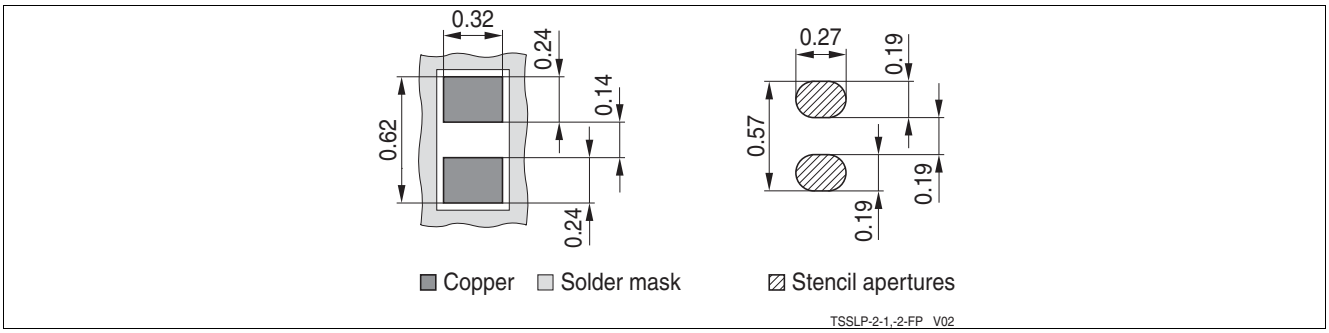

Figure 15 TSSLP-2-3 Footprint (dimension in mm)

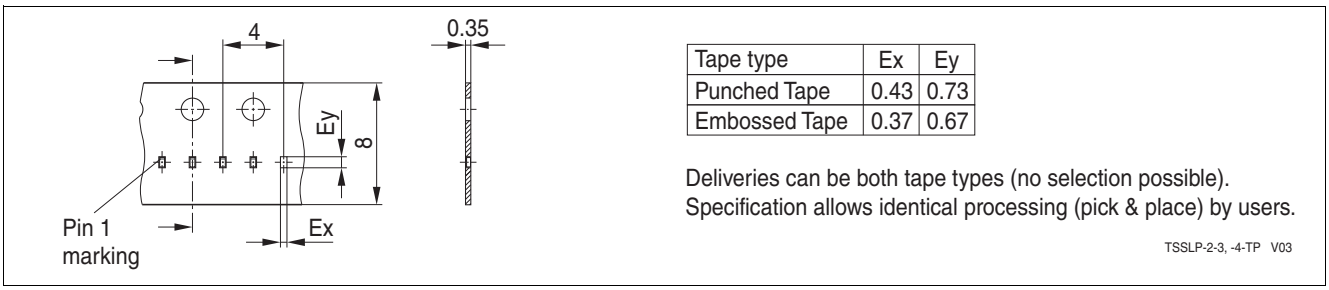

Figure 16 TSSLP-2-3 Packing (dimension in mm)

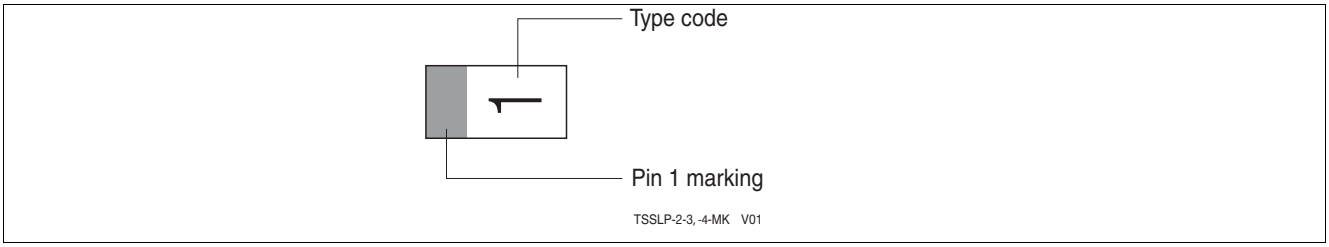

Figure 17 TSSLP-2-3 **Marking example** **Table 1 "Part Information" on Page 3**

References

[1] On-chip ESD protection for integrated circuits, Albert Z. H. Wang, ISBN:0-7923-7647-1

[2] Infineon AG - **Application Note AN210:** Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology

[3] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Package

Revision History: Revision 1.1, 2014-02-13	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.2, 2015-12-14	
All	Layout change

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