

Data Sheet

HMC344ALP3E

FEATURES

- Broadband frequency range: 0.1 GHz to 8 GHz**
- Nonreflective 50 Ω design**
- Low insertion loss: 1.7 dB at 6 GHz**
- High isolation: 36 dB at 6 GHz**
- High input linearity at 250 MHz to 8 GHz**
- P1dB: 28 dBm typical**
- IP3: 44 dBm typical**
- Integrated 2 to 4 line decoder**
- 16-lead, 3 mm × 3 mm LFCSP package**
- ESD HBM rating: 250 V (Class 1A)**

APPLICATIONS

- Broadband telecommunications systems**
- Fiber optics**
- Switched filter banks**
- Wireless Infrastructure below 8 GHz**

GENERAL DESCRIPTION

The HMC344ALP3E is a broadband, nonreflective, single-pole, four-throw (SP4T) switch manufactured using a gallium arsenide (GaAs) metal semiconductor field effect transistor (MESFET) process. This switch offers high isolation, low insertion loss, and on-chip termination of the isolated ports.

The switch operates with a negative supply voltage (V_{EE}) range of -5 V to -3 V and requires two negative logic control voltages.

FUNCTIONAL BLOCK DIAGRAM

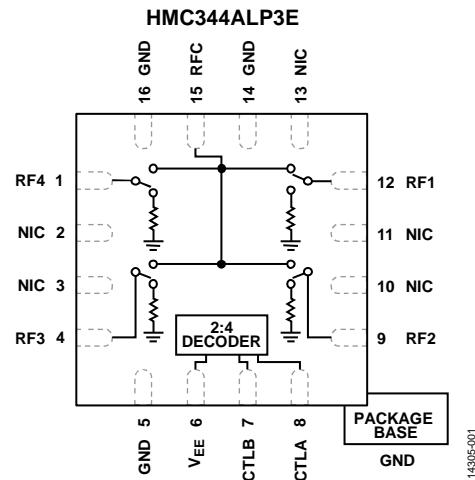


Figure 1.

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The HMC344ALP3E includes an on-chip, binary two-line to four-line decoder that provides logic control from two logic input lines.

The HMC344ALP3E comes in a 3 mm × 3 mm, 16-lead LFCSP package and operates from a 0.1 GHz to 8 GHz frequency range.

Rev. A

Document Feedback

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REVISION HISTORY

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

12/2017—Rev. 01.0316 to Rev. A

Changes to Features Section, Figure 1, and General Description Section.....	1
Changes to Table 1	3
Changes to Table 2	4
Changes to Figure 2, Table 3, and Figure 4	5
Added Figure 3 and Figure 5; Renumbered Sequentially	5
Added Insertion Loss, Return Loss, and Isolation Section and Figure 8	6
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Added Theory of Operation Section	8
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SPECIFICATIONS

$V_{EE} = -3$ V or -5 V, control voltage (V_{CTL}) = 0 V or V_{EE} , case temperature (T_{CASE}) = 25°C , $50\ \Omega$ system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1	8		GHz
INSERTION LOSS						
Between RFC and RF1 to RF4 (On)		0.1 GHz to 2 GHz 2 GHz to 4 GHz 4 GHz to 6 GHz 6 GHz to 8 GHz		1.4 1.4 1.7 2.1	2.0 2.0 2.2 2.5	dB dB dB dB
ISOLATION						
Between RFC and RF1 to RF4 (Off)		0.1 GHz to 2 GHz 2 GHz to 4 GHz 4 GHz to 6 GHz 6 GHz to 8 GHz	39 33 32 28	43 37 36 32		dB dB dB dB
RETURN LOSS						
RFC and RF1 to RF4 (On)		0.1 GHz to 2 GHz 2 GHz to 4 GHz 4 GHz to 6 GHz 6 GHz to 8 GHz 0.1 GHz to 8 GHz		12 12 11 6 11	16 16 16 11 16	dB dB dB dB dB
RF1 to RF4 (Off)						
SWITCHING						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of radio frequency (RF) output		35		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		75		ns
INPUT LINEARITY ¹						
1 dB Power Compression	P1dB	$f = 250$ MHz to 8 GHz $V_{EE} = -5$ V $V_{EE} = -3$ V	23	28		dBm dBm
Third-Order Intercept	IP3	10 dBm per tone, 1 MHz spacing $V_{EE} = -5$ V $V_{EE} = -3$ V	40	44		dBm dBm
SUPPLY						
Voltage	V_{EE}	V_{EE} pin	-5		-3	V
Current	I_{EE}			2.5	6	mA
DIGITAL CONTROL INPUTS						
Voltage	V_{CTL}	CTLA and CTLB pins				
Low	V_{INL}	$V_{EE} = -5$ V $V_{EE} = -3$ V	-3	0		V
High	V_{INH}	$V_{EE} = -5$ V $V_{EE} = -3$ V	-1	0		V
Current	I_{CTL}		-5	-4.2		V
Low	I_{INL}		-3	-2.2		V
High	I_{INH}			40	0.10	μA
						μA

¹ Input linearity performance degrades at frequencies less than 250 MHz.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2.

Parameter	Rating
Negative Supply Voltage (V_{EE})	-7 V
Digital Control Input Voltage Range	$V_{EE} - 0.5$ V to +1 V
RF Input Power $f = 250$ MHz to 8 GHz, $T_{CASE} = 85^\circ\text{C}$ $V_{EE} = -5$ V	
Through Path	28 dBm
Terminated Path	26.5 dBm
Hot Switching	22 dBm
$V_{EE} = -3$ V	
Through Path	25 dBm
Terminated Path	23.5 dBm
Hot Switching	19 dBm
Temperature	
Junction, T_J	150°C
Storage	-65°C to +150°C
Reflow	260°C
Junction to Case Thermal Resistance, θ_{JC}	
Through Path	107°C/W
Terminated Path	137°C/W
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	250 V (Class 1A)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

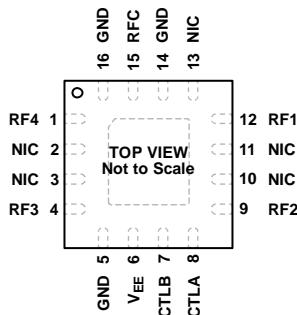
ESD CAUTION



ESD (electrostatic discharge) sensitive device.
Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

HMC344ALP3E



NOTES

1. NIC = NOT INTERNALLY CONNECTED. THESE PINS ARE NOT CONNECTED INTERNALLY; HOWEVER, ALL DATA SHOWN IN THIS DATA SHEET IS MEASURED WHEN THESE PINS ARE CONNECTED TO THE RF/DC GROUND EXTERNALLY.
2. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO THE RF/DC GROUND OF THE PCB.

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Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RF4	RF4 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential does not equal 0 V dc.
2, 3, 10, 11, 13	NIC	Not Internally Connected. These pins are not connected internally; however, all data shown in this data sheet is measured when these pins are connected to the RF/dc ground externally.
4	RF3	RF3 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential does not equal 0 V dc.
5, 14, 16	GND	Ground. These pins connect to the RF/dc ground of the PCB.
6	V _{EE}	Negative Supply Voltage Pin.
7	CTLB	Control Input 2 Pin. See Table 4 for the control voltage truth table.
8	CTLA	Control Input 1 Pin. See Table 4 for the control voltage truth table.
9	RF2	RF2 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential does not equal 0 V dc.
12	RF1	RF1 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential does not equal 0 V dc.
15	RFC	RF Common Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential does not equal 0 V dc.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/dc ground of the PCB.

INTERFACE SCHEMATICS

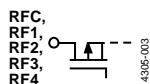


Figure 3. RFC and RF1 to RF4 Interface Schematic

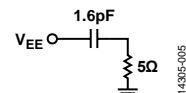
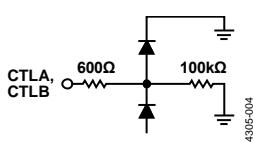
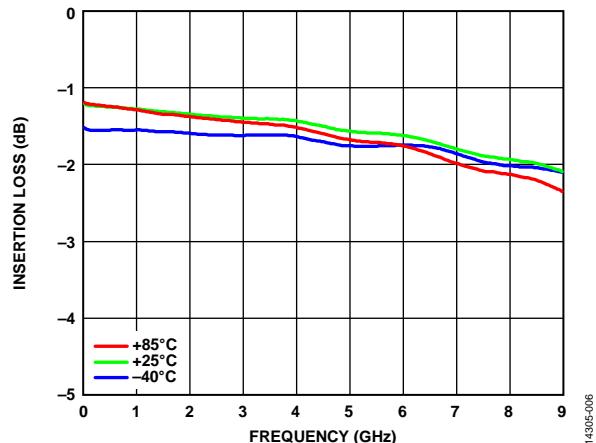
Figure 5. V_{EE} Interface Schematic

Figure 4. CTLA and CTLB Interface Schematic

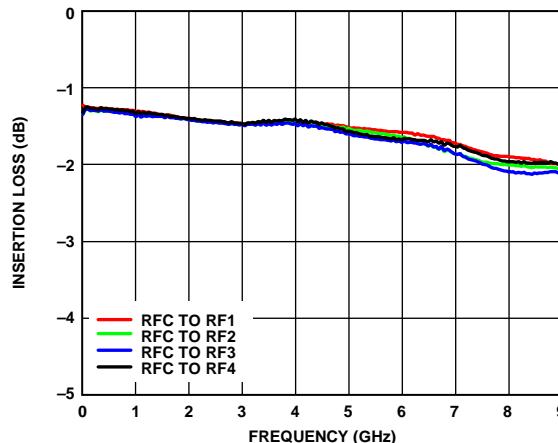
TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION



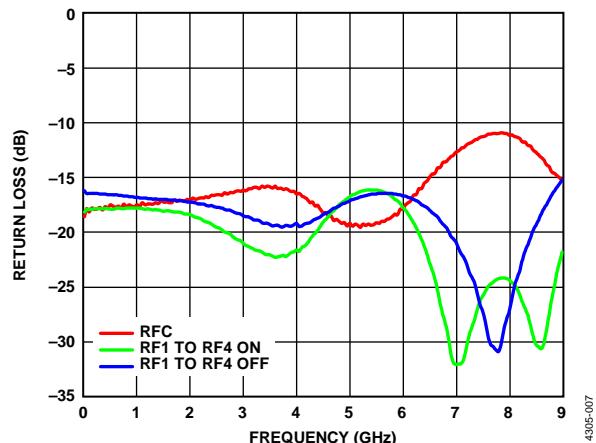
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Figure 6. Insertion Loss vs. Frequency at Various Temperatures, Between RFC and RF1



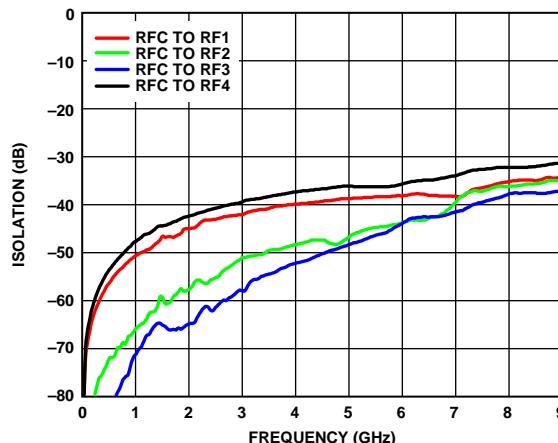
14305-008

Figure 8. Insertion Loss vs. Frequency, Between RFC and RFx



14305-007

Figure 7. Return Loss vs. Frequency for RFC, RF1 to RF4 On, and RF1 to RF4 Off



14305-009

Figure 9. Isolation vs. Frequency, Between RFC and RFx

INPUT POWER COMPRESSION AND INPUT IP3

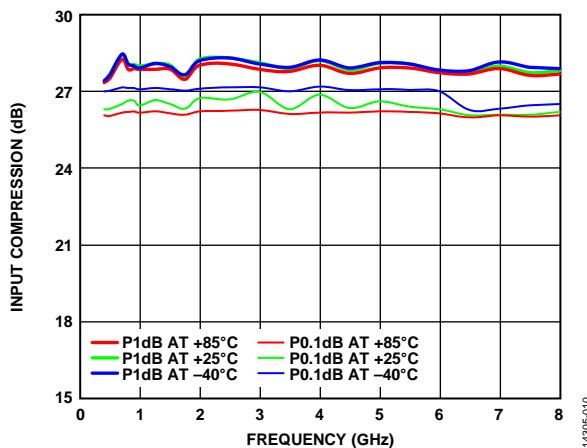


Figure 10. Input Compression vs. Frequency at Various Temperatures,
 $V_{EE} = -5 \text{ V}$

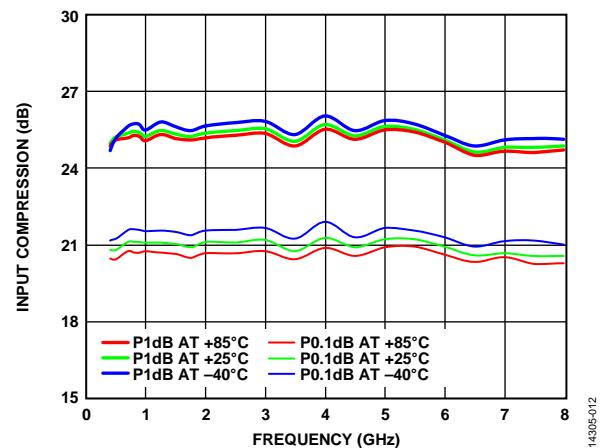


Figure 12. Input Compression vs. Frequency at Various Temperatures,
 $V_{EE} = -3 \text{ V}$

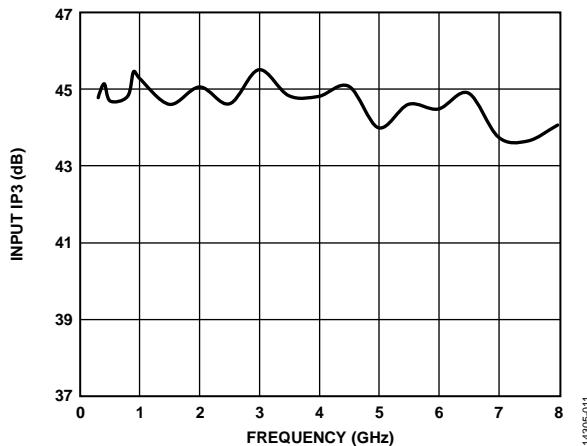


Figure 11. Input IP3 vs. Frequency at Room Temperature,
 $V_{EE} = -5 \text{ V}$

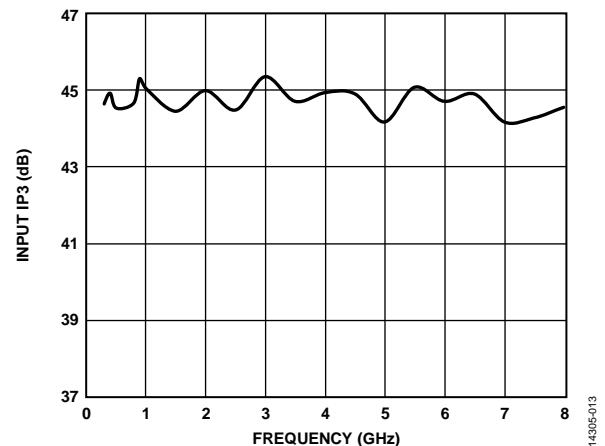


Figure 13. Input IP3 vs. Frequency at Room Temperature,
 $V_{EE} = -3 \text{ V}$

THEORY OF OPERATION

The HMC344ALP3E requires a negative supply voltage at the V_{EE} pin and two logic control inputs at the CTLA and CTLB pins to control the state of the RF paths.

Depending on the logic level applied to the CTLA pin and the CTLB pin, one RF path is in the insertion loss state, while the other three paths are in an isolation state (see Table 4). The insertion loss path conducts the RF signal between the RF throw pin and the RF common pin, and the isolation paths provide high loss between the RF throw pins terminated to internal $50\ \Omega$ resistors and the insertion loss path.

The ideal power-up sequence is as follows:

1. Ground to the die bottom.
2. Power up V_{EE} .
3. Power up the digital control inputs. The relative order of the logic control inputs is not important. However, powering the digital control inputs before the V_{EE} supply can inadvertently become forward-biased and damage the internal ESD protection structures.
4. Apply an RF input signal. The design is bidirectional; the RF input signal can be applied to the RFC pin while the RF throw pins are the outputs, or the RF input signal can be applied to the RF throw pins, while the RFC pin is the output. All of the RF pins are dc-coupled to 0 V, and no dc blocking is required at the RF pins when the RF line potential equals 0 V.

The power-down sequence is the reverse of the power-up sequence.

Table 4. Control Voltage Truth Table

Digital Control Input		RF Paths			
CTLA	CTLB	RFC to RF1	RFC to RF2	RFC to RF3	RFC to RF4
High	High	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
Low	High	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
High	Low	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	Low	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)

APPLICATIONS INFORMATION

EVALUATION BOARD

The EV1HMC344ALP3 is a 4-layer evaluation board. Each copper layer is 0.5 oz (0.7 mil) and separated by dielectric materials. Figure 14 shows the stack up for this evaluation board.

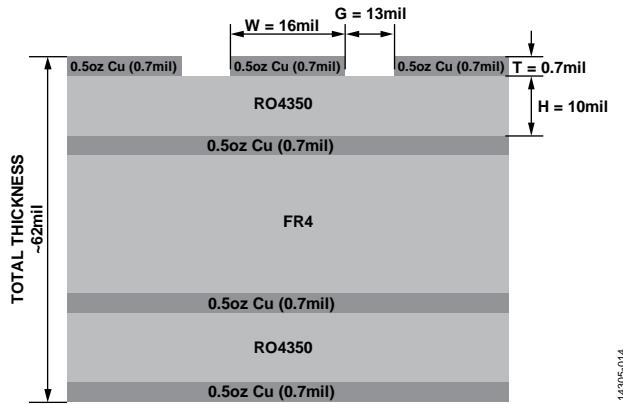


Figure 14. EV1HMC344ALP3 Evaluation Board (Cross Sectional View)

All RF and dc traces are routed on the top copper layer, and the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. The top dielectric material is a 10 mil Rogers RO4350. The middle and bottom dielectric materials provide mechanical strength. The overall board thickness is approximately 62 mil allowing the Subminiature Version A (SMA) launchers to be connected at the board edges.

The RF transmission lines were designed using a coplanar waveguide (CPWG) model, with a trace width of 16 mil and a ground clearance of 13 mil for a characteristic impedance of $50\ \Omega$. For optimal RF and thermal grounding, arrange as many plated through vias as possible around the transmission lines and under the exposed pad of the package.

Figure 15 is the external interface circuit recommended for transistor to transistor level (TTL) compatible control of the negative voltage controlled switches.

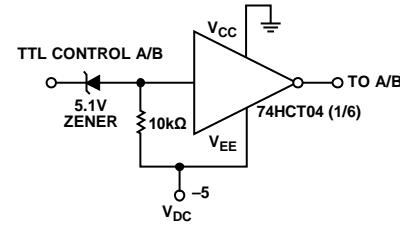


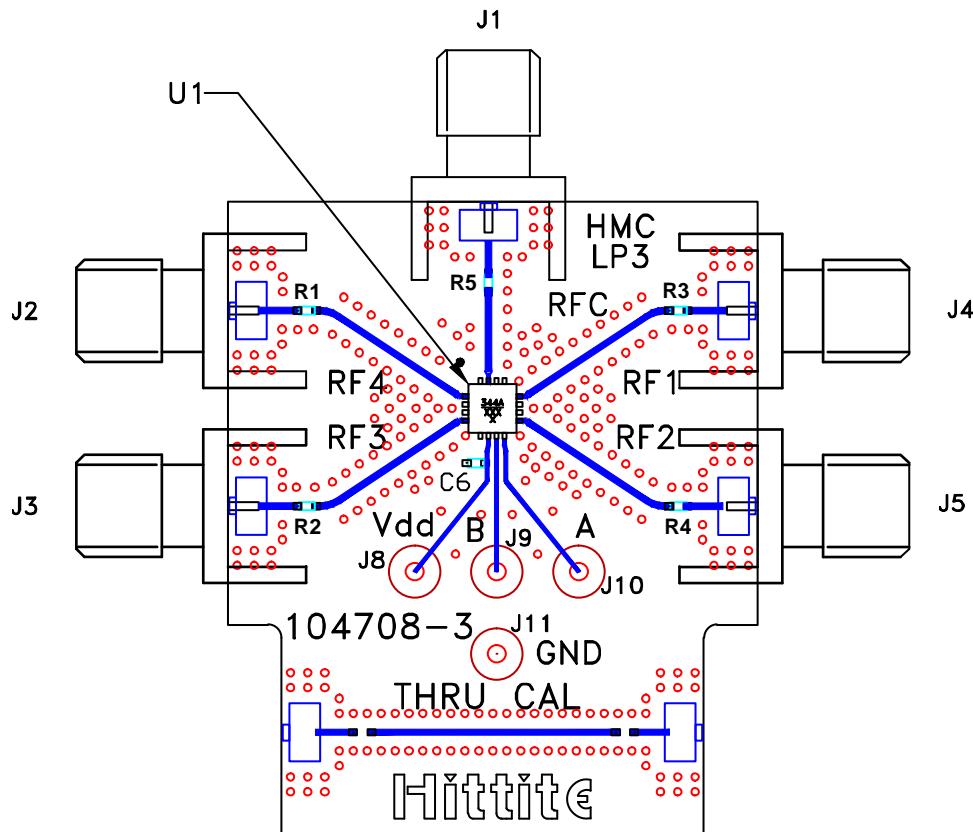
Figure 15. TTL Interface Circuit

Figure 16 shows the layout of the EV1HMC344ALP3 evaluation board with component placement. The power supply port is connected to the V_{EE} test point, J8. Control voltages, CTLA and CTLB, are connected to the A and B test points, J9 and J10. The ground reference is connected to the GND test point, J11. The NIC pins are connected to the PCB ground to maximize isolation. Use a 1 nF bypass capacitor on the supply trace, V_{EE} , to filter high frequency noise.

The RF input and output ports (RFC, RF1 to RF4) connect through $50\ \Omega$ transmission lines to the SMA launchers, J1 to J5. These SMA launchers are soldered onto the board. For connection to the RF pins, R1 to R5 are populated with $0\ \Omega$ resistors. A through calibration line connects the unpopulated J6 and J7 launchers. This transmission line estimates the loss of the PCB over the environmental conditions being evaluated, as shown in Figure 17. Table 5 describes the evaluation board components.

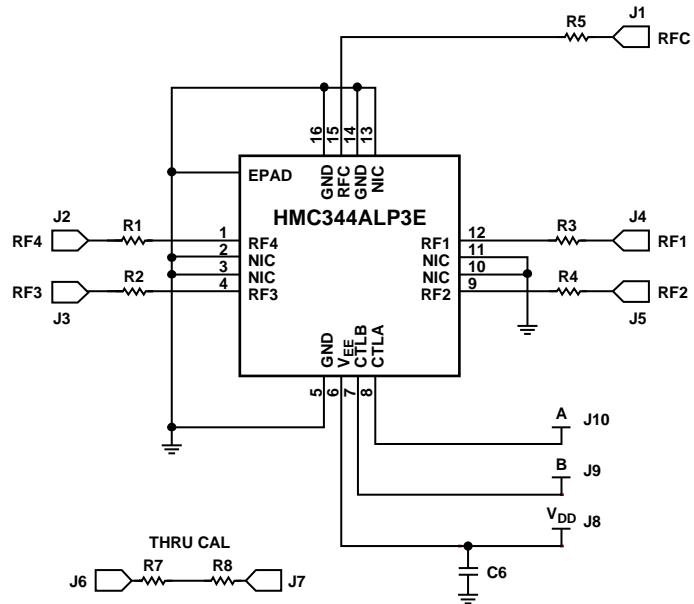
Table 5. Evaluation Board Components

Component	Default Value	Description
R1 to R5	$0\ \Omega$	Resistors, R0402 package
C6	1 nF	Capacitor, C0402 package
R7, R8	Do not insert	Resistors, R0402 package
J1 to J5	Not applicable	PCB mount and SMA launchers
J6, J7	Do not insert	PCB mount and SMA launchers
J8 to J11	Not applicable	DC pins
U1	HMC344ALP3E	SP4T switch
PCB	104708-3	Evaluation PCB



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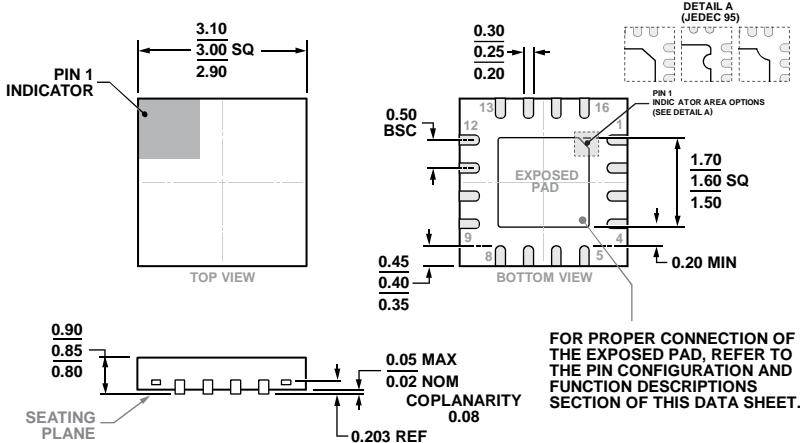
Figure 16. EV1HMC344ALP3 Evaluation Board Component Placement



14305-018

Figure 17. EV1HMC344ALP3 Evaluation Board Schematic

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VEED-4

Figure 18. 16-Lead Lead Frame Chip Scale Package [LFCSP]

3 mm x 3 mm Body and 0.85 mm Package Height

(CP-16-50)

Dimensions shown in millimeters

11-22-2016A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
HMC344ALP3E	-40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-50
HMC344ALP3ETR	-40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-50
EV1HMC344ALP3		Evaluation Board	

¹ All models are RoHS compliant parts.