

# NP36P06SLG

-60V – -36A – P-channel Power MOS FET

R07DS1510EJ0100

Rev.1.00

Application : Automotive

May. 27, 2022

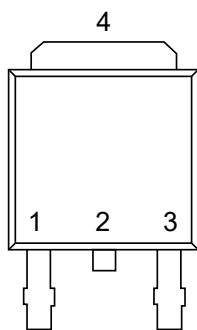
## Description

This product is P-channel MOS Field Effect Transistor designed for high current switching applications.

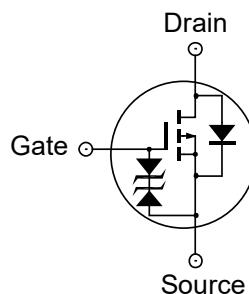
## Features

- Super low on-state resistance :  $R_{DS(on)} = 30 \text{ m}\Omega \text{ Max.}$  (  $V_{GS} = -10 \text{ V}$ ,  $I_D = -18 \text{ A}$  )  
 $R_{DS(on)} = 40 \text{ m}\Omega \text{ Max.}$  (  $V_{GS} = -4.5 \text{ V}$ ,  $I_D = -18 \text{ A}$  )
- Low input capacitance :  $C_{iss} = 3200 \text{ pF Typ.}$
- Built-in gate protection diode
- Designed for automotive application and AEC-Q101 qualified.
- Pb-free (This product does not contain Pb in the external electrode)

## Outline



MP-3ZK (TO-252)



Equivalent circuit

## Absolute Maximum Ratings

( $T_a=25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	-60	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\mp 20$	V
Drain Current (DC) ( $T_c = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\mp 36$	A
Drain Current (pulse)	$I_{D(pulse)}$ Notes <sup>1</sup>	$\mp 108$	A
Total Power Dissipation ( $T_c = 25^\circ\text{C}$ )	$P_{T1}$	56	W
Total Power Dissipation ( $T_a = 25^\circ\text{C}$ )	$P_{T2}$	1.2	W
Channel Temperature	$T_{ch}$	175	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to 175	$^\circ\text{C}$
Single Avalanche Current	$I_{AS}$ Notes <sup>2</sup>	23.4	A
Single Avalanche Energy	$E_{AS}$ Notes <sup>2</sup>	54.8	mJ

Notes 1. PW  $\leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

2. Starting  $T_{ch}=25^\circ\text{C}$ ,  $V_{DD} = -30\text{V}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = -20 \rightarrow 0\text{V}$ ,  $L = 100\mu\text{H}$

## Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-c)}$ <sup>Notes3</sup>	2.68	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-a)}$ <sup>Notes3</sup>	125	°C/W

## Electrical Characteristics

(T<sub>a</sub>=25°C)

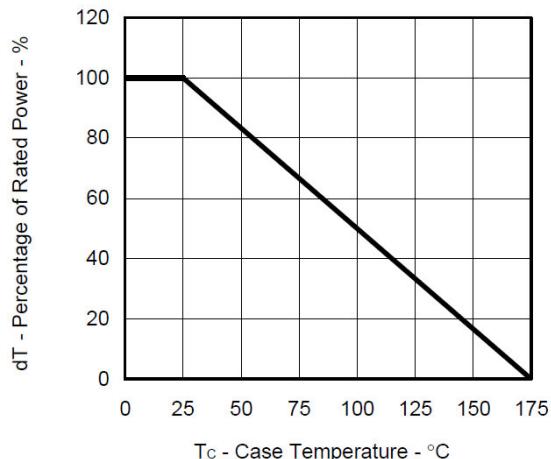
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	-10	μA	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V
Gate Leakage Current	I <sub>GSS</sub>	—	—	±10	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	-1.0	-2.0	-2.5	V	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1mA
Forward Transfer Admittance	y <sub>fs</sub>   <sup>Notes4</sup>	12	—	—	S	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -18 A
Drain to Source On-state Resistance	R <sub>DS(on)1</sub> <sup>Notes4</sup>	—	24	30	mΩ	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -18 A
	R <sub>DS(on)2</sub> <sup>Notes4</sup>	—	27	40	mΩ	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -18 A
Input Capacitance	C <sub>iss</sub>	—	3200	—	pF	V <sub>DS</sub> = -10 V
Output Capacitance	C <sub>oss</sub>	—	350	—	pF	V <sub>GS</sub> = 0 V
Reverse Transfer Capacitance	C <sub>rss</sub>	—	205	—	pF	f = 1 MHz
Turn-on Delay Time	t <sub>d(on)</sub>	—	7	—	ns	V <sub>DD</sub> = -30 V I <sub>D</sub> = -18 A V <sub>GS</sub> = -10 V R <sub>G</sub> = 0 Ω
Rise Time	t <sub>r</sub>	—	12	—	ns	
Turn-off Delay Time	t <sub>d(off)</sub>	—	190	—	ns	
Fall Time	t <sub>f</sub>	—	110	—	ns	
Total Gate Charge	Q <sub>g</sub>	—	52	—	nC	V <sub>DD</sub> = -48 V V <sub>GS</sub> = -10 V I <sub>D</sub> = -36 A
Gate to Source Charge	Q <sub>gs</sub>	—	6.9	—	nC	
Gate to Drain Charge	Q <sub>gd</sub>	—	15	—	nC	
Body Diode Forward Voltage	V <sub>F(S-D)</sub> <sup>Notes4</sup>	—	—	1.2	V	I <sub>F</sub> = -36 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>	—	46	—	ns	I <sub>F</sub> = -36 A, V <sub>GS</sub> = 0 V di/dt = -100 A/μs
Reverse Recovery Charge	Q <sub>rr</sub>	—	75	—	nC	

Notes 3. Designed target value on Renesas measurement condition. Not subject to production test.

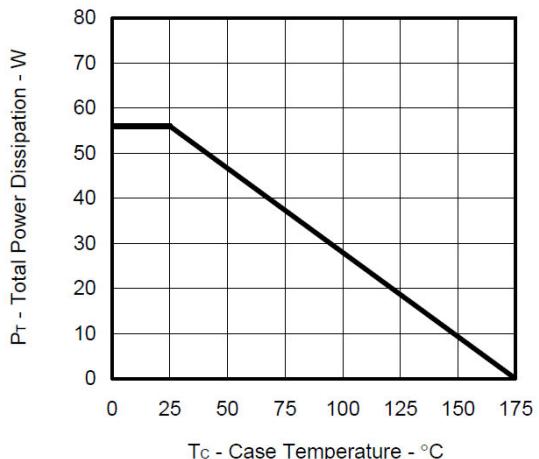
4. Pulse test.

## Typical Characteristics

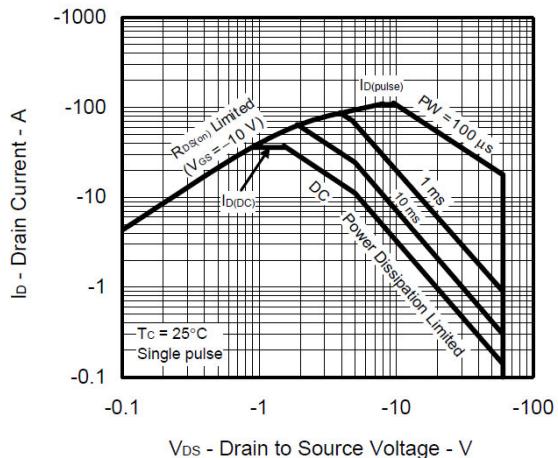
DERATING FACTOR OF FORWARD BIAS  
SAFE OPERATING AREA



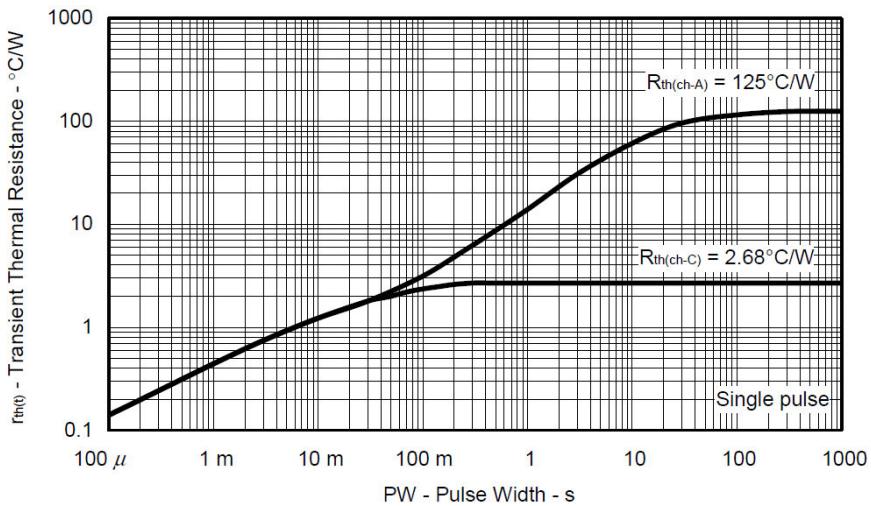
TOTAL POWER DISSIPATION vs.  
CASE TEMPERATURE

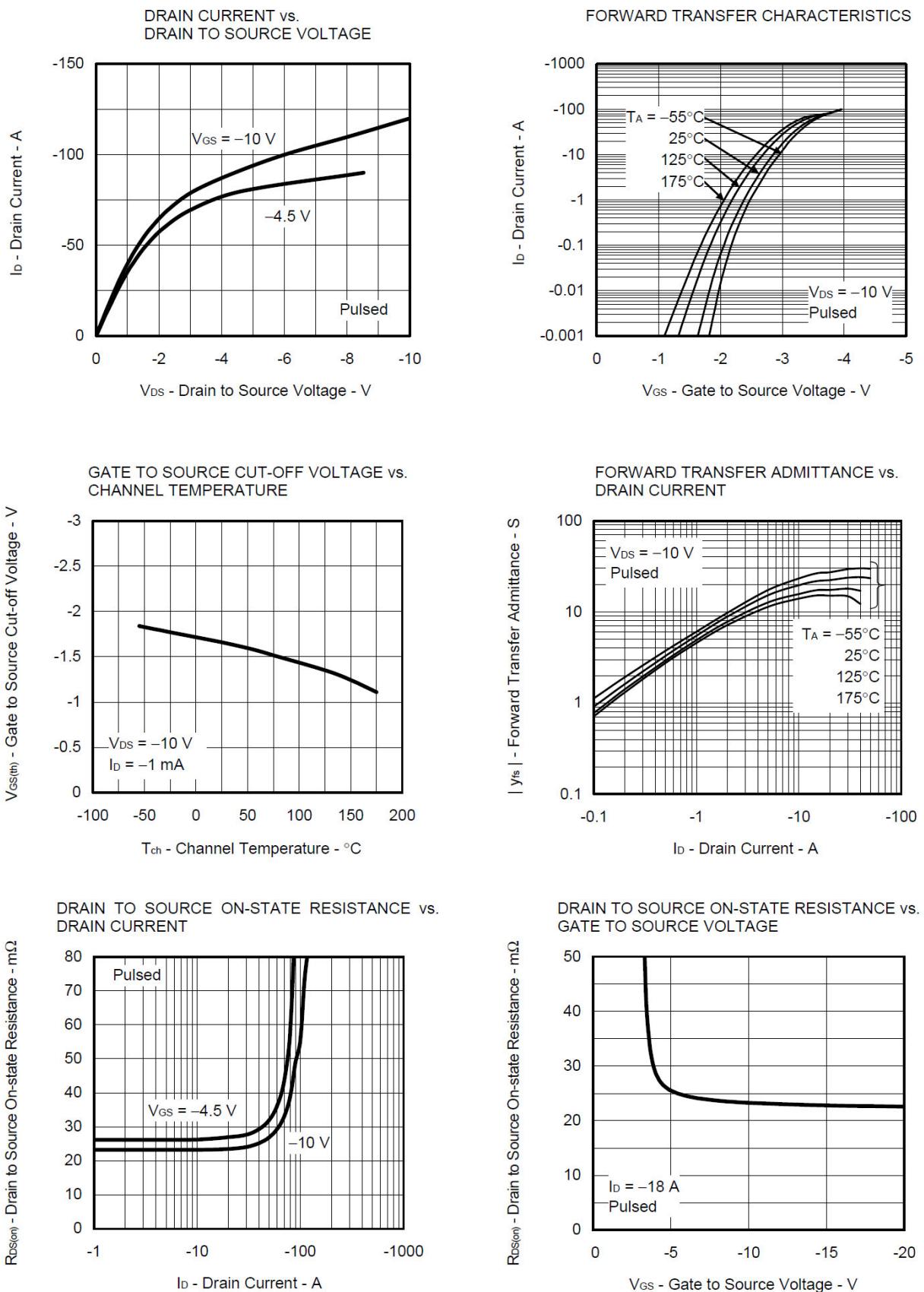


FORWARD BIAS SAFE OPERATING AREA

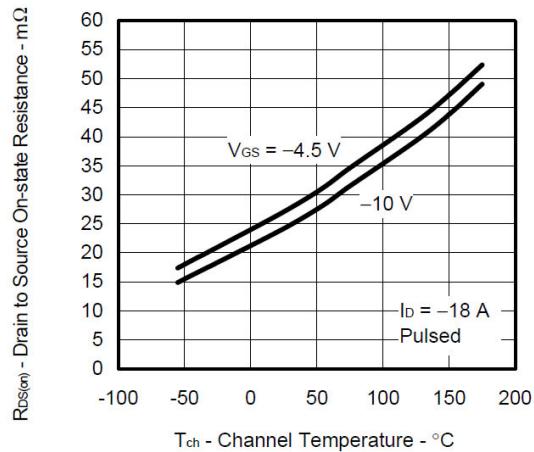


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

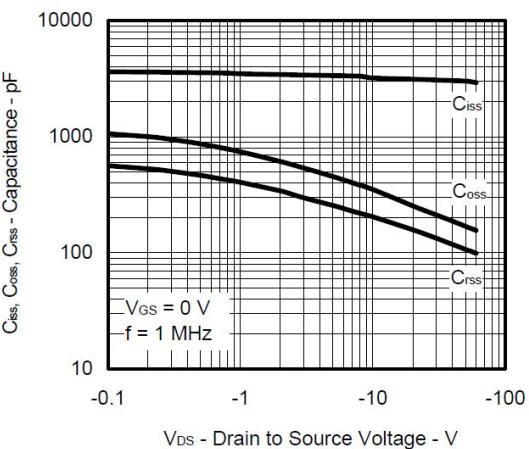




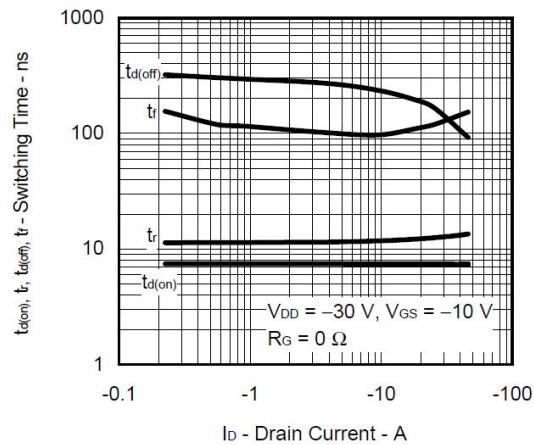
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



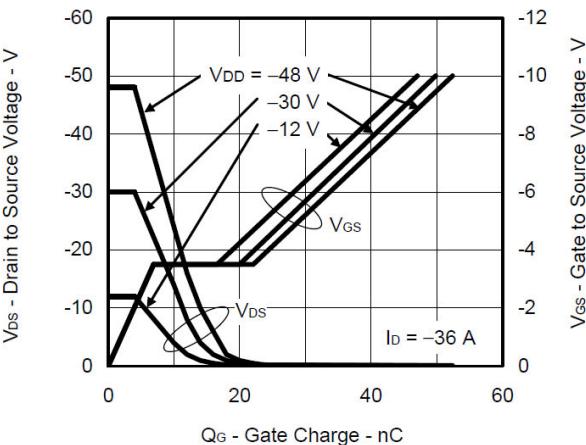
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



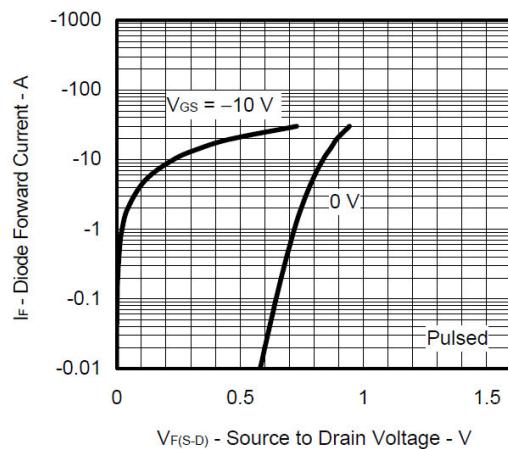
SWITCHING CHARACTERISTICS



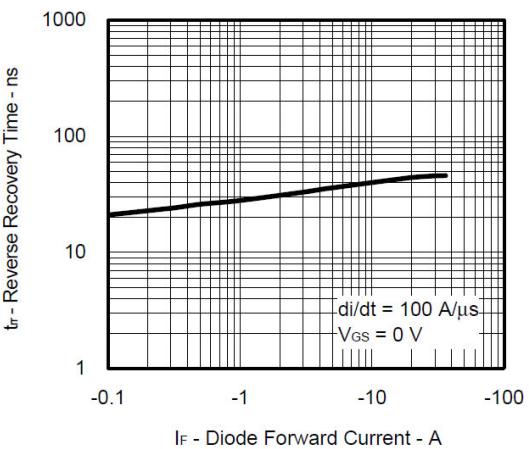
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

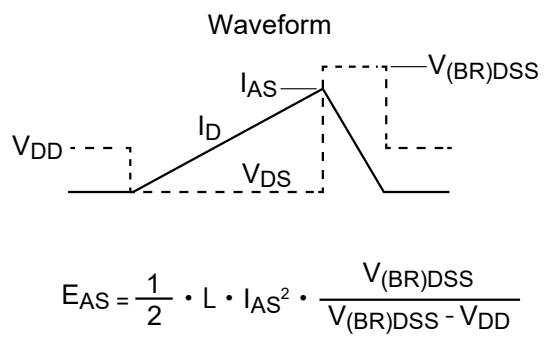
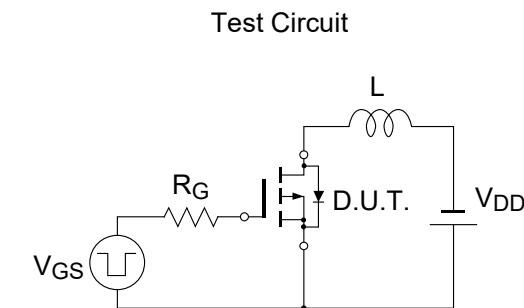


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

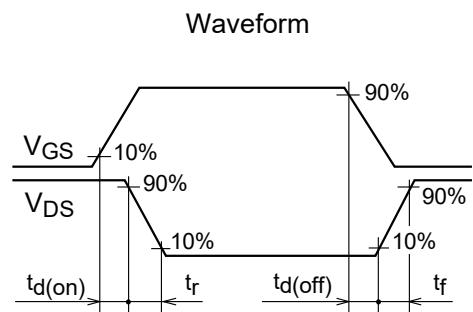
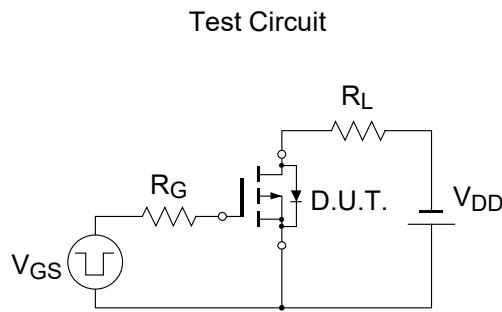


## Test Circuit

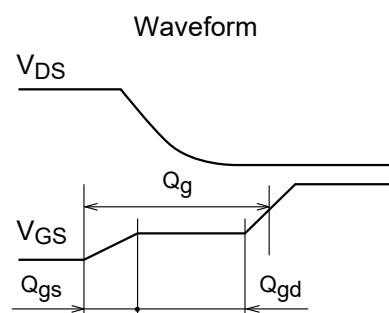
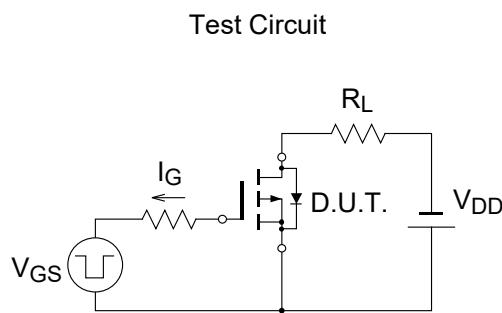
### Avalanche



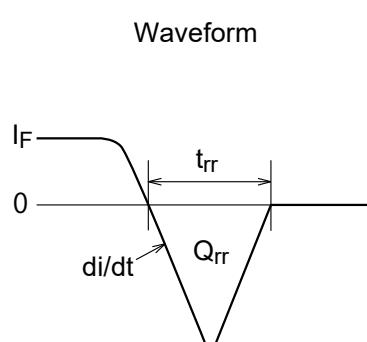
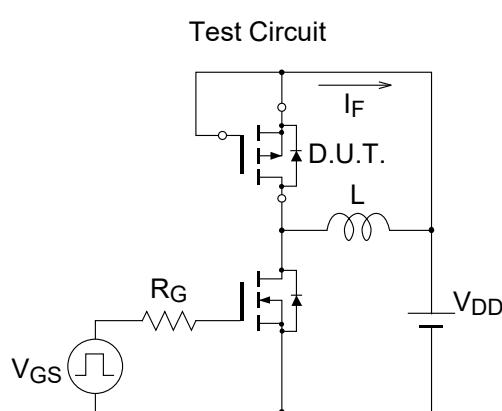
### Switching Time



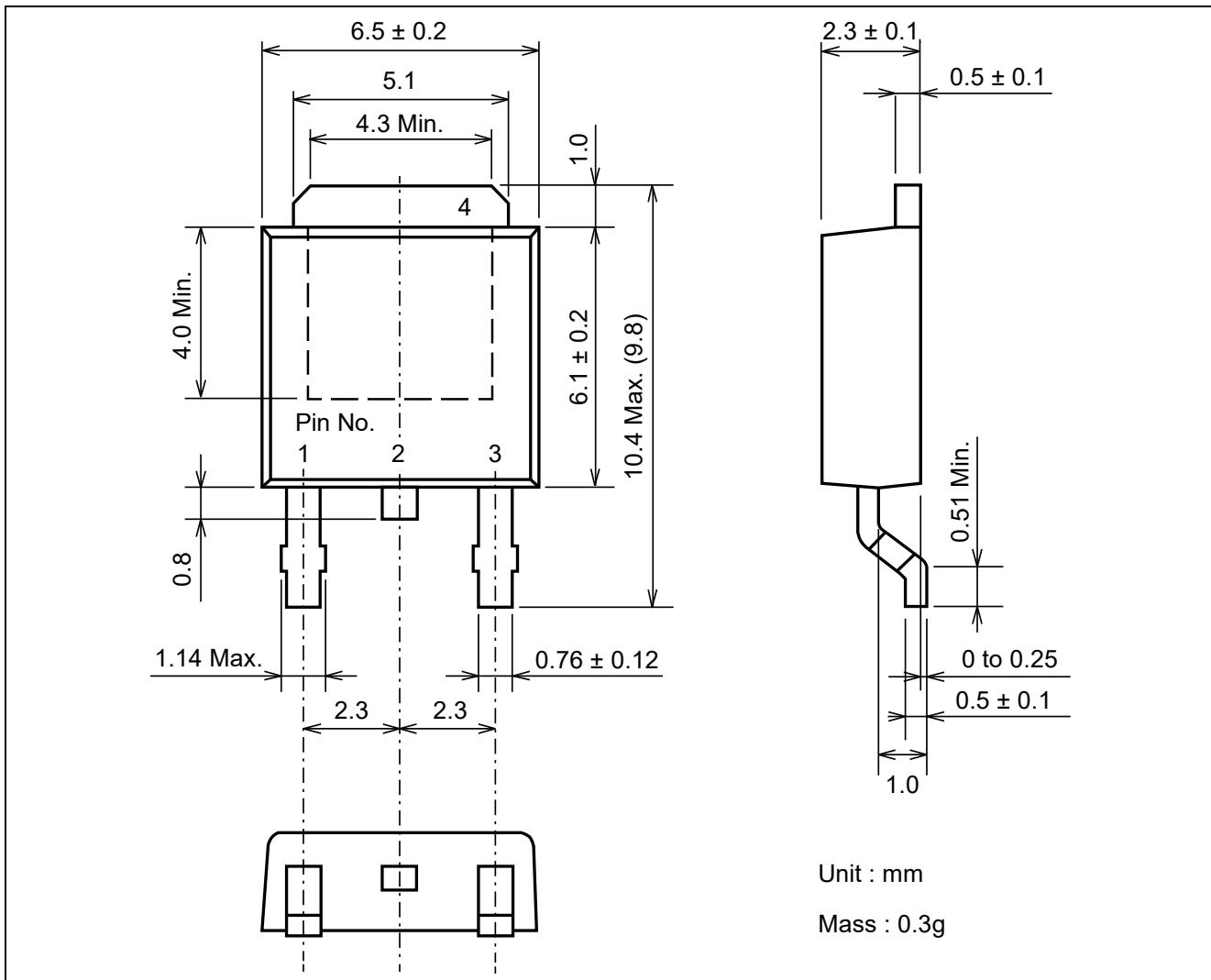
### Gate Charge



### Reverse Recovery



## Package Dimensions



## Ordering Information

Part No.	Quantity	Shipping container
NP36P06SLG-E1-AY	2500pcs/reel	Taping

**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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