



ALPHA & OMEGA
SEMICONDUCTOR

AOD444/AOI444

60V N-Channel MOSFET

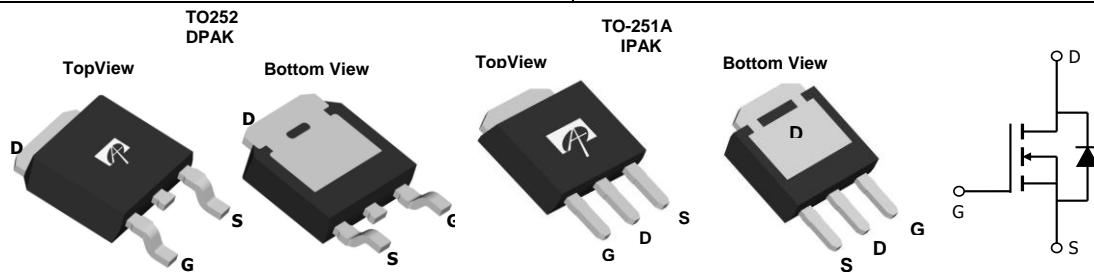
General Description

The AOD444/AOI444 combine advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. Those devices are suitable for use in PWM, load switching and general purpose applications.

Product Summary

V_{DS}	60V
I_D (at $V_{GS}=10V$)	12A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 60mΩ
$R_{DS(ON)}$ (at $V_{GS} = 4.5V$)	< 85mΩ

100% UIS Tested
100% R_g Tested



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	12	A
$T_C=100^\circ C$		9	
Pulsed Drain Current ^C	I_{DM}	30	
Continuous Drain Current	I_{DSM}	4	A
$T_A=70^\circ C$		3	
Avalanche Current ^C	I_{AS}, I_{AR}	19	A
Avalanche energy $L=0.1mH$ ^C	E_{AS}, E_{AR}	18	mJ
Power Dissipation ^B	P_D	20	W
$T_C=100^\circ C$		10	
Power Dissipation ^A	P_{DSM}	2.1	W
$T_A=70^\circ C$		1.3	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	17.4	30	°C/W
Maximum Junction-to-Ambient ^D		50	60	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	4	7.5	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	60			V
$I_{\text{DS}}^{\text{SS}}$	Zero Gate Voltage Drain Current	$V_{DS}=48\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			100	nA
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1	2.4	3	V
$I_{D(\text{ON})}$	On state drain current	$V_{GS}=10\text{V}, V_{DS}=5\text{V}$	30			A
$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=12\text{A}$ $T_J=125^\circ\text{C}$	47	60		$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=6\text{A}$	85	100	67	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=20\text{A}$		14		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.74	1	V
I_S	Maximum Body-Diode Continuous Current				12	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=30\text{V}, f=1\text{MHz}$	360	450	540	pF
C_{oss}	Output Capacitance		40	61	80	pF
C_{rss}	Reverse Transfer Capacitance		16	27	40	pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$	0.6	1.4	2.0	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=30\text{V}, I_D=12\text{A}$		7.5	10	nC
$Q_g(4.5\text{V})$	Total Gate Charge			3.8	5	nC
Q_{gs}	Gate Source Charge			1.2		nC
Q_{gd}	Gate Drain Charge			1.9		nC
$t_{D(\text{on})}$	Turn-On Delay Time	$V_{GS}=10\text{V}, V_{DS}=30\text{V}, R_L=2.5\Omega, R_{\text{GEN}}=3\Omega$		4.2		ns
t_r	Turn-On Rise Time			3.4		ns
$t_{D(\text{off})}$	Turn-Off Delay Time			16		ns
t_f	Turn-Off Fall Time			2		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=12\text{A}, dI/dt=100\text{A}/\mu\text{s}$		27	35	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=12\text{A}, dI/dt=100\text{A}/\mu\text{s}$		30		nC

A. The value of R_{JJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on R_{JJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(\text{MAX})}=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})}=175^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.

D. The R_{JJA} is the sum of the thermal impedance from junction to case R_{JJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

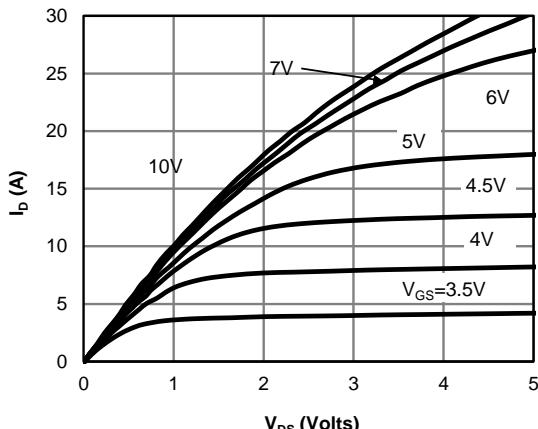
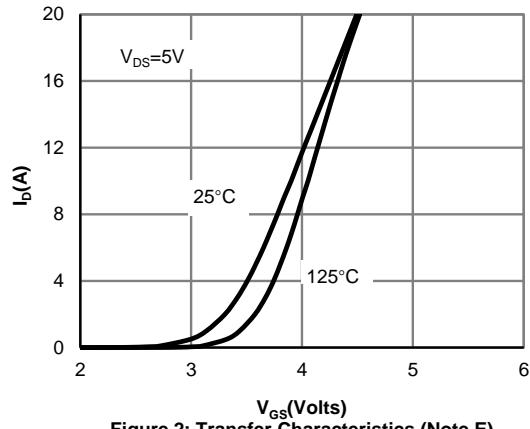
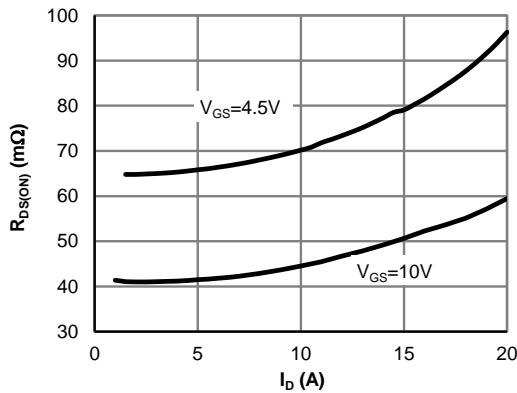
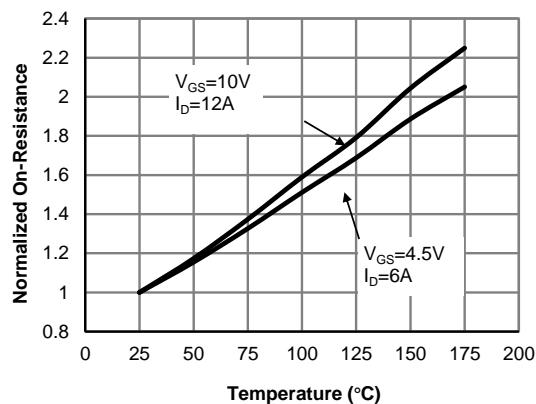
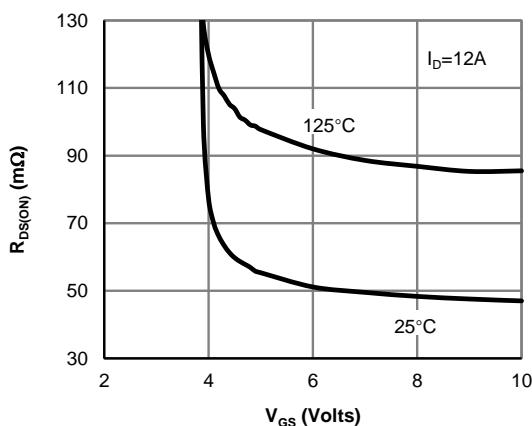
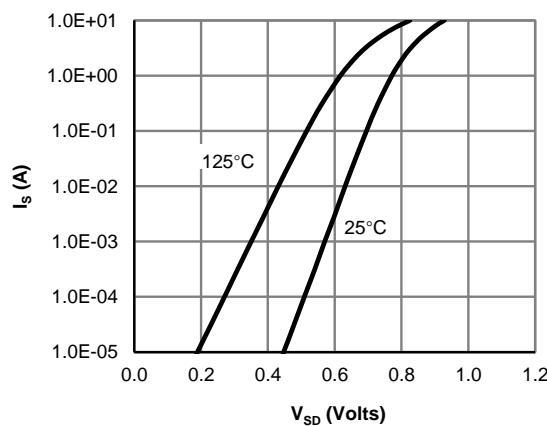
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(\text{MAX})}=175^\circ\text{C}$. The SOA curve provides a single pulse rating.

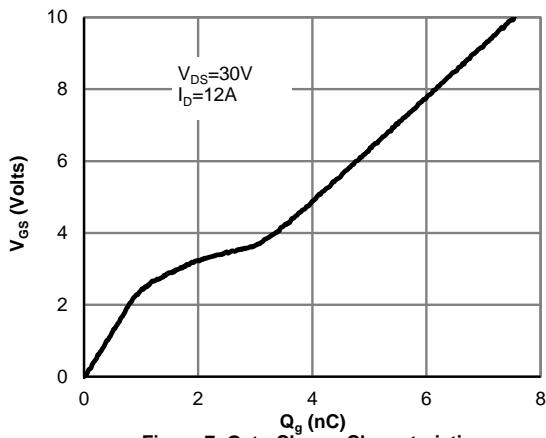
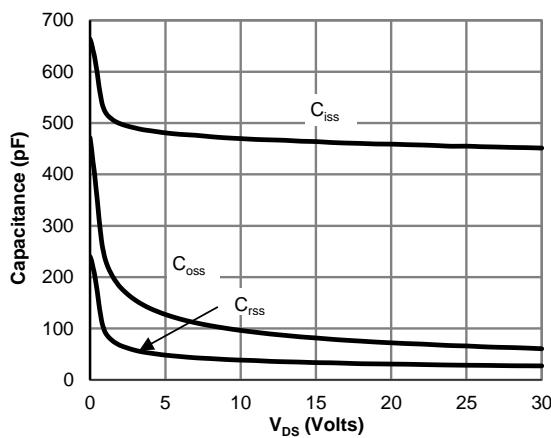
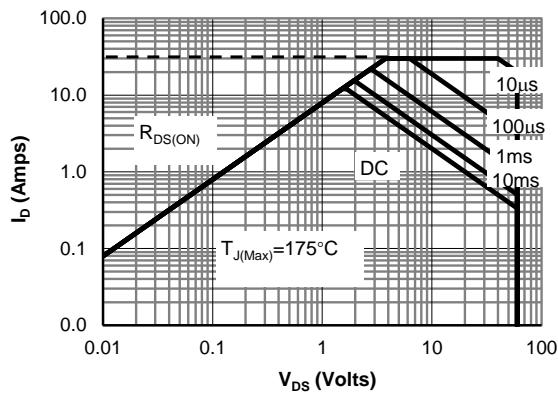
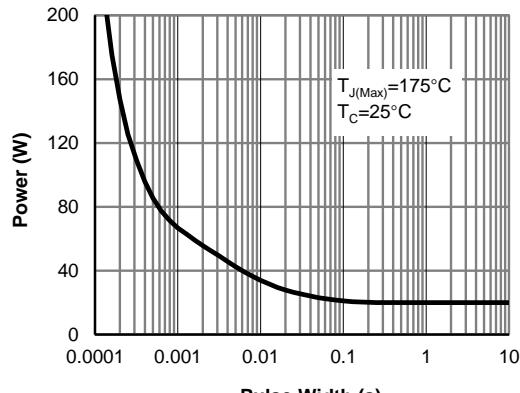
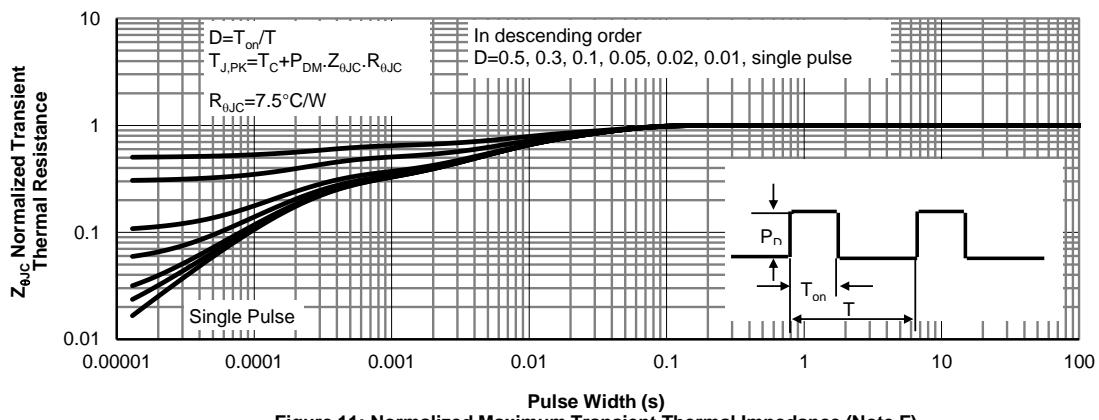
G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Fig 1: On-Region Characteristics (Note E)

Figure 2: Transfer Characteristics (Note E)

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

Figure 4: On-Resistance vs. Junction Temperature (Note E)

Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 7: Gate-Charge Characteristics

Figure 8: Capacitance Characteristics

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

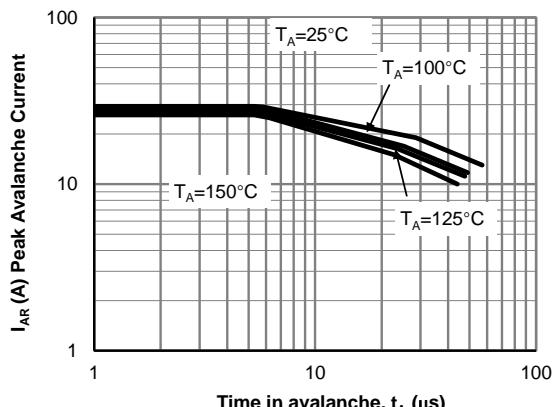
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS


Figure 12: Single Pulse Avalanche capability (Note C)

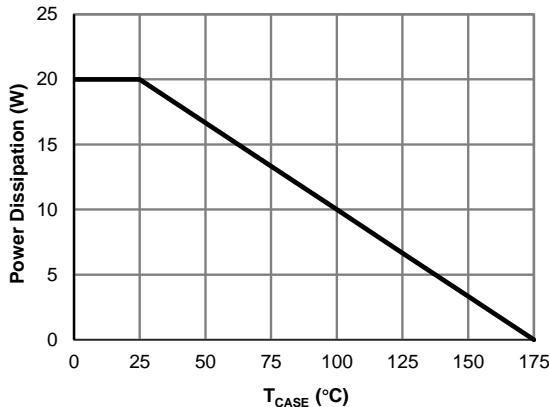


Figure 13: Power De-rating (Note F)

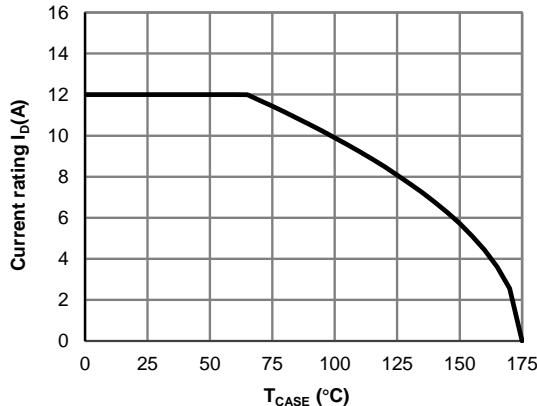


Figure 14: Current De-rating (Note F)

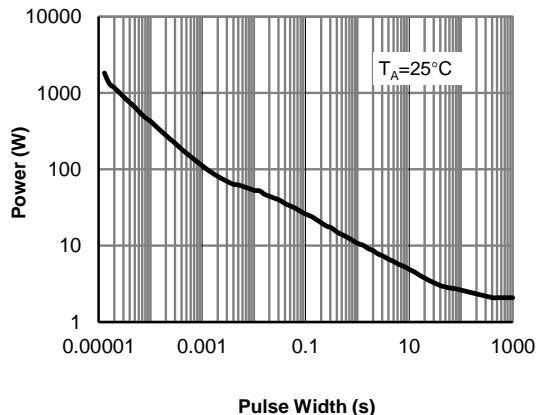


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

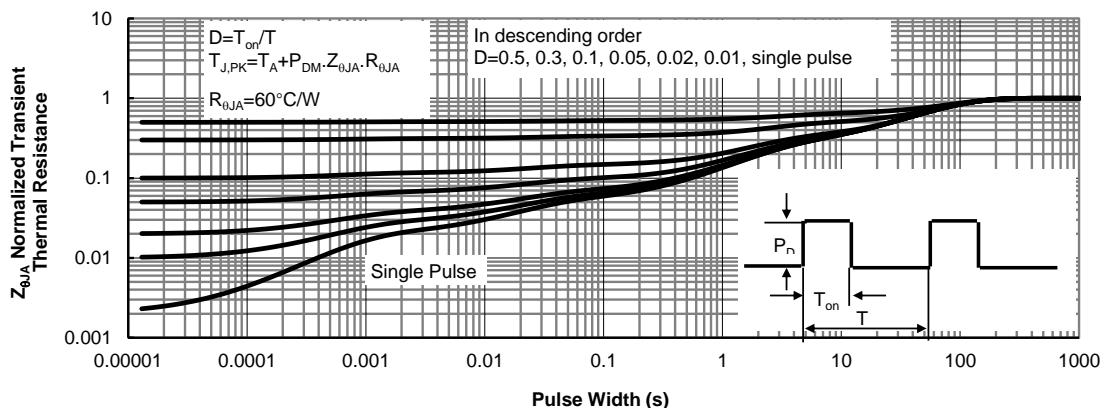
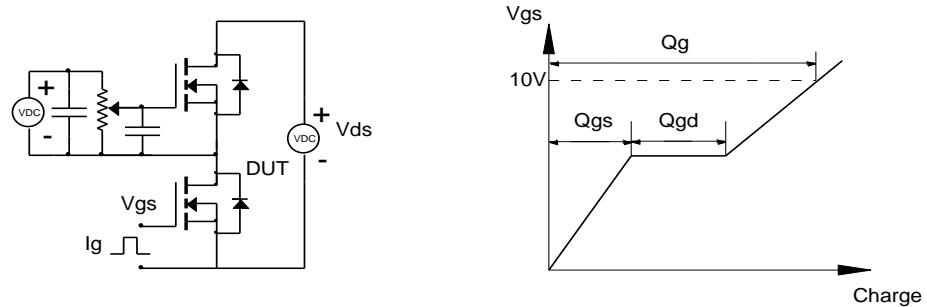
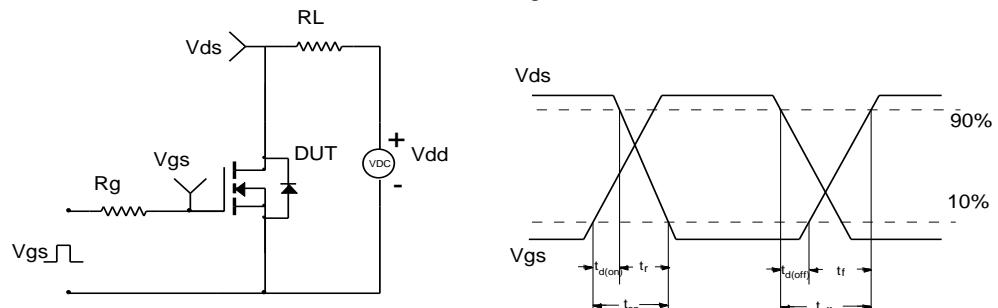
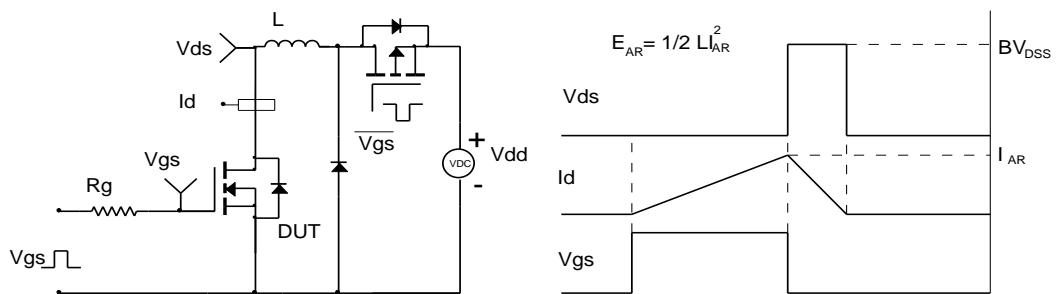


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

Diode Recovery Test Circuit & Waveforms
