

SN74LVC245A Octal Bus Transceiver With 3-State Outputs

1 Features

- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 6.3 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} Supports Live Insertion, Partial-Power-Down Mode and Back Drive protection
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model
 - 1000-V Charged-Device Model

2 Applications

- Cable Modem Termination Systems
- Servers
- LED Displays
- Network Switches
- Telecom Infrastructure
- Motor Drivers
- I/O Expanders

3 Description

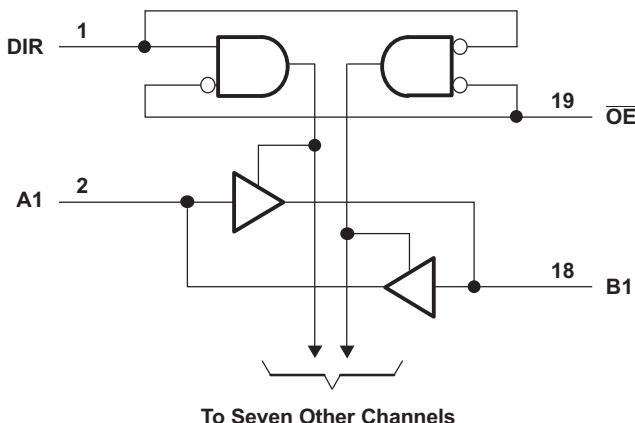
These octal bus transceivers are designed for 1.65-V to 3.6-V V_{CC} operation. The 'LVC245A devices are designed for asynchronous communication between data buses.

Device Information⁽¹⁾

PART NUMBER	PACKAGE (PIN)	BODY SIZE
SN74LVC245A	VQFN (20)	4.50 mm × 3.50 mm
	SSOP (20)	7.50 mm × 5.30 mm
	TSSOP (20)	6.50 mm × 4.40 mm
	TVSOP (20)	5.00 mm × 4.40 mm
	SOIC (20)	12.80 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



Pin numbers shown are for the DB, DGV, DW, N, NS, PW, and RGY packages.



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

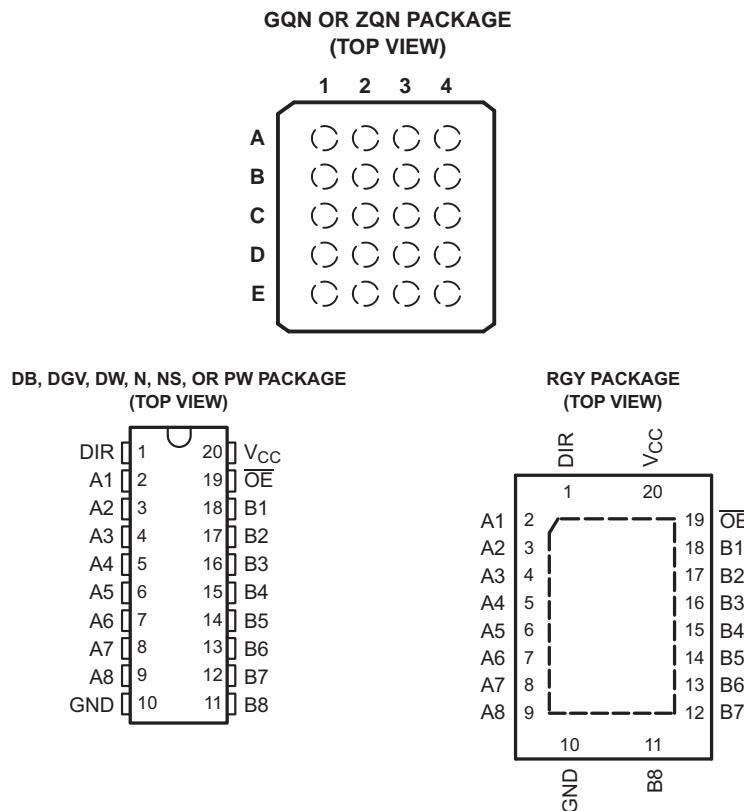
1 Features	1	9.1 Overview	9
2 Applications	1	9.2 Functional Block Diagram	9
3 Description	1	9.3 Feature Description	9
4 Simplified Schematic	1	9.4 Device Functional Modes	9
5 Revision History	2	10 Application and Implementation	10
6 Pin Configuration and Functions	3	10.1 Application Information	10
7 Specifications	4	10.2 Typical Application	10
7.1 Absolute Maximum Ratings	4	11 Power Supply Recommendations	11
7.2 ESD Ratings	4	12 Layout	11
7.3 Recommended Operating Conditions	5	12.1 Layout Guidelines	11
7.4 Thermal Information	5	12.2 Layout Example	11
7.5 Electrical Characteristics	6	13 Device and Documentation Support	12
7.6 Switching Characteristics	6	13.1 Trademarks	12
7.7 Operating Characteristics	7	13.2 Electrostatic Discharge Caution	12
7.8 Typical Characteristics	7	13.3 Glossary	12
8 Parameter Measurement Information	8	14 Mechanical, Packaging, and Orderable Information	12
9 Detailed Description	9		

5 Revision History

Changes from Revision W (May 2013) to Revision X	Page
• Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.	1
• Deleted <i>Ordering Information</i> table.	1

Changes from Revision V (September 2010) to Revision W	Page
• Added –40°C to 125°C temperature specification to <i>Recommended Operating Conditions</i> table.	5

6 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION	
NAME	DB, DGV, DW, NS, PW, and RGY			
A1	2	A1	I/O	Transceiver I/O pin
A2	3	B3	I/O	Transceiver I/O pin
A3	4	B1	I/O	Transceiver I/O pin
A4	5	C2	I/O	Transceiver I/O pin
A5	6	C1	I/O	Transceiver I/O pin
A6	7	D3	I/O	Transceiver I/O pin
A7	8	D1	I/O	Transceiver I/O pin
A8	9	E2	I/O	Transceiver I/O pin
B1	18	B4	I/O	Transceiver I/O pin
B2	17	B2	I/O	Transceiver I/O pin
B3	16	C4	I/O	Transceiver I/O pin
B4	15	C3	I/O	Transceiver I/O pin
B5	14	D4	I/O	Transceiver I/O pin
B6	13	D2	I/O	Transceiver I/O pin
B7	12	E4	I/O	Transceiver I/O pin
B8	11	E3	I/O	Transceiver I/O pin
DIR	1	A2	I	Direction control. When high, the signal propagates from A to B. When low, the signal propagates from B to A.
OE	19	A4	I	Output enable
GND	10	E1	—	Ground
V _{CC}	20	A3	—	Power pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	6.5	V
V_I	Input voltage range ⁽²⁾	-0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_o	Continuous output current		± 50	mA
	Continuous current through V_{CC} or GND		± 100	mA
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

7.2 ESD Ratings

PARAMETER	DEFINITION	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			$T_A = 25^\circ\text{C}$		$-40^\circ\text{C} \text{ TO } 85^\circ\text{C}$		$-40^\circ\text{C} \text{ TO } 125^\circ\text{C}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V_{IH}	High-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		1.7		1.7		
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		2		2		
V_{IL}	Low-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$0.35 \times V_{CC}$		$0.35 \times V_{CC}$		$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7		0.7		0.7	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		0.8		0.8	
V_I	Input voltage		0	5.5	0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 1.65 \text{ V}$		-4		-4		-4	mA
		$V_{CC} = 2.3 \text{ V}$		-8		-8		-8	
		$V_{CC} = 2.7 \text{ V}$		-12		-12		-12	
		$V_{CC} = 3 \text{ V}$		-24		-24		-24	
I_{OL}	Low-level output current	$V_{CC} = 1.65 \text{ V}$		4		4		4	mA
		$V_{CC} = 2.3 \text{ V}$		8		8		8	
		$V_{CC} = 2.7 \text{ V}$		12		12		12	
		$V_{CC} = 3 \text{ V}$		24		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10		10		10	ns/V

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74LVC245A							UNI T		
	DB⁽²⁾	DGV⁽²⁾	DW⁽²⁾	GQN or ZQN⁽²⁾	N⁽²⁾	NS⁽²⁾	PW⁽²⁾			
	20 PINS									
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.5	124.1	92.9	78	59.2	83.6	108.1	44.0	°C/ W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	68.1	39.5	60.6		44.9	49.4	43.0	53.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	61.7	65.5	60.4		40.1	51.2	59.1	22.1	
Ψ_{JT}	Junction-to-top characterization parameter	28.5	2.1	28.2		29.9	21.9	4.7	3.0	
Ψ_{JB}	Junction-to-board characterization parameter	61.2	64.9	60.0		39.9	50.8	58.6	22.2	
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	—	—	—		—	—	—	16.6	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
(2) The package thermal impedance is calculated in accordance with JESD 51-7.
(3) The package thermal impedance is calculated in accordance with JESD 51-5.

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			−40°C TO 85°C		−40°C TO 125°C		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
V _{OH}	I _{OH} = −100 µA	1.65 V to 3.6 V	V _{CC} − 0.2			V _{CC} − 0.2		V _{CC} − 0.2		V	
	I _{OH} = −4 mA	1.65 V	1.29			1.2		1.1			
	I _{OH} = −8 mA	2.3 V	1.9			1.7		1.6			
	I _{OH} = −12 mA	2.7 V	2.2			2.2		2.1			
		3 V	2.4			2.4		2.3			
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V	0.1			0.2		0.2		V	
	I _{OL} = 4 mA	1.65 V	0.24			0.45		0.60			
	I _{OL} = 8 mA	2.3 V	0.3			0.7		0.75			
	I _{OL} = 12 mA	2.7 V	0.4			0.4		0.6			
	I _{OL} = 24 mA	3 V	0.55			0.55		0.75			
I _I	Control inputs	V _I = 0 to 5.5 V	3.6 V	±1			±5	±10		µA	
I _{off}		V _I or V _O = 5.5 V	0	±1			±10	±20		µA	
I _{OZ} ⁽¹⁾		V _O = 0 to 5.5 V	3.6 V	±1			±10	±20		µA	
I _{CC}	V _I = V _{CC} or GND	I _O = 0	3.6 V	1			10	30		µA	
	3.6 V ≤ V _I ≤ 5.5 V ⁽²⁾			1			10	30			
ΔI _{CC}	One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V	500			500	5000		µA	
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	4						pF	
C _{io}	A or B ports ⁽³⁾	V _I = V _{CC} or GND	3.3 V	5.5						pF	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This applies in the disabled state only.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

7.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

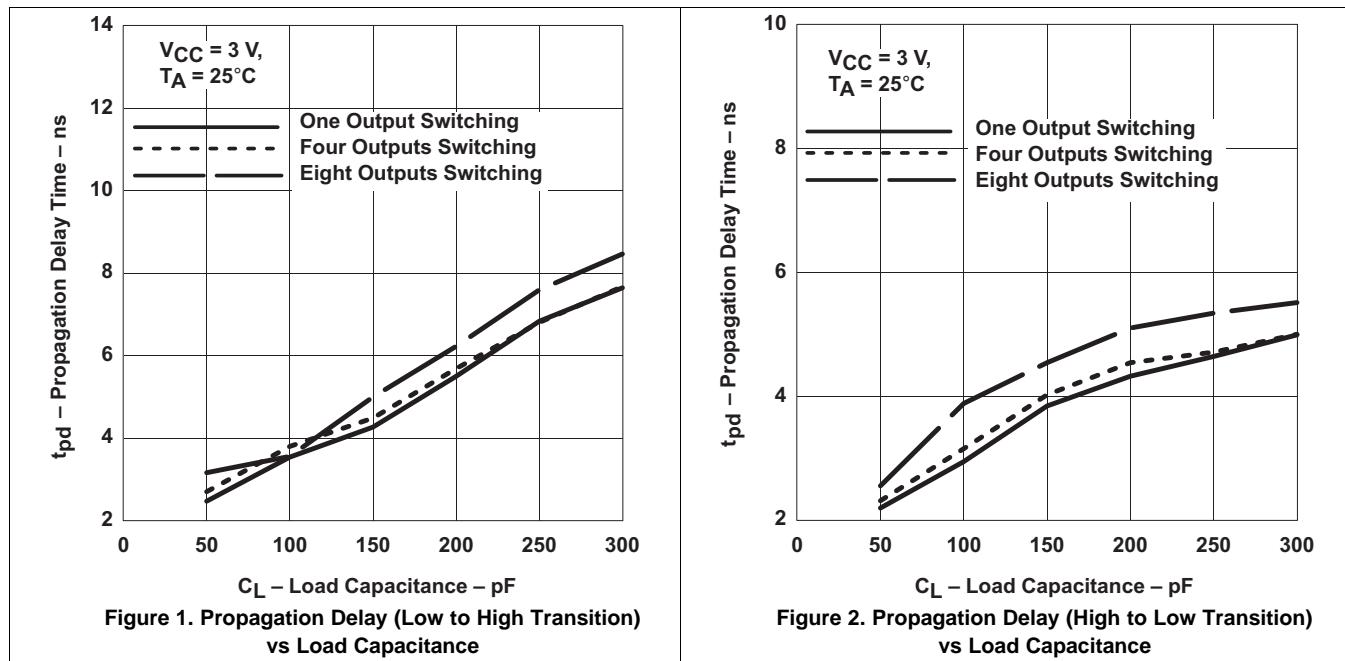
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			−40°C TO 85°C		−40°C TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	1.8 V ± 0.15 V	1	6	12.2	1	12.7	1	13.7	ns
			2.5 V ± 0.2 V	1	3.9	7.8	1	8.3	1	9.1	
			2.7 V	1	4.2	7.1	1	7.3	1	8.3	
			3.3 V ± 0.3 V	1.5	3.8	6.1	1.5	6.3	1.5	7.3	
t _{en}	OE	A or B	1.8 V ± 0.15 V	1	7	14.8	1	15.3	1	16.8	ns
			2.5 V ± 0.2 V	1	4.5	10	1	10.5	1	12	
			2.7 V	1	5.4	9.3	1	9.5	1	11	
			3.3 V ± 0.3 V	1.5	4.4	8.3	1.5	8.5	1.5	10	
t _{dis}	OE	A or B	1.8 V ± 0.15 V	1	7.8	16.5	1	17	1	18	ns
			2.5 V ± 0.2 V	1	4	9	1	9.5	1	10.5	
			2.7 V	1	4.4	8.3	1	8.5	1	9.5	
			3.3 V ± 0.3 V	1.7	4.1	7.3	1.7	7.5	1.7	8.5	
t _{sk(o)}			3.3 V ± 0.3 V					1		1.5	ns

7.7 Operating Characteristics

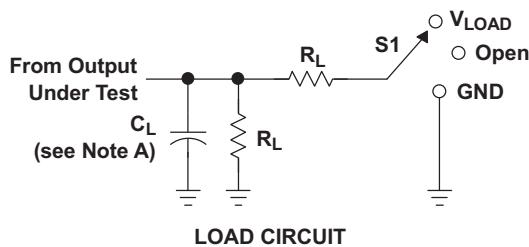
 $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT	
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled $f = 10 \text{ MHz}$	1.8 V	42	pF	
			2.5 V	43		
			3.3 V	45		
	Outputs disabled		1.8 V	1		
			2.5 V	1		
			3.3 V	2		

7.8 Typical Characteristics



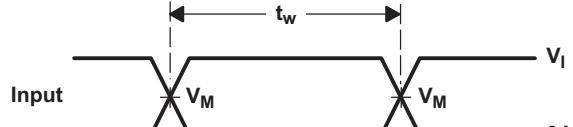
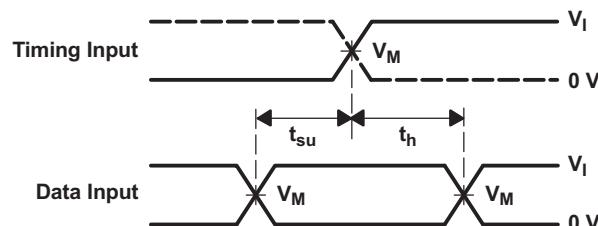
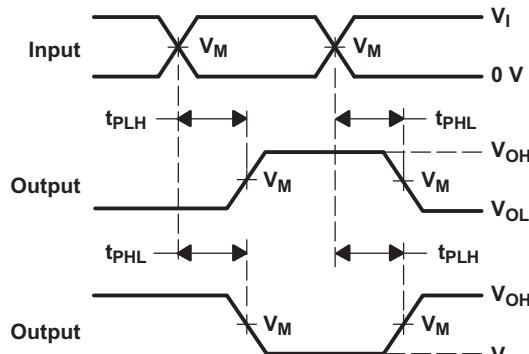
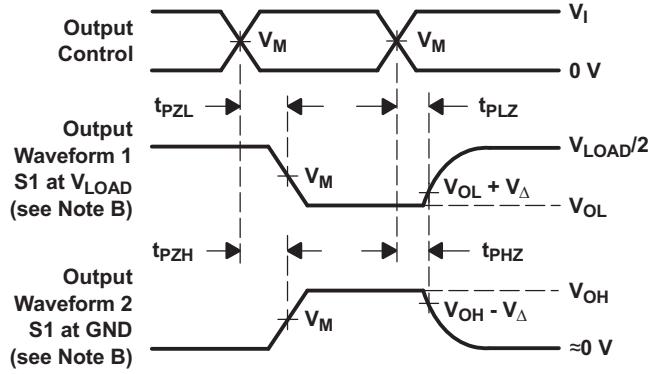
8 Parameter Measurement Information



TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_f/t_f					
$1.8 V \pm 0.15 V$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5 V \pm 0.2 V$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3 V \pm 0.3 V$	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V

VOLTAGE WAVEFORMS
PULSE DURATIONVOLTAGE WAVEFORMS
SETUP AND HOLD TIMESVOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTSVOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PZH} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

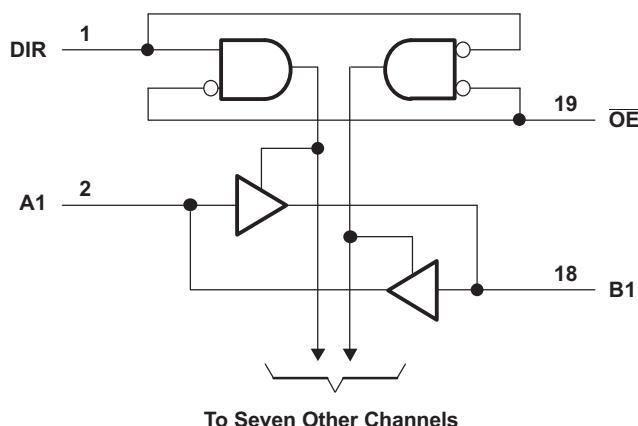
This octal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC245A device is designed for asynchronous communication between data buses. This device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses effectively are isolated.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

9.2 Functional Block Diagram



Pin numbers shown are for the DB, DGV, DW, N, NS, PW, and RGY packages.

9.3 Feature Description

- Allows down voltage translation
 - 5 V to 3.3 V
 - 5 V or 3.3 V to 1.8 V
- Inputs accept voltage levels up to 5.5 V

9.4 Device Functional Modes

Table 1. Function Table

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

SN74LVC245A is a high drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern. The inputs can accept voltages to 5.5 V at any valid V_{CC} making it ideal for down translation.

10.2 Typical Application

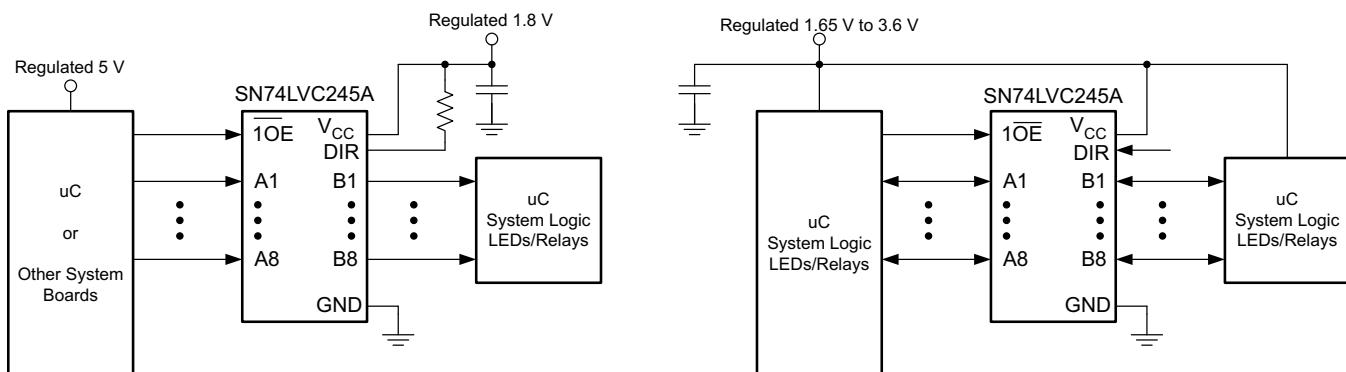


Figure 4. Typical Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
 - For rise time and fall time specifications, see ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
 - For specified high and low levels, see (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
 - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the *Recommended Operating Conditions* table at any valid V_{CC} .
2. Recommend Output Conditions
 - Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.
 - Outputs should not be pulled above V_{CC} .

Typical Application (continued)

10.2.3 Application Curves

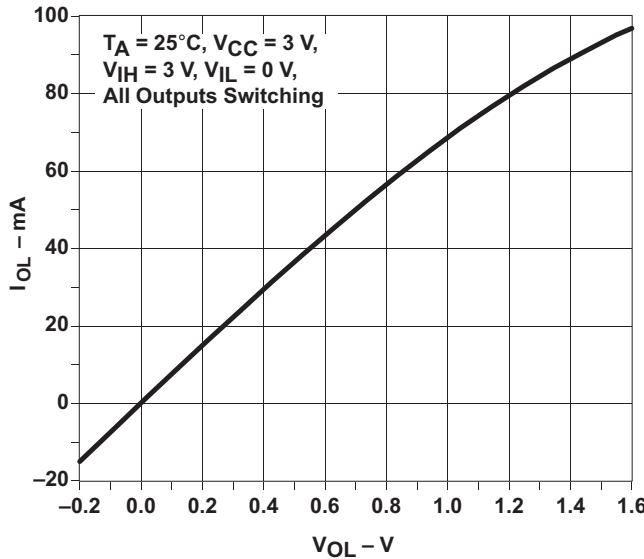


Figure 5. Output Drive Current (I_{OL}) vs LOW-level Output Voltage (V_{OL})

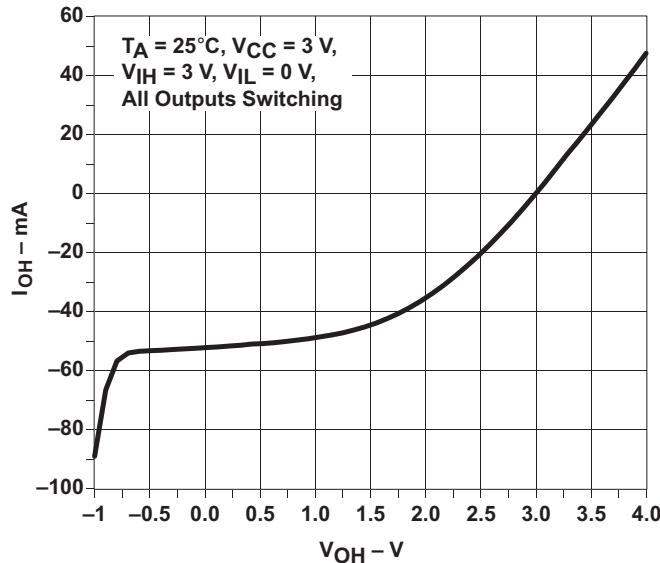


Figure 6. Output Drive Current (I_{OH}) vs HIGH-level Output Voltage (V_{OH})

11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01 μF or 0.022 μF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 7](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient.

12.2 Layout Example

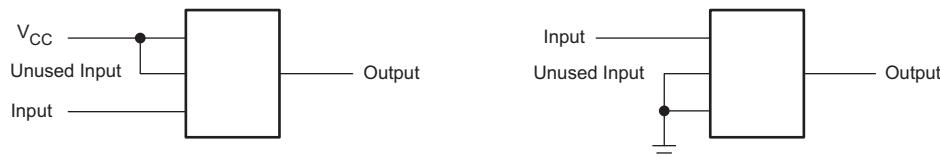


Figure 7. Layout Diagram

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC245ADBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245ADBR.B	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245ADBRE4	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245ADB RG4	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245ADGVR	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245ADGVR.B	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245ADGVRG4	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245ADGVRG4.B	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245ADW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245ADW.B	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245ADWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245ADWR.B	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245ADWRG4	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245AN	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74LVC245AN
SN74LVC245AN.B	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74LVC245AN
SN74LVC245ANE4	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74LVC245AN
SN74LVC245ANS.B	Active	Production	SOP (NS) 20	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245ANSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245ANSR.B	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245ANSRG4	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245ANSRG4.B	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC245A
SN74LVC245APW	Active	Production	TSSOP (PW) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APW.B	Active	Production	TSSOP (PW) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWE4	Active	Production	TSSOP (PW) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWG4	Active	Production	TSSOP (PW) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWR.B	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWRE4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWRG3	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LC245A

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC245APWRG3.B	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWRG4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWRG4.B	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWT	Active	Production	TSSOP (PW) 20	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245APWT.B	Active	Production	TSSOP (PW) 20	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC245A
SN74LVC245ARGYR	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC245A
SN74LVC245ARGYR.B	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC245A
SN74LVC245ARGYRG4	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC245A
SN74LVC245ARGYRG4.B	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC245A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

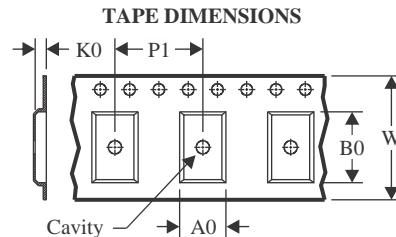
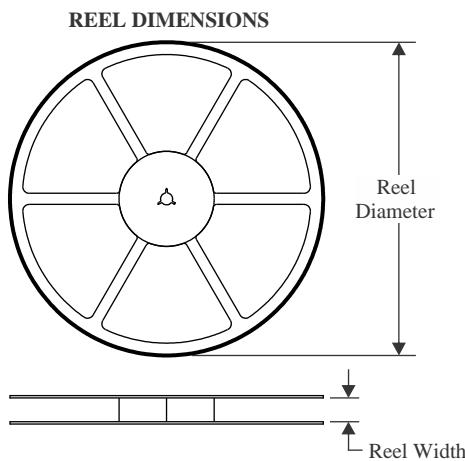
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC245A :

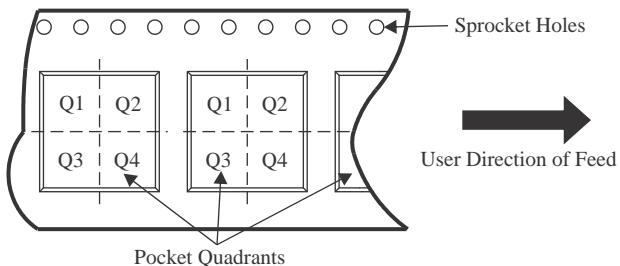
- Enhanced Product : [SN74LVC245A-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

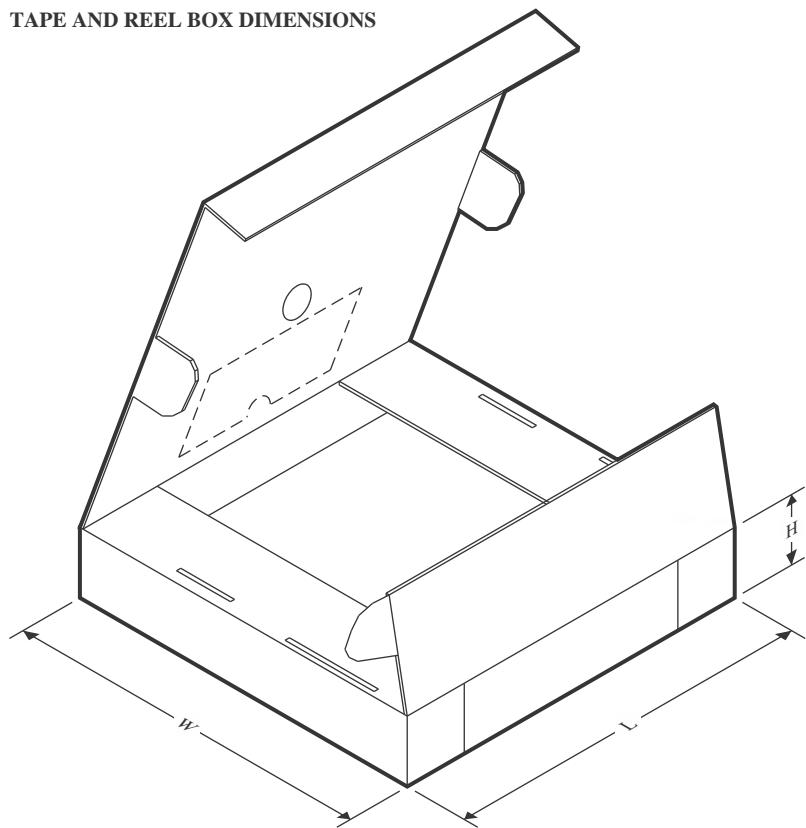
TAPE AND REEL INFORMATION

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

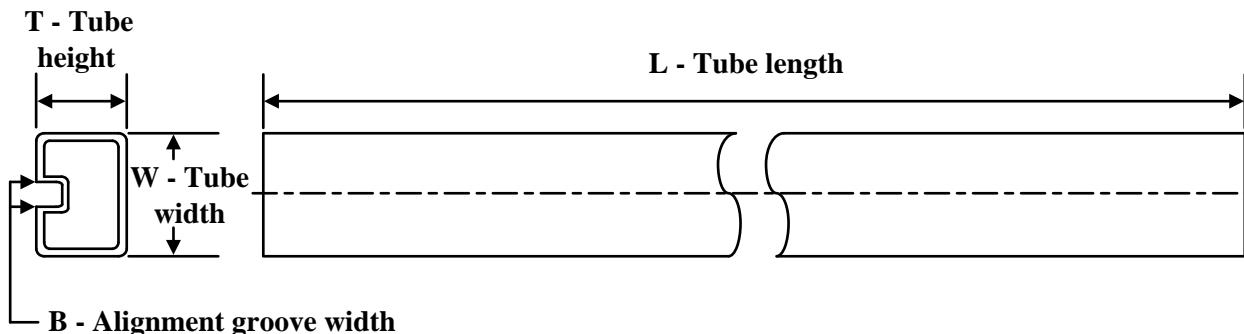
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC245ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVC245ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC245ADGVRG4	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC245ADWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74LVC245ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVC245ANSRG4	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVC245APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVC245APWRG3	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC245APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVC245APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVC245ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
SN74LVC245ARGYRG4	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC245ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LVC245ADGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74LVC245ADGVRG4	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74LVC245ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LVC245ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LVC245ANSRG4	SOP	NS	20	2000	356.0	356.0	45.0
SN74LVC245APWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LVC245APWRG3	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74LVC245APWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LVC245APWT	TSSOP	PW	20	250	353.0	353.0	32.0
SN74LVC245ARGYR	VQFN	RGY	20	3000	353.0	353.0	32.0
SN74LVC245ARGYRG4	VQFN	RGY	20	3000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
SN74LVC245ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVC245ADW.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVC245AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74LVC245AN.B	N	PDIP	20	20	506	13.97	11230	4.32
SN74LVC245ANE4	N	PDIP	20	20	506	13.97	11230	4.32
SN74LVC245ANS.B	NS	SOP	20	40	530	10.5	4000	4.1
SN74LVC245APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVC245APW.B	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVC245APWE4	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVC245APWG4	PW	TSSOP	20	70	530	10.2	3600	3.5

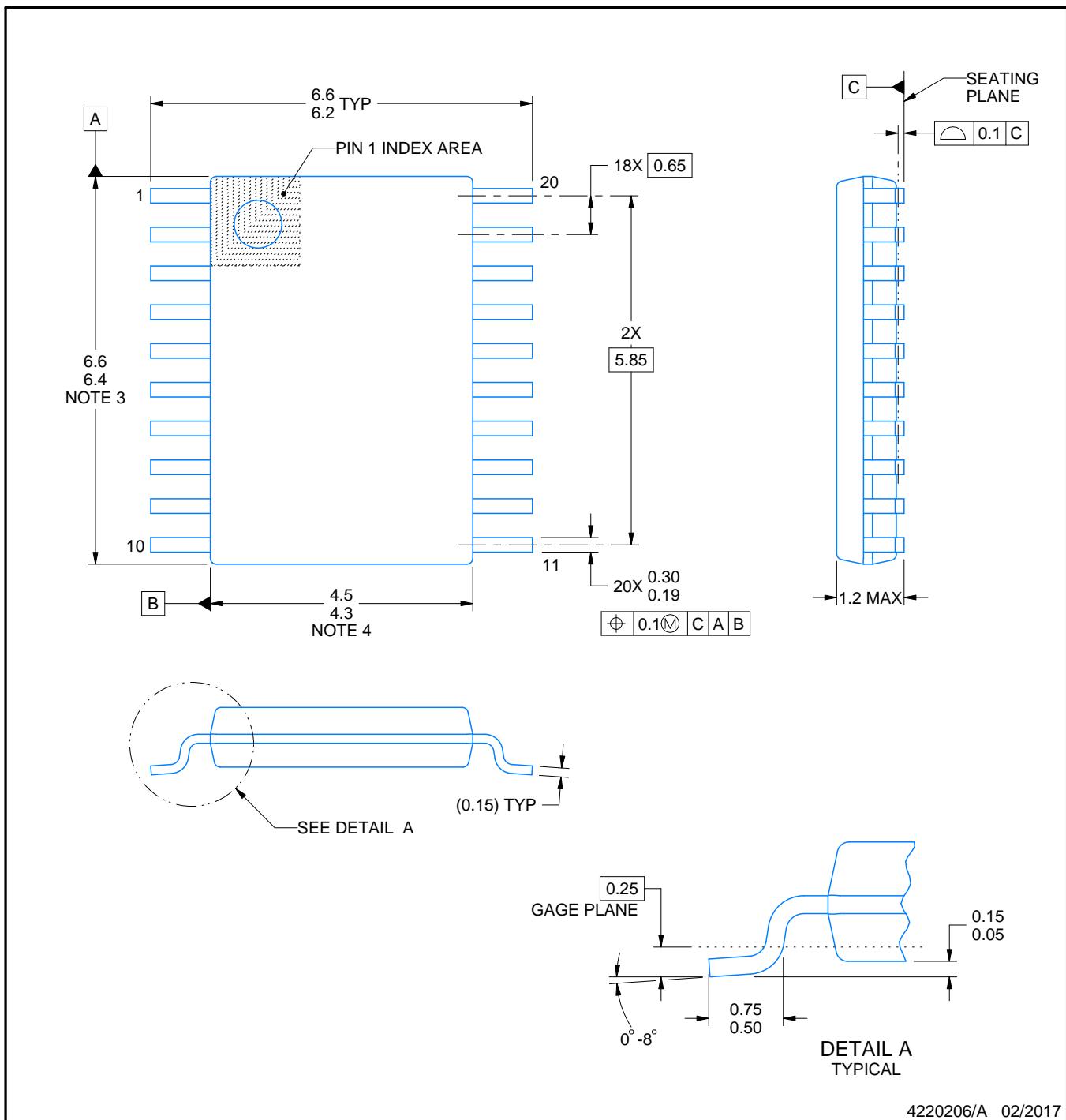
PACKAGE OUTLINE

PW0020A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

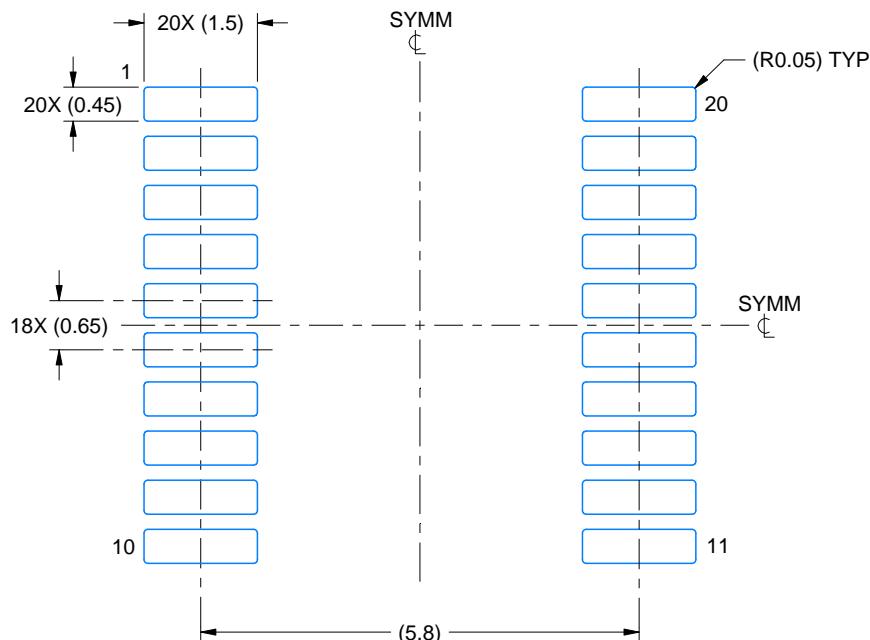
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

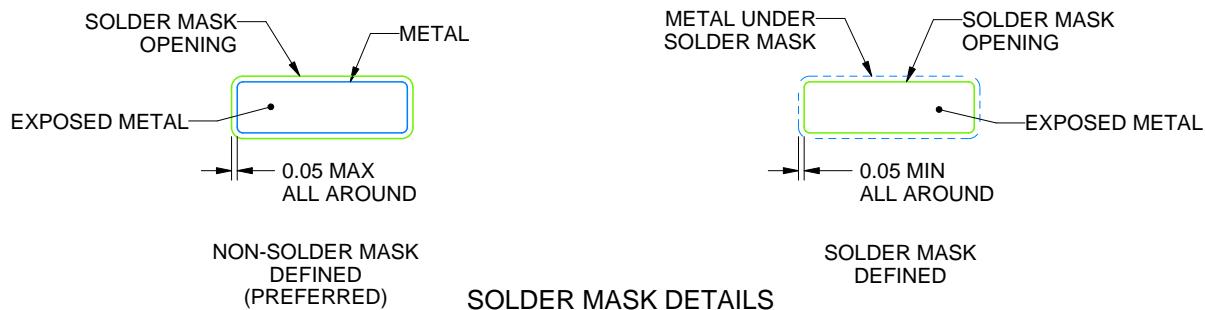
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

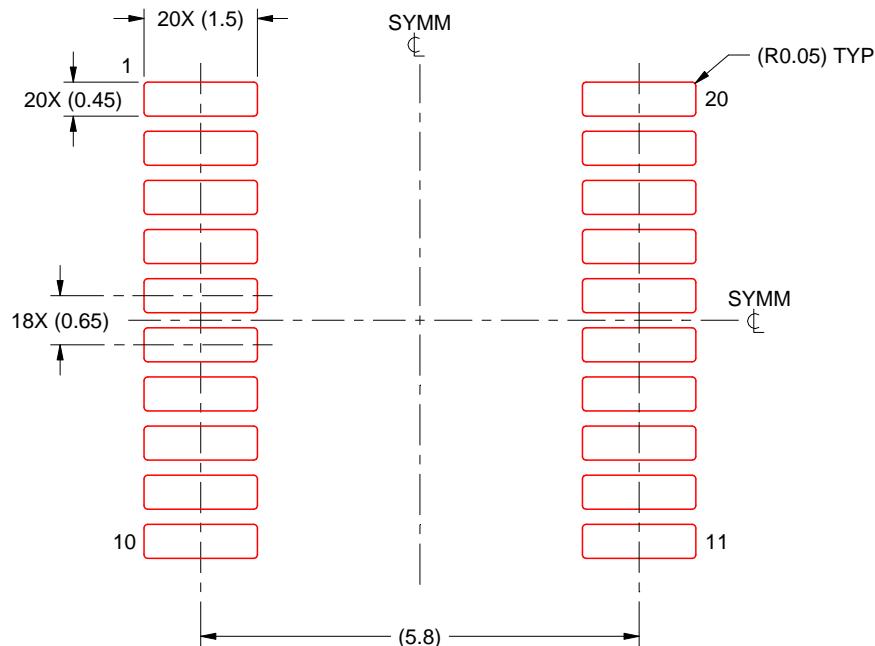
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

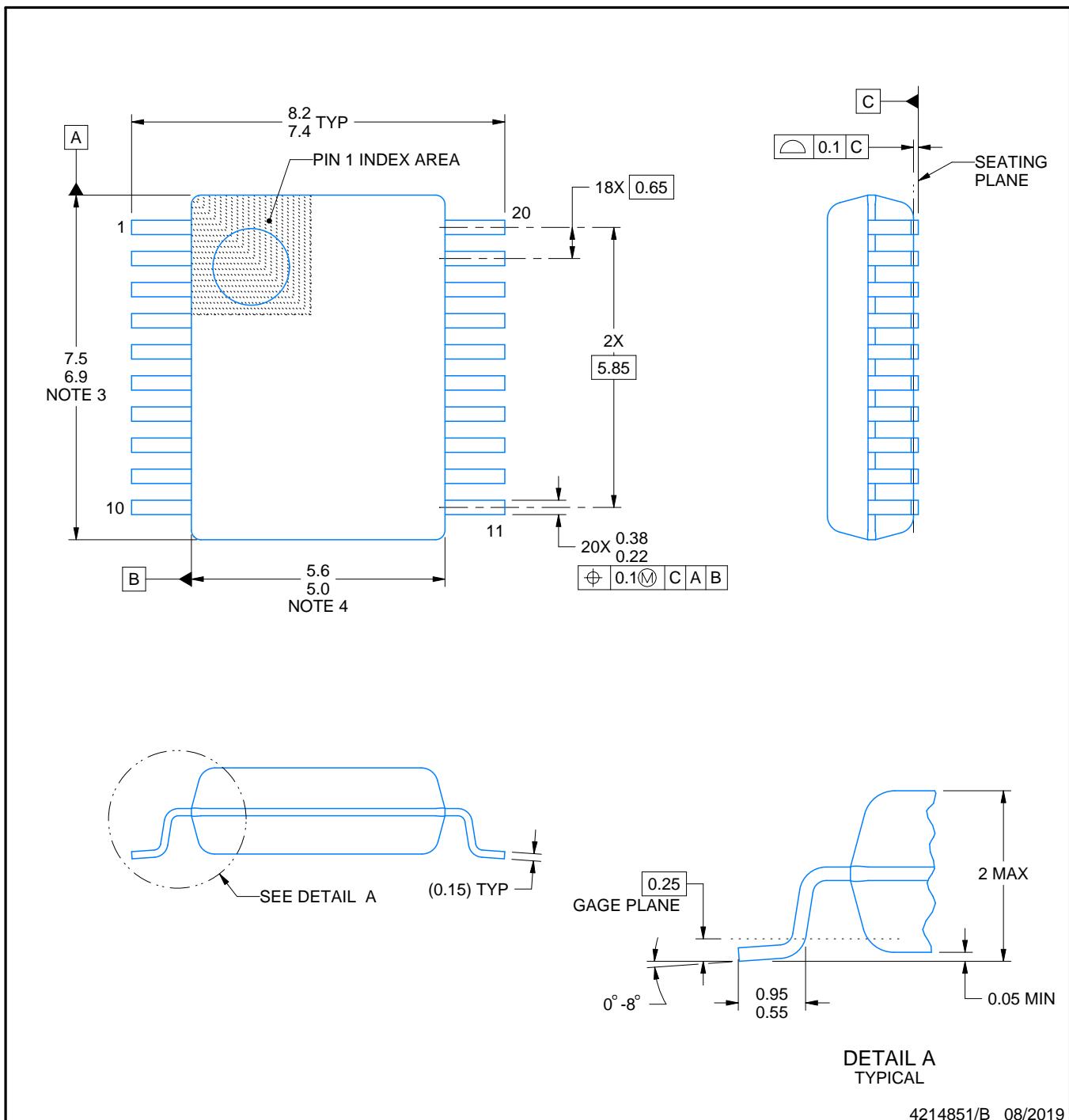
PACKAGE OUTLINE

DB0020A



SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

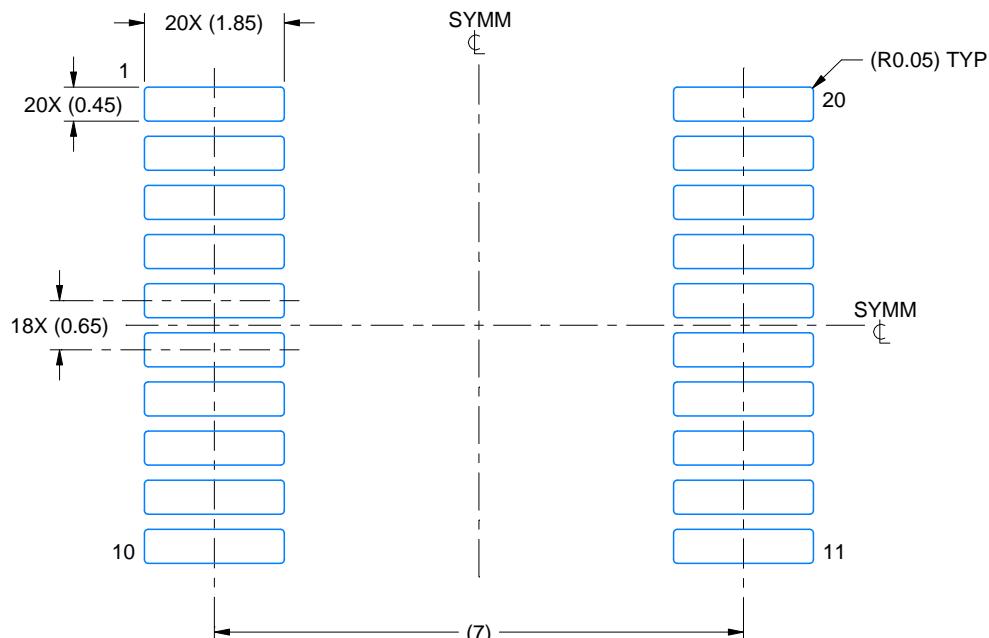
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

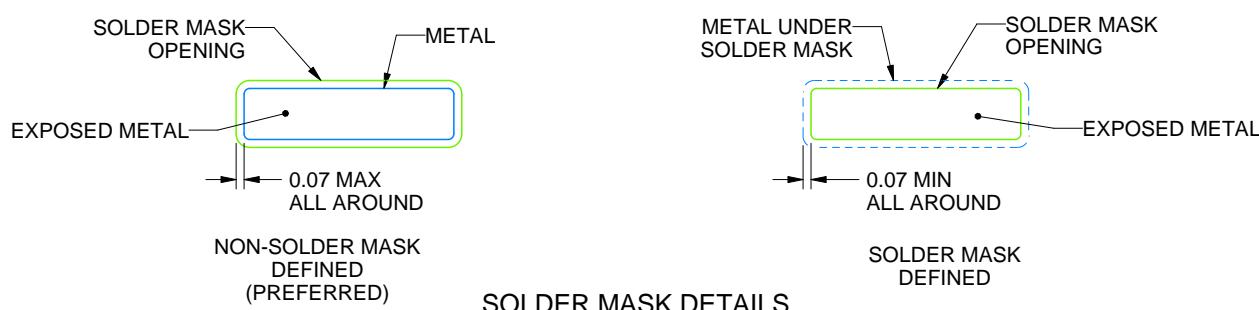
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

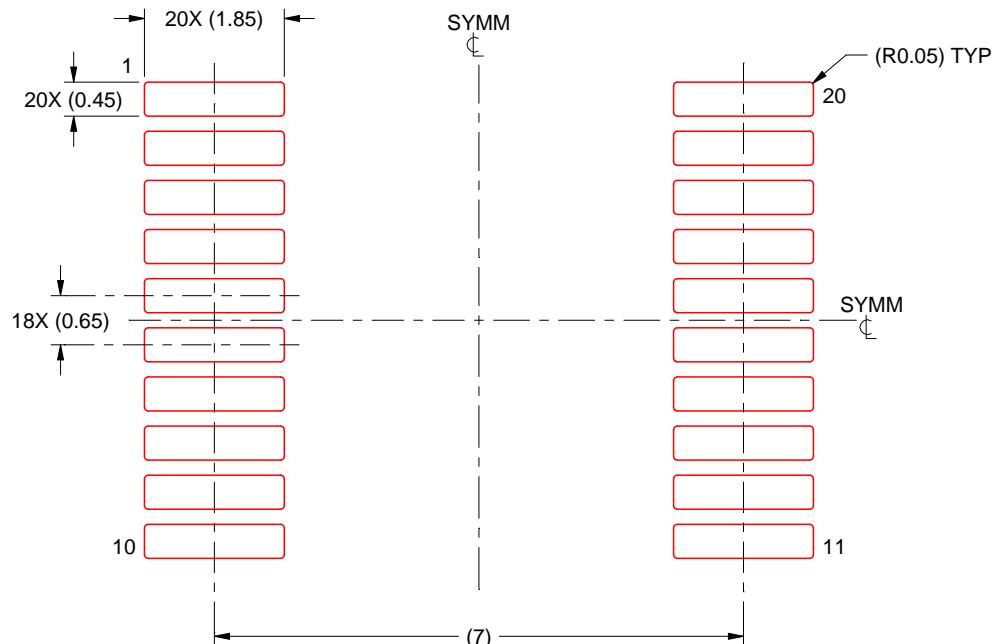
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

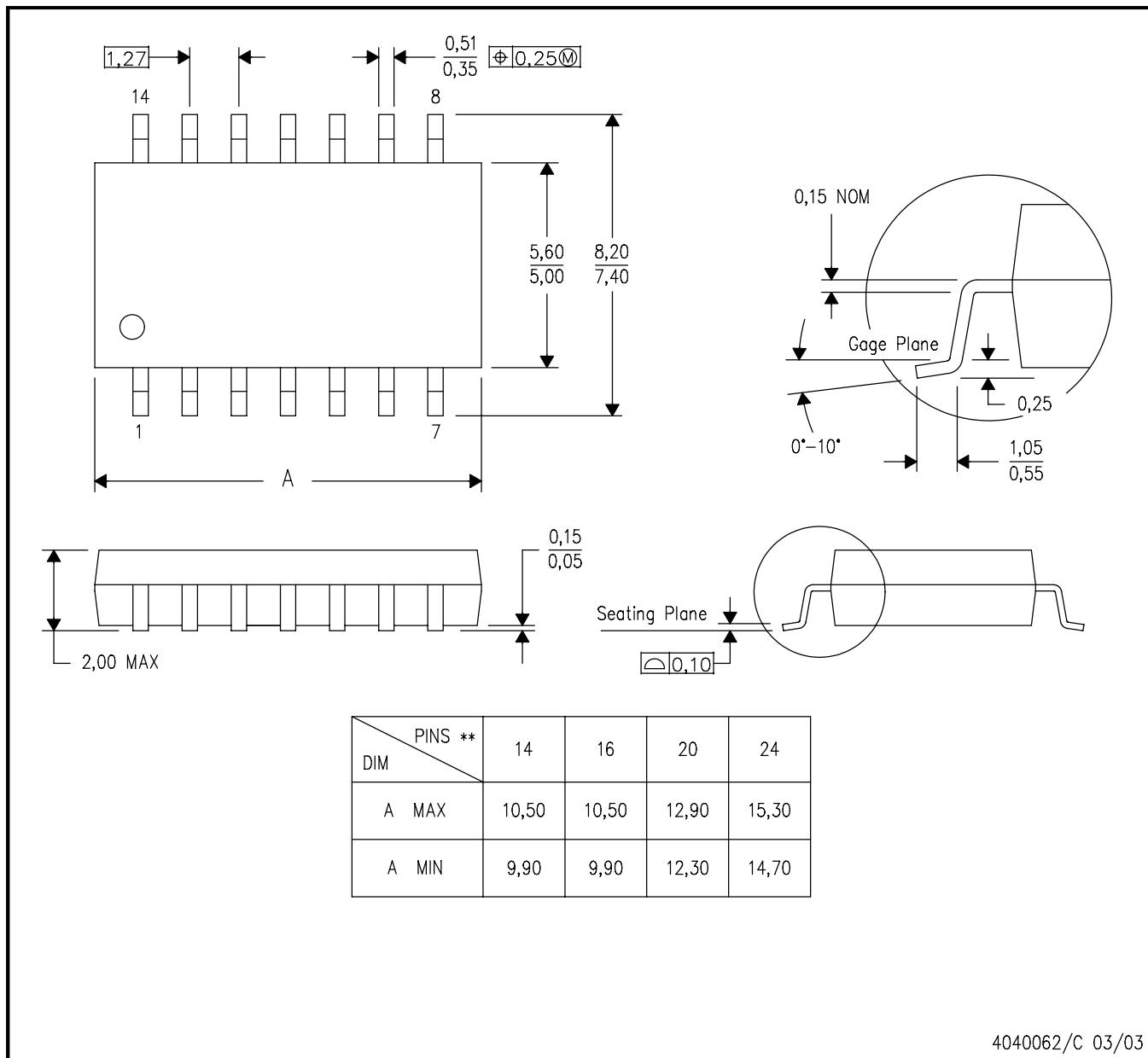
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



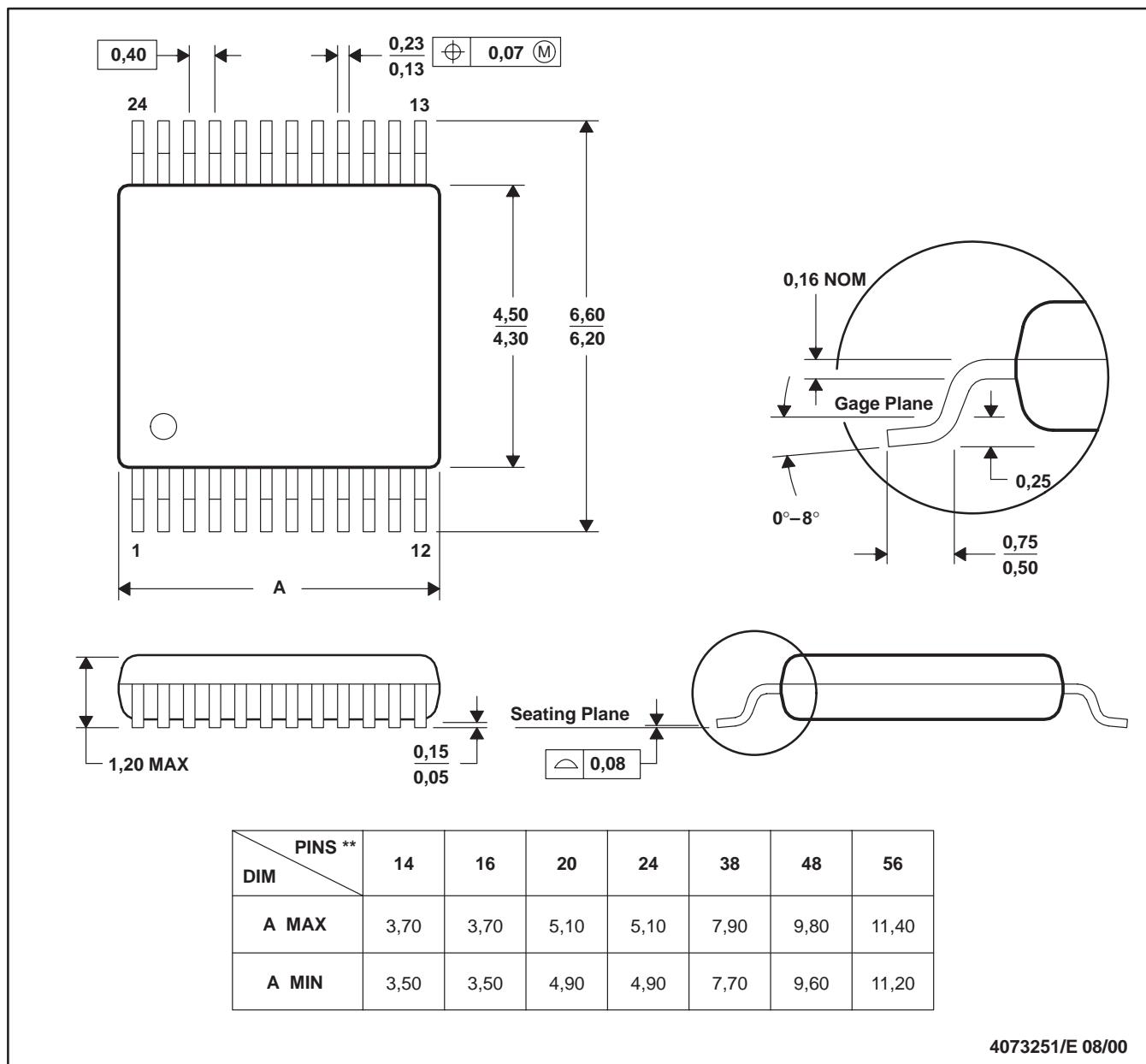
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

4040062/C 03/03

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 - D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

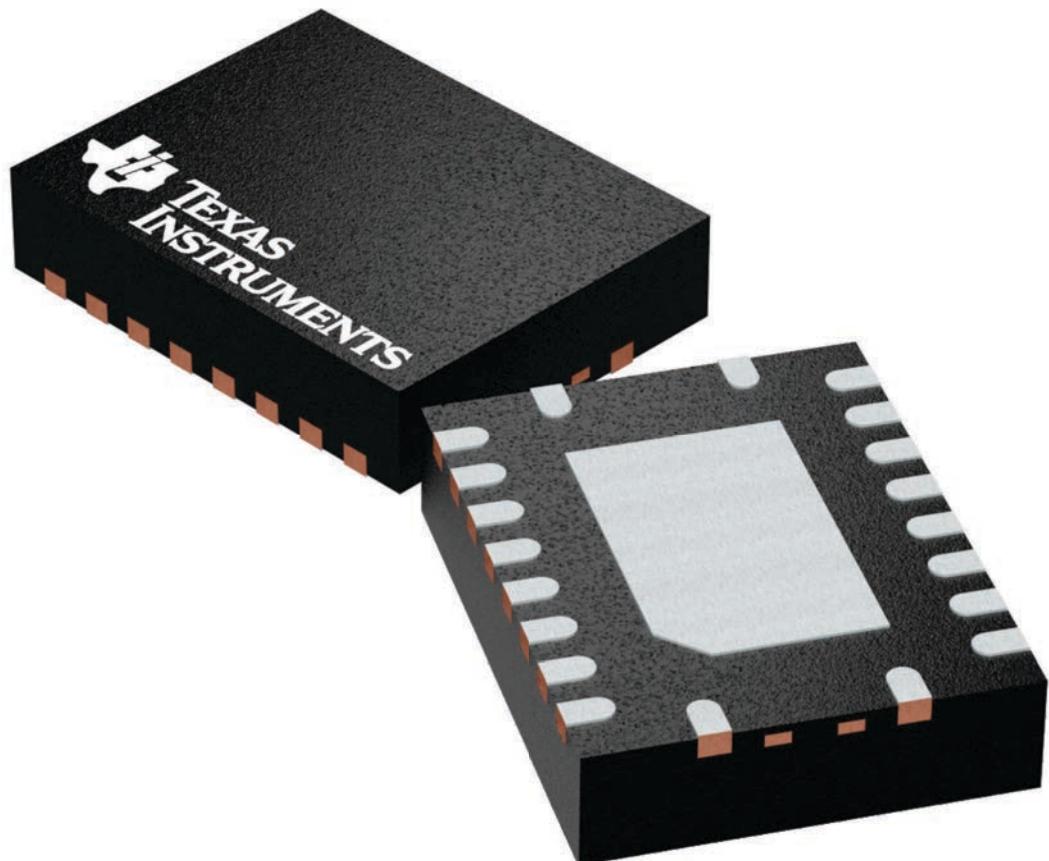
RGY 20

VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

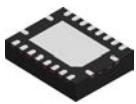
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225264/A

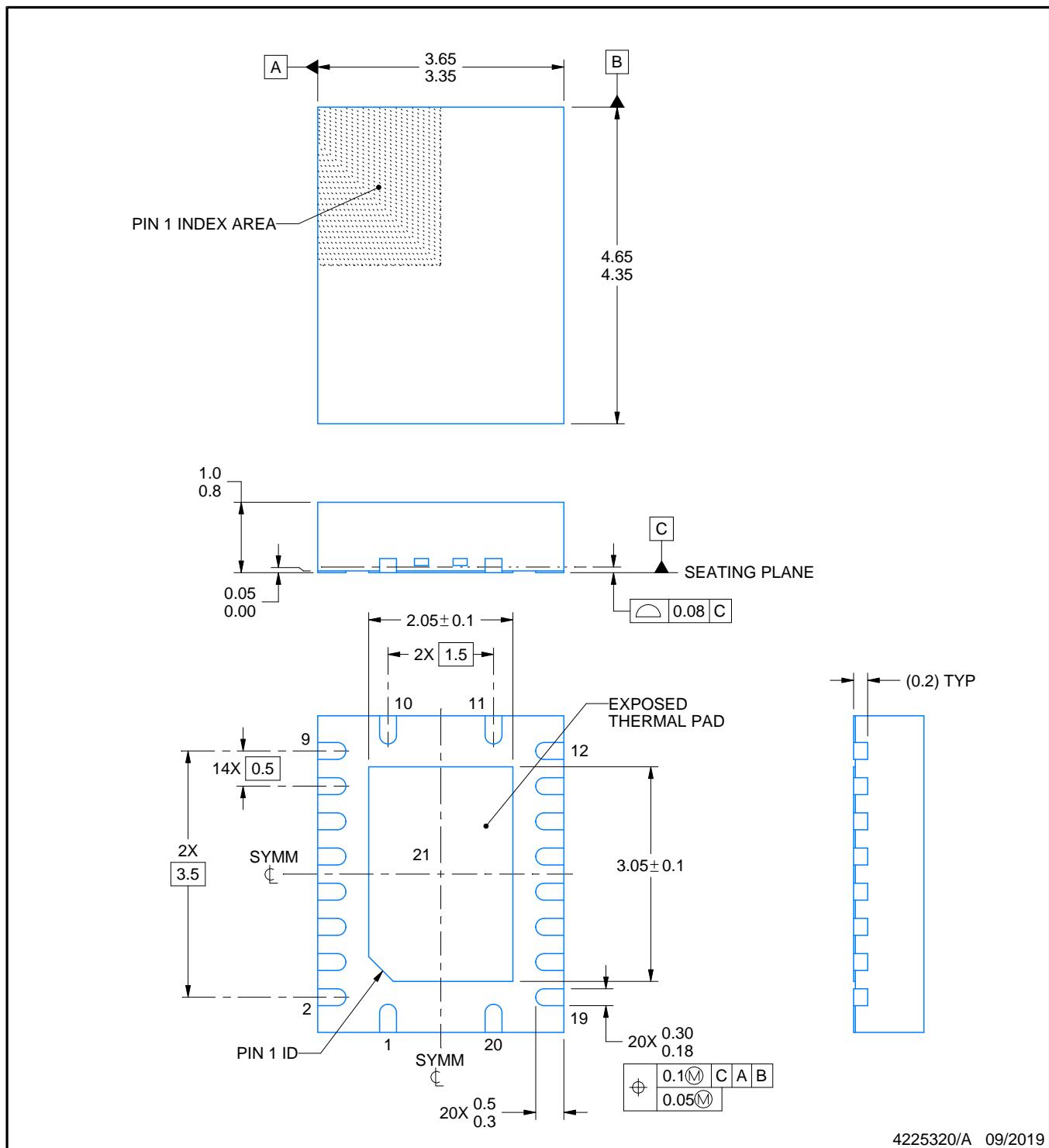
PACKAGE OUTLINE

RGY0020A



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4225320/A 09/2019

NOTES:

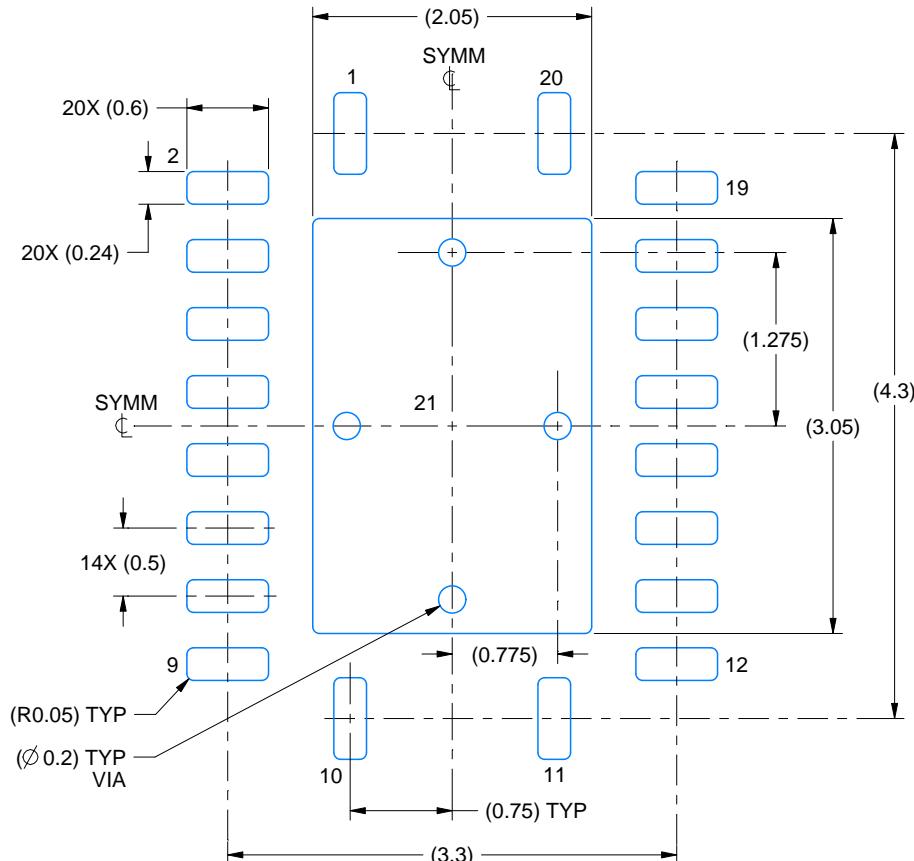
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

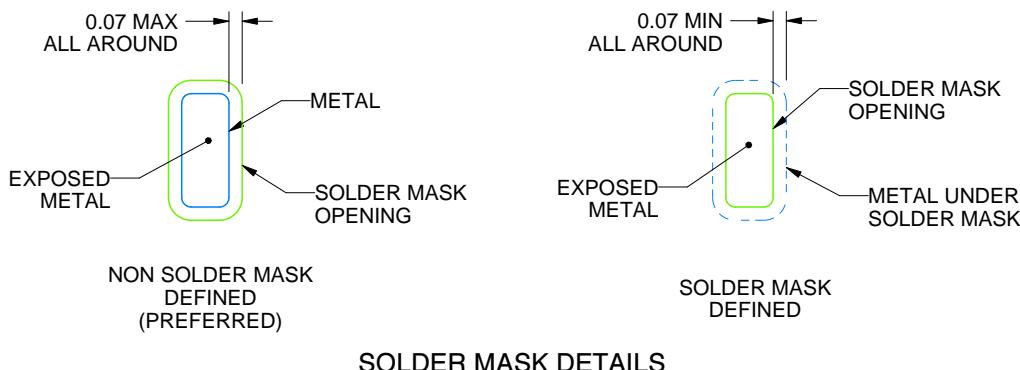
RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

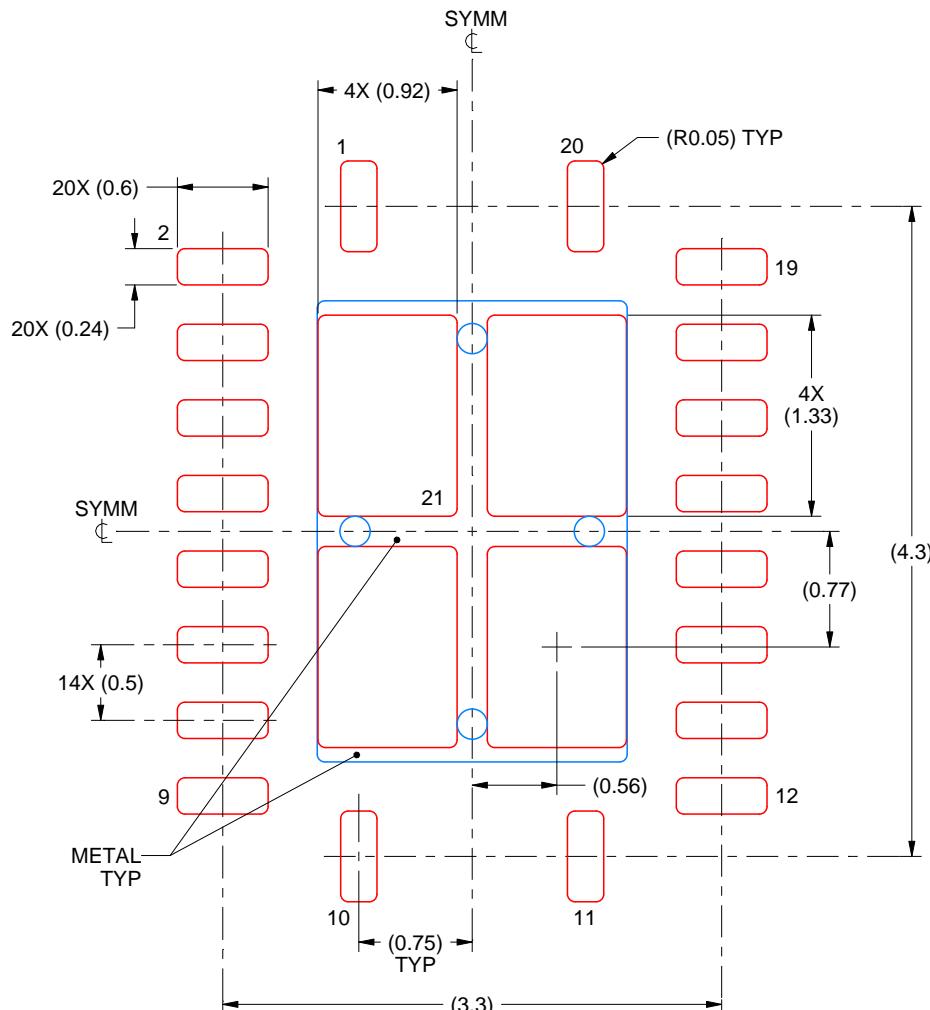
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225320/A 09/2019

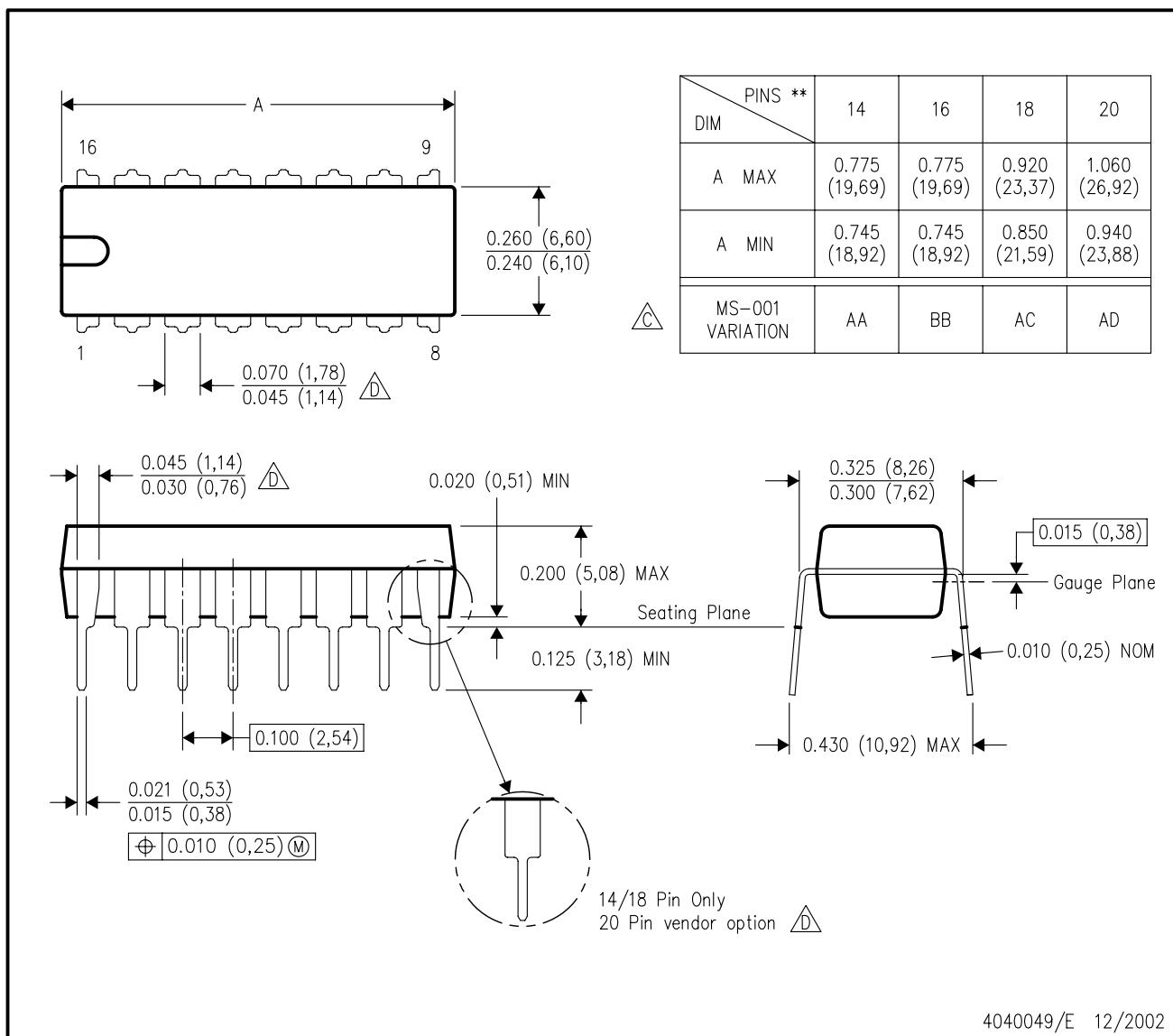
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



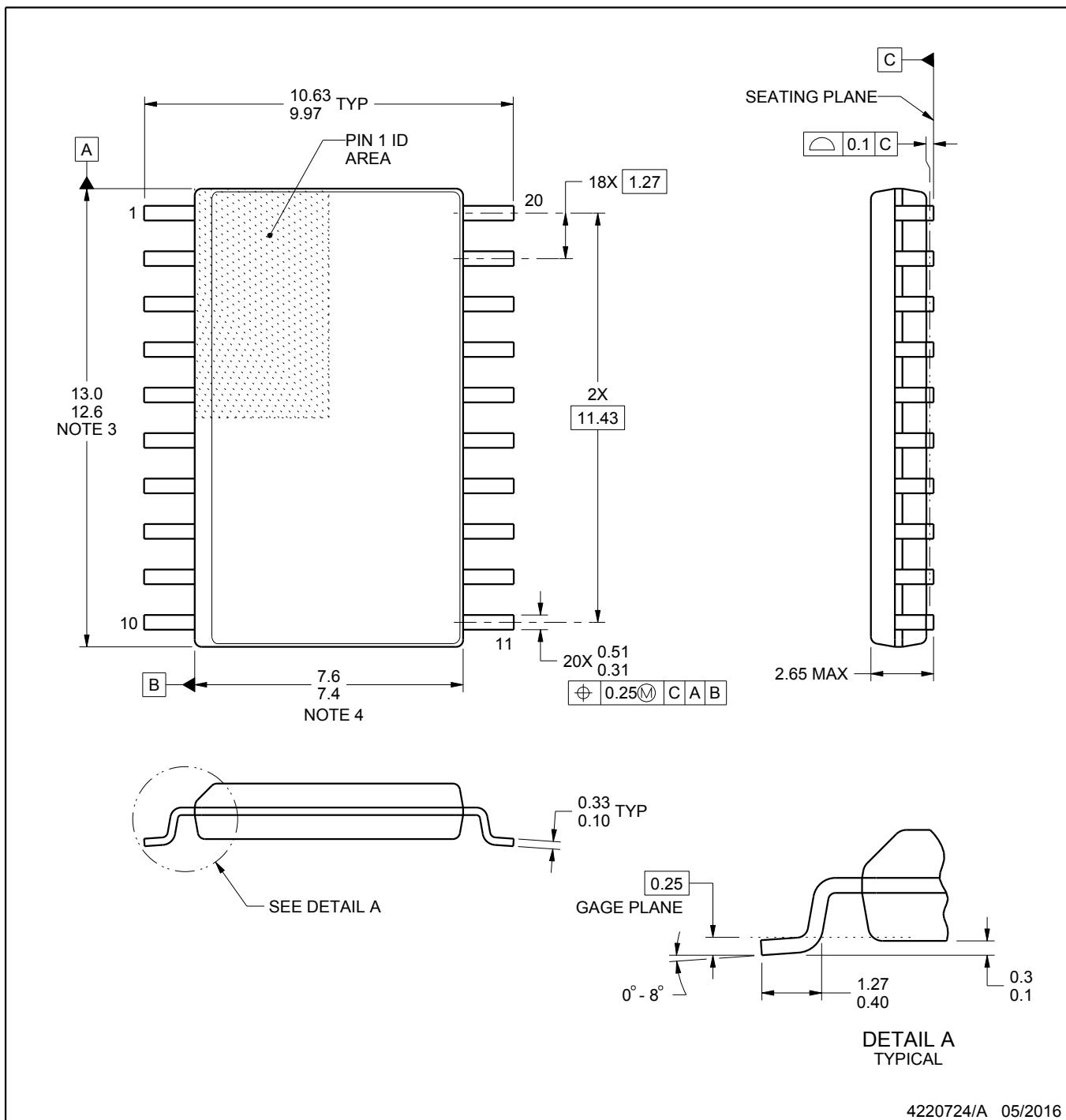
PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



NOTES:

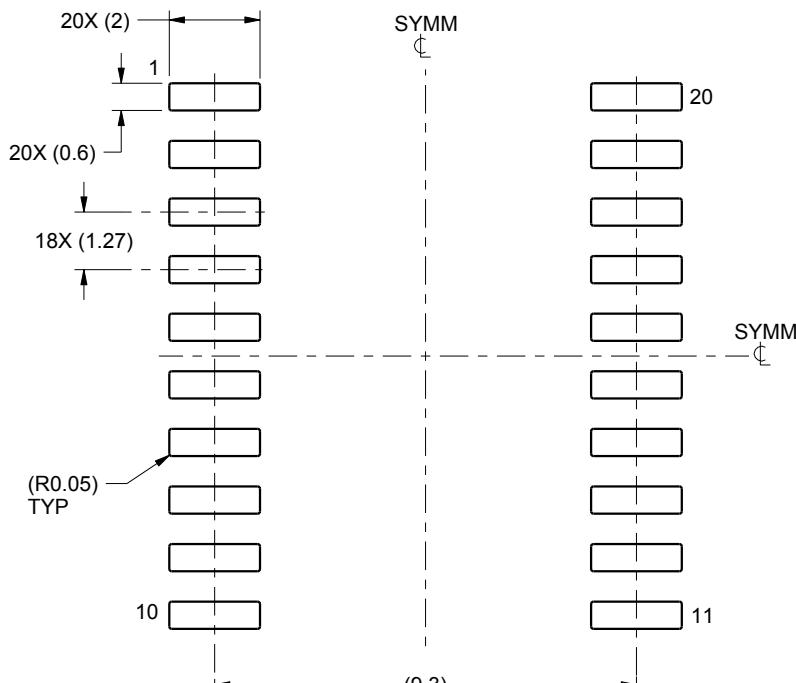
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

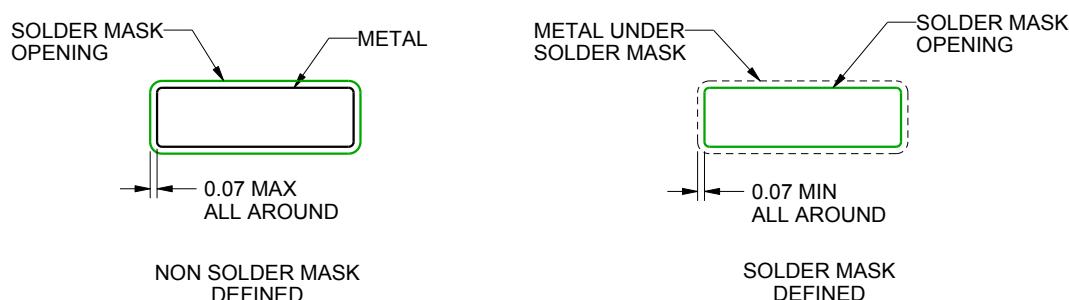
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

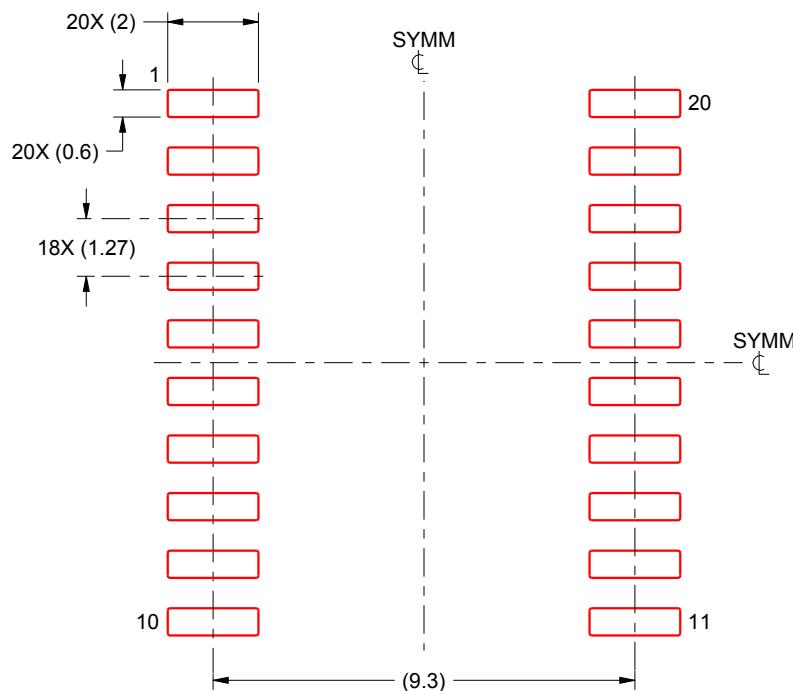
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated