



# BUK6D56-60E

60 V, N-channel Trench MOSFET

3 April 2019

Product data sheet

## 1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Extended temperature range  $T_j = 175^\circ\text{C}$
- Side wettable flanks for optical solder inspection
- ElectroStatic Discharge (ESD) protection > 2 kV HBM (class H2)
- Trench MOSFET technology
- AEC-Q101 qualified

## 3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

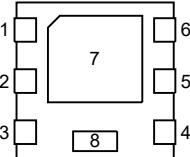
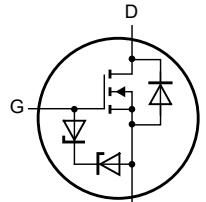
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25^\circ\text{C}$	-	-	60	60	V
$V_{GS}$	gate-source voltage		-20	-	20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{sp} = 25^\circ\text{C}$	-	-	11	11	A
$P_{tot}$	total power dissipation	$T_{sp} = 25^\circ\text{C}$	-	-	15	15	W
<b>Static characteristics</b>							
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 4\text{ A}; T_j = 25^\circ\text{C}$	-	42	56	56	$\text{m}\Omega$

## 5. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 Transparent top view	 017aaa255
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

## 6. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
BUK6D56-60E	DFN2020MD-6	plastic, leadless thermal enhanced ultra thin small outline package; 6 terminals; 0.65 mm pitch; 2 mm x 2 mm x 0.65 mm body	SOT1220

## 7. Marking

**Table 4. Marking codes**

Type number	Marking code
BUK6D56-60E	4V

## 8. Limiting values

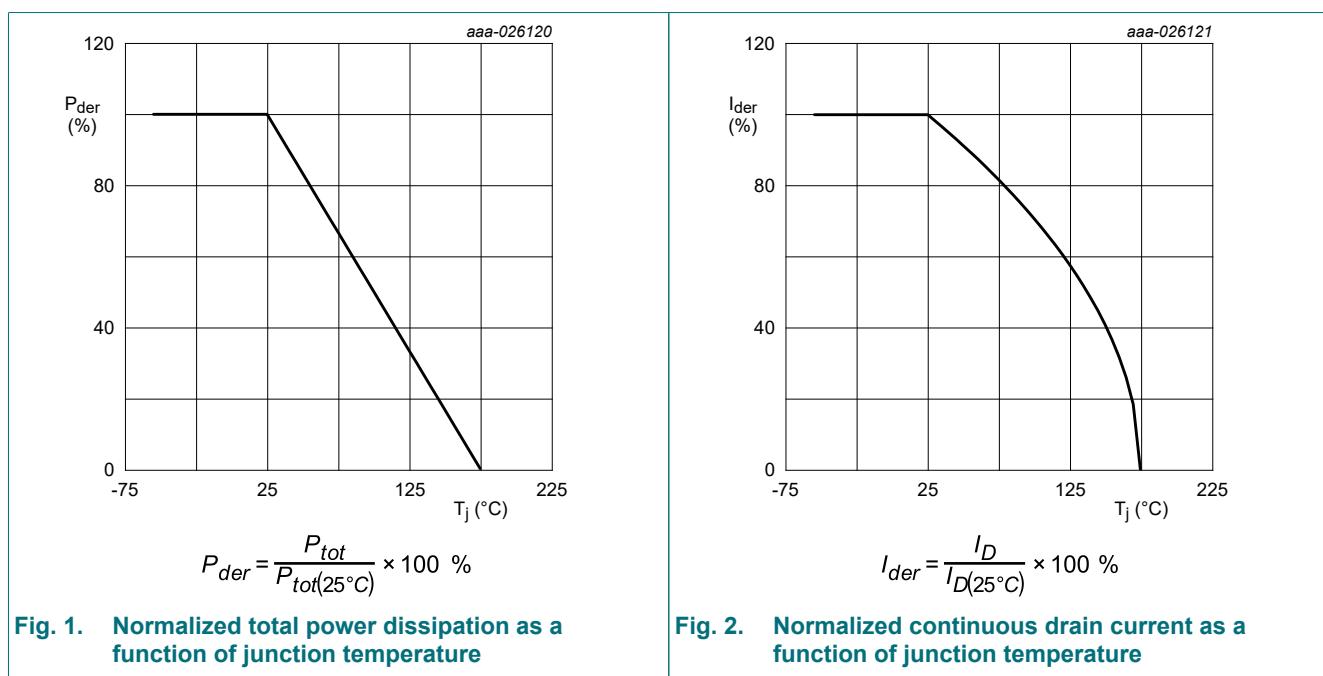
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C	-	60	60	V
V <sub>GS</sub>	gate-source voltage		-20	20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>sp</sub> = 25 °C	-	11	11	A
		V <sub>GS</sub> = 10 V; T <sub>sp</sub> = 100 °C	-	8	8	A
		V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 25 °C	[1]	-	4	A
I <sub>DM</sub>	peak drain current	T <sub>sp</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 µs	-	-	44	A
P <sub>tot</sub>	total power dissipation	T <sub>sp</sub> = 25 °C	-	15	15	W
		T <sub>amb</sub> = 25 °C	[1]	-	2	W
T <sub>j</sub>	junction temperature		-	-55	175	°C
T <sub>amb</sub>	ambient temperature		-	-55	175	°C
T <sub>stg</sub>	storage temperature		-	-65	175	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>sp</sub> = 25 °C	-	11	11	A
		T <sub>amb</sub> = 25 °C	[1]	-	2	A
I <sub>SM</sub>	peak source current	single pulse; t <sub>p</sub> ≤ 10 µs; T <sub>sp</sub> = 25 °C	-	-	44	A
<b>ESD maximum rating</b>						
V <sub>ESD</sub>	electrostatic discharge voltage	HBM	[2]	-	2000	V
<b>Avalanche ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 0.5 A; DUT in avalanche (unclamped)	-	-	15	mJ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

[2] Measured between all pins.



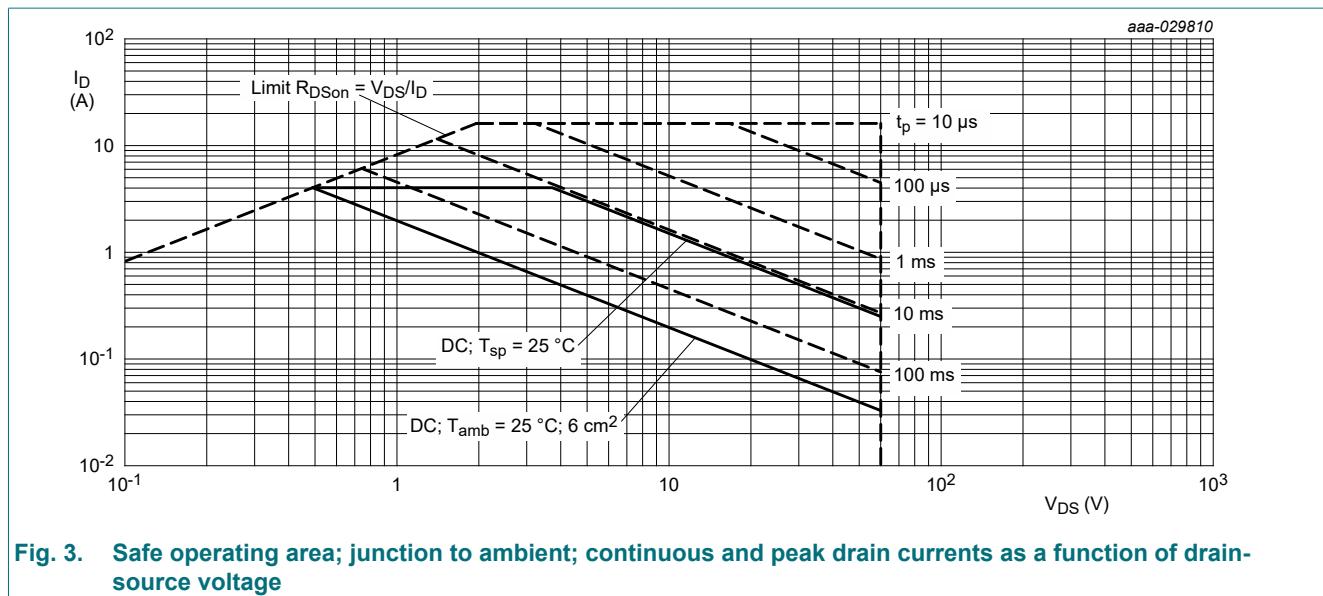


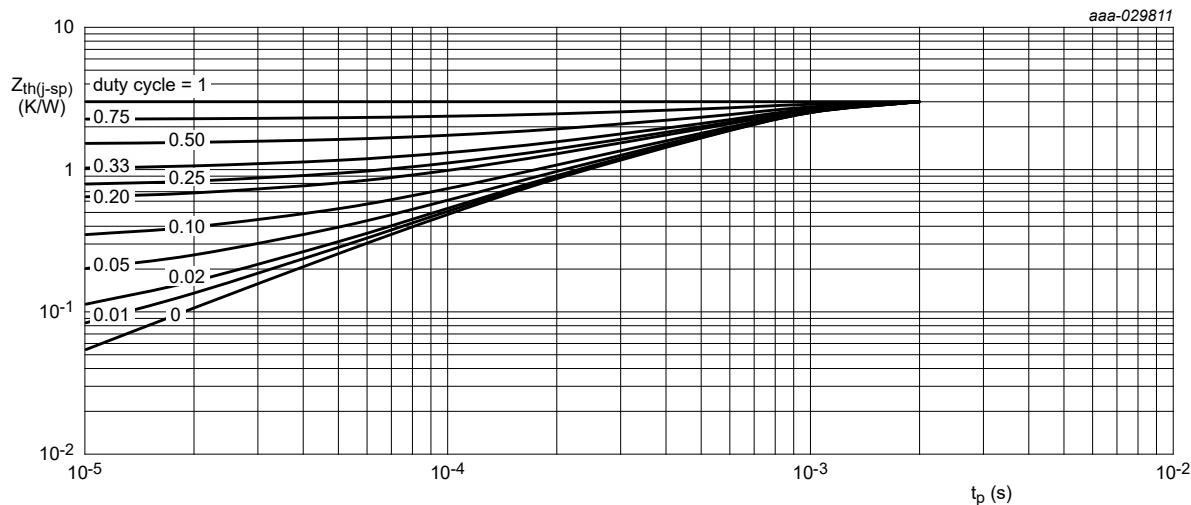
Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

## 9. Thermal characteristics

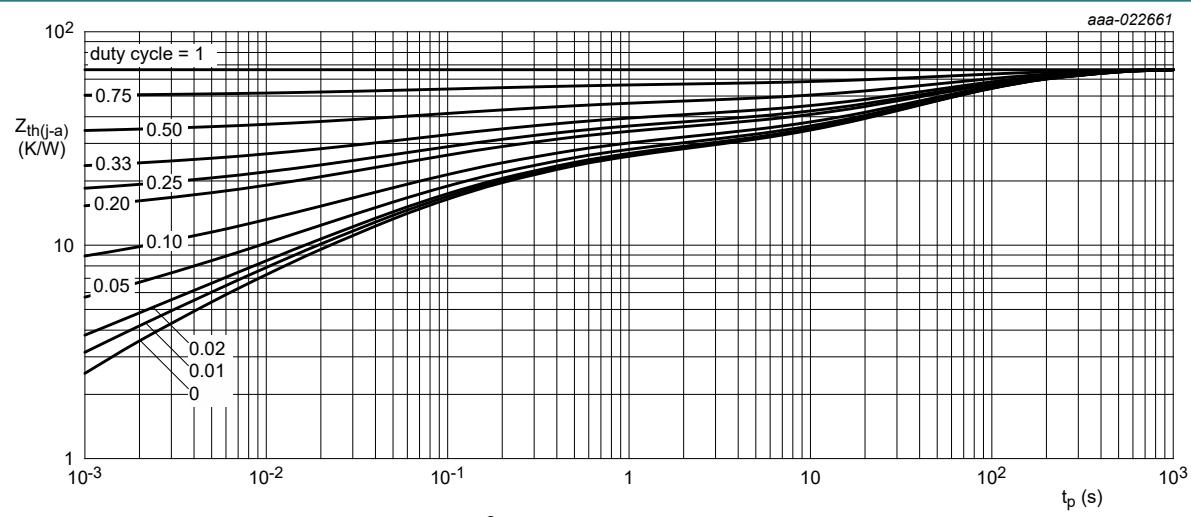
**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	66	76	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	5	10	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.



**Fig. 4. Transient thermal impedance from junction to solder point as a function of pulse duration; typical values**



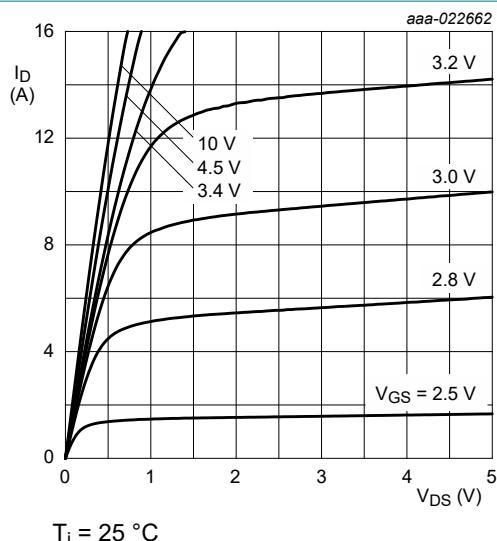
FR4 PCB, mounting pad for drain 6 cm<sup>2</sup>

**Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

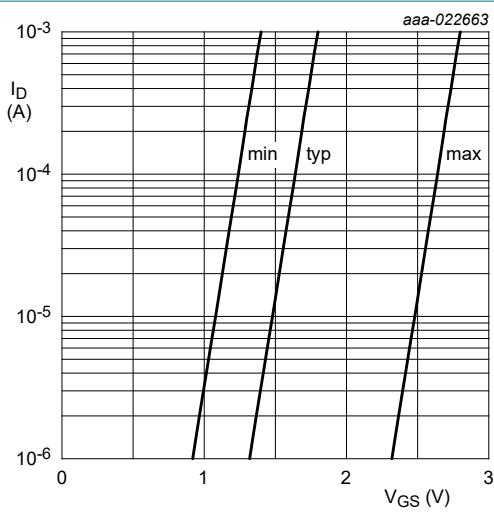
## 10. Characteristics

**Table 7. Characteristics**

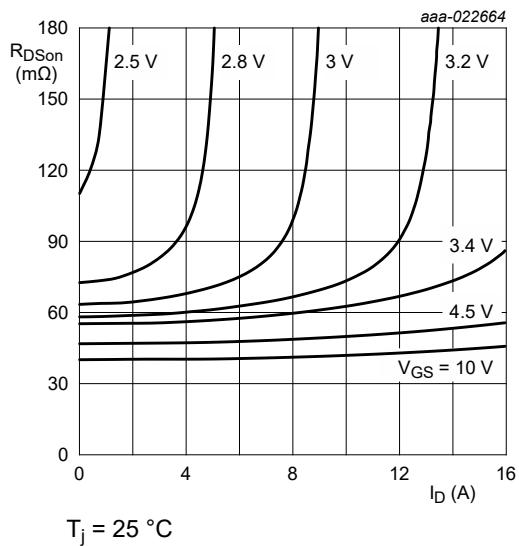
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Static characteristics</b>							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$		60	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25^\circ C$		1.3	1.7	2.7	V
$I_{DSS}$	drain leakage current	$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25^\circ C$		-	-	1	$\mu A$
		$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125^\circ C$		-	-	20	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	10	$\mu A$
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	-10	$\mu A$
		$V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	1	$\mu A$
		$V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	-1	$\mu A$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 4 A; T_j = 25^\circ C$		-	42	56	$m\Omega$
		$V_{GS} = 10 V; I_D = 4 A; T_j = 175^\circ C$		-	91	122	$m\Omega$
		$V_{GS} = 4.5 V; I_D = 3.6 A; T_j = 25^\circ C$		-	48	69	$m\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = 10 V; I_D = 4 A; T_j = 25^\circ C$		-	17	-	S
$R_G$	gate resistance	$f = 1 MHz$		-	2	-	$\Omega$
<b>Dynamic characteristics</b>							
$Q_{G(tot)}$	total gate charge	$V_{DS} = 30 V; I_D = 4 A; V_{GS} = 10 V; T_j = 25^\circ C$		-	7.5	12	nC
$Q_{GS}$	gate-source charge			-	1	-	nC
$Q_{GD}$	gate-drain charge			-	1.2	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 30 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25^\circ C$		-	435	-	pF
$C_{oss}$	output capacitance			-	47	-	pF
$C_{rss}$	reverse transfer capacitance			-	26	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 V; I_D = 4 A; V_{GS} = 10 V; R_{G(ext)} = 6 \Omega; T_j = 25^\circ C$		-	4.5	-	ns
$t_r$	rise time			-	4	-	ns
$t_{d(off)}$	turn-off delay time			-	13.5	-	ns
$t_f$	fall time			-	7	-	ns
<b>Source-drain diode</b>							
$V_{SD}$	source-drain voltage	$I_S = 2 A; V_{GS} = 0 V; T_j = 25^\circ C$		-	0.8	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 1.4 A; dI_S/dt = -100 A/\mu s; V_{GS} = 0 V; V_{DS} = 30 V; T_j = 25^\circ C$		-	13	-	ns
$Q_r$	recovered charge			-	6	-	nC



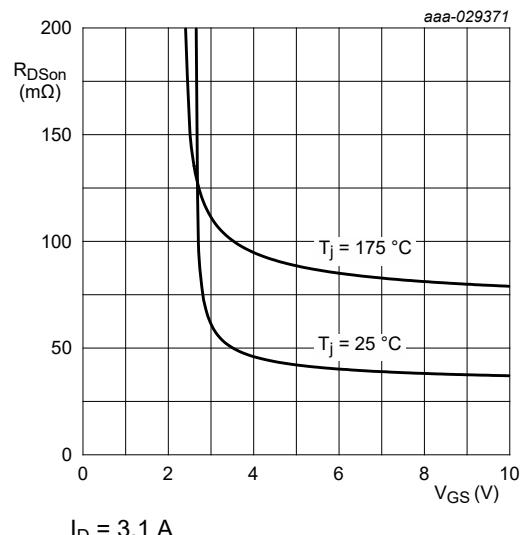
**Fig. 6.** Output characteristics: drain current as a function of drain-source voltage; typical values



**Fig. 7.** Sub-threshold drain current as a function of gate-source voltage



**Fig. 8.** Drain-source on-state resistance as a function of drain current; typical values



**Fig. 9.** Drain-source on-state resistance as a function of gate-source voltage; typical values

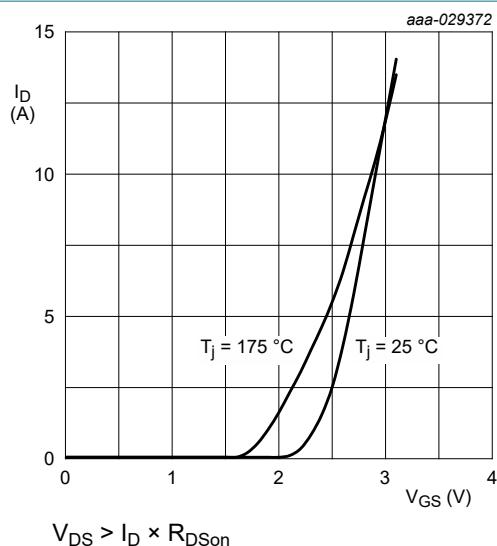


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

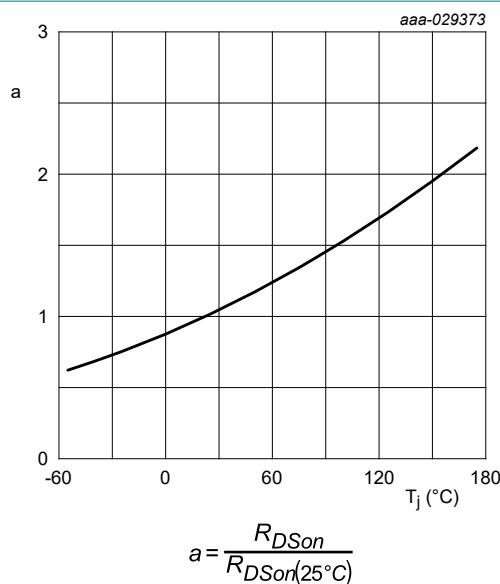


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

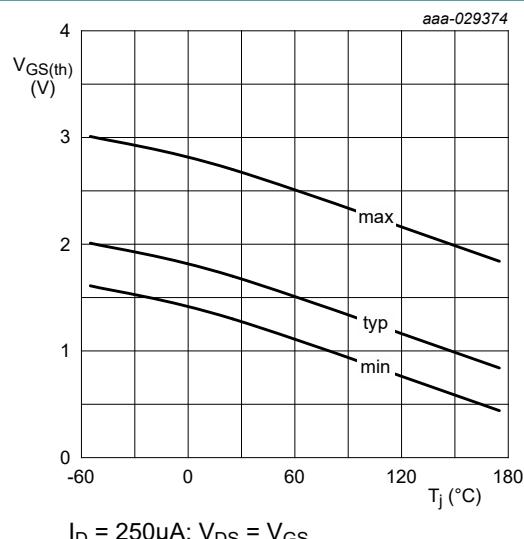


Fig. 12. Gate-source threshold voltage as a function of junction temperature

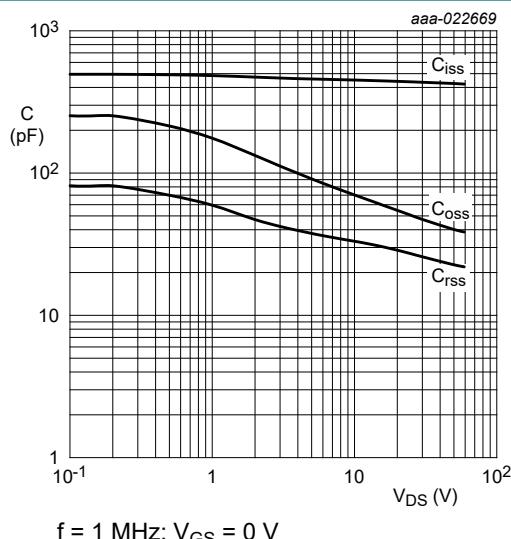
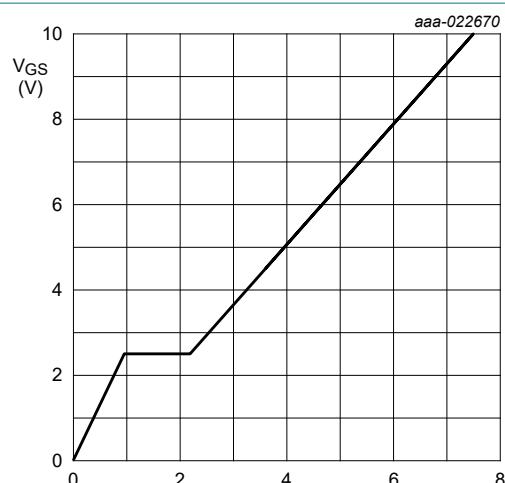


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = 30$  V;  $I_D = 4$  A

Fig. 14. Gate-source voltage as a function of gate charge; typical values

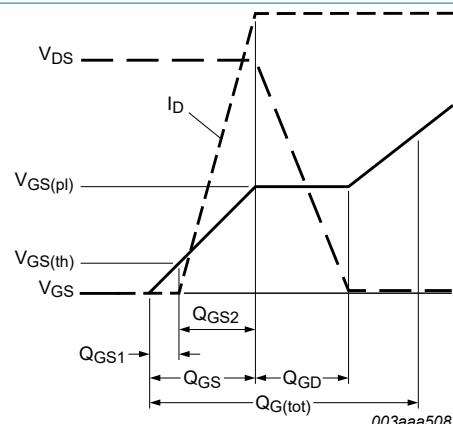
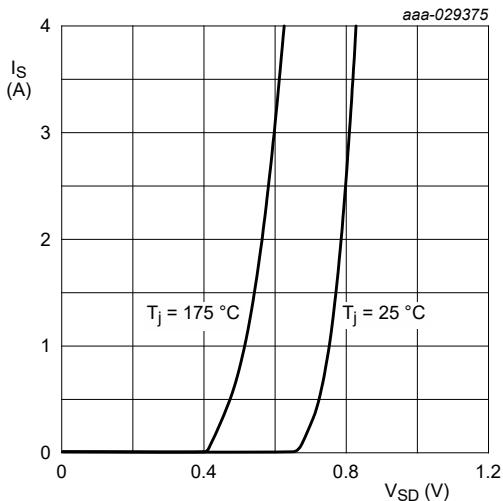


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0$  V

Fig. 16. Source current as a function of source-drain voltage; typical values

## 11. Test information

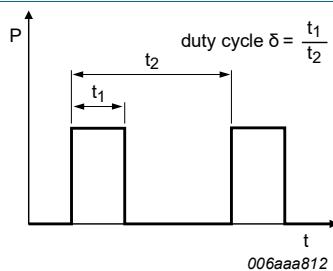


Fig. 17. Duty cycle definition

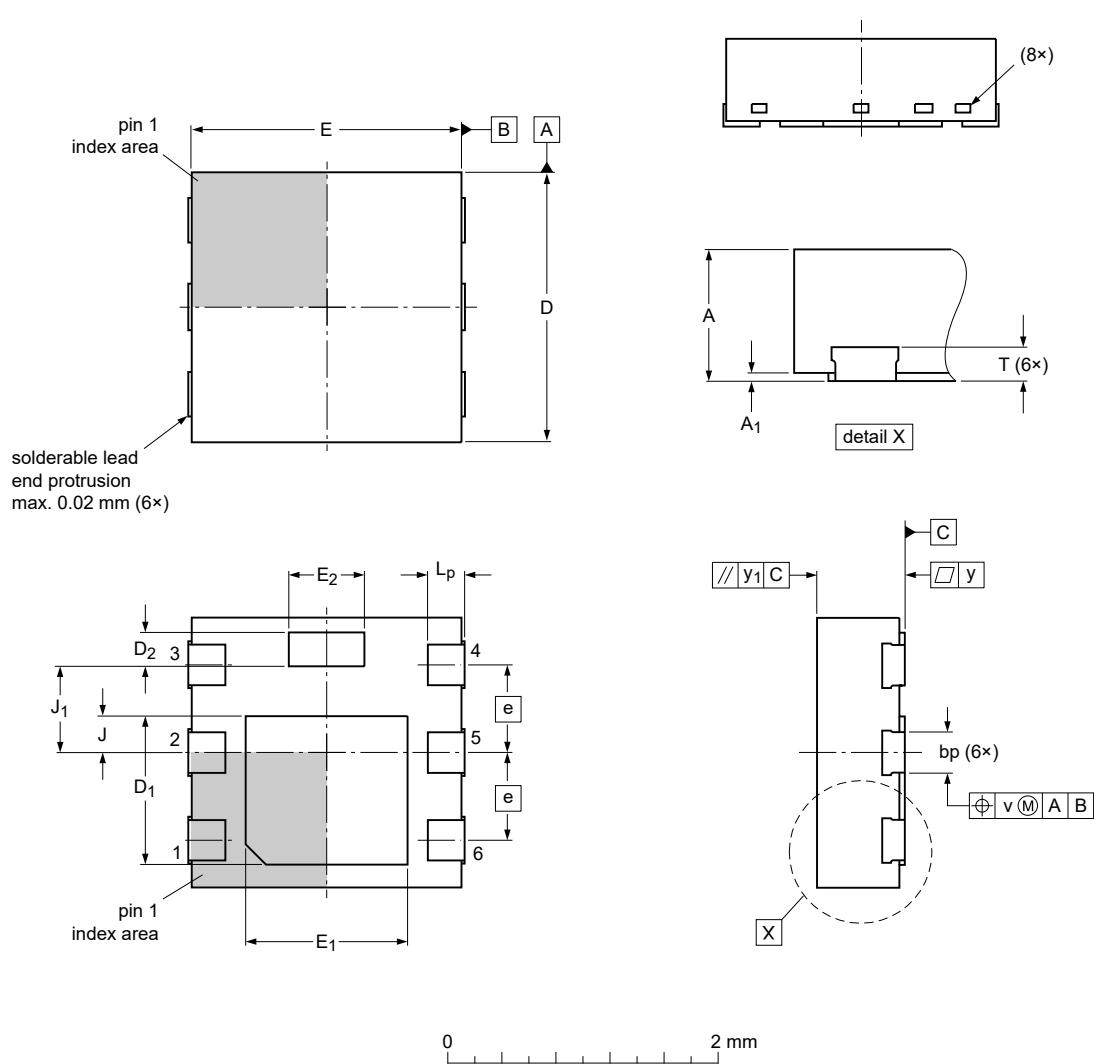
### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

## 12. Package outline

DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm

SOT1220



Dimensions (mm are the original dimensions)

0 2 mm  
scale

Unit	A	A <sub>1</sub>	bp	D	D <sub>1</sub>	D <sub>2</sub>	E	E <sub>1</sub>	E <sub>2</sub>	e	J	J <sub>1</sub>	L <sub>p</sub>	T	v	y	y <sub>1</sub>
mm																	
min		0.25	1.9	1.0	0.2	1.9	1.1	0.51					0.2	0.10			
nom		0.40	0.35	0.35	0.27	0.21	0.27	0.27	0.64	0.65	0.27	0.64	0.2	0.16	0.1	0.05	0.1
max	0.65	0.04	0.35	2.1	1.2	0.3	2.1	1.3	0.61				0.3	0.22			

Note

1. Dimension A is including plating thickness.

sot1220\_po

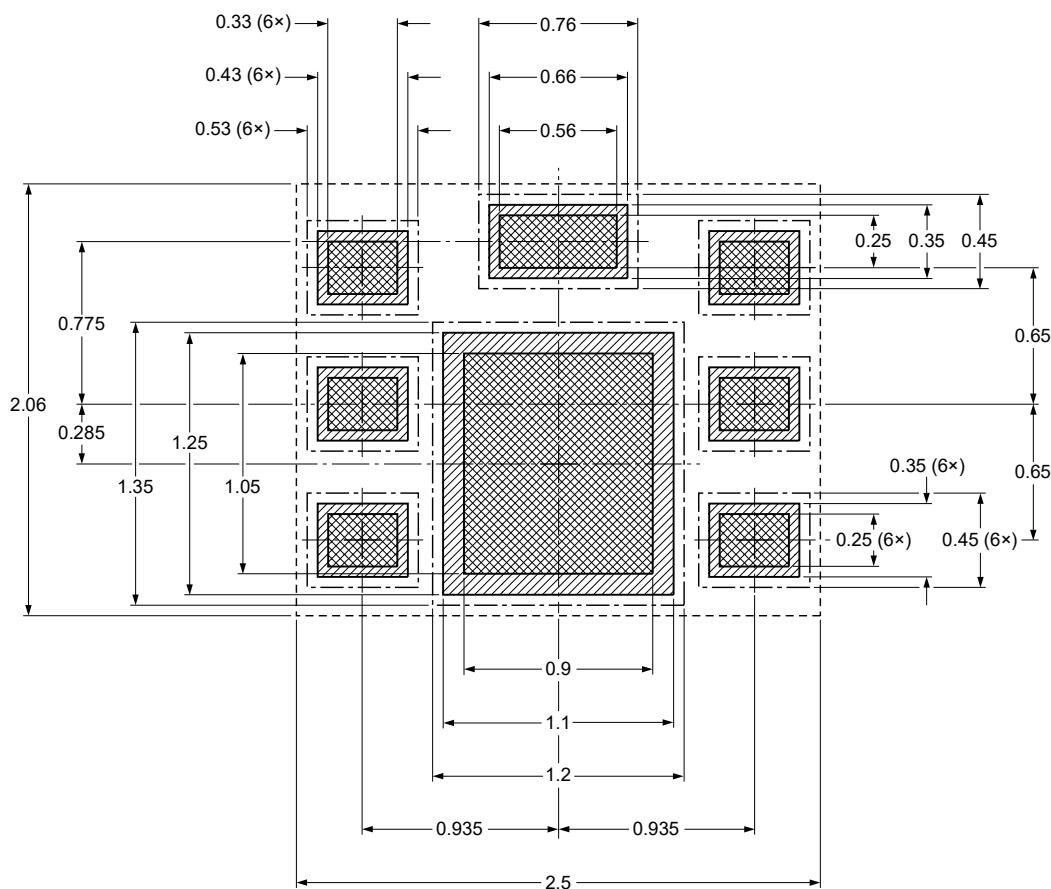
Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1220					-18-05-30- 18-06-07

Fig. 18. Package outline DFN2020MD-6 (SOT1220)

## 13. Soldering

Footprint information for reflow soldering of DFN2020MD-6 package

SOT1220



solder land

solder land plus solder paste

solder paste deposit

solder resist

--- occupied area

Dimensions in mm

sot1220\_fr

**Fig. 19. Reflow soldering footprint for DFN2020MD-6 (SOT1220)**

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BUK6D56-60E v.1	20190403	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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