

## High Performance, Polyphase Energy, and Class S Power Quality Monitoring IC

### FEATURES

- ▶ 7 high performance, 24-bit Σ-Δ ADCs
  - ▶ 101 dB SNR at 8 kSPS with PGA = 1
  - ▶ Wide input voltage range:  $\pm 1$  V, 707 mV rms full scale at gain = 1
  - ▶ Differential inputs
- ▶  $\pm 25$  ppm/ $^{\circ}$ C maximum channel drift (including ADC, internal  $V_{REF}$ , PGA drift) enabling 10000:1 dynamic input range, Class 0.2 metrology with standard external components
- ▶ With the optional ADSW-PQ-CLS Power Quality Library, the complete IEC 61000-4-30 Class S power quality standard is implemented including:
  - ▶ Power frequency 10 sec average
  - ▶ Magnitude of the supply
  - ▶ Dips and swells
  - ▶ Interruptions
  - ▶ Rapid voltage change
  - ▶ Flicker
  - ▶ Mains signaling voltage
  - ▶ Underdeviation and overdeviation
  - ▶ Voltage and current
    - ▶ Magnitude
    - ▶ Harmonics
    - ▶ Interharmonics
    - ▶ Unbalance
    - ▶ THD
    - ▶ Waveform recording
- ▶ Optional ADSW-PQ-CLS Power Quality Library compatible with ARM<sup>®</sup> Cortex microcontrollers
- ▶ VRMS one-cycle and IRMS one-cycle refreshed each cycle
- ▶ VRMS and IRMS filtered and updated every sample
- ▶ 10 cycle rms/12 cycle rms
- ▶ Period registers to calculate line frequency, one per phase
- ▶ Zero crossing and zero-crossing timeout
- ▶ Phase angle measurements
- ▶ Supports CTs
- ▶ Multipoint phase and gain compensations for CTs
- ▶ Rogowski coils with the addition of an external analog integrator
- ▶ Continuous resampled data available
- ▶ Waveform buffer
- ▶ Advanced metrology feature set
  - ▶ Total and fundamental active power, volt amperes reactive (VAR), volt amperes (VA), watthour, VAR hour, and VA hour
- ▶ Total and fundamental IRMS and VRMS
- ▶ Power factor
- ▶ Supports active energy standards: IEC 62053-21 and IEC 62053-22, EN50470-3, OIML R46, and ANSI C12.20
- ▶ Supports reactive energy standards: IEC 62053-23 and IEC 62053-24
- ▶ High speed communication port: 20 MHz SPI
- ▶ Integrated temperature sensor with 12-bit successive approximation register (SAR) ADC
- ▶  $\pm 3$ °C accuracy from  $-40$ °C to  $+85$ °C

### APPLICATIONS

- ▶ Energy and power monitoring
- ▶ Standards compliant power quality monitoring
- ▶ Protective devices
- ▶ Machine health
- ▶ Smart power distribution units
- ▶ Polyphase energy meters

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**REVISION HISTORY****5/2022—Revision 0: Initial Version**

## GENERAL DESCRIPTION

The ADE9430 is a highly accurate, fully integrated, polyphase energy and power quality monitoring device. Superior analog performance and a digital signal processing (DSP) core enable accurate energy monitoring over a wide dynamic range. An integrated high end reference ensures low drift over temperature with a combined drift of less than  $\pm 25 \text{ ppm}/^\circ\text{C}$  maximum for the entire channel including a programmable gain amplifier (PGA) and an analog-to-digital converter (ADC).

The ADE9430 offers a complete power quality monitoring capability by providing instantaneous total as well as fundamental measurements on rms, frequency, phase angle, power factor active, reactive, and apparent powers and energies. Using the optional ADSW-PQ-CLS Power Quality Library, advanced power quality features, such as dip and swell monitoring, power frequency, voltage total harmonic distortion (VTHD), and current total harmonic distortion (ITHD), are enabled. The one cycle rms, 10 cycle rms/12 cycle rms, and the optional ADSW-PQ-CLS Power Quality Library features are calculated according to IEC 61000-4-30 Class S. To request access to the ADSW-PQ-CLS, fill out the software request form at: [Software Request Form | Analog Devices](#), where the target technology must be power quality monitoring and the processor/system on chip (SoC) is the ADE9430.

The ADE9430 offers a resampled waveform of 1024 points per 10 cycles or 12 cycles. Resampling simplifies the fast Fourier transform (FFT) calculation of at least 40 harmonics in an external processor.

The ADE9430 simplifies the implementation and certification of energy and power quality monitoring systems by providing tight integration of acquisition and calculation engines. The integrated ADCs and DSP engine calculate various parameters and provide data through user accessible registers or indicate events through interrupt pins. With seven dedicated ADC channels, the ADE9430 can be used on a 3-phase system or up to three single-phase systems. This device supports current transformers (CTs) or Rogowski coils when used with external analog integrator for current measurements.

The ADE9430 absorbs most of the complexity in calculations for a power quality monitoring system. Combining a simple host microcontroller and the optional ADSW-PQ-CLS Power Quality Library, the ADE9430 enables the design of standalone monitoring or protection systems, or low cost nodes uploading data into the cloud.

Note that throughout this data sheet, multifunction pins, such as CF4/EVENT/DREADY, are referred to either by the entire pin name or by a single function of the pin, for example, EVENT, when only that function is relevant.

## TYPICAL APPLICATIONS CIRCUIT

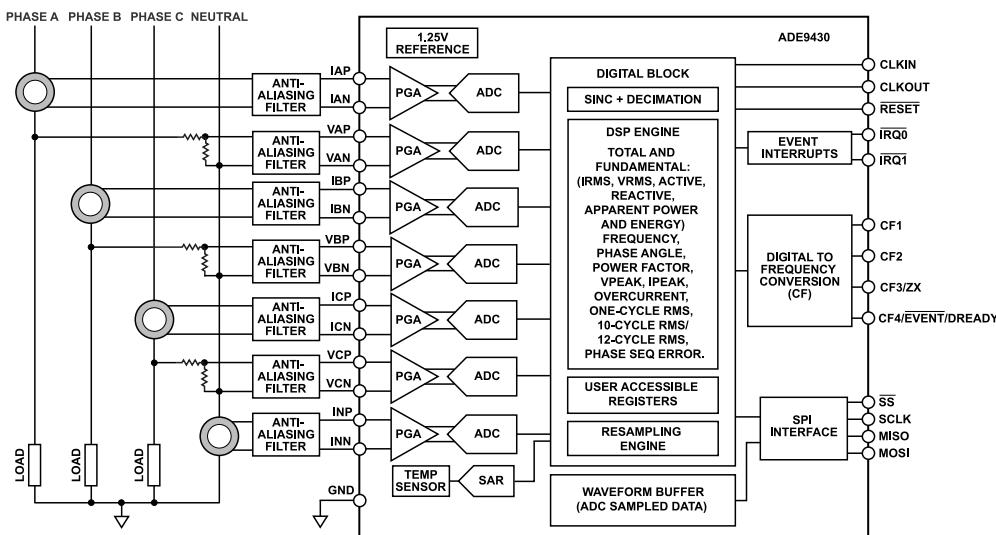


Figure 1. Typical Application Circuit

**SPECIFICATIONS**

V<sub>DD</sub> = 2.97 V to 3.63 V, GND = AGND = DGND = 0 V, on-chip reference, CLKIN = 24.576 MHz crystal (XTAL), T<sub>MIN</sub> to T<sub>MAX</sub> = -40°C to +85°C, and T<sub>A</sub> = 25°C (typical), unless otherwise noted.

**Table 1.**

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY (MEASUREMENT ERROR PER PHASE)					
Total Active Energy	0.1			%	Over a dynamic range of 5000 to 1, 10 sec accumulation
	0.2			%	Over a dynamic range of 10,000 to 1, 20 sec accumulation
Total Reactive Energy	0.1			%	Over a dynamic range of 5000 to 1, 10 sec accumulation
	0.2			%	Over a dynamic range of 10,000 to 1, 20 sec accumulation
Total Apparent Energy	0.1			%	Over a dynamic range of 1000 to 1, 2 sec accumulation
	0.5			%	Over a dynamic range of 5000 to 1, 10 sec accumulation
Fundamental Active Energy	0.1			%	Over a dynamic range of 5000 to 1, 2 sec accumulation
	0.2			%	Over a dynamic range of 10,000 to 1, 10 sec accumulation
Fundamental Reactive Energy	0.1			%	Over a dynamic range of 5000 to 1, 2 sec accumulation
	0.2			%	Over a dynamic range of 10,000 to 1, 10 sec accumulation
Fundamental Apparent Energy	0.1			%	Over a dynamic range of 5000 to 1, 2 sec accumulation
	0.5			%	Over a dynamic range of 10,000 to 1, 10 sec accumulation
IRMS and VRMS	0.1			%	Over a dynamic range of 1000 to 1
	0.5			%	Over a dynamic range of 5000 to 1
Fundamental IRMS, VRMS	0.1			%	Over a dynamic range of 1000 to 1
	0.5			%	Over a dynamic range of 5000 to 1
Active Power, VAR, VA	0.2			%	Over a dynamic range of 1000 to 1
	0.4			%	Over a dynamic range of 3000 to 1
Power Factor (PF) Error	±0.001			%	Over a dynamic range of 5000 to 1
128-Point per Line Cycle or 1024 Point over 10 Cycles Resampled Data	0.1			%	An FFT is performed to receive the magnitude response; this error is the worst case error in the magnitude caused by the resampling algorithm distortion; the input signal is 50 Hz fundamental and ninth harmonic both at half of full scale
	-72			dB	Amplitude of highest spur; input signal is 50 Hz fundamental and ninth harmonic both at half of full scale
	1.25			%	An FFT is performed to receive the magnitude response; this error is the worst case error in the magnitude caused by resampling algorithm distortion; input signal is 50 Hz fundamental and 31 <sup>st</sup> harmonic, both at half of full scale
	-38			dB	Amplitude of highest spur; input signal is 50 Hz fundamental and 31 <sup>st</sup> harmonic, both at half of full scale
10 Cycle/12 Cycle IRMS and VRMS <sup>1</sup>	0.2			%	Data sourced before high-pass filter (HPF), no dc offset at inputs, over a dynamic range of 100 to 1
VRMS and IRMS 1 Cycle	0.2%			%	Data sourced before HPF, no dc offset at inputs, over a dynamic range of 100 to 1
Line Period Measurement	0.001			Hz	Resolution at 50 Hz
Current to Current, Voltage to Voltage, and Voltage to Current Angle Measurement	0.018			Degrees	Resolution at 50 Hz
ADC					
PGA Gain Settings (PGA_GAIN)		1, 2, or 4		V/V	PGA gain setting is referred to as the PGA_GAIN register
Differential Input Voltage Range (VxP to VxN, IxP to IxN)	-1/Gain		+1/Gain	V	707 mV rms, when V <sub>REF</sub> = 1.25 V, this voltage corresponds to 53 million codes
Maximum Operating Voltage on Analog Input Pins (VxP, VxN, IxP, and IxN)	-0.6		+0.6	V	Voltage on the pin with respect to ground (GND = AGND = DGND = REFGND)
Signal-to-Noise Ratio (SNR) <sup>2</sup>					
PGA = 1		96		dB	32 kSPS, sinc4 output, input voltage (V <sub>IN</sub> ) = -0.5 dB from half of full scale

**SPECIFICATIONS****Table 1.**

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PGA = 4		101		dB	8 kSPS, sinc4 + infinite impulse response (IIR), low-pass filter (LPF) output, $V_{IN} = -0.5$ dB from half of full scale
		93		dB	32 kSPS, sinc4 output
		96		dB	8 kSPS, sinc4 + IIR LPF output
Total Harmonic Distortion (THD) <sup>2</sup>					
PGA = 1	-101	-95		dB	32 kSPS, sinc4 output, $V_{IN} = -0.5$ dB from half of full scale
	-101	-95		dB	8 kSPS, sinc4 + IIR LPF output, $V_{IN} = -0.5$ dB from half of full scale
PGA = 4	-107	-99		dB	32 kSPS, sinc4 output
	-107	-99		dB	8 kSPS, sinc4 + IIR LPF output
Signal-to-Noise and Distortion Ratio					
PGA = 1	95			dB	32 kSPS, sinc4 output, $V_{IN} = -0.5$ dB from half of full scale
	98			dB	8 kSPS, sinc4 + IIR LPF output, $V_{IN} = -0.5$ dB from half of full scale
PGA = 4	93			dB	32 kSPS, sinc4 output
	96			dB	8 kSPS, sinc4 + IIR LPF output
Spurious-Free Dynamic Range (SFDR) <sup>2</sup>					
PGA = 1	100			dB	32 kSPS, sinc4 output, $V_{IN} = -0.5$ dB from half of full scale
	100			dB	8 kSPS, sinc4 + IIR LPF output, $V_{IN} = -0.5$ dB from half of full scale
Output Pass Band (0.1dB)					
Sinc4 Outputs	1.344			kHz	32 kSPS, sinc4 output
Sinc4 + IIR LPF Outputs	1.344			kHz	8 kSPS output
Output Bandwidth (-3 dB) <sup>2</sup>					
Sinc4 Outputs	7.2			kHz	32 kSPS, sinc4 output
Sinc4 + IIR LPF Outputs	3.2			kHz	8 kSPS output
Crosstalk <sup>2</sup>	-120			dB	At 50 Hz or 60 Hz, see the <a href="#">Terminology</a> section
AC Power Supply Rejection Ratio (AC PSRR) <sup>2</sup>	-120			dB	At 50 Hz, see the <a href="#">Terminology</a> section
Common-Mode Rejection Ratio (AC CMRR) <sup>2</sup>	115			dB	At 100 Hz and 120 Hz
Gain Error	±0.3	±1		%Typ	See the <a href="#">Terminology</a> section
Gain Drift <sup>2</sup>	±3			ppm/°C	See the <a href="#">Terminology</a> section
Offset	±0.040	±3.8		mV	See the <a href="#">Terminology</a> section
Offset Drift <sup>2</sup>	0	±2		µV/°C	See the <a href="#">Terminology</a> section
Channel Drift (PGA, ADC, and Internal Voltage Reference ( $V_{REF}$ ))	±7	±25		ppm/°C	PGA = 1, internal $V_{REF}$
	±7	±25		ppm/°C	PGA = 2, internal $V_{REF}$
	±7	±25		ppm/°C	PGA = 4, internal $V_{REF}$
Differential Input Impedance (DC)	165	185		kΩ	PGA = 1, see the <a href="#">Terminology</a> section
	80	90		kΩ	PGA = 2
	40	45		kΩ	PGA = 4
INTERNAL VOLTAGE REFERENCE					Nominal = 1.25 V ± 1 mV
Voltage Reference	1.250			V	$T_A = 25^\circ\text{C}$ , REF pin
Temperature Coefficient <sup>2</sup>	±5	±20		ppm/°C	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ , tested during device characterization
EXTERNAL VOLTAGE REFERENCE					
Input Voltage (REF)	1.2 or 1.25			V	REFGND must be tied to GND, AGND, and DGND, a 1.25 V external reference is preferred; the half of full-scale values mentioned in this data sheet are for a voltage reference of 1.25 V
Input Impedance	7.5			kΩ	

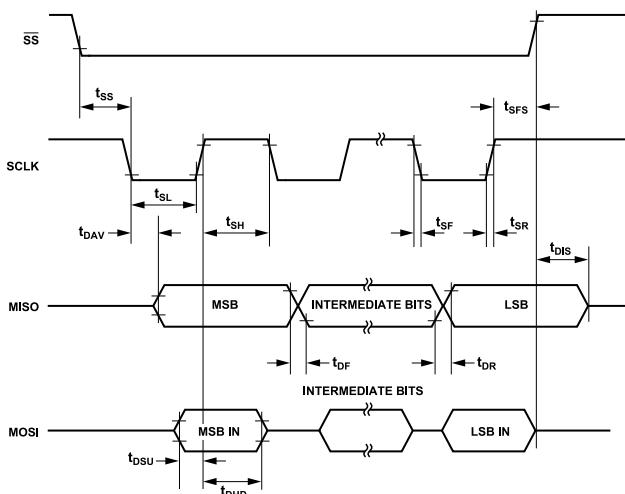
**SPECIFICATIONS****Table 1.**

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE SENSOR					
Temperature Accuracy		$\pm 2$		°C	-10°C to +40°C
		$\pm 3$		°C	-40°C to +85°C
Temperature Readout Step Size			0.3	°C	
CRYSTAL OSCILLATOR					All specifications use CLKIN = 24.576 MHz $\pm$ 30 ppm
Input Clock Frequency	24.33	24.576	24.822	MHz	
Internal Capacitance on CLKIN and CLKOUT		4		pF	
Internal Feedback Resistance Between CLKIN and CLKOUT		2.45		MΩ	
Transconductance ( $g_m$ )	5	8		mA/V	
EXTERNAL CLOCK INPUT					
Input Clock Frequency	24.330	24.576	24.822	MHz	$\pm 1\%$
Duty Cycle <sup>2</sup>	45:55	50:50	55:45	%	
CLKIN Logic Input Voltage					3.3 V tolerant
High, $V_{INH}$	1.2			V	$V_{DD} = 2.97$ V to 3.63 V
Low, $V_{INL}$			0.5	V	$V_{DD} = 2.97$ V to 3.63 V
LOGIC INPUTS (PM0, PM1, RESET, MOSI, SCLK, and SS)					
Input Voltage					
$V_{INH}$	2.4			V	
$V_{INL}$		0.8		V	
Input Current, $I_{IN}$		15		μA	$V_{IN} = 0$ V
Internal Capacitance, $C_{IN}$		10		pF	
LOGIC OUTPUTS					
MISO, IRQ0, and IRQ1					
Output Voltage					
High, $V_{OH}$	2.4			V	Source current ( $I_{SOURCE}$ ) = 4 mA
Low, $V_{OL}$		0.8		V	Sink current ( $I_{SINK}$ ) = 4 mA
$C_{IN}$		10		pF	
CF1, CF2, CF3, and CF4					
Output Voltage					
$V_{OH}$	2.4			V	$I_{SOURCE} = 7$ mA
$V_{OL}$		0.8		V	$I_{SINK} = 8$ mA
$C_{IN}$		10		pF	
LOW DROPOUT (LDO) REGULATORS					
Analog Supply Voltage ( $AV_{DD}$ )		1.9		V	
Digital Supply Voltage ( $DV_{DD}$ )		1.7		V	
POWER SUPPLY					
$V_{DD}$	2.97	3.3	3.63	V	Power-on reset (POR) level is 2.4 V to 2.6 V
Supply Current ( $I_{DD}$ )					
Power Save Mode 0 (PSM0)		15	17	mA	Normal mode
		14.5	16.5	mA	Normal mode, six ADCs enabled
Power Save Mode 3 (PSM3)		90	300	nA	Idle, $V_{DD} = 3.3$ V, $AV_{DD} = 0$ V, $DV_{DD} = 0$ V

<sup>1</sup> Enables implementation of IEC 61000-4-30 Class S.<sup>2</sup> Tested during device characterization.

**SPECIFICATIONS****TIMING CHARACTERISTICS****Table 2.**

Parameter	Symbol	Min	Typ	Max	Unit
SS to SCLK Edge	$t_{SS}$	10			ns
SCLK Frequency	$f_{SCLK}$			20	MHz
SCLK Low Pulse Width	$t_{SL}$	20			ns
SCLK High Pulse Width	$t_{SH}$	20			ns
Data Output Valid After SCLK Edge	$t_{DAV}$			20	ns
Data Input Setup Time Before SCLK Edge	$t_{DSU}$	10			ns
Data Input Hold Time After SCLK Edge	$t_{DHD}$	10			ns
Data Output Fall Time	$t_{DF}$			10	ns
Data Output Rise Time	$t_{DR}$			10	ns
SCLK Fall Time	$t_{SF}$			10	ns
SCLK Rise Time	$t_{SR}$			10	ns
MISO Disable Time After SS Rising Edge	$t_{DIS}$			100	ns
SS High After SCLK Edge	$t_{SFS}$	0			ns



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**Figure 2. Serial Port Interface (SPI) Timing Diagram**

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Rating
VDD to GND	-0.3 V to +3.96 V
Analog Input Voltage to GND, IAP, IAN, IBP, IBN, ICP, ICN, INP, INN, VAP, VAN, VBP, VBN, VCP, VCN	-2 V to +2 V
Reference Input Voltage to REFGND	-0.3 V to +2 V
Digital Input Voltage to GND	-0.3 V to VDD + 0.3 V
Digital Output Voltage to GND	-0.3 V to VDD + 0.3 V
Operating Temperature	
Industrial Range	-40°C to +85°C
Storage Range	-65°C to +150°C
Junction	125°C
Lead (Soldering, 10 sec) <sup>1</sup>	260°C

<sup>1</sup> Analog Devices recommends that reflow profiles used in soldering RoHS compliant devices conform to J-STD-020D.1 from JEDEC. Refer to JEDEC for the latest revision of this standard.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$  and  $\theta_{JC}$  are specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
CP-40-7 <sup>1</sup>	27.14	3.13	°C/W

<sup>1</sup> The junction to air measurement uses a 2S2P JEDEC test board with 4 × 4 standard JEDEC vias. The junction to case measurement uses a 1S0P JEDEC test board with 4 × 4 standard JEDEC vias. See JEDEC standard JESD51-2.

## ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in and ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001-2012.

Field induced charged-device model (FICDM) per JESD22-C101E.

Machine model (MM) per ANSI/ESD STMD5.2 MM ratings are for characterization only.

## ESD Ratings for the ADE9430

Table 5. ADE9430, 40-Lead LFCSP

ESD Model <sup>1</sup>	Withstand Threshold	Class
HBM	3.75 kV	2
FICDM	1.25 kV	IV
MM	300 V	Not applicable

<sup>1</sup> Analog Devices recommends that reflow profiles used in soldering RoHS compliant devices conform to J-STD-020D.1 from JEDEC. Refer to JEDEC for the latest revision of this standard.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

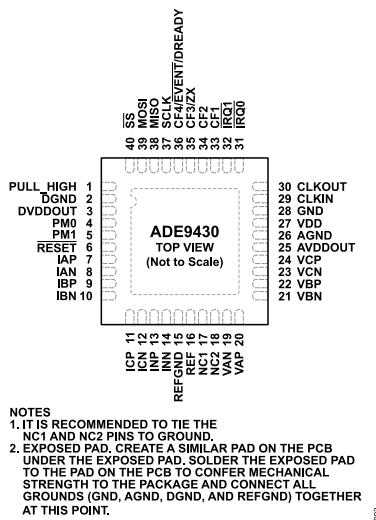


Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PULL_HIGH	Pull High. Tie this pin to VDD.
2	DGND	Digital Ground. This pin provides the ground reference for the digital circuitry in the ADE9430. Because the digital return currents in the ADE9430 are small, it is acceptable to connect this pin to the analog ground plane of the whole system. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.
3	DVDDOUT	1.8 V Output of the Digital LDO Regulator. Decouple this pin with a 0.1 $\mu$ F ceramic capacitor in parallel with a 4.7 $\mu$ F ceramic capacitor.
4	PM0	Power Mode Pin 0. PM0, combined with PM1, defines the power mode. For normal operation, ground PM0 and PM1.
5	PM1	Power Mode Pin 1. PM1 combined with PM0, defines the power mode. For normal operation, ground PM0 and PM1.
6	RESET	Reset Input, Active Low. This pin must stay low for at least 1 $\mu$ s to trigger a hardware reset.
7, 8	IAP, IAN	Analog Inputs, Channel IA. The IAP (positive) and IAN (negative) inputs are fully differential voltage inputs with a maximum differential level of $\pm 1$ V. This channel also has an internal PGA of 1, 2, or 4.
9, 10	IBP, IBN	Analog Inputs, Channel IB. The IBP (positive) and IBN (negative) inputs are fully differential voltage inputs with a maximum differential level of $\pm 1$ V. This channel also has an internal PGA of 1, 2, or 4.
11, 12	ICP, ICN	Analog Inputs, Channel IC. The ICP (positive) and ICN (negative) inputs are fully differential voltage inputs with a maximum differential level of $\pm 1$ V. This channel also has an internal PGA of 1, 2, or 4.
13, 14	INP, INN	Analog Inputs, Channel IN. The INP (positive) and INN (negative) inputs are fully differential voltage inputs with a maximum differential level of $\pm 1$ V. This channel also has an internal PGA of 1, 2, or 4.
15	REFGND	Ground Reference, Internal Voltage Reference. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.
16	REF	Voltage Reference. The REF pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.25 V. An external reference source of 1.2 V to 1.25 V can also be connected at this pin. In either case, decouple REF to REFGND with a 0.1 $\mu$ F ceramic capacitor in parallel with a 4.7 $\mu$ F ceramic capacitor. After reset, the on-chip reference is enabled. To use the internal voltage reference with the external circuits, a buffer is required.
17	NC1	No Connection. It is recommended to tie this pin to ground.
18	NC2	No Connection. It is recommended to tie this pin to ground.
19, 20	VAN, VAP	Analog Inputs, Channel VA. The VAP (positive) and VAN (negative) inputs are fully differential voltage inputs with a maximum differential level of $\pm 1$ V. This channel also has an internal PGA of 1, 2, or 4.
21, 22	VBN, VBP	Analog Inputs, Channel VB. The VBP (positive) and VBN (negative) inputs are fully differential voltage inputs with a maximum differential level of $\pm 1$ V. This channel also has an internal PGA of 1, 2, or 4.
23, 24	VCN, VCP	Analog Inputs, Channel VC. The VCP (positive) and VCN (negative) inputs are fully differential voltage inputs with a maximum differential level of $\pm 1$ V. This channel also has an internal PGA of 1, 2, or 4.
25	AVDDOUT	1.9 V Output of the Analog LDO Regulator. Decouple AVDDOUT with a 0.1 $\mu$ F ceramic capacitor in parallel with a 4.7 $\mu$ F ceramic capacitor. Do not connect external active circuitry to this pin.
26	AGND	Analog Ground Reference. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

**Table 6. Pin Function Descriptions**

Pin No.	Mnemonic	Description
27	VDD	Supply Voltage. The VDD pin provides the supply voltage. Decouple VDD to GND with a ceramic 0.1 $\mu$ F capacitor in parallel with a 10 $\mu$ F ceramic capacitor.
28	GND	Supply Ground Reference. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.
29	CLKIN	Crystal/Clock Input. Connect a crystal across CLKIN and CLKOUT to provide a clock source. Alternatively, an external clock can be provided at this logic input.
30	CLKOUT	Crystal Output. Connect a crystal across CLKIN and CLKOUT to provide a clock source. When using CLKOUT to drive external circuits, connect an external buffer.
31	$\overline{\text{IRQ0}}$	Interrupt Request Output. This pin is an active low logic output. See the <a href="#">Interrupts and Events</a> section for information about events that trigger interrupts.
32	$\overline{\text{IRQ1}}$	Interrupt Request Output. This pin is an active low logic output. See the <a href="#">Interrupts and Events</a> section for information about events that trigger interrupts.
33	CF1	Calibration Frequency Logic Output 1. The CF1, CF2, CF3, and CF4 outputs provide power information based on the CFxSEL bits in the CFMODE register. Use these outputs for operational and calibration purposes. Scale the full-scale output frequency by writing to the CFxDEN registers (see the <a href="#">Digital to Frequency Conversion—CFx Output</a> section and the <a href="#">ADE9430 Technical Reference Manual</a> ).
34	CF2	CF Logic Output 2. This pin indicates CF2.
35	CF3/ZX	CF Logic Output 3/Zero Crossing. This pin indicates CF3 or zero crossing.
36	CF4/ $\overline{\text{EVENT}}$ /DREADY	CF Logic Output 4/Event Pin/Data Ready. This pin indicates CF4, events, or when new data is ready.
37	SCLK	Serial Clock Input for the SPI Port. All serial data transfers synchronize to this clock (see the <a href="#">Accessing On-Chip Data</a> section). The SCLK pin has a Schmitt trigger input for use with a clock source that has a slow edge transition time, for example, optoisolator outputs.
38	MISO	Data Output for the SPI Port.
39	MOSI	Data Input for the SPI Port.
40	$\overline{\text{SS}}$	Chip Select for the SPI Port.
	EPAD	Exposed Pad. Create a similar pad on the PCB under the exposed pad. Solder the exposed pad to the pad on the PCB to confer mechanical strength to the package and connect all grounds (GND, AGND, DGND, and REFGND) together at this point.

## TYPICAL PERFORMANCE CHARACTERISTICS

### ENERGY LINEARITY OVER SUPPLY AND TEMPERATURE

Total energies obtained from a sinusoidal voltage with an amplitude of 50% of full scale and a frequency of 50 Hz, a sinusoidal current with variable amplitudes from 100% of full scale down to 0.01% or 0.02% of full scale and a frequency of 50 Hz. Fundamental energies obtained with a fundamental voltage component, with an amplitude of 50% of full scale in phase with a fifth harmonic, a current with a 50 Hz component that has variable amplitudes from 100% of full scale down to 0.01% of full scale, and a fifth harmonic with a constant amplitude of 40% of fundamental unless otherwise noted.

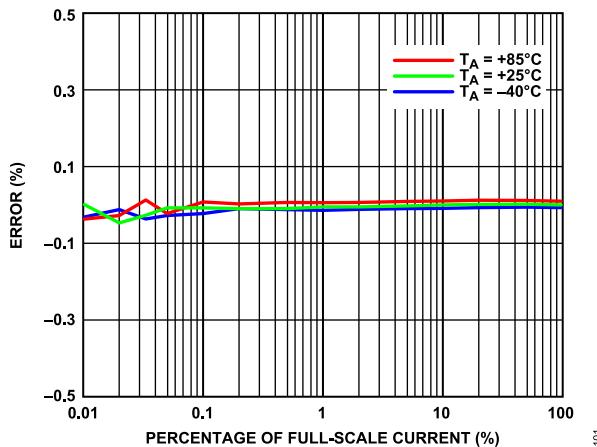


Figure 4. Total Active Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1

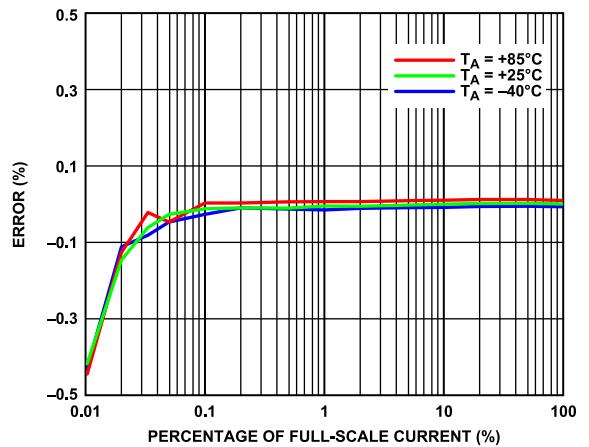


Figure 6. Total Apparent Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1

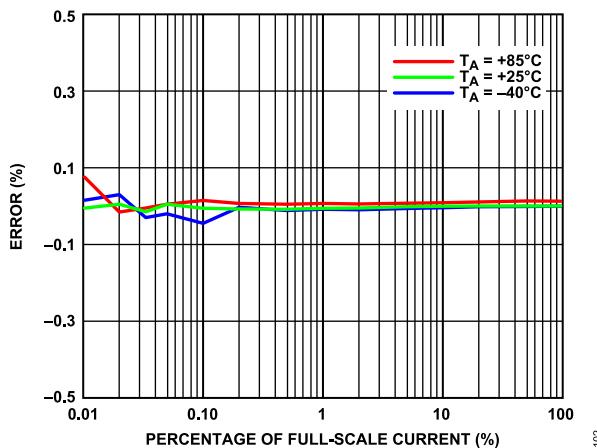


Figure 5. Total Reactive Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 0

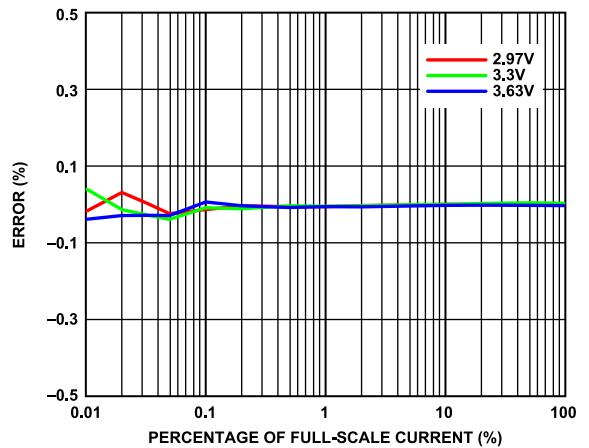


Figure 7. Total Active Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1,  $T_A = 25^\circ\text{C}$

## TYPICAL PERFORMANCE CHARACTERISTICS

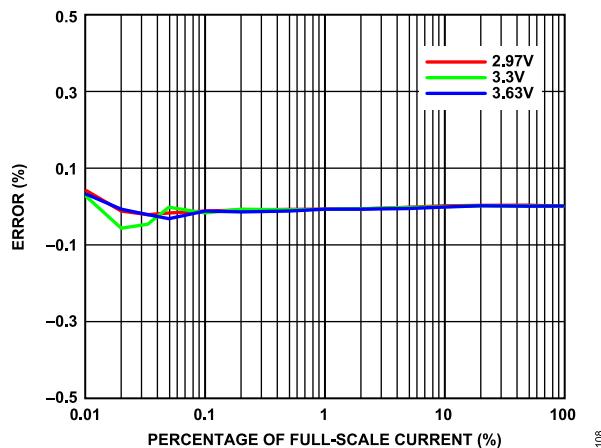


Figure 8. Total Reactive Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 0,  $T_A = 25^\circ\text{C}$

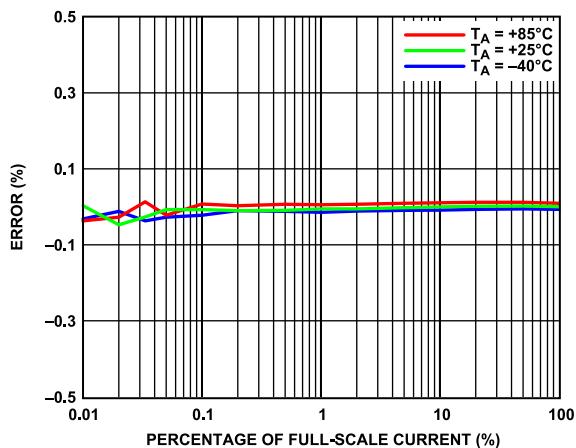


Figure 11. Fundamental Reactive Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 0

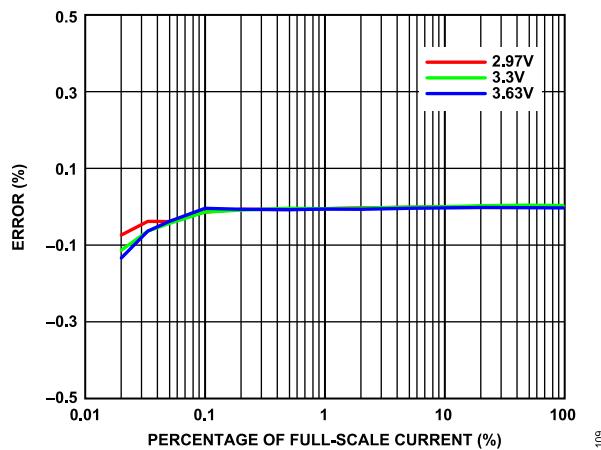


Figure 9. Total Apparent Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1,  $T_A = 25^\circ\text{C}$

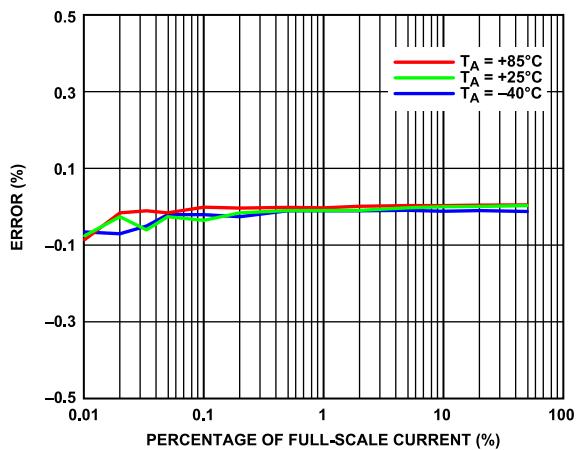


Figure 12. Fundamental Apparent Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1

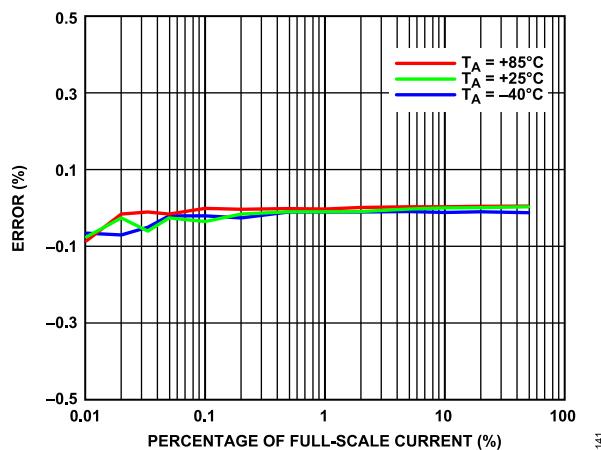


Figure 10. Fundamental Active Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1

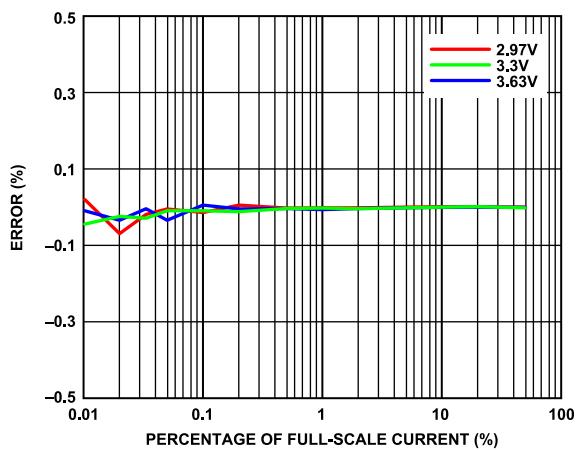


Figure 13. Fundamental Active Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1,  $T_A = 25^\circ\text{C}$

## TYPICAL PERFORMANCE CHARACTERISTICS

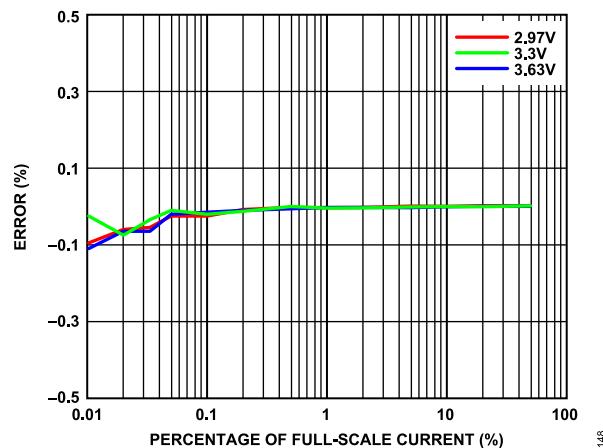


Figure 14. Fundamental Reactive Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 0,  $T_A = 25^\circ\text{C}$

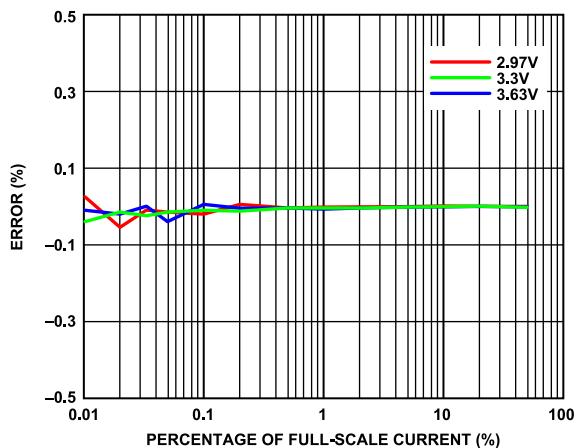
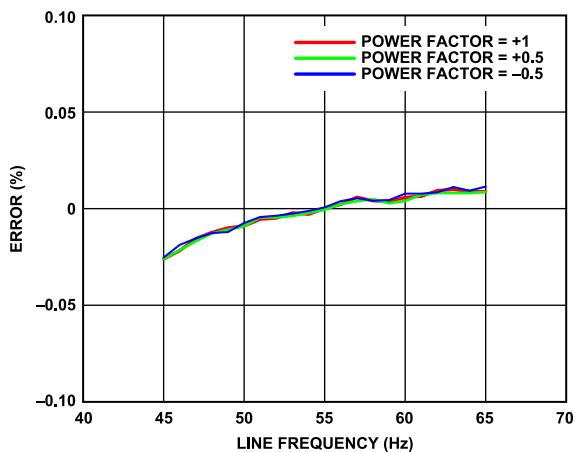


Figure 15. Fundamental Apparent Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1,  $T_A = 25^\circ\text{C}$

## TYPICAL PERFORMANCE CHARACTERISTICS

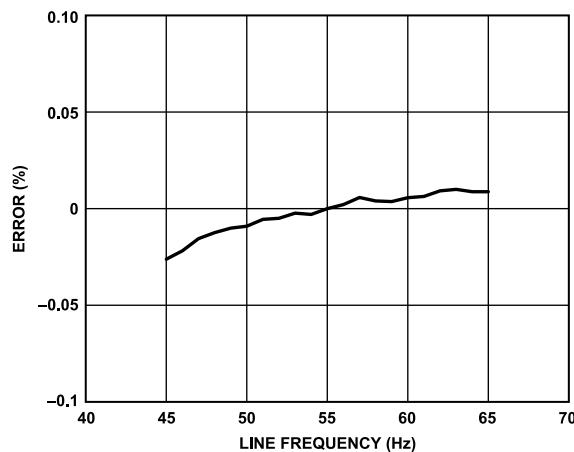
### ENERGY ERROR OVER FREQUENCY AND POWER FACTOR

Total energies obtained from a sinusoidal voltage with an amplitude of 50% of full scale, a sinusoidal current with a constant amplitude of 10% of full scale, and a variable frequency between 45 Hz and 65 Hz. Fundamental energies obtained with a fundamental voltage at 50 Hz, with an amplitude of 50% of full scale in phase with the fifth harmonic, a current that has constant amplitude of 10% of full scale, and a fifth harmonic with a constant amplitude of 40% of fundamental, unless otherwise noted.



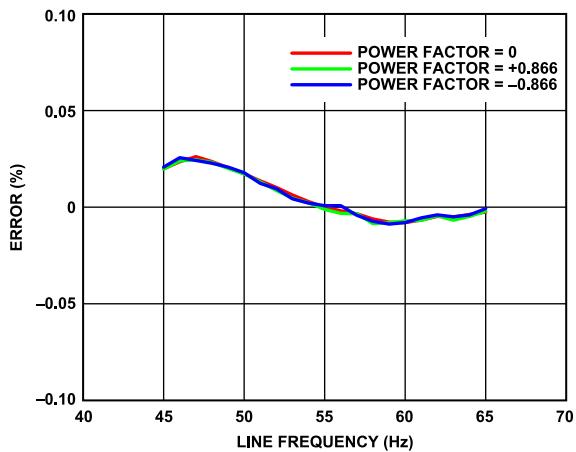
113

**Figure 16.** Total Active Energy Error vs. Line Frequency, Power Factor = -0.5, Power Factor = +0.5, and Power Factor = +1



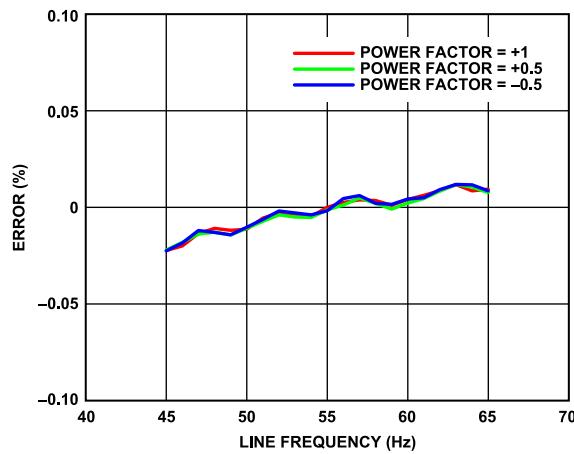
115

**Figure 18.** Total Apparent Energy Error vs. Line Frequency



114

**Figure 17.** Total Reactive Energy Error vs. Line Frequency, Power Factor = -0.866, Power Factor = 0, and Power Factor = +0.866



115

**Figure 19.** Fundamental Active Energy Error vs. Line Frequency, Power Factor = -0.5, Power Factor = +0.5, and Power Factor = +1

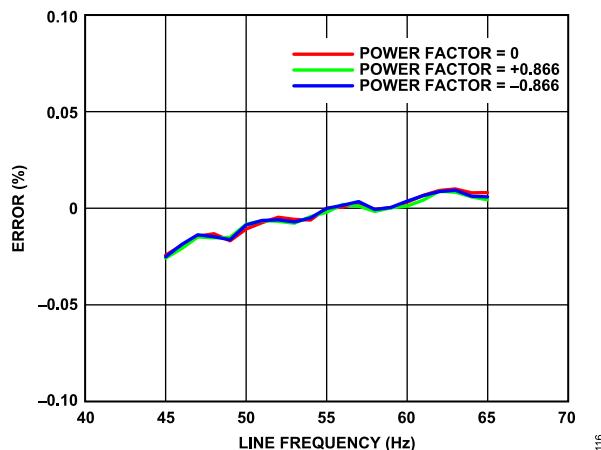
**TYPICAL PERFORMANCE CHARACTERISTICS**

Figure 20. Fundamental Reactive Energy Error vs. Line Frequency, Power Factor = -0.866, Power Factor = 0, and Power Factor = +0.866

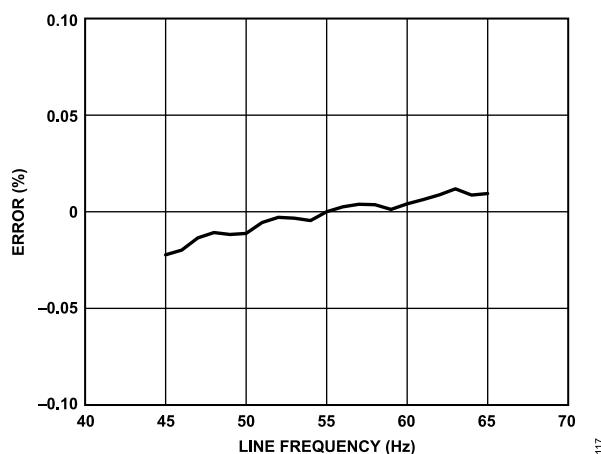


Figure 21. Fundamental Apparent Energy Error vs. Line Frequency

## TYPICAL PERFORMANCE CHARACTERISTICS

### ENERGY LINEARITY REPEATABILITY

Total energies obtained from a sinusoidal voltage with an amplitude of 50% of full scale and a frequency of 50 Hz, a sinusoidal current with variable amplitudes from 100% of full scale down to 0.01% of full scale, and a frequency of 50 Hz. Fundamental energies obtained with a fundamental voltage component, with an amplitude of 50% of full scale in phase with the fifth harmonic, a current with a 50 Hz component that has variable amplitudes from 100% of full scale down to 0.01% of full scale, and a fifth harmonic with a constant amplitude of 40% of fundamental. Measurements at 25°C repeated 30 times, unless otherwise noted.

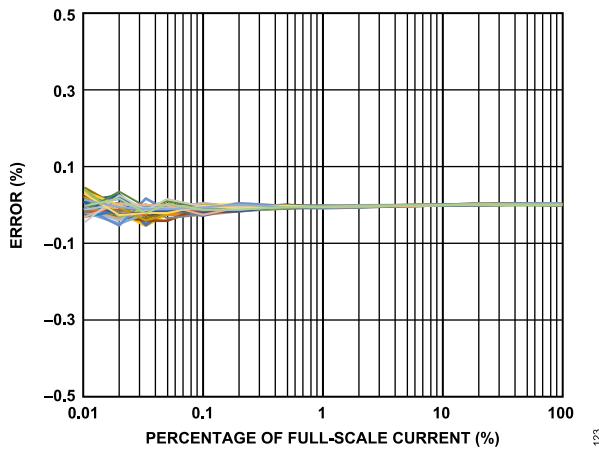


Figure 22. Total Active Energy Error as a Percentage of Full-Scale Current,  
Power Factor = 1 (Standard Deviation  $\sigma = 0.02\%$  at 0.01% of Full-Scale  
Current)

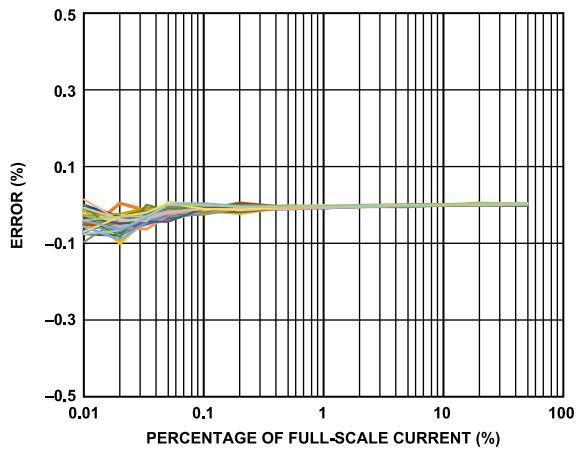


Figure 24. Fundamental Active Energy Error as a Percentage of Full-Scale Current,  
Power Factor = 1 (Standard Deviation  $\sigma = 0.03\%$  at 0.01% of Full-Scale Current)

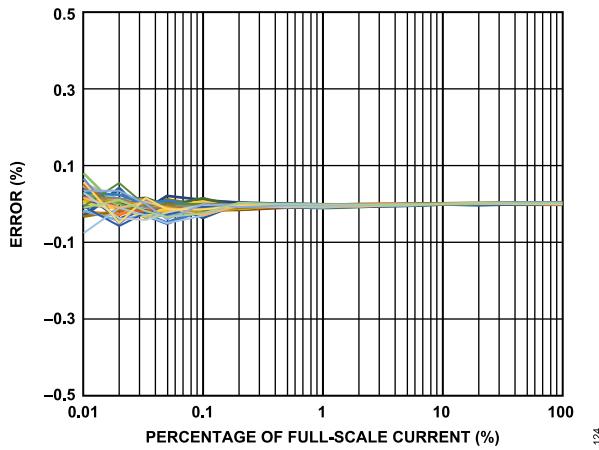


Figure 23. Total Reactive Energy Error as a Percentage of Full-Scale Current,  
Power Factor = 0 (Standard Deviation  $\sigma = 0.03\%$  at 0.01% of Full-Scale  
Current)

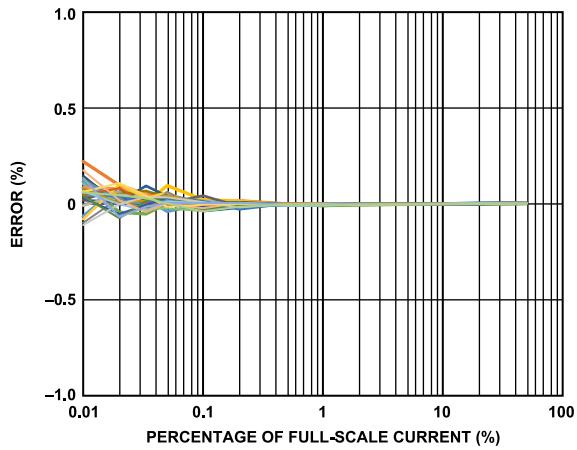


Figure 25. Fundamental Reactive Energy Error as a Percentage of Full-Scale Current,  
Power Factor = 0 (Standard Deviation  $\sigma = 0.04\%$  at 0.01% of Full-Scale Current)

## TYPICAL PERFORMANCE CHARACTERISTICS

### RMS LINEARITY OVER TEMPERATURE AND RMS ERROR OVER FREQUENCY

RMS linearity obtained with a sinusoidal current and voltage with variable amplitudes from 100% of full scale down to 0.01% of full scale using a frequency of 50 Hz. Total rms error over frequency obtained with a sinusoidal current amplitude of 10% of full scale and voltage amplitude of 50% of full scale. Fundamental rms error over frequency obtained with a sinusoidal current amplitude of 10% of full scale, a voltage amplitude of 50% of full scale, and a fifth harmonic with a constant amplitude of 40% of fundamental, unless otherwise noted.

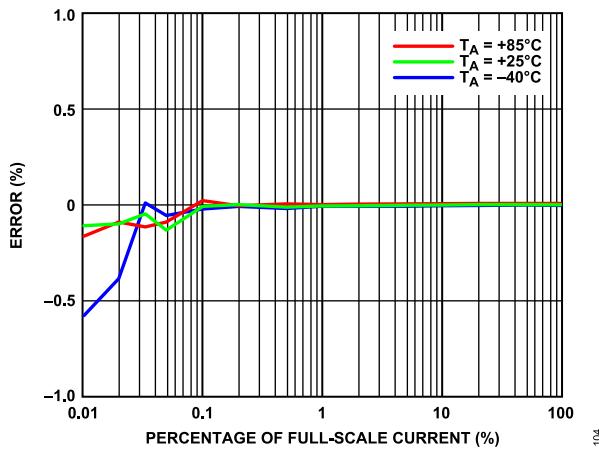


Figure 26. Current RMS Error as a Percentage of Full-Scale Current over Temperature

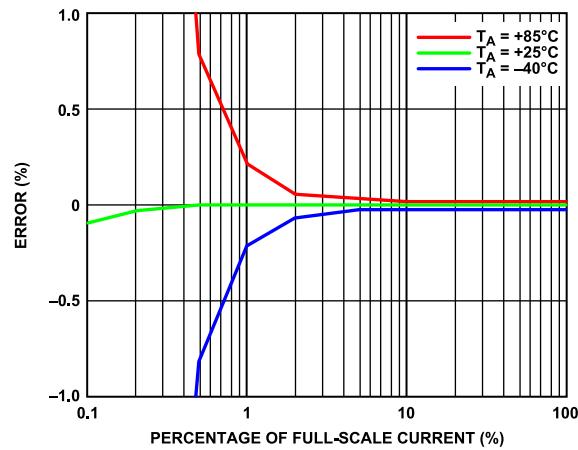


Figure 28. 10 Cycle Current RMS/12 Cycle Current Error as a Percentage of Full-Scale Current over Temperature, Data Sourced Before High-Pass Filter and Calibrated for Offset, Register CONFIG0, Bit RMS\_SRC\_SEL = 1

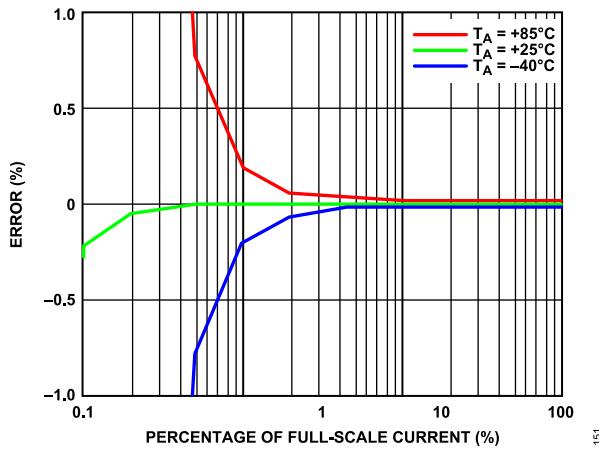


Figure 27. One-Cycle Current RMS Error as a Percentage of Full-Scale Current over Temperature, Data Sourced Before High-Pass Filter and Calibrated for Offset, Register CONFIG0, Bit RMS\_SRC\_SEL = 1

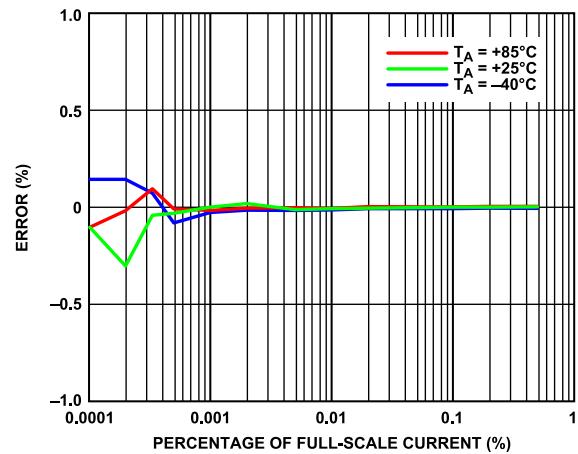


Figure 29. Fundamental Current RMS Error as a Percentage of Full-Scale Current over Temperature

## TYPICAL PERFORMANCE CHARACTERISTICS

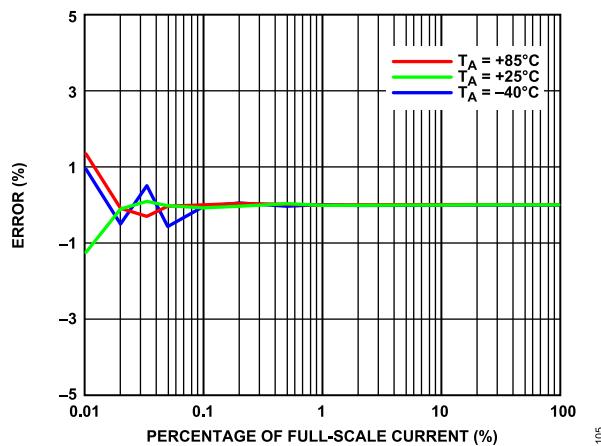


Figure 30. One-Cycle Current RMS Error as a Percentage of Full-Scale Current over Temperature, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS\_SRC\_SEL = 0

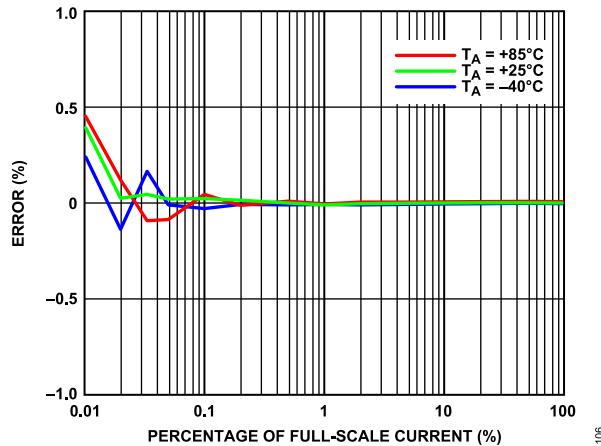


Figure 31. 10 Cycle Current RMS/12 Cycle Current Error as a Percentage of Full-Scale Current over Temperature, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS\_SRC\_SEL = 0

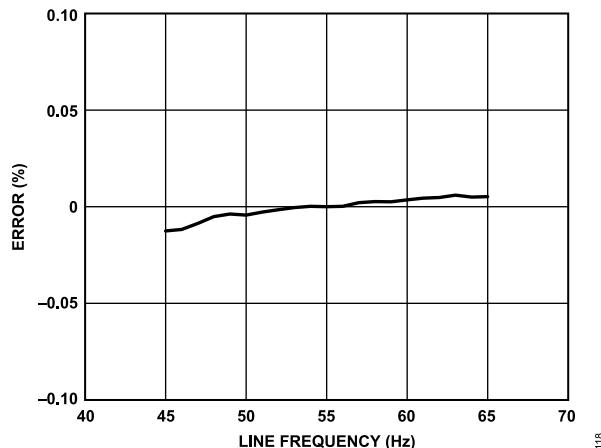


Figure 32. Current RMS Error vs. Line Frequency

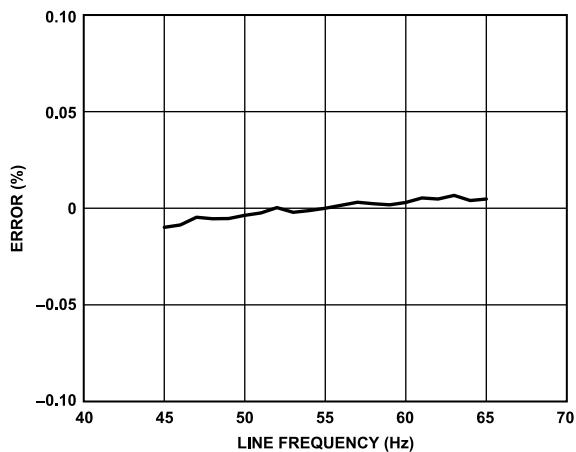


Figure 33. Fundamental Current RMS Error vs. Line Frequency

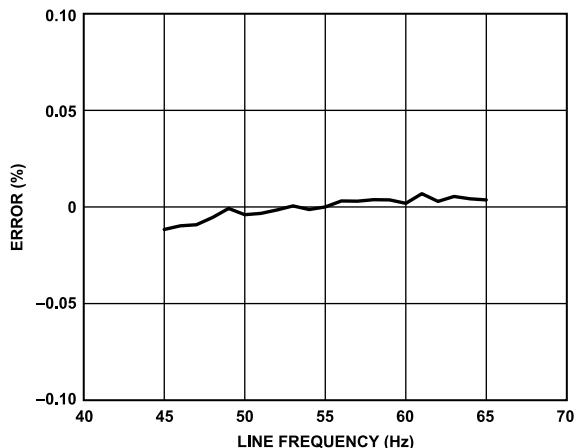


Figure 34. One-Cycle Current RMS Error vs. Line Frequency, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS\_SRC\_SEL = 0

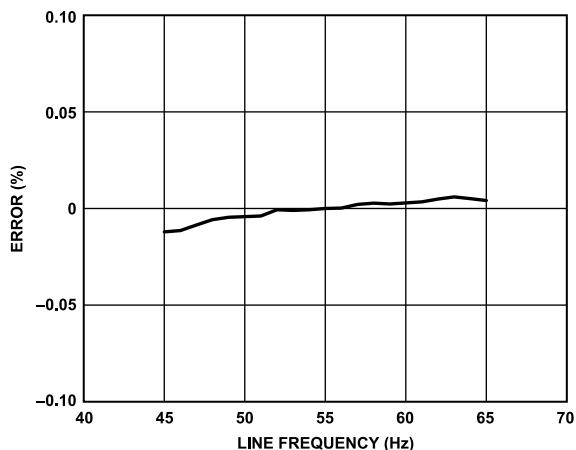
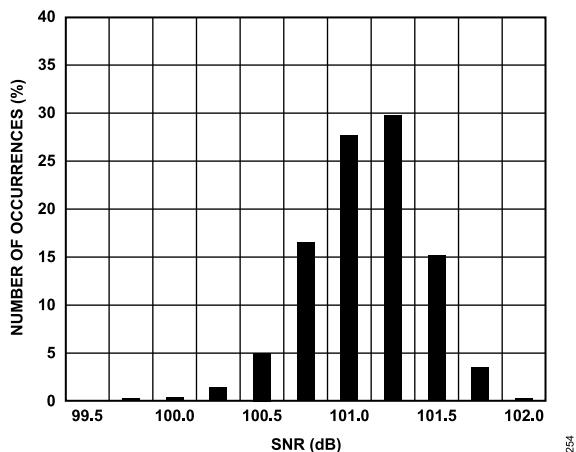


Figure 35. 10 Cycle Current RMS/12 Cycle Current Error vs. Line Frequency, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS\_SRC\_SEL = 0

**TYPICAL PERFORMANCE CHARACTERISTICS****SIGNAL-TO-NOISE RATIO PERFORMANCE**

*Figure 36. SNR Histogram of ADC SNR for 1000 Devices Tested at  $T_A = 25^\circ\text{C}$  with PGA\_GAIN = 1 and 8 kSPS Data Rate*

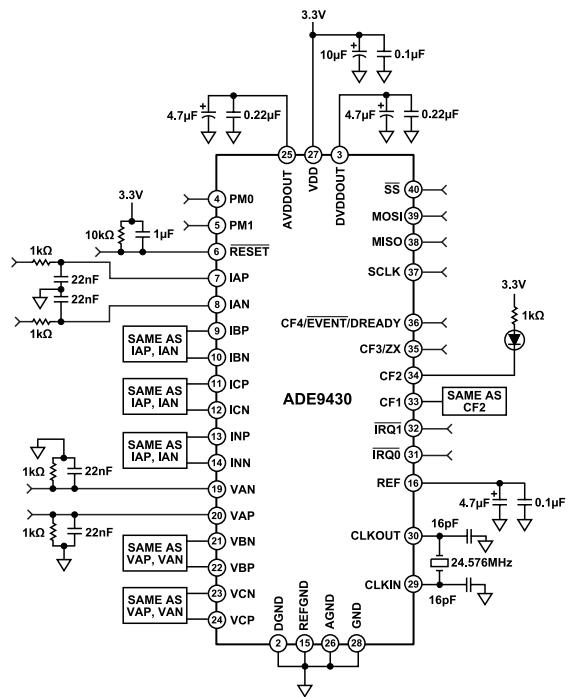
**TEST CIRCUIT**

Figure 37. Test Circuit

## TERMINOLOGY

### Crosstalk

Crosstalk is measured by grounding one channel and applying a full-scale 50 Hz or 60 Hz signal on all other channels. The crosstalk is equal to the ratio between the grounded ADC output value and its ADC full-scale output value. The ADC outputs are acquired for 100 sec. Crosstalk is expressed in decibels.

### Differential Input Impedance DC

The differential input impedance dc represents the impedance between the IxP and IxN pair or VxP and VxN pair. It varies with the PGA gain selection as indicated in the [Table 1](#).

### ADC Offset

ADC offset is the difference between the average measured ADC output code with both inputs connected to GND and the ideal ADC output code of zero. ADC offset is expressed in mV.

### ADC Offset Drift over Temperature

The ADC offset drift is the change in offset over temperature. It is measured at  $-40^{\circ}\text{C}$ ,  $+25^{\circ}\text{C}$ , and  $+85^{\circ}\text{C}$ . Calculate the offset drift over temperature as follows:

$$\text{Drift} =$$

$$\max \left( \left| \frac{\text{Offset}(-40^{\circ}\text{C}) - \text{Offset}(+25^{\circ}\text{C})}{(-40^{\circ}\text{C} - +25^{\circ}\text{C})} \right|, \left| \frac{\text{Offset}(+85^{\circ}\text{C}) - \text{Offset}(+25^{\circ}\text{C})}{(+85^{\circ}\text{C} - +25^{\circ}\text{C})} \right| \right) \quad (1)$$

Offset drift is expressed in  $\mu\text{V}/^{\circ}\text{C}$ .

### ADC Gain Error

ADC gain error represents the difference between the measured ADC output code (minus the offset) and the ideal output code when an external voltage reference of 1.2 V is used. The difference is expressed as a percentage of the ideal code. It represents the overall gain error of one channel.

### ADC Gain Drift over Temperature

This temperature coefficient includes the temperature variation of the ADC gain while using an external voltage reference of 1.2 V. It represents the overall temperature coefficient of one current or voltage channel. With an external voltage reference of 1.2 V in use, the ADC gain is measured at  $-40^{\circ}\text{C}$ ,  $+25^{\circ}\text{C}$ , and  $+85^{\circ}\text{C}$ . Then, the temperature coefficient is computed as follows:

$$\text{Drift} =$$

$$\max \left( \left| \frac{\text{Gain}(-40^{\circ}\text{C}) - \text{Gain}(+25^{\circ}\text{C})}{\text{Gain}(+25^{\circ}\text{C}) \times (-40^{\circ}\text{C} - +25^{\circ}\text{C})} \right|, \left| \frac{\text{Gain}(+85^{\circ}\text{C}) - \text{Gain}(+25^{\circ}\text{C})}{\text{Gain}(+25^{\circ}\text{C}) \times (+85^{\circ}\text{C} - +25^{\circ}\text{C})} \right| \right) \quad (2)$$

Gain drift is measured in ppm/ $^{\circ}\text{C}$ .

### AC Power Supply Rejection (PSRR)

AC PSRR quantifies the measurement error as a percentage of reading when the dc power supply is nominal ( $V_{\text{NOM}}$ ) and modulated with ac, and the inputs are grounded. For the ac PSRR measurement, 20 sec samples are captured with nominal supplies (3.3 V, which is  $V_1$ ) and a second set ( $V_2$ ) is captured with an additional ac signal (330 mV peak at 50 Hz) introduced onto the supplies. Then, the PSRR is expressed as  $\text{PSRR} = 20 \log_{10}(V_2/V_1)$ .

### Signal-to-Noise Ratio (SNR)

SNR is calculated by inputting a 50 Hz signal, and samples are acquired for 2 sec. The amplitudes for each frequency up to the bandwidth given in as the ADC output bandwidth (-3 dB) are calculated. To determine the SNR, the signal at 50 Hz is compared to the sum of the power from all the other frequencies, removing power from its harmonics. The value for SNR is expressed in decibels.

### Signal-to-Noise-and-Distortion Ratio (SINAD)

SINAD is calculated by inputting a 50 Hz signal, and samples are acquired for 2 sec. The amplitudes for each frequency up to the bandwidth given in as the ADC output bandwidth (-3 dB) are calculated. To determine the SINAD, the signal at 50 Hz is compared to the sum of the power from all the other frequencies. The value for SINAD is expressed in decibels.

### Total Harmonic Distortion (THD)

THD is calculated by inputting a 50 Hz signal, and samples are acquired for over 2 sec. The amplitudes for each frequency up to the bandwidth given in as the ADC output bandwidth (-3 dB) are calculated. To determine the THD, the amplitudes of the 50 Hz harmonics up to the bandwidth are root sum squared. The value for THD is expressed in decibels.

### Spurious-Free Dynamic Range (SFDR)

SFDR is calculated by inputting a 50 Hz signal, and samples are acquired for over 2 sec. The amplitudes for each frequency up to the bandwidth given in as the ADC output bandwidth (-3 dB) are calculated. To determine the SFDR, the amplitude of the largest signal that is not a harmonic of 50 Hz is recorded. The value for SFDR is expressed in decibels.

### ADC Output Pass Band

The ADC output pass band is the bandwidth within 0.1 dB, resulting from the digital filtering in the sinc4 and sinc4 + IIR LPF.

### ADC Output Bandwidth

The ADC output bandwidth is the bandwidth within -3 dB, resulting from the digital filtering in the sinc4 and sinc4 + IIR LPF.

## THEORY OF OPERATION

### MEASUREMENTS

#### Current Channel

The ADE9430 has three phase current channels and one neutral current channel. The phase current channel datapath for IA, IB, and

IC is shown in Figure 38 and datapath for the neutral channel is shown in Figure 39. See the [ADE9430 Technical Reference Manual](#) for additional information.

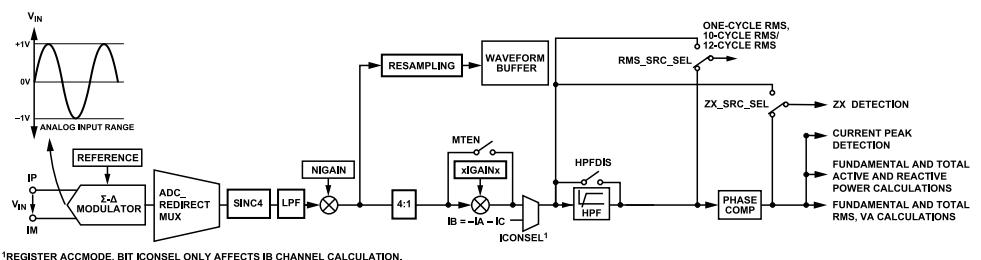


Figure 38. Current Channel (IA, IB, IC) Datapath

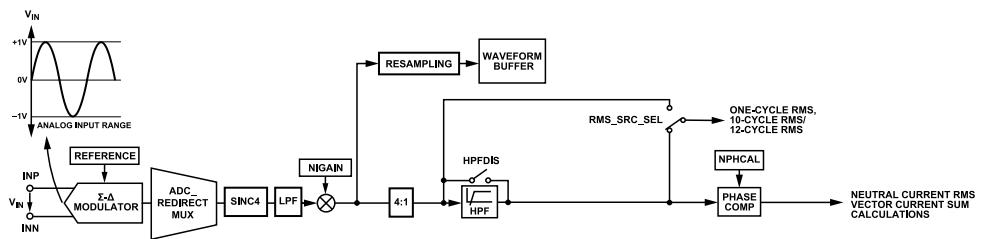


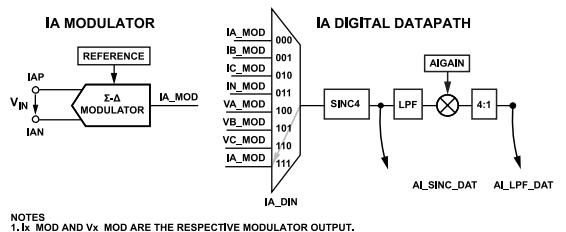
Figure 39. Neutral Current Channel (IN) Datapath

## THEORY OF OPERATION

### ADC\_REDIRECT Multiplexer

The ADE9430 provides a multiplexer that allows any ADC output to be redirected to any digital processing datapath (see [Figure 40](#)).

By default, each modulator is mapped to its corresponding datapath. See the [ADE9430 Technical Reference Manual](#) for additional information.



*Figure 40. ADC\_REDIRECT Modulator to Digital Datapath Multiplexing*

### Current Channel Gain, xIGAIN

The ADE9430 provides current gain calibration registers (AIGAIN, BIGAIN, CIGAIN, and NIGAIN), one for each current channel.

The current channel gain varies with xIGAIN as shown in the following equation:

$$\text{Current Channel Gain} = (1 + (xIGAIN/N)^{27})$$

See the [ADE9430 Technical Reference Manual](#) for additional information.

### IB Calculation Using ICONSEL

Write to the ICONSEL bit in the ACCMODE register to calculate  $I_B = -I_A - I_C$ . This setting can help save the cost of a current transformer in some 3-wire delta configurations. See the [ADE9430 Technical Reference Manual](#) for additional information.

### High-Pass Filter

A high-pass filter removes dc offsets for accurate rms and energy measurements. This filter is enabled by default with a corner frequency of 1.25 Hz.

To disable the high-pass filter on all current and voltage channels set the HPFDIS bit in the CONFIG0 register. The corner frequency is configured with the HPF\_CRN bits in the CONFIG2 register. See the [ADE9430 Technical Reference Manual](#) for additional information.

### Phase Compensation

The ADE9430 provides a phase compensation register for each current channel: APHCALx, BPHCALx, CPHCALx, and NPHCAL.

The phase calibration range is  $-15^\circ$  to  $+2.25^\circ$  at 50 Hz and  $-15^\circ$  to  $+2.7^\circ$  at 60 Hz.

Use the following equation to calculate the  $xPHCALx$  value for a given phase correction ( $\phi$ )° angle. Phase correction ( $\phi$ )° is positive to correct a current that lags the voltage and negative to correct a current that leads the voltage, as seen in a current transformer.

$$xPHCALx = \left( \frac{\sin(\phi - \omega) + \sin\omega}{\sin(2\omega - \phi)} \right) \times 2^{27} \quad (3)$$

$$\omega = 2\pi \times f_{LINE}/f_{DSP}$$

where:

$f_{LINE}$  is the line frequency.

$f_{DSP}$  is 8 kHz.

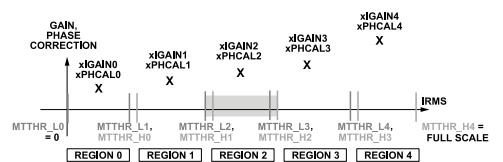
See the [ADE9430 Technical Reference Manual](#) for additional information.

### Multipoint Phase and Gain Calibration

The ADE9430 allows multipoint gain and phase compensation with hysteresis on the IA, IB, and IC current channels. The multipoint gain and phase compensation is not applied to the resampled data. The current channel gain and phase compensation vary as a function of the calculated input current rms amplitude in xIRMS. There are five gain registers (xIGAIN0 to xIGAIN4) and five phase calibration registers (xPHCAL0 to xPHCAL4) for each channel. Set the MTEN bit in the CONFIG0 register to enable multipoint gain and phase calibration. MTEN = 0 by default.

The gain and phase calibration factor is applied based on the xIRMS current amplitude and the MTTHR\_Lx and the MTTHR\_Hx register values, as shown in [Figure 41](#).

See the [ADE9430 Technical Reference Manual](#) for additional information.



*Figure 41. Multipoint Phase and Gain Calibration*

### Voltage Channel

The ADE9430 has three voltage channels. The datapaths for the VA, VB, and VC voltage channels are shown in [Figure 42](#). The xVGAIN registers calibrate the voltage channel of each phase. The xVGAIN registers have the same scaling as the xIGAIN registers. See the [ADE9430 Technical Reference Manual](#) for additional information.

## THEORY OF OPERATION

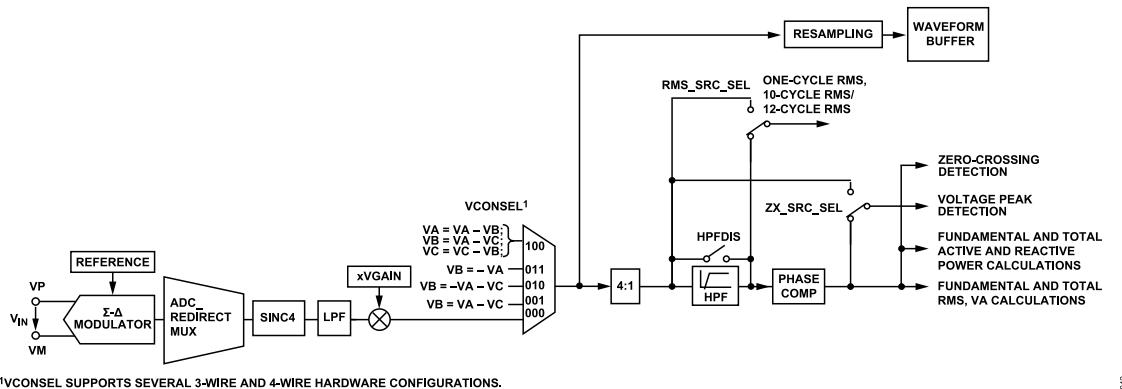


Figure 42. Voltage Channel Datapath

### RMS and Power Measurements

The ADE9430 calculates the total and fundamental values of rms current, rms voltage, active power, reactive power, and apparent power. The fundamental algorithm requires initialization of the network frequency using the SELFREQ bit in the ACCMODE register and the nominal voltage in the VLEVEL register. Calculate the VLEVEL value according to the following equation:

$$VLEVEL = x \times 1,144,084$$

Where  $x$  is the dynamic range that the nominal input signal is at with respect to full scale.

For instance, if the signal is at  $\frac{1}{2}$  of full scale,  $x = 2$ .

$$VLEVEL = 2 \times 1,144,084$$

See the [ADE9430 Technical Reference Manual](#) for additional information.

### Total and Fundamental RMS

The ADE9430 offers the total and fundamental current and voltage rms measurements on all phase channels. The datapath is shown in [Figure 43](#).

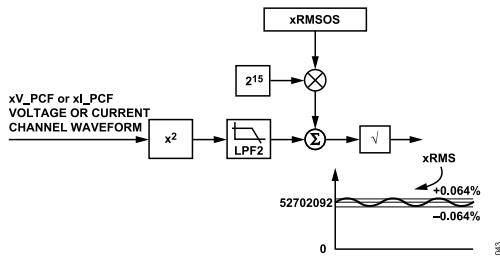


Figure 43. Filter-Based Total RMS

The total rms calculations, one for each channel (AIRMS, BIRMS, CIRMS, NIRMS, AVRMS, BVRMS, and CVRMS), are updated every 8 kSPS. The fundamental rms calculations available in the AIFRMS, BIFRMS, CIFRMS, AVFRMS, BVFRMS, and CVFRMS

registers are also updated every 8 kSPS. The fundamental rms is not available for the neutral channel.

The xRMS and xFRMS value at full scale is 52,702,092 decimals.

The total and fundamental rms measurements can be calibrated for gain and offset. Perform gain calibration on the respective current and voltage channel datapath. The following equations indicate how the offset calibration registers modify the result in the corresponding rms registers:

$$xRMS = \sqrt{xRMS_0^2 + 2^{15} \times xRMOSOS} \quad (4)$$

Where  $xRMS_0$  is the initial xRMS register value before offset calibration.

$$xFRMS = \sqrt{xFRMS_0^2 + 2^{15} \times xFRMOSOS} \quad (5)$$

The ADE9430 also calculates the rms of the sum of  $I_A + I_B + I_C \pm I_N$  and stores the result in ISUMRMS. The ISUM\_CFG bits in the CONFIG0 register configure the components included in summation.

See the [ADE9430 Technical Reference Manual](#) for additional information.

### Total and Fundamental Active Power

The ADE9430 offers total and fundamental active power measurements on all channels. To calculate the total active power for Phase A, see [Figure 44](#).

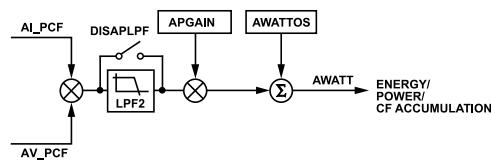


Figure 44. Total Active Power, AWATT, Calculation for Phase A

The active power calculations, one for each channel (AWATT, BWATT, and CWATT), are updated every 8 kSPS. The fundamental active power is also updated every 8 kSPS and is available in the

## THEORY OF OPERATION

AFWATT, BFWATT, and CFWATT registers. With full-scale inputs, the xWATT and xFWATT value are 20,694,066 decimals.

Enable the LPF2 (DISRPLPF = 0) for normal operation. Disable LPF2 by setting DISRPLPF in the CONFIG0 register to obtain instantaneous total active power. DISRPLPF is zero at reset.

The total and fundamental measurements can be calibrated for gain and offset. The following equations indicate how the gain and offset calibration registers modify the results in the corresponding power registers:

$$xWATT = \left(1 + \frac{xPGAIN}{2^{27}}\right)xWATT_0 + xWATTOS \quad (6)$$

$$\begin{aligned} xFWATT = & \left(1 + \frac{xPGAIN}{2^{27}}\right)xFWATT_0 \\ & + xFWATTOS \end{aligned} \quad (7)$$

$xPGAIN$  is a common gain to total and fundamental components of active, reactive, and apparent powers.

See the [ADE9430 Technical Reference Manual](#) for additional information.

## Total and Fundamental Reactive Power

The ADE9430 offers the total and fundamental reactive power measurements on all channels. [Figure 45](#) shows how to perform the total reactive power calculation.

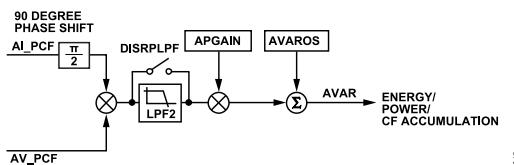


Figure 45. Total Reactive Power, AVAR, Calculation

The reactive power calculations, one for each channel AVAR, BVAR, and CVAR, are updated every 8 kSPS. The fundamental reactive power is also updated every 8 kSPS and is available in the AFVAR, BFVAR, and CFVAR registers. With full-scale inputs, the xVAR and xFVAR value are 20,694,066.

Enable the LPF2 (DISRPLPF = 0) for normal operation. Disable LPF2 by setting DISRPLPF in the CONFIG0 register to obtain instantaneous total reactive power. DISRPLPF is 0 at reset.

The following equations indicate how the gain and offset calibration registers modify the result in the corresponding power registers:

$$xVAR = \left(1 + \frac{xPGAIN}{2^{27}}\right)xVAR_0 + xVAROS \quad (8)$$

$$xFVAR = \left(1 + \frac{xPGAIN}{2^{27}}\right)xFVAR_0 + xFVAROS \quad (9)$$

See the [ADE9430 Technical Reference Manual](#) for additional information.

## Total and Fundamental Apparent Power

The ADE9430 offers the total and fundamental apparent power measurements on all channels. See [Figure 46](#) for how to calculate the total apparent power for Phase A.

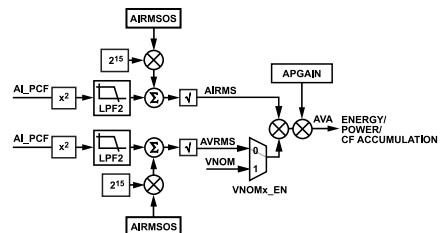


Figure 46. Total Apparent Power, AVA, Calculation for Phase A

The total apparent power calculations, one for each channel AVA, BVA, and CVA, are updated every 8 kSPS. The fundamental apparent power is also updated every 8 kSPS and is available in the AFVA, BFVA, and CFVA registers. With full-scale inputs, the xVA and xFVA value are 20,694,066 decimals.

The ADE9430 offers a register (VNOM) that can be set to a value to correspond to the desired voltage rms value. If the VNOM\_EN bits in the CONFIG0 register are set, VNOM multiplies by xIRMS when calculating xVA.

See the [ADE9430 Technical Reference Manual](#) for additional information.

## No Load Detection, Energy Accumulation, and Power Accumulation Features

The ADE9430 calculates the total and fundamental values of active, reactive, and apparent energy for all the three phases. The ADE9430 can have signed, absolute, positive, or negative only accumulation on active and reactive energies using the WATTACC and VARACC bits in the ACCMODE register. The default accumulation mode is signed. See the [ADE9430 Technical Reference Manual](#) for additional information.

### No Load Detection Feature

The ADE9430 has a no load detection for each phase and energy to prevent energy accumulation due to noise. If the accumulated energy over the user defined time period is below the user defined threshold, zero energy is accumulated into the energy register. The NOLOAD\_TMR bits in the EP\_CFG register determine the no load time period and the ACT\_NL\_LVL, REACT\_NL\_LVL, and APP\_NL\_LVL registers contain the user defined no load threshold. The no load status is available in the PHNOLOAD register, the IRQ1 interrupt, and the EVENT pin.

See the [ADE9430 Technical Reference Manual](#) for additional information.

## THEORY OF OPERATION

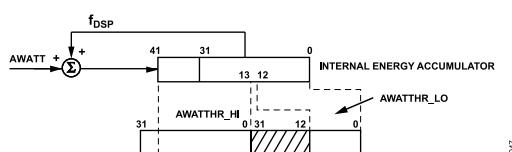
### Energy Accumulation

The energy is accumulated into a 42-bit signed internal energy register at 8 kSPS. The internal register can accumulate a user defined number of samples or half line cycles configured by EGY\_TMR\_MODE bit in the EP\_CFG register. When half line cycle accumulation is enabled, configure the zero-crossing source using the ZX\_SEL bits in the ZX\_LP\_SEL register. The number of samples or half line cycles is set in the EGY\_TIME register. The maximum value of EGY\_TIME is 8191d. With full-scale inputs, the internal register overflows in 13.3 sec. For a 50 Hz signal, EGY\_TIME must be lower than 1329 decimals to prevent overflow during half line cycle accumulation.

After EGY\_TIME + 1 samples or half line cycles, the EGYRDY bit is set in the STATUS0 register and the energy register is updated. The data from the internal energy register is added or latched to the user energy register depending on the EGY\_LD\_ACCUM bit setting in the EP\_CFG register.

The energy register is signed and is 45 bits wide, split between two 32-bit registers, as shown in [Figure 47](#). The user energy can reset on a read using the RD\_RST\_EN bit in the EP\_CFG register. With full-scale inputs, the user energy register overflows in 106.3 sec.

See the [ADE9430 Technical Reference Manual](#) for additional information.



*Figure 47. Internal Energy Register to AWATTHR\_HI and AWATTHR\_LO*

## THEORY OF OPERATION

### Power Accumulation

The ADE9430 accumulates the total and fundamental values of active, reactive, and apparent power for all the three phases into respective xWATT\_ACC and xFWATT\_ACC, xVAR\_ACC and xFVAR\_ACC, and xVA\_ACC, and xFVA\_ACC 32-bit signed registers. The number of samples accumulated is set using the PWR\_TIME register. The PWR\_RDY bit in the STATUS0 register is set after PWR\_TIME + 1 samples accumulate at 8 kSPS. The maximum value of the PWR\_TIME register is 8191 decimals, and the maximum power accumulation time is 1.024 sec.

The xSIGN bits in the PHSIGN register indicate the sign of accumulated powers over the PWR\_TIME interval. The PWR\_SIGN\_SEL[1:0] bits allow the user to select whether the power sign change follows the total or fundamental energies. When sign of the accumulated power changes, the corresponding REVx bits in the STATUS0 register are set and IRQ0 generates an interrupt.

The ADE9430 allows the user to accumulate total active power and VAR powers into separate positive and negative values into the PWATT\_ACC and NWATT\_ACC, and PVAR\_ACC and NVAR\_ACC registers. A new accumulation from zero begins when the power update interval set in PWR\_TIMER elapses.

See the [ADE9430 Technical Reference Manual](#) for additional information.

### Digital to Frequency Conversion—CFx Output

The ADE9430 includes four pulse outputs that are proportional to the energy accumulation in the CF1 through CF4 output pins.

[Figure 48](#) shows a block diagram of the CFx pulse generation. CF3 is multiplexed with ZX, and CF4 is multiplexed with EVENT and DREADY.

See the [ADE9430 Technical Reference Manual](#) for additional information.

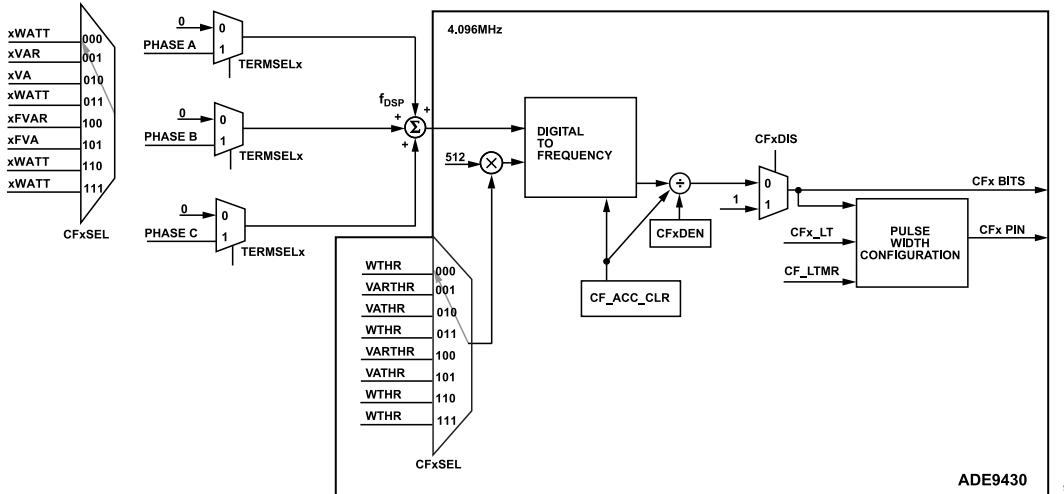


Figure 48. Digital to Frequency Conversion for CFx

## THEORY OF OPERATION

### Energy and Phase Selection

The CFxSEL bits in the CFMODE register select which type of energy to output on the CFx pins. The TERMSELx bits in the COMPMODE register select which phase energies to include in the CFx output.

For example, with CF1SEL = 000 and TERMSEL1 = 111, CF1 indicates the total active power output of Phase A, Phase B, and Phase C.

See the [ADE9430 Technical Reference Manual](#) for additional information.

### Configuring the CFx Pulse Width

The value of the CFx\_LT and the CF\_LTMR bits in the CF\_LCFG register determines the pulse width.

The maximum CFx with threshold (xTHR) = 0x00100000 and CFxDEN = 2 is 78.9 kHz. It is recommended to have xTHR = 0x00100000.

See the [ADE9430 Technical Reference Manual](#) for additional information.

### CFx Pulse Sign

The SUMxSIGN bits in the PHSIGN register indicate whether the sum of the energy that went into the last CFx pulse is positive or negative. The REVPSUMx bits in the STATUS0 register and the EVENT\_STATUS register indicate if the CFx polarity changed sign. This feature generates an interrupt on  $\overline{IRQ0}$ .

See the [ADE9430 Technical Reference Manual](#) for additional information.

### Clearing the CFx Accumulator

To clear the accumulation in the digital to frequency converter and CFDEN counter, write 1 to the CF\_ACC\_CLR bit in the CONFIG1 register. The CF\_ACC\_CLR bit automatically clears itself. See the [ADE9430 Technical Reference Manual](#) for additional information.

## POWER QUALITY MEASUREMENTS

### Zero-Crossing Detection

The ADE9430 offers zero-crossing detection on the VA, VB, VC, IA, IB, and IC input signals. The neutral current channel, IN, does

not contain a zero-crossing detection circuit. [Figure 49](#) and [Figure 50](#) show the current and voltage channel datapaths preceding zero-crossing detection.

Use the ZX\_SRC\_SEL bit in the CONFIG0 register to select data before the high-pass filter or after phase compensation to configure the inputs to zero-crossing detection. ZX\_SRC\_SEL is zero by default after reset.

To provide protection from noise, voltage channel zero-crossing events (ZXVA, ZXVB, and ZXVC) do not generate if the absolute value of the LPF1 output voltage is smaller than the threshold, ZXTHRSH. The current channel zero-crossing detection outputs (ZXIA, ZXIB, and ZXIC) are active for all input signals levels.

Calculate the zero-crossing threshold, ZXTHRSH, from the following equation:

$$ZXTHRSH =$$

$$\frac{(V_{PCF} \text{ at Full Scale}) \times (\text{LPF1 Attenuation})}{x \times 32 \times 2^8} \quad (10)$$

where:

$V_{PCF}$  at Full Scale is  $\pm 74,532,013$  decimal.

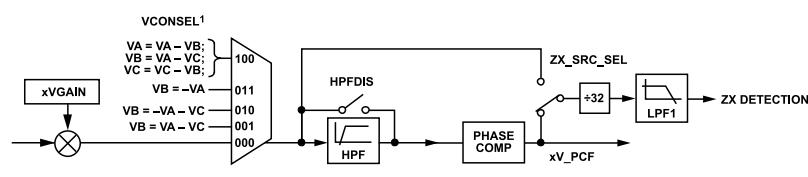
LPF1 Attenuation is 0.86 at 50 Hz and 0.81 at 60 Hz.

x is the dynamic range below which the voltage channel zero-crossing must be blocked.

The ADE9430 can calculate the combined zero crossings for all three phases as  $(V_A + V_B - V_C)/2$  by configuring the ZX\_SEL bits in the ZX\_LP\_SEL register. If VCONSEL is not equal to 0, the VB component in the combined zero-crossing circuit is set to zero.

The zero-crossing detection circuits have two different output rates: 8 kSPS and 1024 kSPS. The 8 kSPS zero-crossing signal calculates the line period, updates the ZXx bits in the STATUS1 register, and monitors the zero-crossing timeout, phase sequence error detection, resampling, and energy accumulation functions. The 1024 kSPS zero-crossing signal calculates the angle and updates the zero-crossing output on the CF3/ZX pin.

See the [ADE9430 Technical Reference Manual](#) for additional information.

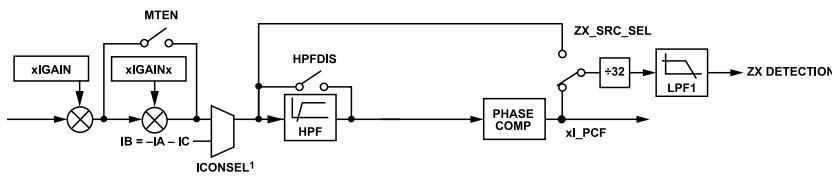


<sup>1</sup>VCONSEL SUPPORTS SEVERAL 3-WIRE AND 4-WIRE HARDWARE CONFIGURATIONS.

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Figure 49. Voltage Channel Signal Chain Preceding Zero-Crossing Detection

## THEORY OF OPERATION



<sup>1</sup>ICONSEL ONLY AFFECTS IB CHANNEL CALCULATION.

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Figure 50. Current Channel Signal Chain Preceding Zero-Crossing Detection

### CF3/ZX

The CF3/ZX pin can output zero crossings using the CF3\_CFG bit in the CONFIG1 register. To configure the source for zero crossing, use the ZX\_SEL bits in ZX\_LP\_SEL register. The CF3/ZX output pin goes from low to high when a negative to positive transition is detected and from high to low when a positive to negative transition occurs.

See the [ADE9430 Technical Reference Manual](#) for additional information.

### Zero-Crossing Timeout

If a zero crossing is not received after  $(ZXTOUT + 1)/8000$  sec, the corresponding ZXT0x bit in the STATUS1 register is set and generates an interrupt on the  $\overline{IRQ1}$  pin.

See the [ADE9430 Technical Reference Manual](#) for additional information.

### Line Period Calculation

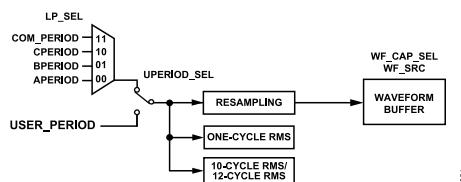
The ADE9430 calculates the line period for the Phase A, Phase B, and Phase C voltages and the combined voltage signal, and the results are available in the APERIOD, BPERIOD, CPERIOD, and COM\_PERIOD registers, respectively.

Calculate the line period,  $t_L$ , from the xPERIOD register, according to the following equation:

$$t_L = \frac{xPERIOD + 1}{8000 \times 2^{16}} \text{ (sec)} \quad (11)$$

If the calculated period value is outside the 40 Hz to 70 Hz range, or if zero crossings for that phase are not detected, the xPERIOD register is coerced to correspond to 50 Hz or 60 Hz, depending on SELFREQ bit in the ACCMODE register.

See the [ADE9430 Technical Reference Manual](#) for additional information.



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Figure 51. Line Period Selection for Resampling

### Angle Measurement

The ADE9430 provides nine angle measurements. ANGL\_IA\_IB, ANGL\_IB\_IC, and ANGL\_IA\_IC provide phase angle between currents. ANGL\_VA\_VB, ANGL\_VB\_VC, and ANGL\_VA\_VC provide phase angle between voltages. ANGL\_VA\_IA, ANGL\_VB\_IB, and ANGL\_VC\_IC provide phase angle between voltage and currents. To convert angle register reading to degrees, use the following equations.

For a 50 Hz system,

$$\text{Angle (Degrees)} = \text{ANGL}_x_y \times 0.017578125$$

For a 60 Hz system,

$$\text{Angle (Degrees)} = \text{ANGL}_x_y \times 0.02109375$$

See the [ADE9430 Technical Reference Manual](#) for additional information.

### Phase Sequence Error Detection

The ADE9430 monitors phase sequences and sets the SEQERR bit in the STATUS1 register if a sequence error occurs or a phase drops below ZXTHRSH. SEQ\_CYC determines the number of cycles to monitor to generate the sequence error. To generate an interrupt on  $\overline{IRQ1}$ , set the SEQERR bit in the MASK1 register.

See the [ADE9430 Technical Reference Manual](#) for additional information.

### One-Cycle RMS Measurement

One-cycle rms is an rms measurement performed over one line cycle, updated every period not synchronized to zero crossings. This measurement is provided for voltage and current on all phases plus the neutral current. All the one cycle rms measurements are performed over the same time interval and update at the same time, as indicated by the RMSONE RDY bit in the STATUS0 register. The results are stored in the AIRMSONE, BIRMSONE, CIRMSONE, NIRMSONE, AVRMSONE, BVRMSONE, and CVRMSONE registers. The xRMSONE register reading with full-scale inputs is 52,702,092d.

It is recommended to select the data before the high-pass filter for the one cycle measurement by setting the RMS\_SRC\_SEL bit in the CONFIG0 register.

## THEORY OF OPERATION

The LP\_SEL bits in the ZX\_LP\_SEL register select which line period measurement sets the number of samples used in the one cycle rms measurement. Alternatively, set the UPERIOD\_SEL bit in the CONFIG2 register to set the desired period in the USER\_PERIOD register for line period measurement. An offset correction register is available for improved performance with small input signal levels, xRMSONEOS.

The signal chain is shown in Figure 52.

See the [ADE9430 Technical Reference Manual](#) for additional information.

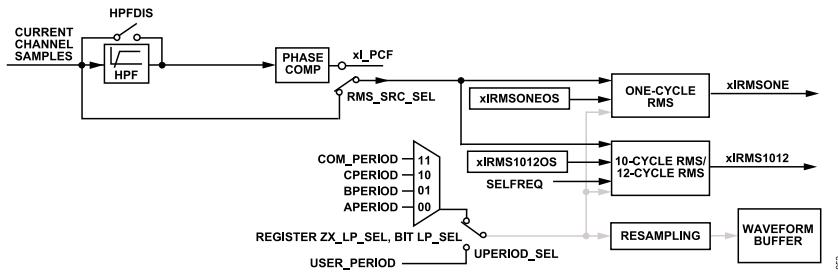


Figure 52. One Cycle RMS, 10 Cycle RMS, and 12 Cycle RMS Measurements

## THEORY OF OPERATION

### 10 Cycle RMS/12 Cycle RMS

The 10 cycle rms/12 cycle rms measurement is performed over 10 cycles on a 50 Hz network or 12 cycles on a 60 Hz network. The SELFREQ bit in the ACCMODE register selects whether the network is 50 Hz or 60 Hz. Then, the UPERIOD\_SEL bit in the CONFIG2 register selects whether to use a measured line period or a user configured value in the USER\_PERIOD register to set the number of samples used in the calculation.

An offset correction register is available for improved performance with small input signal levels, xRMS1012OS. The xRMS1012 register reading with full-scale inputs is 52,702,092d.

The signal chain is shown in Figure 52. See the [ADE9430 Technical Reference Manual](#) for additional information.

### Overcurrent Indication

The ADE9430 monitors the one cycle value on current channels to determine overcurrent events. If a one cycle rms current is greater than the user configured threshold in the OILVL register, the OI bit in the STATUS1 register is set. The overcurrent event generates an interrupt on the IRQ1 pin.

The OC\_EN bits in the CONFIG3 register select which phases to monitor for overcurrent events. The OIPHASE bits in the OISTATUS register indicate which current channels exceeded the threshold. The overcurrent value is stored in the corresponding OIA, OIB, or OIC registers.

See the [ADE9430 Technical Reference Manual](#) for additional information.

### Peak Detection

The ADE9430 records the peak value measured on the current and voltage channels from the xl\_PCF and xv\_PCF waveforms. The PEAKSEL bits in the CONFIG3 register allow the user to select which phases to monitor.

The IPEAK register stores the peak current value in the IPEAKVAL bits and indicates which phase currents reached the value in the IPPHASE bits. IPEAKVAL is equal to  $xl\_PCF/2^5$ .

Similarly, VPEAK stores the peak voltage value in the VPEAKVAL bits. VPEAKVAL is equal to  $xv\_PCF/2^5$ . After a read, the VPEAK and IPEAK registers reset.

See the [ADE9430 Technical Reference Manual](#) for additional information.

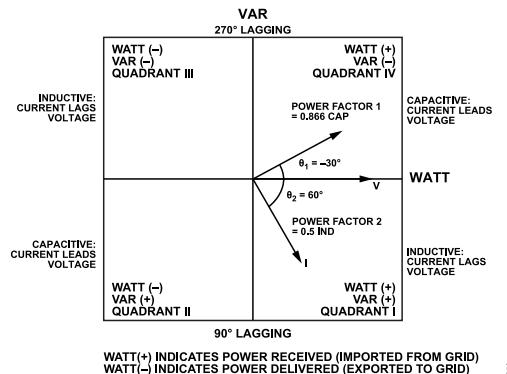
### Power Factor

The power factor calculation, one for each channel (APF, BPF, and CPF), is updated every 1.024 sec.

The sign of the APF calculation follows the sign of AWATT. To determine if power factor is leading or lagging, refer to the sign of

the total or fundamental reactive energy and the sign of the xPF or xWATT value, as indicated in Figure 53.

See the [ADE9430 Technical Reference Manual](#) for additional information.



**Figure 53. Active Power and VAR Sign for Capacitive and Inductive Loads**

The power factor result is stored in 5.27 format. The highest power factor value is 0x07FF FFFF, which corresponds to a power factor of 1. A power factor of -1 is stored as 0xF800 0000. To determine the power factor from the xPF register value, use the following equation:

$$\text{Power Factor} = xPF \times 2^{-27}$$

### Total Harmonic Distortion (THD)

A THD calculation is available on the IA, IB, IC, VA, VB, and VC channels in the ADSW-PQ-CLS Power Quality Library. To request access to the ADSW-PQ-CLS, fill out the software request form at: [Software Request Form | Analog Devices](#), where the target technology must be power quality monitoring and the processor/system on chip (SoC) is the ADE9430.

### Resampling

The ADE9430 resamples the input data to provide 1024 points for 10/12 cycles, selected by SELFREQ. The resampled data is available for all current channels and voltage channels in the waveform buffer. Each resampled waveform sample is stored as a 16-bit signed integer in the waveform buffer. See the [ADE9430 Technical Reference Manual](#) for additional information.

### Temperature

The temperature reading is available in the TEMP\_RSLT register. To convert the temperature range into Celsius, use the following equation:

$$\text{Temperature } (\text{°C}) = \text{TEMP\_RSLT} \times (-\text{TEMP\_GAIN}/65536) + (\text{TEMP\_OFFSET}/32)$$

During manufacturing of each device, the TEMP\_GAIN and TEMP\_OFFSET bits of Register TEMP\_TRIM are programmed. To

## THEORY OF OPERATION

configure the temperature sensor, program the TEMP\_CFG register. See the [ADE9430 Technical Reference Manual](#) for additional information.

## APPLICATIONS INFORMATION

### WAVEFORM BUFFER

The ADE9430 has a waveform buffer comprised of 2048, 32-bit memory locations.

Continuous resampled waveforms with 1024 points per 10 or 12 line cycles processed by the DSP. The data rate varies with the line period. The waveform buffer holds approximately 100 ms of waveform data per channel.

Use the SPI burst read mode to read the waveform buffer contents. The default value bursts out all the channels in the waveform buffer.

The waveform buffer generates an interrupt on  $\overline{\text{IRQ}0}$  after half the buffer is full and the last address is filled. The DSP must be on to use the waveform buffer.

See the [ADE9430 Technical Reference Manual](#) for additional information.

### INTERRUPTS AND EVENTS

The ADE9430 has three pins ( $\overline{\text{IRQ}0}$ ,  $\overline{\text{IRQ}1}$ , and CF4/ $\overline{\text{EVENT}}$ / $\overline{\text{DREADY}}$ ) that can be used as interrupts to the host processor. The  $\overline{\text{IRQ}0}$  and  $\overline{\text{IRQ}1}$  pins go low when an enabled interrupt occurs and stay low until the event is acknowledged by setting the corresponding status bit in the STATUS0 and STATUS1 registers, respectively. The bits in the MASK0 and MASK1 registers configure respective interrupts. The  $\overline{\text{EVENT}}$  function, which can multiplex with the CF4 and DREADY options, tracks the state of the enabled signals and goes low and high with these internal signals. The CF4\_CFG bits in CONFIG1 register set the CF4/EVENT/DREADY pin functionality.

See the [ADE9430 Technical Reference Manual](#) for additional information.

### ACCESSING ON-CHIP DATA

#### SPI Protocol Overview

The ADE9430 has an SPI-compatible interface, consisting of four pins: SCLK, MOSI, MISO, and  $\overline{\text{SS}}$ . The ADE9430 is always an SPI subordinate; it never initiates SPI communication. The SPI is compatible with 16-bit and 32-bit read and write operations. The maximum serial clock frequency supported by this interface is 20 MHz.

The ADE9430 provides SPI burst read functionality on certain registers and the waveform buffer that allows multiple registers to be read after sending one CMD\_HDR.

See the [ADE9430 Technical Reference Manual](#) for additional information.

The ADE9430 SPI port calculates a 16-bit cyclic redundancy check (CRC-16) of the data sent out on its MOSI pin so that the integrity of the data received by the main can be checked. The CRC of the data sent out on the MOSI pin during the last register read is offered in a 16-bit register, CRC\_SPI, and can be appended to the SPI read data as part of the SPI transaction.

#### Additional Communication Verification Registers

The ADE9430 includes three registers that allow SPI operation verification. The LAST\_CMD (Address 0x4AE), LAST\_DATA\_16 (Address 0x4AC), and LAST\_DATA\_32 (Address 0x423) registers record the received CMD\_HDR and the last read or transmitted data. See the [ADE9430 Technical Reference Manual](#) for additional information.

#### CRC of Configuration Registers

The configuration register CRC feature in the ADE9430 monitors certain externally and internally accessible register values. It also optionally includes 15 registers that are individually selectable in the CRC\_OPTEN register. The result is stored in the CRC\_RSLT register. The ADE9430 generates an interrupt on  $\overline{\text{IRQ}1}$  if any of the monitored registers change the value of the CRC\_RSLT register.

See the [ADE9430 Technical Reference Manual](#) for additional information.

#### Configuration Lock

The configuration lock feature prevents changes to the ADE9430 configuration. To enable this feature, write 0x3C64 to the WR\_LOCK register. To disable the feature, write 0x4AD1 to the WR\_LOCK register.

To determine whether this feature is active, read the WR\_LOCK register, which reads as 1 if the protection is enabled and 0 if it is disabled.

When this feature is enabled, it prevents writing to addresses from Address 0x000 to Address 0x073 and Address 0x400 to Address 0x4FE. See the [ADE9430 Technical Reference Manual](#) for additional information.

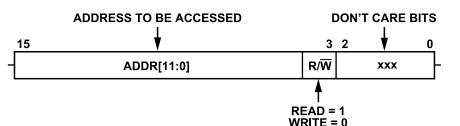
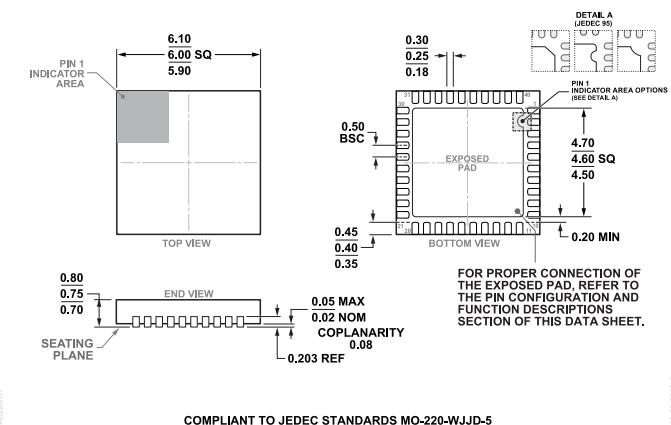


Figure 54. Command Header, CMD\_HDR

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD-5

110-0202018A

**Figure 55. 40-Lead Lead Frame Chip Scale Package [LFCSP]****6 mm × 6 mm Body and 0.75 mm Package Height****(CP-40-7)****Dimensions shown in millimeters**

Updated: May 16, 2022

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Packing Quantity	Package Option
ADE9430ACPZ	-40°C to +85°C	40-Lead LFCSP (6 mm × 6 mm with EPAD)	Tray, 490	CP-40-7
ADE9430ACPZ-RL	-40°C to +85°C	40-Lead LFCSP (6 mm × 6 mm with EPAD)	Reel, 2500	CP-40-7

<sup>1</sup> Z = RoHS Compliant Part.

## EVALUATION BOARDS

Model <sup>1</sup>	Description
EVAL-ADE9430ARDZ	Evaluation Board

<sup>1</sup> Z = RoHS Compliant Part.