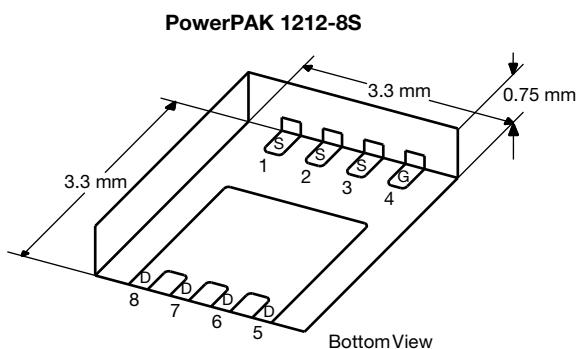


## P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) Max.	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
- 20	0.0045 at V <sub>GS</sub> = - 4.5 V	- 50 <sup>e</sup>	93 nC
	0.0063 at V <sub>GS</sub> = - 2.5 V	- 50 <sup>e</sup>	
	0.0115 at V <sub>GS</sub> = - 1.8 V	- 50 <sup>e</sup>	


**Ordering Information:**

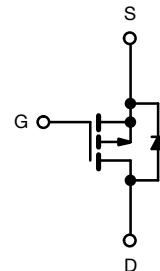
SiSS23DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

**FEATURES**

- TrenchFET® Power MOSFET
- Low Thermal Resistance PowerPAK® Package with Small Size and Low 0.75 mm Profile
- 100 % R<sub>g</sub> and UIS Tested
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**
**APPLICATIONS**

- Smart Phones, Tablet PCs, Mobile Computing
  - Battery Switch
  - Load Switch
  - Power Management
  - Battery Management



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	- 20	V
Gate-Source Voltage	V <sub>GS</sub>	± 8	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	- 50 <sup>e</sup>	A
		- 50 <sup>e</sup>	
		- 27 <sup>a, b</sup>	
		- 21 <sup>a, b</sup>	
Pulsed Drain Current (t = 100 µs)	I <sub>DM</sub>	- 200	
Continuous Source-Drain Diode Current	I <sub>S</sub>	- 47.5	
		- 4 <sup>a, b</sup>	
Avalanche Current	I <sub>AS</sub>	- 23	mJ
Single-Pulse Avalanche Energy	E <sub>AS</sub>	26	
Maximum Power Dissipation	P <sub>D</sub>	57	W
		36	
		4.8 <sup>a, b</sup>	
		3 <sup>a, b</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 50 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>c, d</sup>		260	

Notes:

- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Package limited.

**THERMAL RESISTANCE RATINGS**

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a, b</sup>	$R_{thJA}$	21	26	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	1.7	2.2	

Notes:

- a. Surface mounted on 1" x 1" FR4 board.  
 b. Maximum under steady state conditions is 63 °C/W.

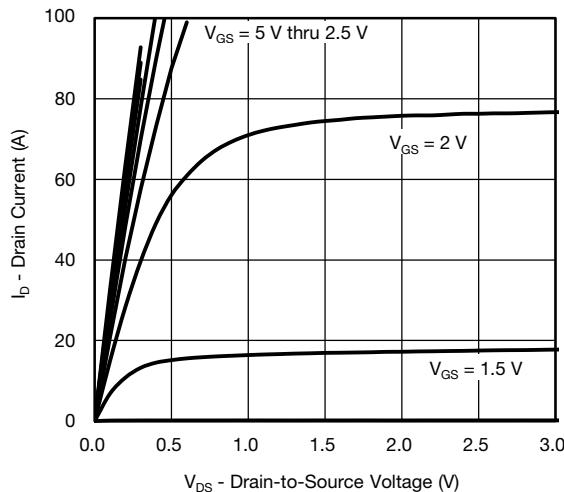
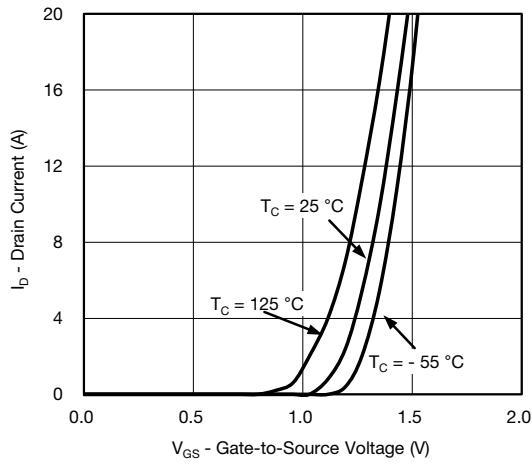
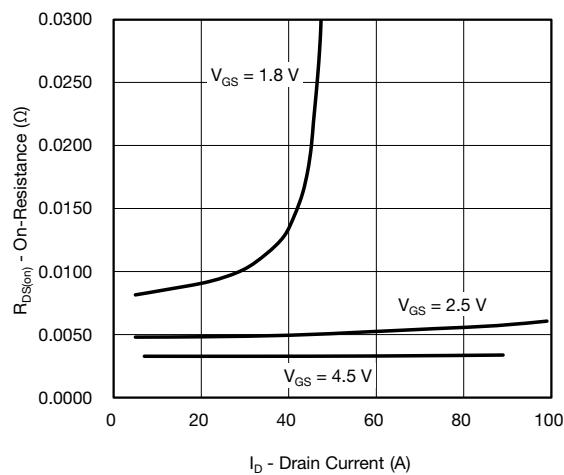
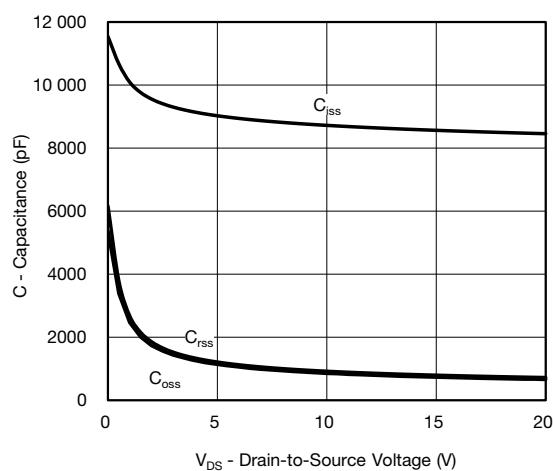
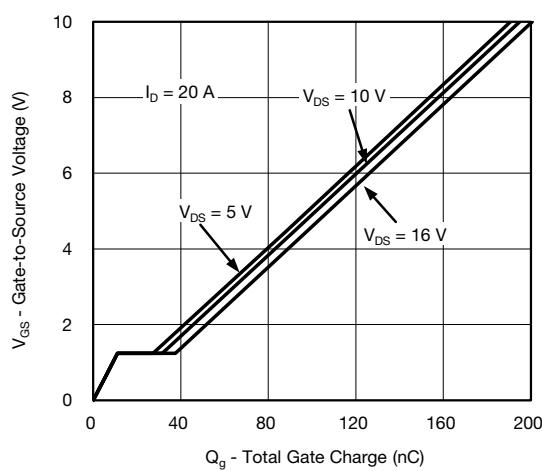
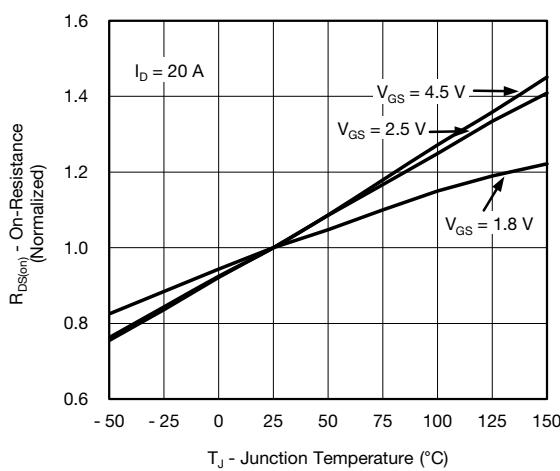
**SPECIFICATIONS ( $T_J = 25$  °C, unless otherwise noted)**

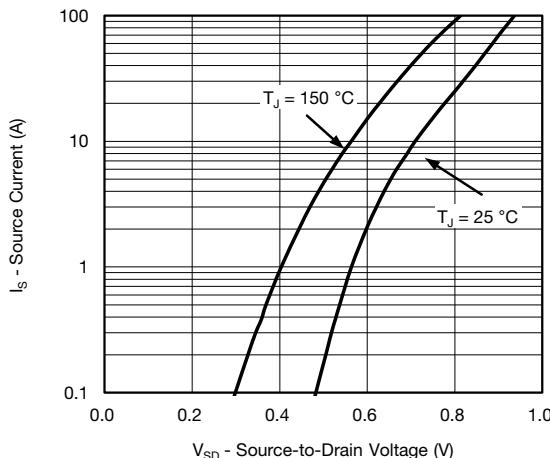
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0$ V, $I_D = - 250$ μA	- 20			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = - 250$ μA		- 12		mV/ °C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			3.4		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = - 250$ μA	- 0.4		- 0.9	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = \pm 8$ V			± 100	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = - 20$ V, $V_{GS} = 0$ V			- 1	μA
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} = - 20$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			- 10	
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{DS} \leq - 5$ V, $V_{GS} = - 4.5$ V	- 20			A
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = - 10$ V, $I_D = - 20$ A		0.0035	0.0045	Ω
		$V_{GS} = - 4.5$ V, $I_D = - 20$ A		0.0051	0.0063	
		$V_{GS} = - 2.5$ V, $I_D = - 10$ A		0.0081	0.0115	
		$V_{GS} = - 1.8$ V, $I_D = - 10$ A				
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = - 15$ V, $V_{GS} = 0$ V, $f = 1$ MHz		8840		pF
Output Capacitance	$C_{oss}$			835		
Reverse Transfer Capacitance	$C_{rss}$			900		
Total Gate Charge	$Q_g$	$V_{DS} = - 15$ V, $V_{GS} = - 10$ V, $I_D = - 20$ A		195	300	nC
Gate-Source Charge	$Q_{gs}$			93	140	
Gate-Drain Charge	$Q_{gd}$			12		
Gate Resistance	$R_g$			21		
Turn-On Delay Time	$t_{d(on)}$	$f = 1$ MHz $V_{DD} = - 10$ V, $R_L = 1$ Ω $I_D \geq - 10$ A, $V_{GEN} = - 4.5$ V, $R_g = 1$ Ω	0.5	2.6	5.2	Ω
Rise Time	$t_r$			45	90	ns
Turn-Off DelayTime	$t_{d(off)}$			50	100	
Fall Time	$t_f$			140	280	
Turn-On Delay Time	$t_{d(on)}$			50	100	
Rise Time	$t_r$	$V_{DD} = - 10$ V, $R_L = 1$ Ω $I_D \geq - 10$ A, $V_{GEN} = - 10$ V, $R_g = 1$ Ω	15	30		ns
Turn-Off DelayTime	$t_{d(off)}$			5	10	
Fall Time	$t_f$			150	300	
				40	80	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25$ °C			- 50 <sup>c</sup>	A
Pulse Diode Forward Current <sup>d</sup>	$I_{SM}$				- 200	
Body Diode Voltage	$V_{SD}$	$I_F = - 10$ A		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = - 10$ A, $dl/dt = 100$ A/μs, $T_J = 25$ °C		30	60	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			15	30	nC
Reverse Recovery Fall Time	$t_a$			16		ns
Reverse Recovery Rise Time	$t_b$			14		

Notes:

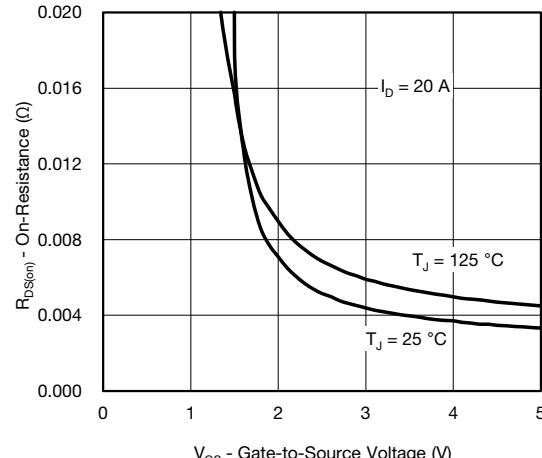
- a. Pulse test; pulse width  $\leq 300$  μs, duty cycle  $\leq 2$  %.  
 b. Guaranteed by design, not subject to production testing.  
 c. Package limited.  
 d.  $t = 100$  μs.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

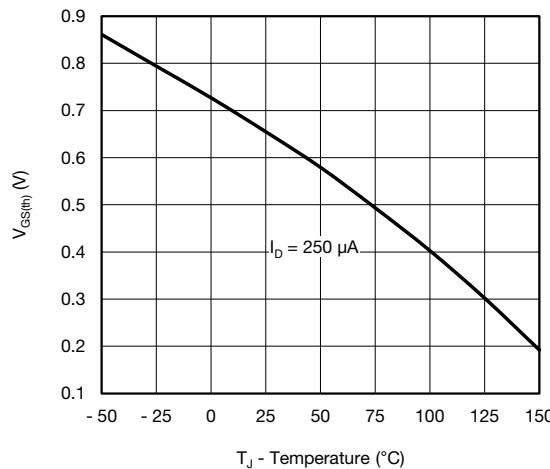
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current and Gate Voltage**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

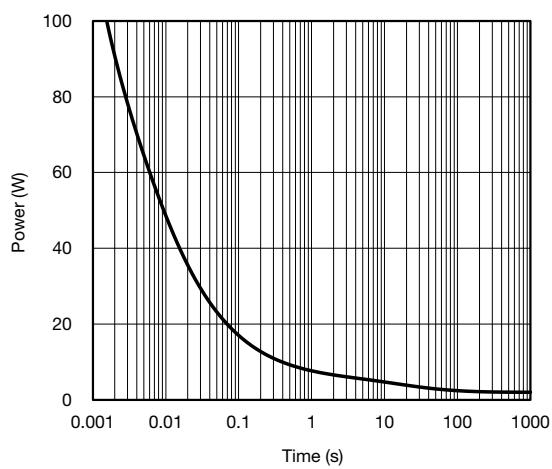
Source-Drain Diode Forward Voltage



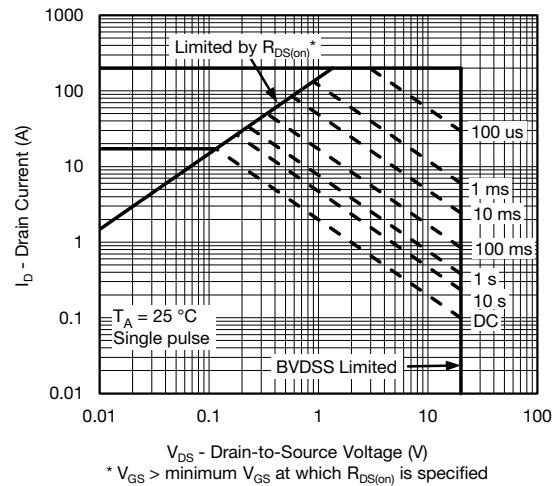
On-Resistance vs. Gate-to-Source Voltage



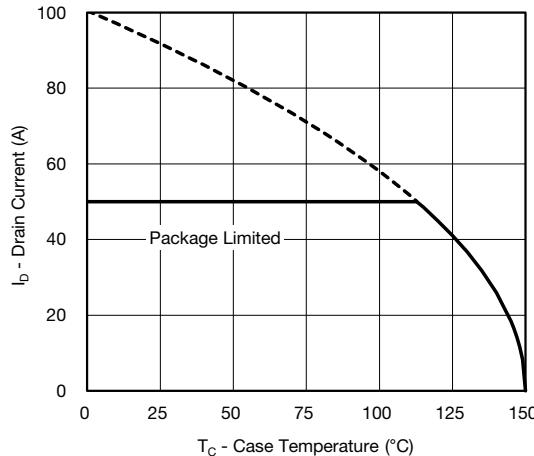
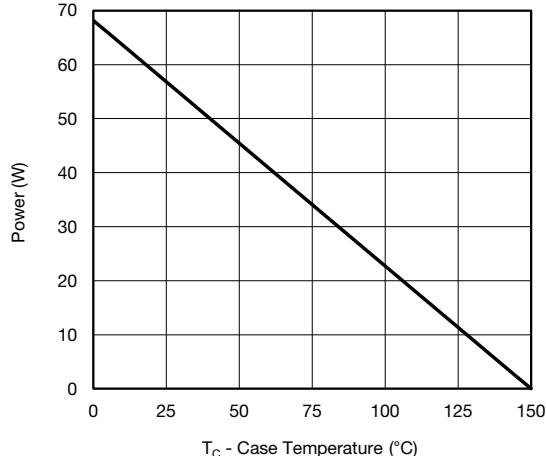
Threshold Voltage



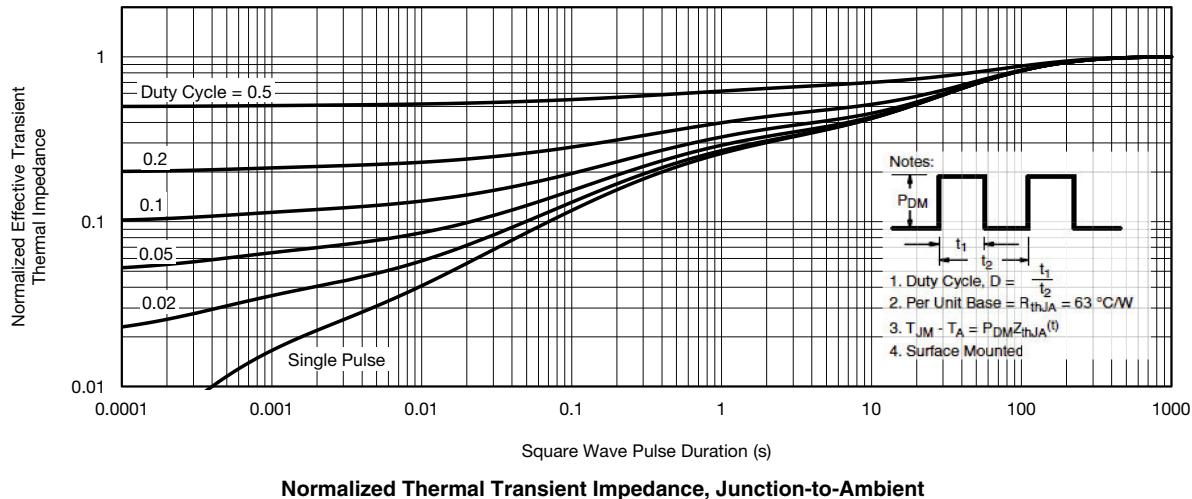
Single Pulse Power, Junction-to-Ambient

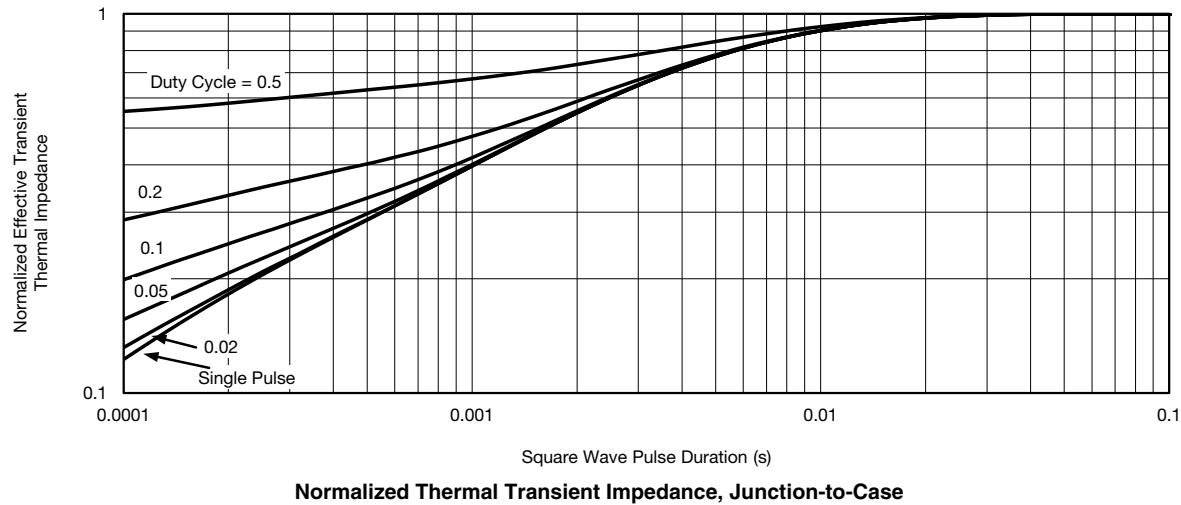


Safe Operating Area, Junction-to-Ambient

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Current Derating\***

**Power, Junction-to-Case**

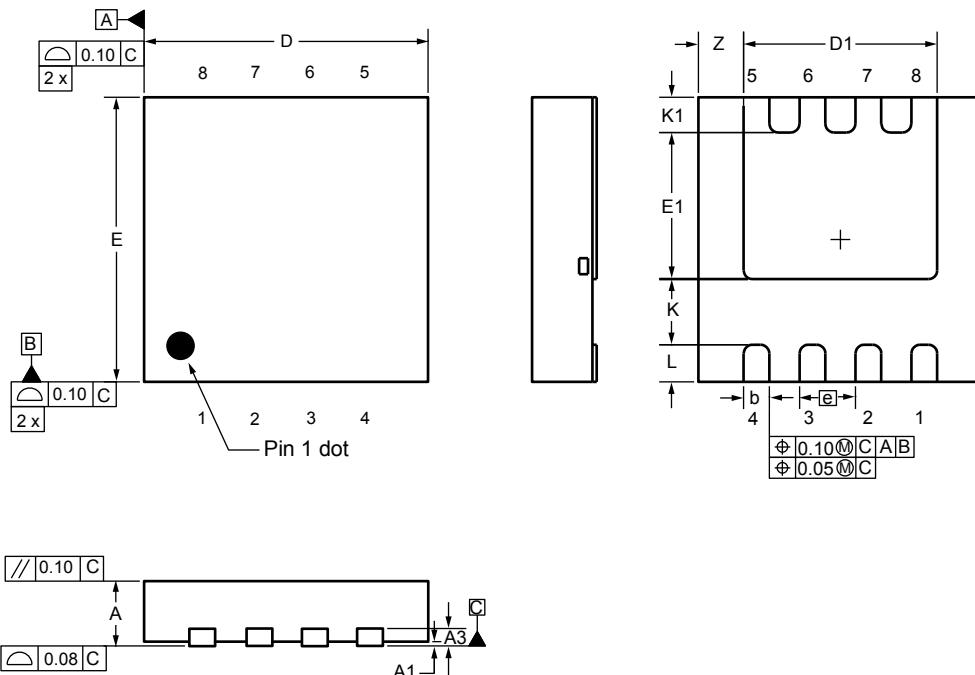
\* The power dissipation  $P_D$  is based on  $T_{J(\max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.


**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

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## Case Outline for PowerPAK® 1212-8S



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.67	0.75	0.83	0.026	0.030	0.033
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 ref.			0.008 ref		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 bsc.			0.026 bsc.		
K	0.76 ref.			0.030 ref.		
K1	0.41 ref.			0.016 ref.		
L	0.33	0.43	0.53	0.013	0.017	0.021
Z	0.525 ref.			0.021 ref.		

ECN: C20-0862-Rev. B, 20-Jul-2020  
DWG: 6008



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