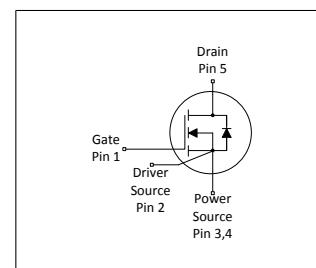
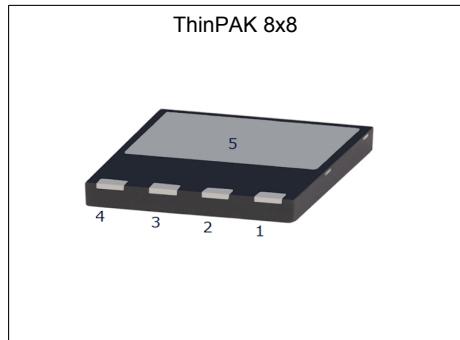


MOSFET

600V CoolMOS™ CFD7 Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. The latest CoolMOS™ CFD7 is the successor to the CoolMOS™ CFD2 series and is an optimized platform tailored to target soft switching applications such as phase-shift full-bridge (ZVS) and LLC. Resulting from reduced gate charge (Q_g), best-in-class reverse recovery charge (Q_{rr}) and improved turn off behavior CoolMOS™ CFD7 offers highest efficiency in resonant topologies. As part of Infineon's fast body diode portfolio, this new product series blends all advantages of a fast switching technology together with superior hard commutation robustness, without sacrificing easy implementation in the design-in process. The CoolMOS™ CFD7 technology meets highest efficiency and reliability standards and furthermore supports high power density solutions. Altogether, CoolMOS™ CFD7 makes resonant switching topologies more efficient, more reliable, lighter and cooler.



Features

- Ultra-fast body diode
- Low gate charge
- Best-in-class reverse recovery charge (Q_{rr})
- Improved MOSFET reverse diode dv/dt and di_F/dt ruggedness
- Lowest FOM $R_{DS(on)} * Q_g$ and $R_{DS(on)} * E_{oss}$
- Best-in-class $R_{DS(on)}$ in SMD and THD packages



Benefits

- Excellent hard commutation ruggedness
- Highest reliability for resonant topologies
- Highest efficiency with outstanding ease-of-use / performance tradeoff
- Enabling increased power density solutions



Potential applications

Suitable for Soft Switching topologies
Optimized for phase-shift full-bridge (ZVS), LLC Applications – Server, Telecom, EV Charging

Product Validation: Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	95	$m\Omega$
$Q_{g,typ}$	51	nC
$I_{D,pulse}$	97	A
$E_{oss} @ 400V$	5.9	μJ
Body diode di_F/dt	1300	$A/\mu s$

Type / Ordering Code	Package	Marking	Related Links
IPL60R095CFD7	PG-VSON-4	60R095F7	see Appendix A

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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	25 16.0	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,\text{pulse}}$	-	-	97	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	114	mJ	$I_D=5.3\text{A}; V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.57	mJ	$I_D=5.3\text{A}; V_{DD}=50\text{V}$; see table 10
Avalanche current, single pulse	I_{AS}	-	-	5.3	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\ldots 400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f > 1 \text{ Hz}$)
Power dissipation	P_{tot}	-	-	147	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-40	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	-	Ncm	-
Continuous diode forward current	I_S	-	-	25	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,\text{pulse}}$	-	-	97	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	70	V/ns	$V_{DS}=0\ldots 400\text{V}, I_{SD}\leq 25\text{A}, T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di _F /dt	-	-	1300	A/ μs	$V_{DS}=0\ldots 400\text{V}, I_{SD}\leq 25\text{A}, T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	$V_{rms}, T_C=25^\circ\text{C}, t=1\text{min}$

¹⁾ Limited by $T_{j,\text{max}}$.

²⁾ Pulse width t_p limited by $T_{j,\text{max}}$

³⁾ Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.85	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm ² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	reflow MSL2A

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	600	-	-	V	$V_{\text{GS}}=0\text{V}$, $I_D=1\text{mA}$
Gate threshold voltage	$V_{(\text{GS})\text{th}}$	3.5	4	4.5	V	$V_{\text{DS}}=V_{\text{GS}}$, $I_D=0.57\text{mA}$
Zero gate voltage drain current ¹⁾	I_{DSS}	-	-	1 47	μA	$V_{\text{DS}}=600\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_j=25^\circ\text{C}$ $V_{\text{DS}}=600\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_j=125^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{\text{GS}}=20\text{V}$, $V_{\text{DS}}=0\text{V}$
Drain-source on-state resistance	$R_{\text{DS}(\text{on})}$	-	0.076 0.172	0.095 -	Ω	$V_{\text{GS}}=10\text{V}$, $I_D=11.4\text{A}$, $T_j=25^\circ\text{C}$ $V_{\text{GS}}=10\text{V}$, $I_D=11.4\text{A}$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	8	-	Ω	$f=1\text{MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2103	-	pF	$V_{\text{GS}}=0\text{V}$, $V_{\text{DS}}=400\text{V}$, $f=250\text{kHz}$
Output capacitance	C_{oss}	-	40	-	pF	$V_{\text{GS}}=0\text{V}$, $V_{\text{DS}}=400\text{V}$, $f=250\text{kHz}$
Effective output capacitance, energy related ²⁾	$C_{\text{o(er)}}$	-	73	-	pF	$V_{\text{GS}}=0\text{V}$, $V_{\text{DS}}=0\ldots400\text{V}$
Effective output capacitance, time related ³⁾	$C_{\text{o(tr)}}$	-	752	-	pF	$I_D=\text{constant}$, $V_{\text{GS}}=0\text{V}$, $V_{\text{DS}}=0\ldots400\text{V}$
Turn-on delay time	$t_{\text{d(on)}}$	-	37	-	ns	$V_{\text{DD}}=400\text{V}$, $V_{\text{GS}}=10\text{V}$, $I_D=9.4\text{A}$, $R_G=5.3\Omega$; see table 9
Rise time	t_r	-	14.5	-	ns	$V_{\text{DD}}=400\text{V}$, $V_{\text{GS}}=10\text{V}$, $I_D=9.4\text{A}$, $R_G=5.3\Omega$; see table 9
Turn-off delay time	$t_{\text{d(off)}}$	-	127	-	ns	$V_{\text{DD}}=400\text{V}$, $V_{\text{GS}}=10\text{V}$, $I_D=9.4\text{A}$, $R_G=5.3\Omega$; see table 9
Fall time	t_f	-	5.7	-	ns	$V_{\text{DD}}=400\text{V}$, $V_{\text{GS}}=10\text{V}$, $I_D=9.4\text{A}$, $R_G=5.3\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	12	-	nC	$V_{\text{DD}}=400\text{V}$, $I_D=9.4\text{A}$, $V_{\text{GS}}=0$ to 10V
Gate to drain charge	Q_{gd}	-	18	-	nC	$V_{\text{DD}}=400\text{V}$, $I_D=9.4\text{A}$, $V_{\text{GS}}=0$ to 10V
Gate charge total	Q_g	-	51	-	nC	$V_{\text{DD}}=400\text{V}$, $I_D=9.4\text{A}$, $V_{\text{GS}}=0$ to 10V
Gate plateau voltage	V_{plateau}	-	5.6	-	V	$V_{\text{DD}}=400\text{V}$, $I_D=9.4\text{A}$, $V_{\text{GS}}=0$ to 10V

¹⁾ Maximum specification is defined by calculated six sigma upper confidence bound

²⁾ $C_{\text{o(er)}}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

³⁾ $C_{\text{o(tr)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	1.0	-	V	$V_{GS}=0V$, $I_F=11.4A$, $T_j=25^\circ C$
Reverse recovery time	t_{rr}	-	103	206	ns	$V_R=400V$, $I_F=9.4A$, $di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	0.53	1.06	μC	$V_R=400V$, $I_F=9.4A$, $di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	8.9	-	A	$V_R=400V$, $I_F=9.4A$, $di_F/dt=100A/\mu s$; see table 8

4 Electrical characteristics diagrams

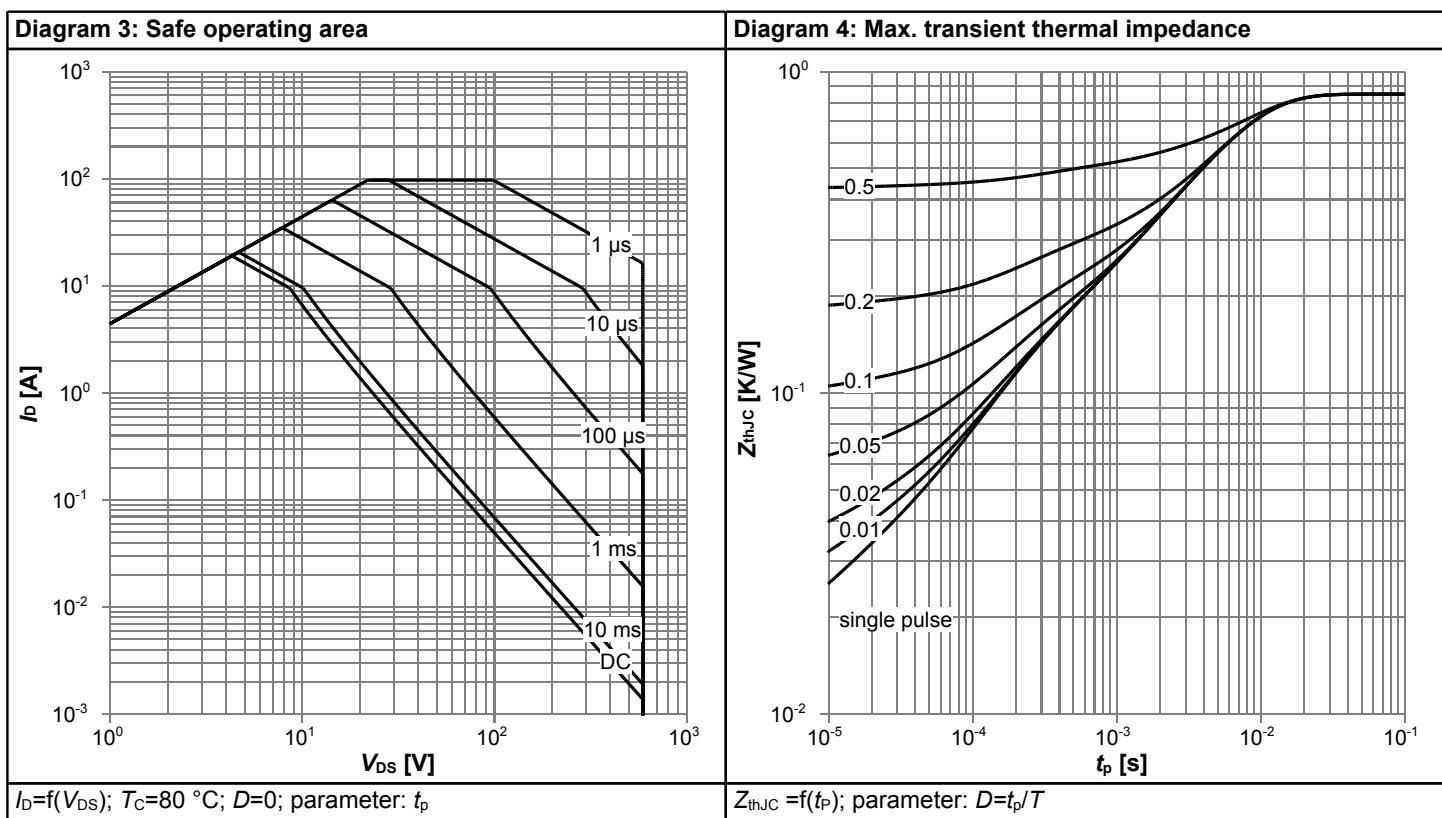
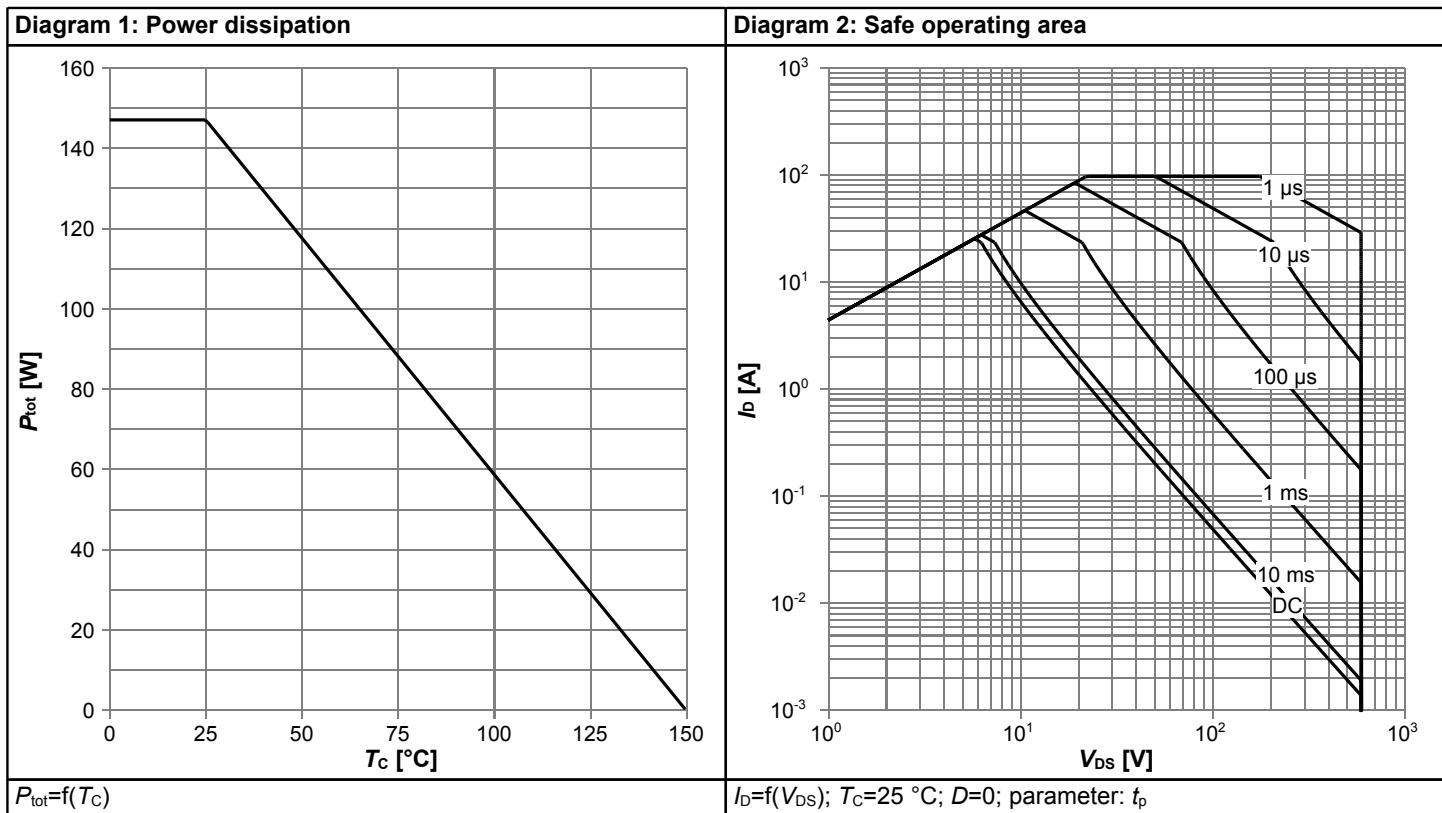
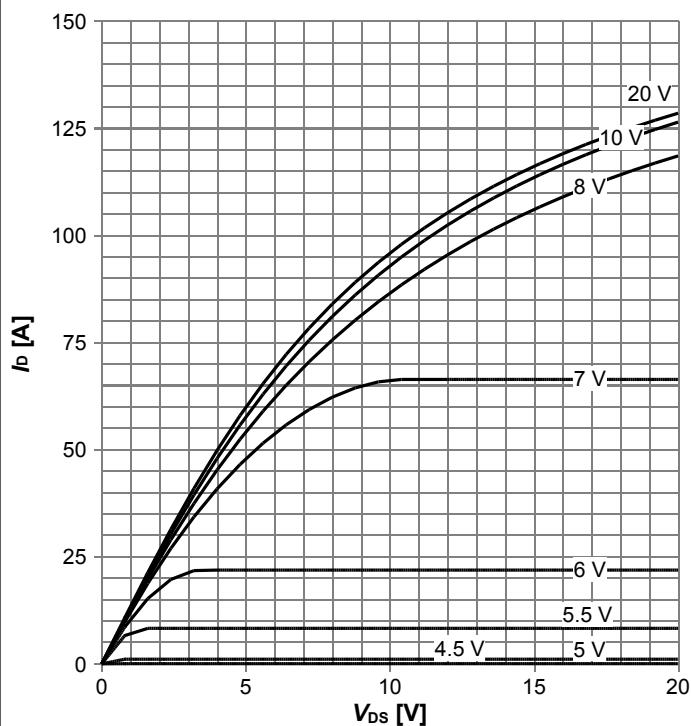
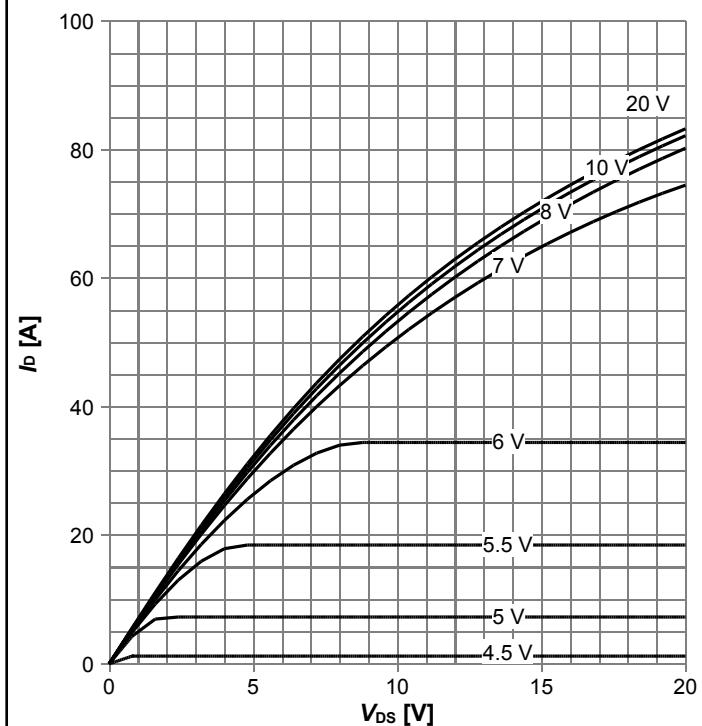


Diagram 5: Typ. output characteristics



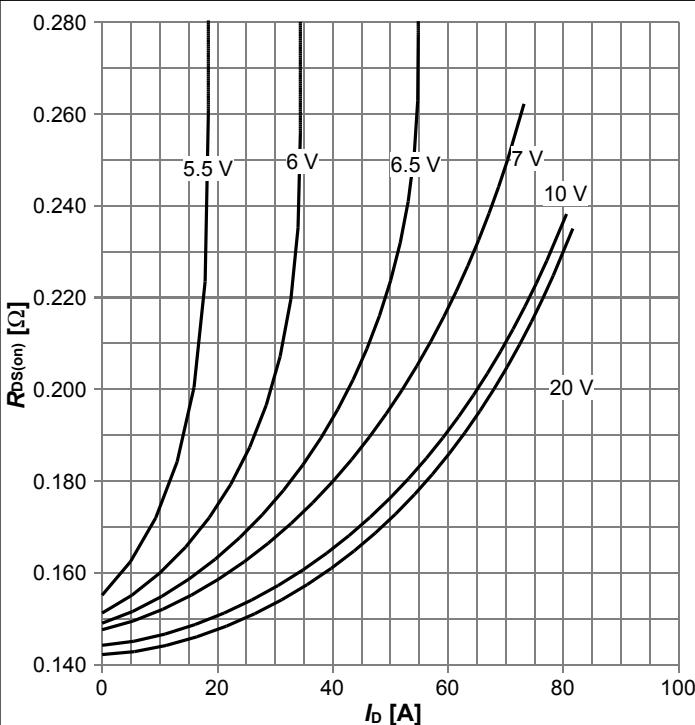
$I_D=f(V_{DS})$; $T_j=25\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



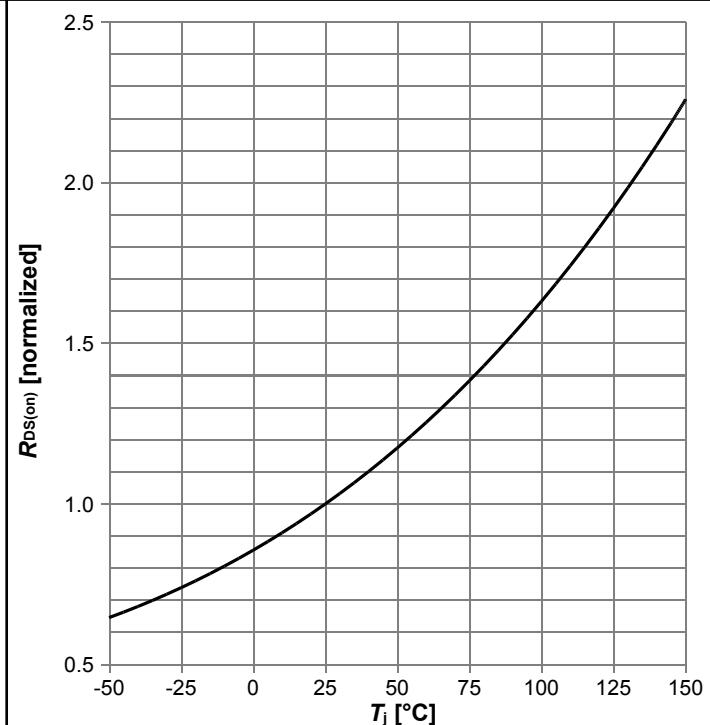
$I_D=f(V_{DS})$; $T_j=125\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



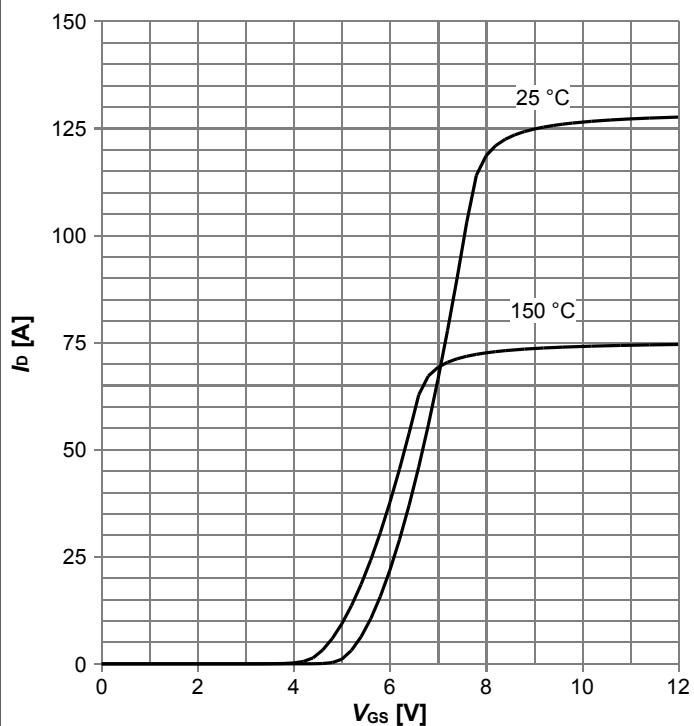
$R_{DS(on)}=f(I_D)$; $T_j=125\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



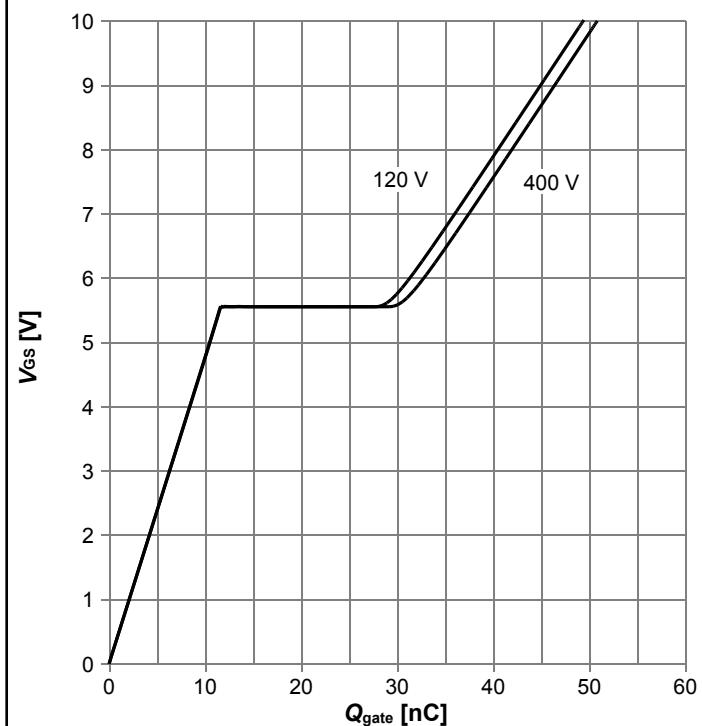
$R_{DS(on)}=f(T_j)$; $I_D=11.4\text{ A}$; $V_{GS}=10\text{ V}$

Diagram 9: Typ. transfer characteristics



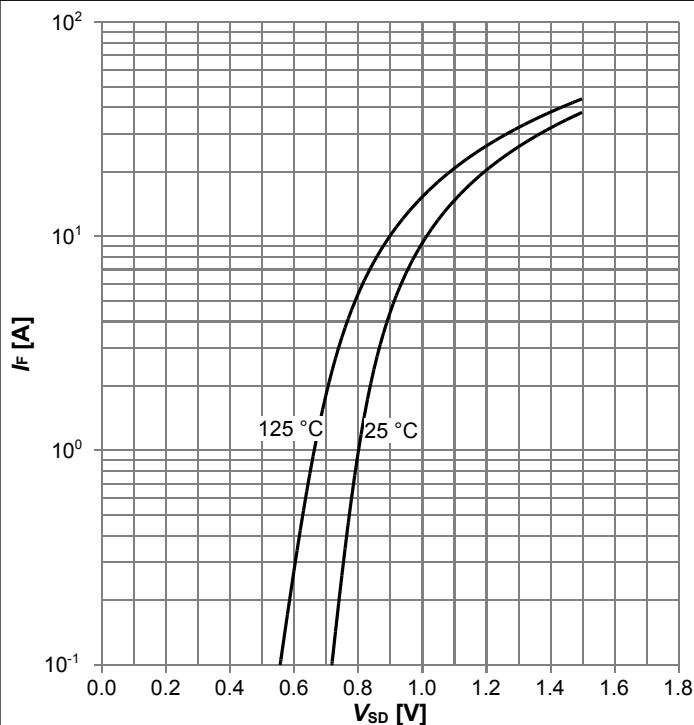
$I_D=f(V_{GS})$; $V_{DS}=20\text{V}$; parameter: T_j

Diagram 10: Typ. gate charge



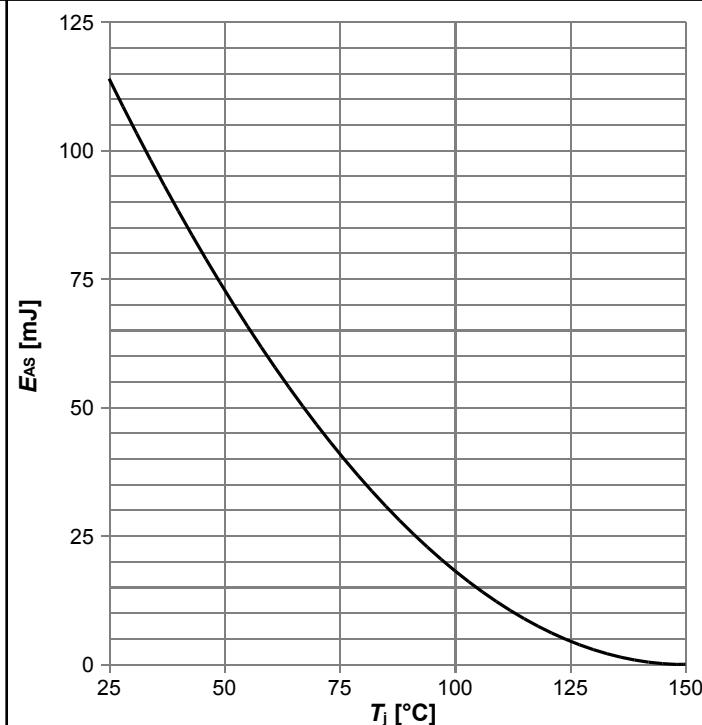
$V_{GS}=f(Q_{gate})$; $I_D=9.4\text{ A}$ pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



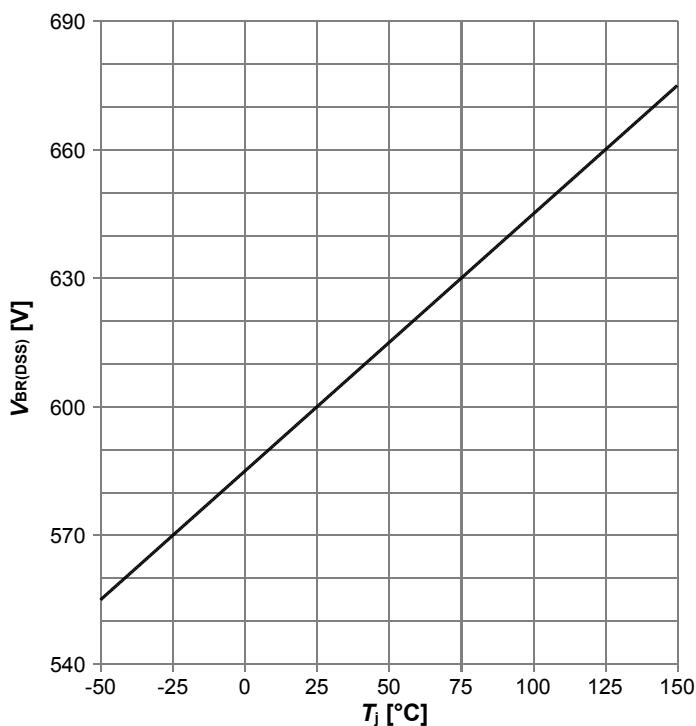
$I_F=f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



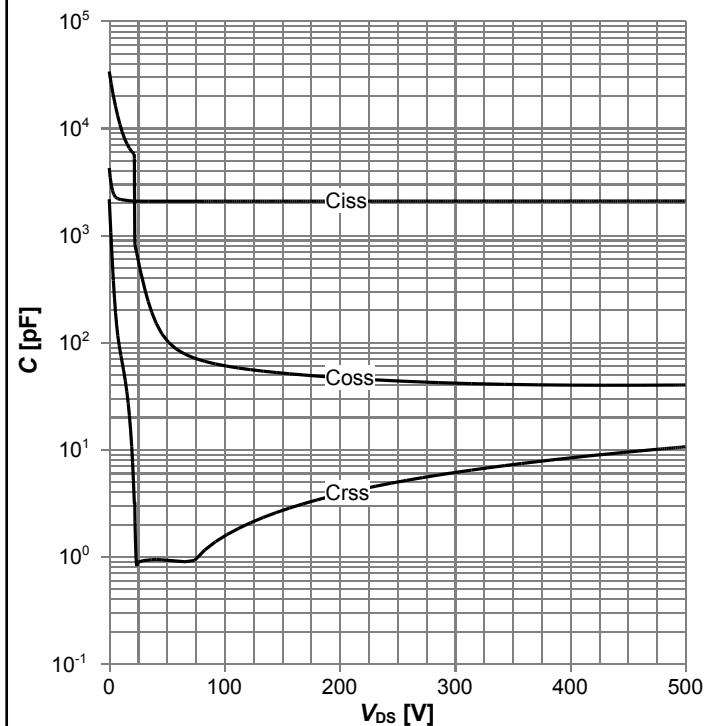
$E_{AS}=f(T_j)$; $I_D=5.3\text{ A}$; $V_{DD}=50\text{ V}$

Diagram 13: Drain-source breakdown voltage



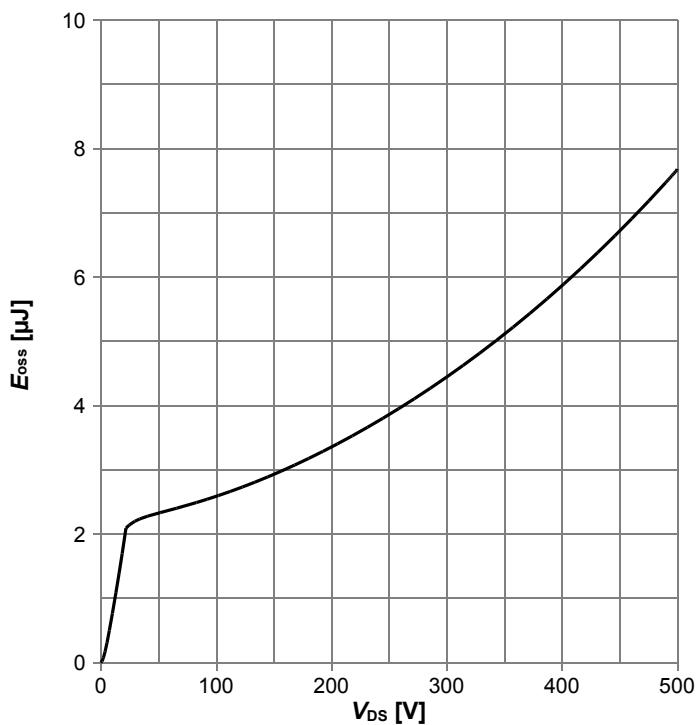
$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$

Diagram 14: Typ. capacitances



$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 250 \text{ kHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss} = f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics

Test circuit for diode characteristics	Diode recovery waveform
<p>$R_g1 = R_g2$</p>	

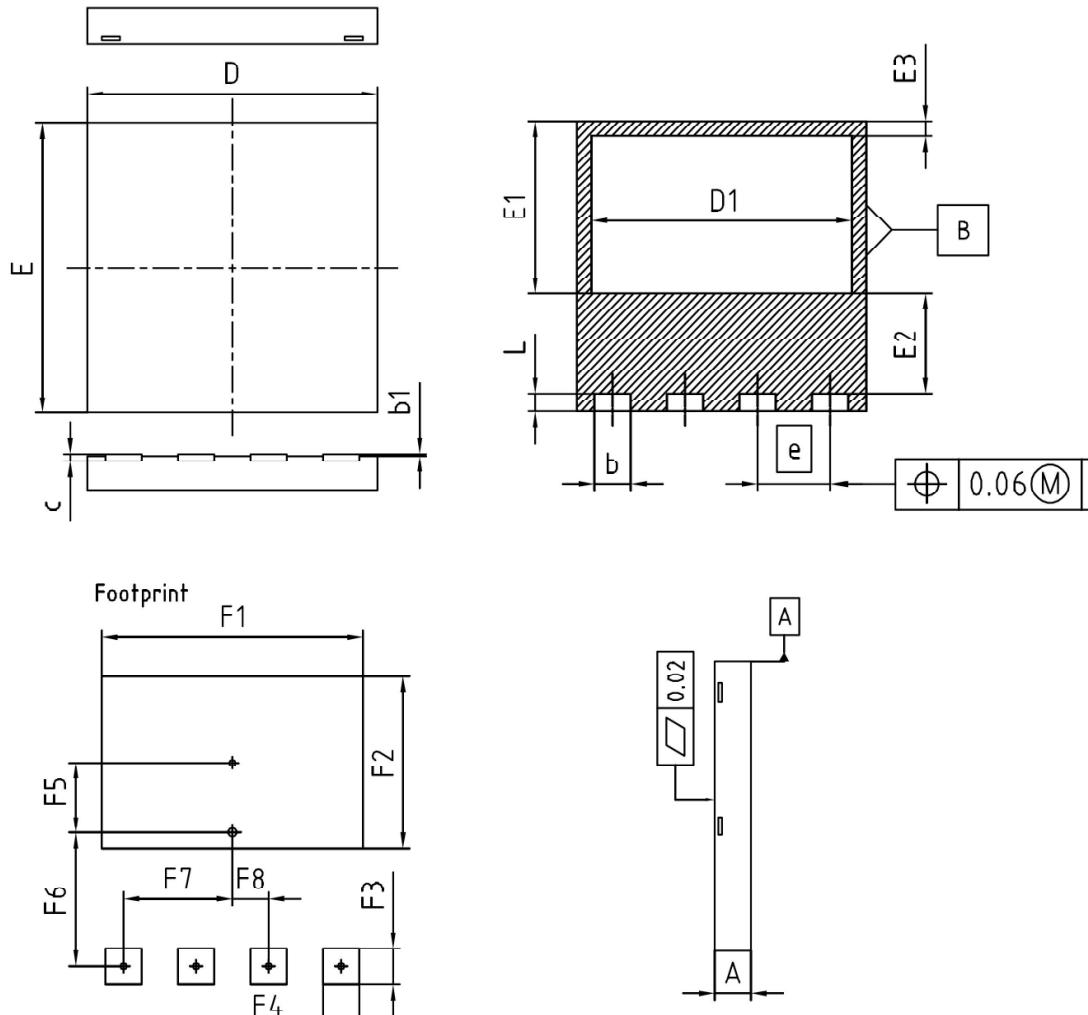
Table 9 Switching times

Switching times test circuit for inductive load	Switching times waveform

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform

6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.90	1.10	0.035	0.043
b1	0.00	0.05	0.000	0.002
c	0.10	0.30	0.004	0.012
D	7.90	8.10	0.311	0.319
D1	7.10	7.30	0.280	0.287
E	7.90	8.10	0.311	0.319
E1	4.65	4.85	0.183	0.191
E2	2.65	2.85	0.104	0.112
E3	0.30	0.50	0.012	0.020
e	2.00 (BSC)		0.079 (BSC)	
L	0.40	0.60	0.016	0.024
N	4		4	
F1	7.20		0.283	
F2	4.75		0.187	
F3	1.00		0.039	
F4	1.00		0.039	
F5	1.43		0.056	
F6	4.20		0.165	
F7	3.00		0.118	
F8	1.00		0.039	

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ISSUE DATE
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REVISION
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Figure 1 Outline PG-VSON-4, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS CFD7 Webpage:** www.infineon.com
- **IFX CoolMOS CFD7 application note:** www.infineon.com
- **IFX CoolMOS CFD7 simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPL60R095CFD7

Revision: 2018-04-20, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2018-04-20	Release of final version

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