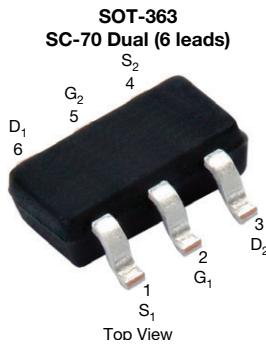


N- and P-Channel 30 V (D-S) MOSFET



Marking code: RG

PRODUCT SUMMARY		
	N-CHANNEL	P-CHANNEL
V_{DS} (V)	30	-30
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm 10$ V	0.388	0.890
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm 4.5$ V	0.525	1.700
Q_g typ. (nC)	0.55	0.8
I_D (A) ^a	0.7	-0.5
Configuration	N- and p-pair	

FEATURES

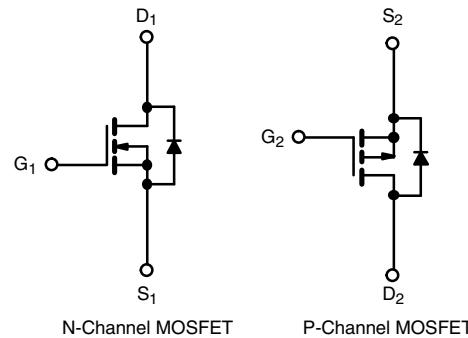
- TrenchFET® power MOSFET
- 100 % R_g tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- DC/DC converter
- Load switch



ORDERING INFORMATION

Package	SOT-363
Lead (Pb)-free and halogen-free	Si1539CDL-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	N-CHANNEL		P-CHANNEL		UNIT
		TYP.	MAX.	TYP.	MAX.	
Drain-source voltage	V_{DS}	30		-30		V
Gate-source voltage	V_{GS}	± 20		± 20		
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	I_D	0.7	-0.5		A
	$T_C = 70$ °C		0.6	-0.4		
	$T_A = 25$ °C		0.7 b, c	-0.4 b, c		
	$T_A = 70$ °C		0.5 b, c	-0.4 b, c		
Source-drain current diode current	$T_C = 25$ °C	I_S	0.3	-0.3		A
	$T_A = 25$ °C		0.2 b, c	-0.2 b, c		
Pulsed drain current	I_{DM}	2		-1		
Maximum power dissipation	$T_C = 25$ °C	P_D	0.34	0.34		W
	$T_C = 70$ °C		0.22	0.22		
	$T_A = 25$ °C		0.29 b, c	0.29 b, c		
	$T_A = 70$ °C		0.18 b, c	0.18 b, c		
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150				°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	N-CHANNEL		P-CHANNEL		UNIT
		TYP.	MAX.	TYP.	MAX.	
Maximum junction-to-ambient ^{b, d}	R_{thJA}	365	438	365	438	°C/W
Maximum junction-to-foot (drain)	R_{thJF}	308	370	308	370	

Notes

- Based on $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- Maximum under steady state conditions is 486 °C/W (N-channel) and 486 °C/W (P-channel)

SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP. ^a	MAX.	UNIT
Static								
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	N-Ch	30	-	-	V	
		$V_{GS} = 0 \text{ V}$, $I_D = -250 \mu\text{A}$	P-Ch	-30	-	-		
V _{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$	N-Ch	-	30	-	mV/ $^\circ\text{C}$	
		$I_D = -250 \mu\text{A}$	P-Ch	-	-18	-		
$V_{GS(\text{th})}$ temperature coefficient	$\Delta V_{GS(\text{th})}/T_J$	$I_D = 250 \mu\text{A}$	N-Ch	-	-3.6	-		
		$I_D = -250 \mu\text{A}$	P-Ch	-	3.3	-		
Gate-source threshold voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	N-Ch	1.2	-	2.5	V	
		$V_{DS} = V_{GS}$, $I_D = -250 \mu\text{A}$	P-Ch	-1.2	-	-2.5		
Gate-body leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$	N-Ch	-	-	± 100	nA	
			P-Ch	-	-	± 100		
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$	N-Ch	-	-	1	μA	
		$V_{DS} = -30 \text{ V}$, $V_{GS} = 0 \text{ V}$	P-Ch	-	-	-1		
		$V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^\circ\text{C}$	N-Ch	-	-	10		
		$V_{DS} = -30 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^\circ\text{C}$	P-Ch	-	-	-10		
On-state drain current ^b	$I_{D(on)}$	$V_{DS} = 5 \text{ V}$, $V_{GS} = 10 \text{ V}$	N-Ch	2	-	-	A	
		$V_{DS} = -5 \text{ V}$, $V_{GS} = -10 \text{ V}$	P-Ch	-1	-	-		
Drain-source on-state resistance ^b	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = 0.6 \text{ A}$	N-Ch	-	0.323	0.388	Ω	
		$V_{GS} = -10 \text{ V}$, $I_D = -0.4 \text{ A}$	P-Ch	-	0.740	0.890		
		$V_{GS} = 4.5 \text{ V}$, $I_D = 0.1 \text{ A}$	N-Ch	-	0.437	0.525		
		$V_{GS} = -4.5 \text{ V}$, $I_D = -0.1 \text{ A}$	P-Ch	-	1.4	1.7		
Forward transconductance ^b	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 0.6 \text{ A}$	N-Ch	-	1.2	-	S	
		$V_{DS} = -15 \text{ V}$, $I_D = -0.4 \text{ A}$	P-Ch	-	0.6	-		
Dynamic ^a								
Input capacitance	C_{iss}	N-Channel $V_{DS} = 15 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	N-Ch	-	28	-	pF	
			P-Ch	-	34	-		
Output capacitance	C_{oss}		N-Ch	-	10	-		
			P-Ch	-	12	-		
Reverse transfer capacitance	C_{rss}		N-Ch	-	5	-		
			P-Ch	-	7	-		
Total gate charge	Q_g	$V_{DS} = 15 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 0.6 \text{ A}$	N-Ch	-	1	1.5	nC	
		$V_{DS} = -15 \text{ V}$, $V_{GS} = -10 \text{ V}$, $I_D = -0.4 \text{ A}$	P-Ch	-	1.5	3		
Gate-source charge	Q_{gs}	N-Channel $V_{DS} = 15 \text{ V}$, $V_{GS} = 4.5 \text{ V}$, $I_D = 0.6 \text{ A}$	N-Ch	-	0.55	1.1		
			P-Ch	-	0.8	1.2		
Gate-drain charge	Q_{gd}		N-Ch	-	0.2	-		
			P-Ch	-	0.4	-		
Gate resistance	R_g	$f = 1 \text{ MHz}$	N-Ch	-	0.2	-	Ω	
			P-Ch	-	0.35	-		

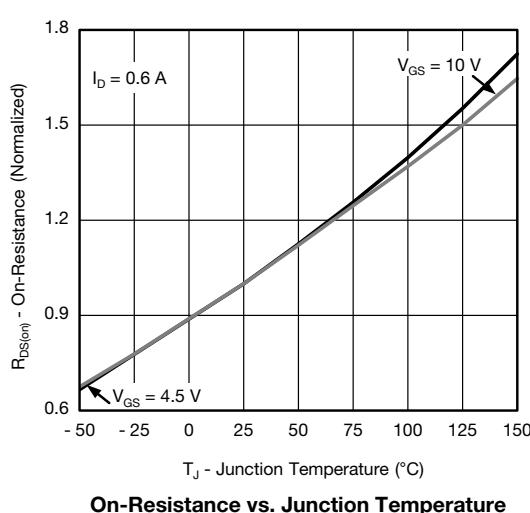
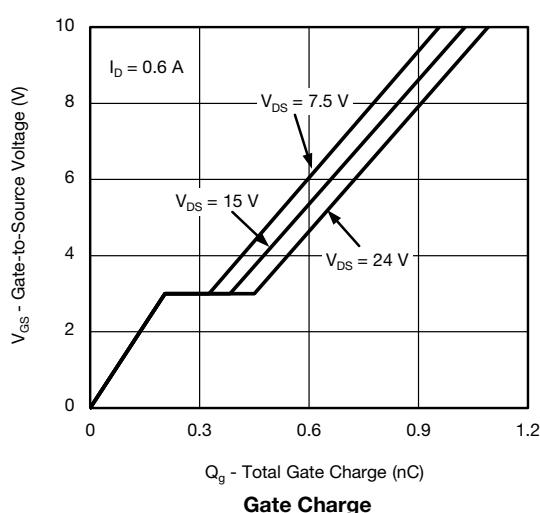
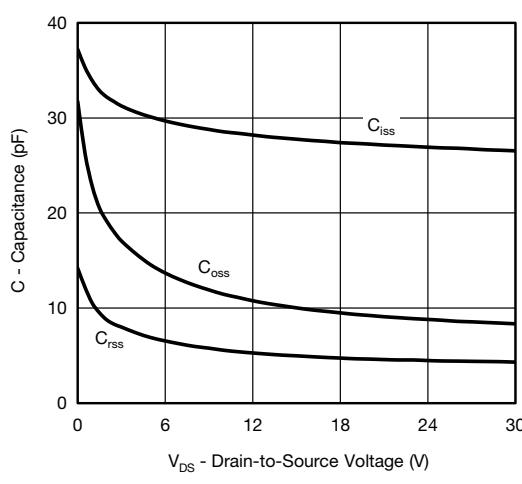
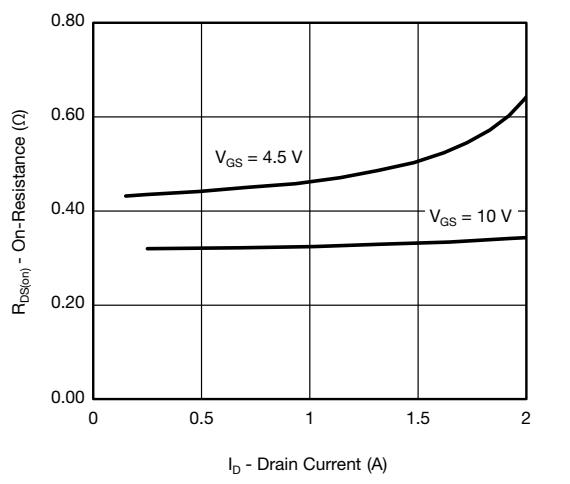
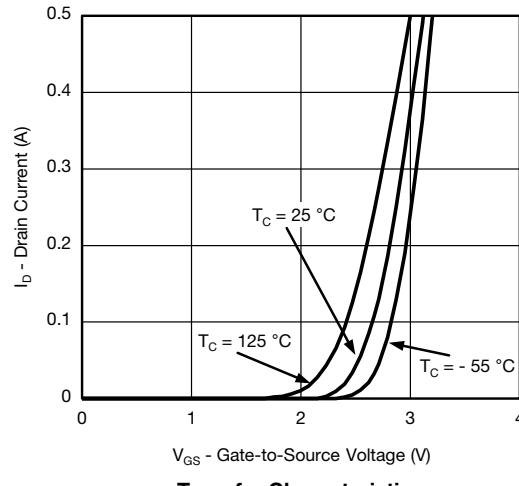
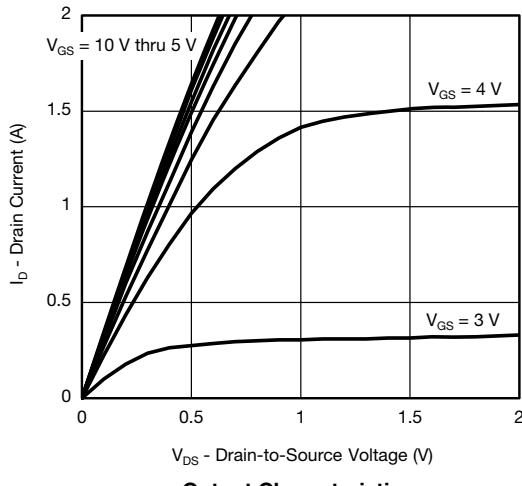
SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

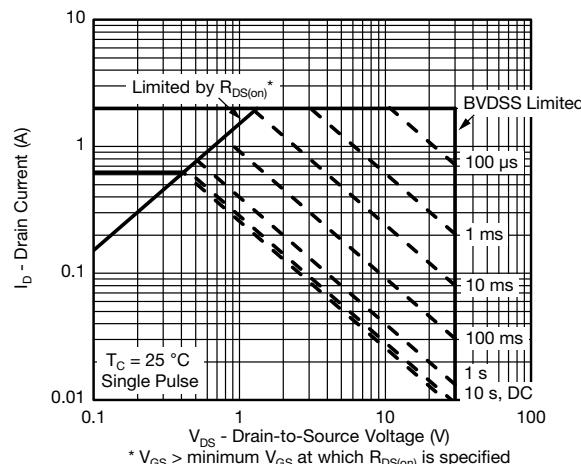
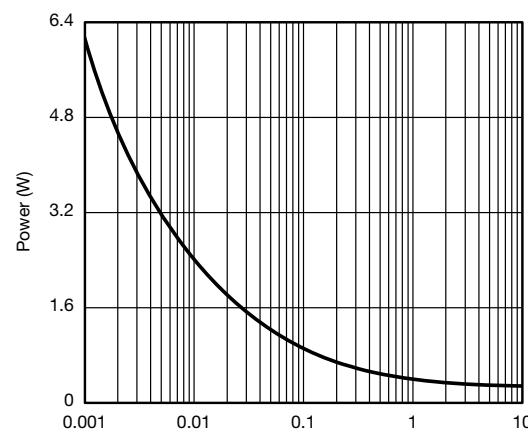
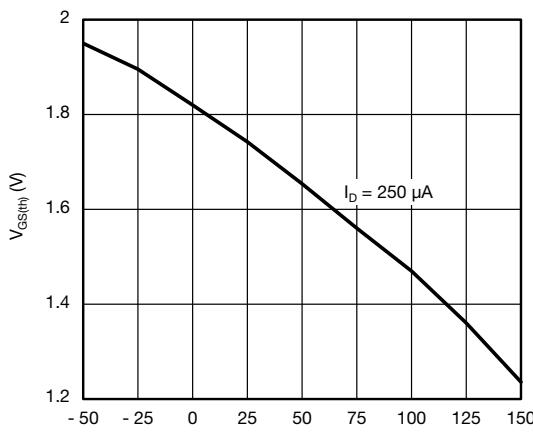
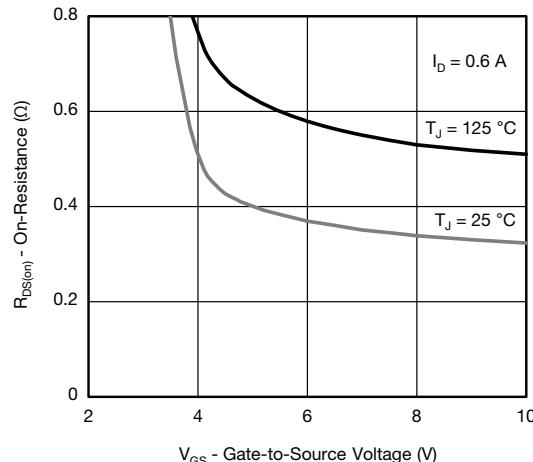
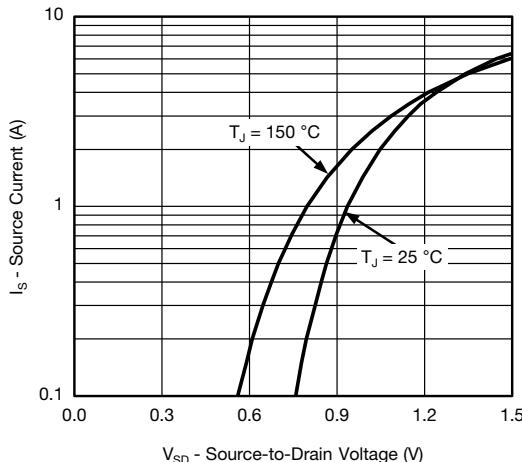
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP. ^a	MAX.	UNIT	
Dynamic ^a							
Turn-on delay time	$t_{d(on)}$	N-Channel $V_{DD} = 15 \text{ V}$, $R_L = 30 \Omega$ $I_D \geq 0.5 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 1 \Omega$ P-Channel $V_{DD} = -15 \text{ V}$, $R_L = 38 \Omega$ $I_D \leq -0.4 \text{ A}$, $V_{GEN} = -10 \text{ V}$, $R_g = 1 \Omega$	N-Ch	-	2	4	
Rise time	t_r		P-Ch	-	1	2	
Turn-off delay time	$t_{d(off)}$		N-Ch	-	14	21	
Fall time	t_f		P-Ch	-	9	18	
Turn-on delay time	$t_{d(on)}$		N-Ch	-	11	20	
Rise time	t_r		P-Ch	-	8	16	
Turn-off delay time	$t_{d(off)}$		N-Ch	-	9	18	
Fall time	t_f		P-Ch	-	8	16	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	$T_C = 25^\circ\text{C}$ N-Channel $V_{DD} = 15 \text{ V}$, $R_L = 30 \Omega$ $I_D \geq 0.5 \text{ A}$, $V_{GEN} = 4.5 \text{ V}$, $R_g = 1 \Omega$ P-Channel $V_{DD} = -15 \text{ V}$, $R_L = 38 \Omega$ $I_D \leq -0.4 \text{ A}$, $V_{GEN} = -4.5 \text{ V}$, $R_g = 1 \Omega$	N-Ch	-	-	0.3	
Pulse diode forward current ^a	I_{SM}		P-Ch	-	-	-0.3	
Body diode voltage	V_{SD}		N-Ch	-	-	2	
Body diode reverse recovery time	t_{rr}		P-Ch	-	-	-1	
Body diode reverse recovery charge	Q_{rr}		N-Ch	-	0.8	1.2	
Reverse recovery fall time	t_a		P-Ch	-	-0.8	-1.2	
Reverse recovery rise time	t_b		N-Ch	-	10	20	
			P-Ch	-	16	24	
$I_F = 0.5 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$							
$I_F = -0.5 \text{ A}$, $dI/dt = -100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$							
ns A V ns nC ns							

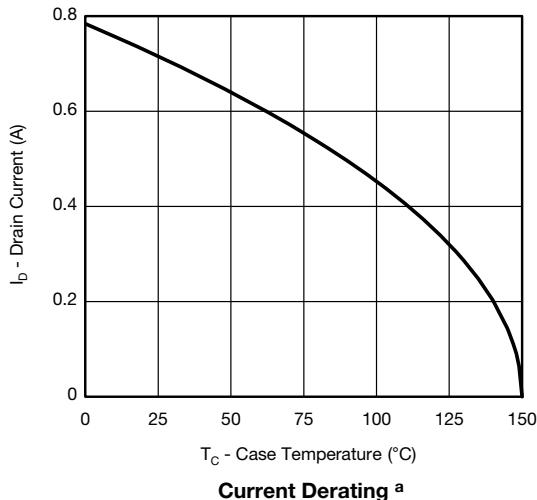
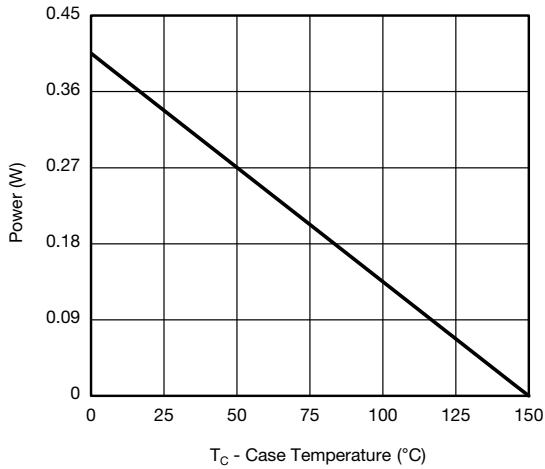
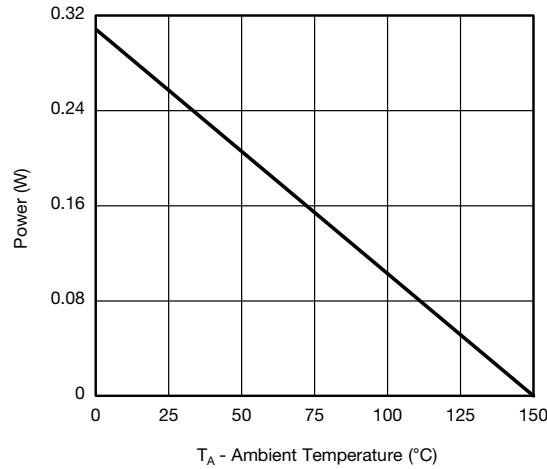
Notes

- a. Guaranteed by design, not subject to production testing
- b. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$

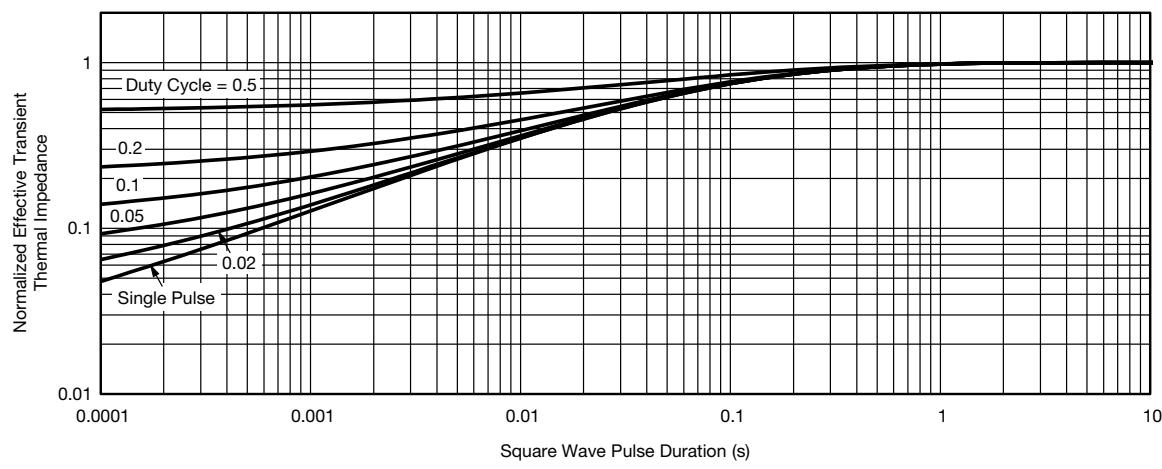
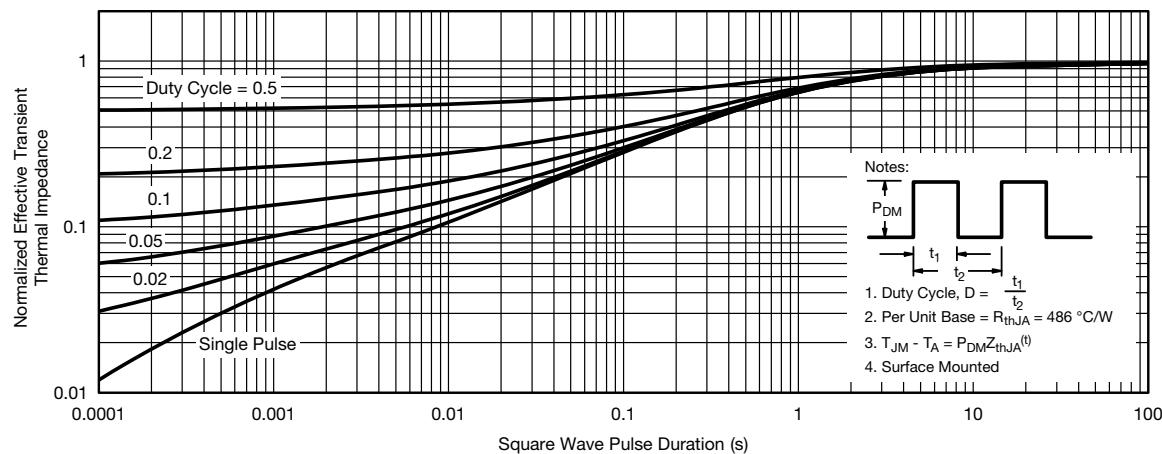
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

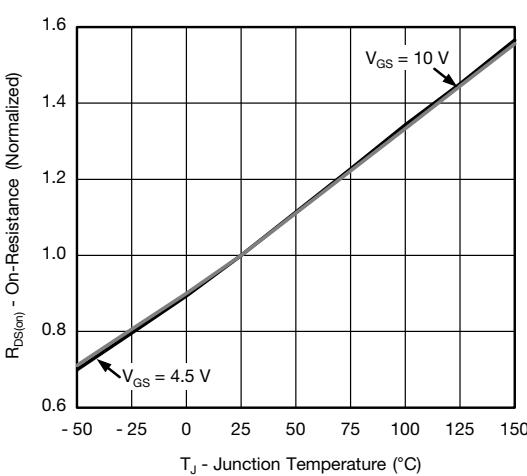
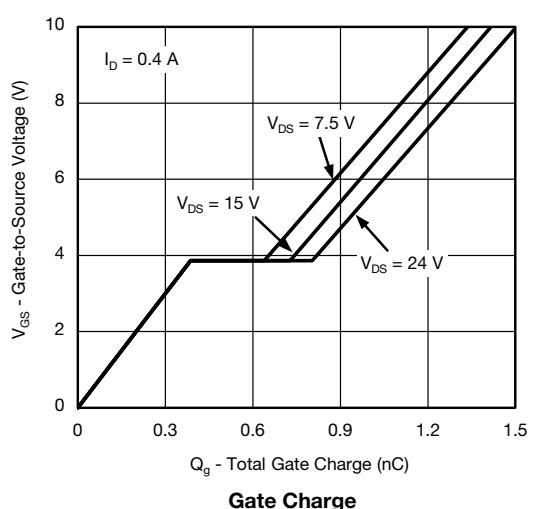
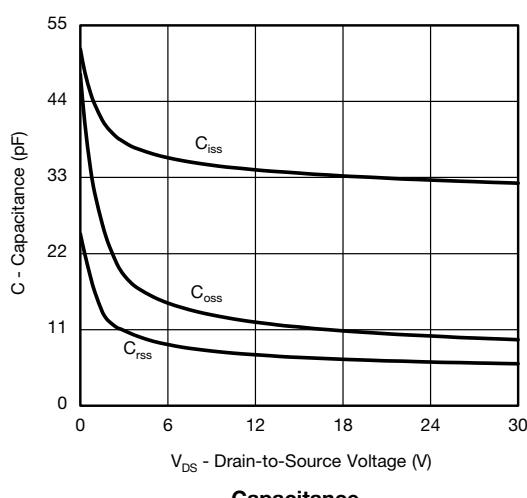
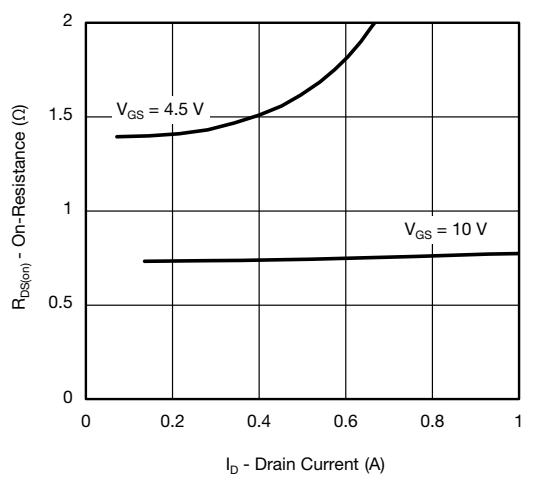
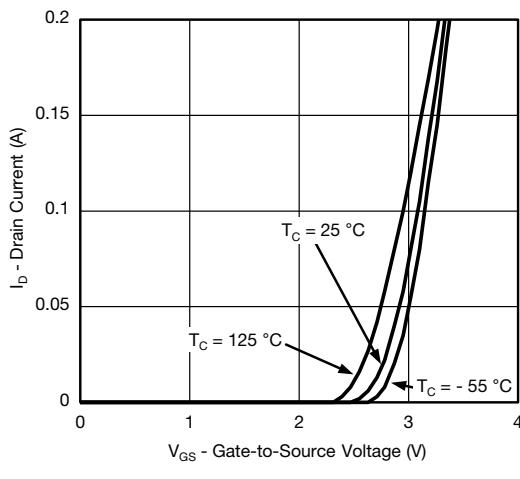
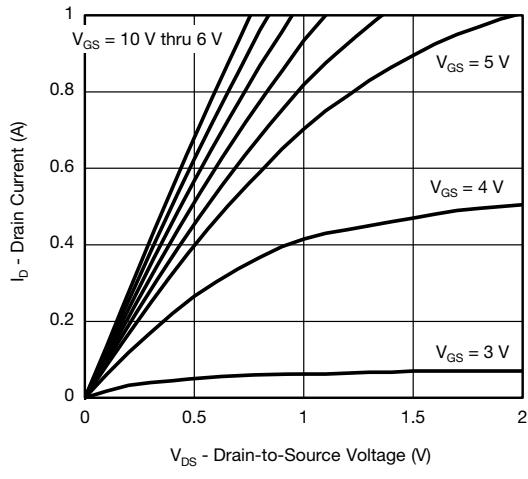
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


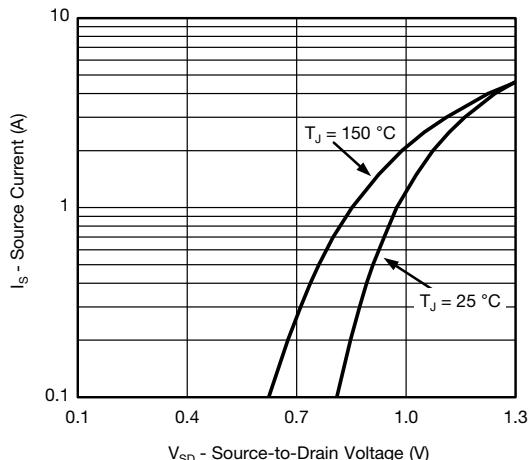
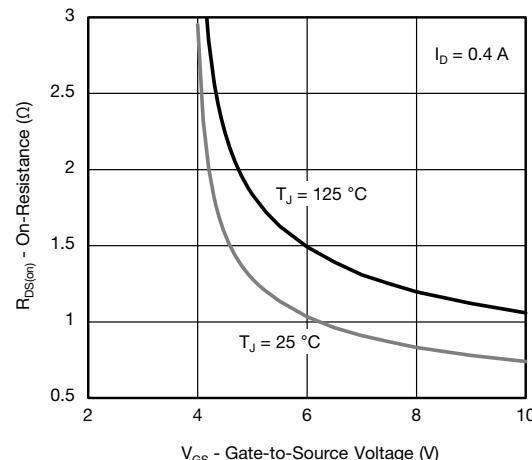
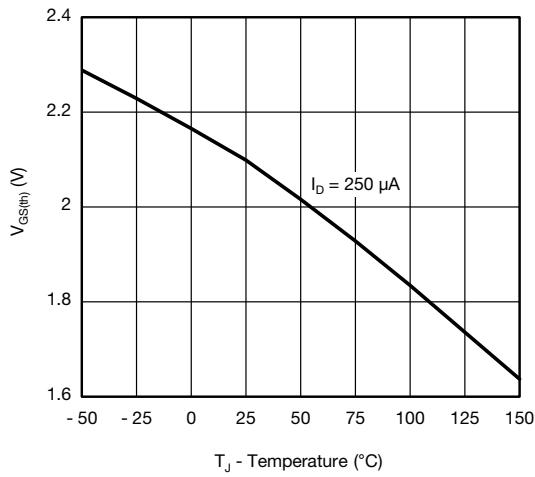
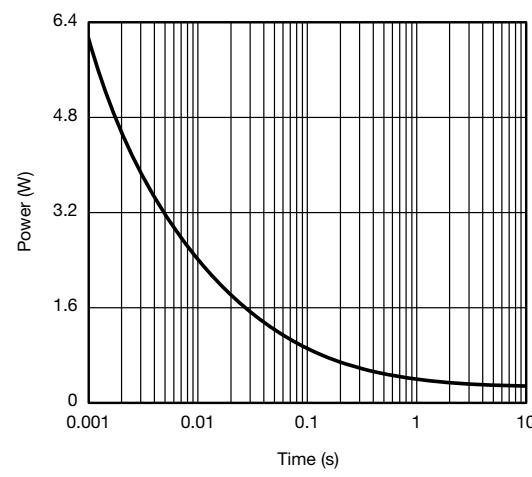
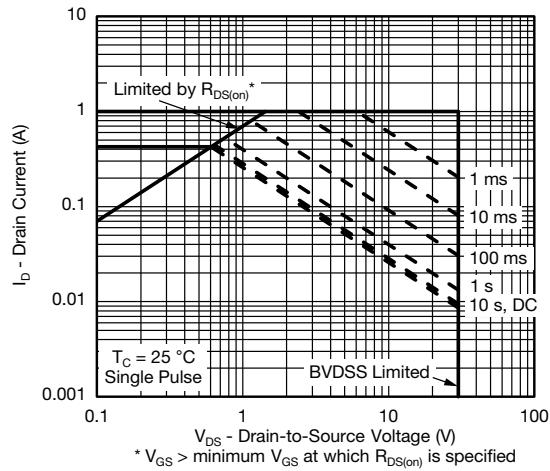
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


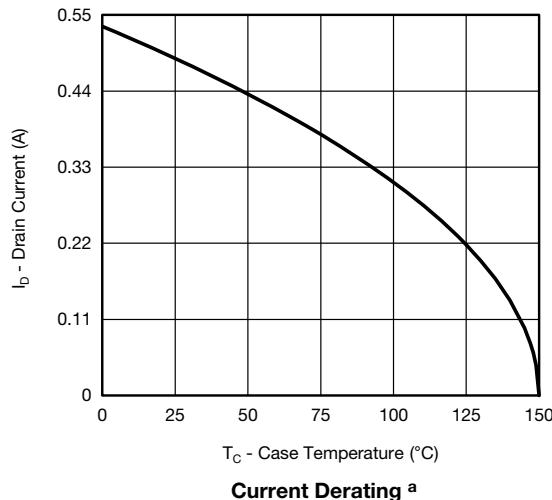
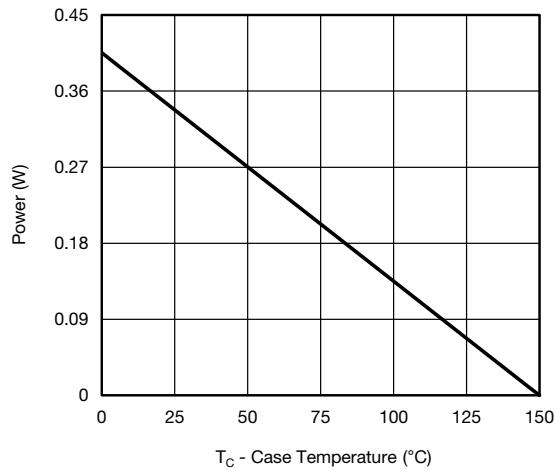
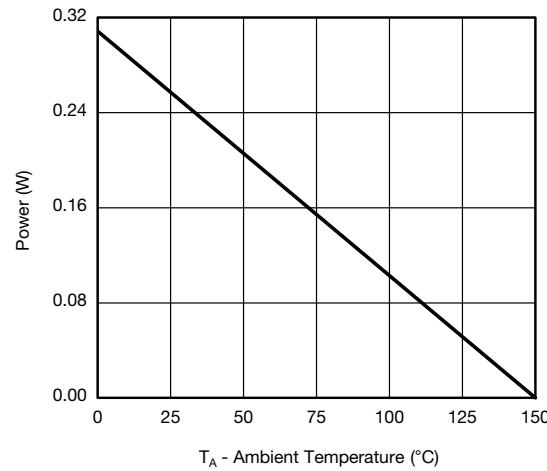
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power Derating, Junction-to-Foot

Power Derating, Junction-to-Ambient
Note

- a. The power dissipation P_D is based on T_J max.= 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

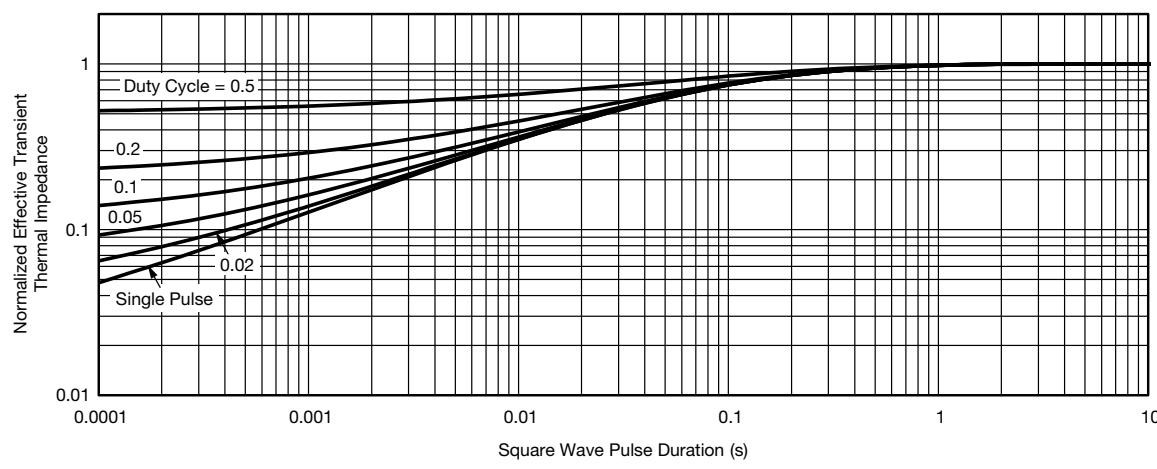
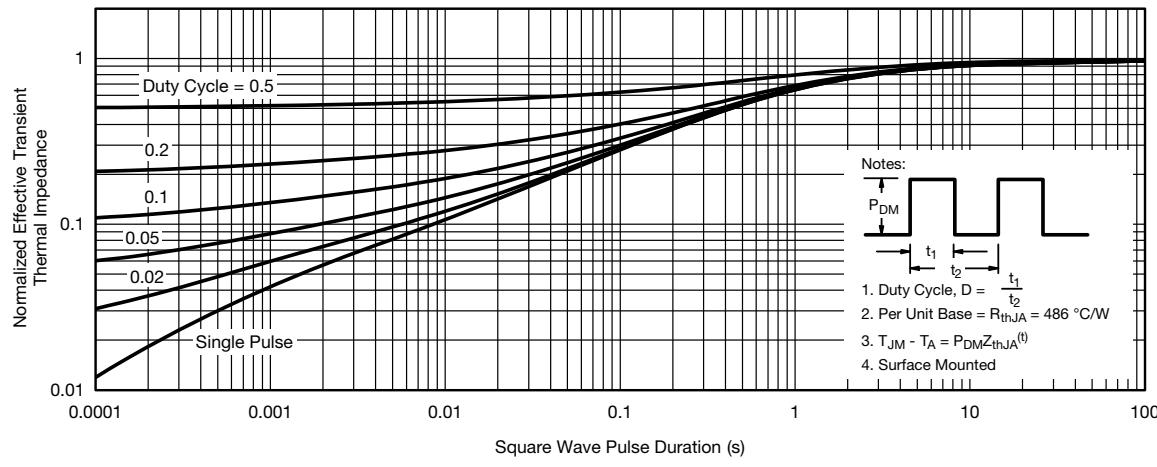
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P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


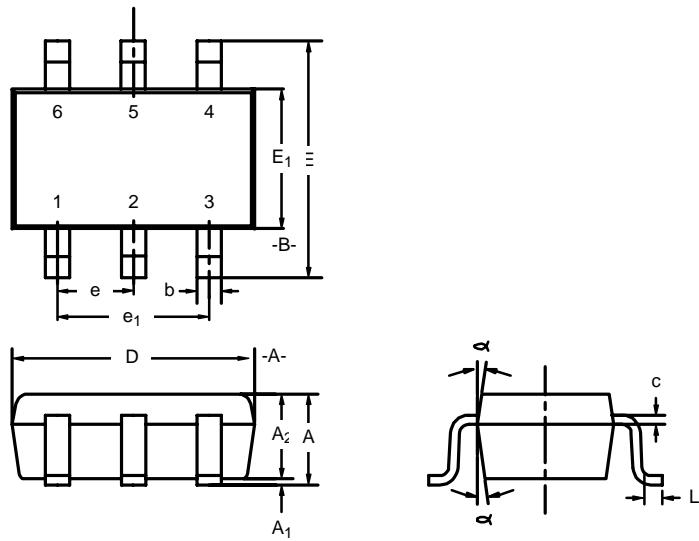
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power, Junction-to-Ambient

Safe Operating Area, Junction-to-Ambient

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power Derating, Junction-to-Foot

Power Derating, Junction-to-Ambient
Note

- a. The power dissipation P_D is based on T_J max.= 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67469.

SC-70: 6-LEADS


Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	—	1.10	0.035	—	0.043
A₁	—	—	0.10	—	—	0.004
A₂	0.80	—	1.00	0.031	—	0.039
b	0.15	—	0.30	0.006	—	0.012
c	0.10	—	0.25	0.004	—	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E₁	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e₁	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5550

Dual-Channel LITTLE FOOT® SC-70 6-Pin MOSFET Recommended Pad Pattern and Thermal Performance

INTRODUCTION

This technical note discusses the pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for dual-channel LITTLE FOOT power MOSFETs in the SC-70 package. These new Vishay Siliconix devices are intended for small-signal applications where a miniaturized package is needed and low levels of current (around 250 mA) need to be switched, either directly or by using a level shift configuration. Vishay provides these devices with a range of on-resistance specifications in 6-pin versions. The new 6-pin SC-70 package enables improved on-resistance values and enhanced thermal performance.

PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the dual-channel SC-70 device in the 6-pin configuration.

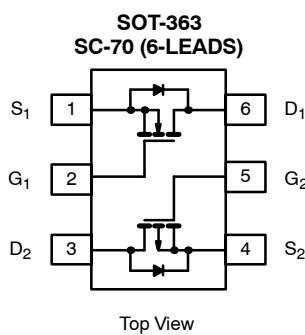


FIGURE 1.

For package dimensions see outline drawing SC-70 (6-Leads) (<http://www.vishay.com/doc?71154>)

BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (<http://www.vishay.com/doc?72286>) for the 6-pin SC-70. This basic pad pattern is sufficient for the low-power

applications for which this package is intended. For the 6-pin device, increasing the pad patterns yields a reduction in thermal resistance on the order of 20% when using a 1-inch square with full copper on both sides of the printed circuit board (PCB).

EVALUATION BOARDS FOR THE DUAL SC70-6

The 6-pin SC-70 evaluation board (EVB) measures 0.6 inches by 0.5 inches. The copper pad traces are the same as described in the previous section, *Basic Pad Patterns*. The board allows interrogation from the outer pins to 6-pin DIP connections permitting test sockets to be used in evaluation testing.

The thermal performance of the dual SC-70 has been measured on the EVB with the results shown below. The minimum recommended footprint on the evaluation board was compared with the industry standard 1-inch square FR4 PCB with copper on both sides of the board.

THERMAL PERFORMANCE

Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the dual SC-70 6-pin package measured as junction-to-foot thermal resistance is 300°C/W typical, 350°C/W maximum. The “foot” is the drain lead of the device as it connects with the body. Note that these numbers are somewhat higher than other LITTLE FOOT devices due to the limited thermal performance of the Alloy 42 lead-frame compared with a standard copper lead-frame.

Junction-to-Ambient Thermal Resistance (dependent on PCB size)

The typical $R_{\theta JA}$ for the dual 6-pin SC-70 is 400°C/W steady state. Maximum ratings are 460°C/W for the dual. All figures based on the 1-inch square FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the dual 6-pin SC-70 package at two different ambient temperatures.

SC-70 (6-PIN)

Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$
$P_D = \frac{150°C - 25°C}{400°C/W}$	$P_D = \frac{150°C - 60°C}{400°C/W}$
$P_D = 312\text{ mW}$	$P_D = 225\text{ mW}$

NOTE: Although they are intended for low-power applications, devices in the 6-pin SC-70 will handle power dissipation in excess of 0.2 W.

Testing

To aid comparison further, Figure 2 illustrates the dual-channel SC-70 thermal performance on two different board sizes and two different pad patterns. The results display the thermal performance out to steady state. The measured steady state values of $R\theta_{JA}$ for the dual 6-pin SC-70 are as follows:

LITTLE FOOT SC-70 (6-PIN)	
1) Minimum recommended pad pattern (see Figure 2) on the EVB of 0.5 inches x 0.6 inches.	518°C/W
2) Industry standard 1" square PCB with maximum copper both sides.	413°C/W

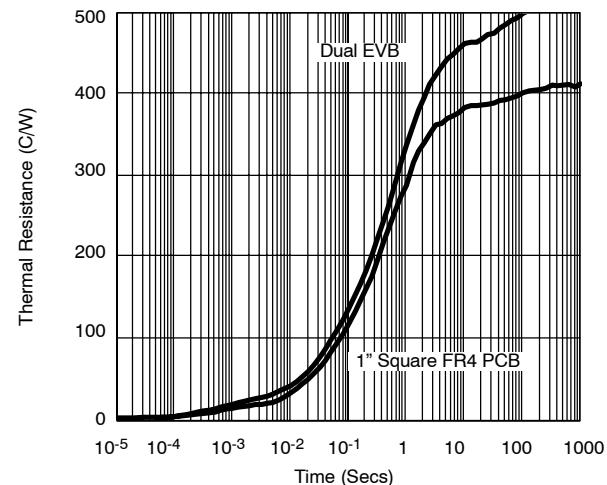


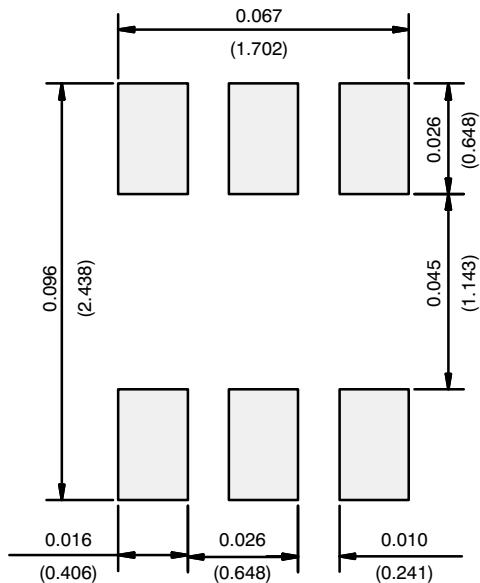
FIGURE 2. Comparison of Dual SC70-6 on EVB and 1" Square FR4 PCB.

The results show that if the board area can be increased and maximum copper traces are added, the thermal resistance reduction is limited to 20%. This fact confirms that the power dissipation is restricted with the package size and the Alloy 42 leadframe.

ASSOCIATED DOCUMENT

Single-Channel LITTLE FOOT SC-70 6-Pin MOSFET Copper Leadframe Version, REcommended Pad Pattern and Thermal Performance, AN815, (<http://www.vishay.com/doc?71334>).

RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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