

# ISOM811x Single-Channel Opto-Emulator With Analog Transistor Output

## 1 Features

- Footprint compatible, pin-to-pin upgrade to industry-standard phototransistor optocouplers
- 1-channel LED-emulator input
- Current transfer ratio (CTR) at  $I_F = 5\text{mA}$ ,  $V_{CE} = 5\text{V}$ :
  - ISOM8110, ISOM8115: 100% to 155%
  - ISOM8111, ISOM8116: 150% to 230%
  - ISOM8112, ISOM8117: 255% to 380%
  - ISOM8113, ISOM8118: 375% to 560%
- High collector-emitter voltage:  $V_{CE} (\text{max}) = 80\text{V}$
- Robust  $\text{SiO}_2$  isolation barrier
  - Isolation rating: Up to  $5000\text{VRMS}$
  - Working voltage: Up to  $750\text{VRMS}$ ,  $1061\text{V}_{\text{PK}}$
  - Surge capability: Up to  $10\text{kV}_{\text{PK}}$
- Temperature range:  $-55^\circ\text{C}$  to  $125^\circ\text{C}$
- Response time:  $3\mu\text{s}$  (typical) at  $V_{CE} = 10\text{V}$ ,  $I_C = 2\text{mA}$ ,  $R_L = 100\Omega$
- **Safety Related Certifications** (Planned)
  - UL 1577 recognition,  $3750\text{VRMS}$  and  $5000\text{VRMS}$  isolation
  - IEC 62368-1, IEC 61010-1 certifications

## 2 Applications

- **Switching power supply**
- **Programmable Logic Controller (PLC)**
- **Factory automation & control**
- **Data acquisition**
- **Motor drive I/O and position feedback**

## 3 Description

The ISOM811x devices are single-channel optocoupler-emulators with LED-emulator input and transistor output. The devices are footprint compatible and pin-to-pin upgrades for many traditional optocouplers, allowing enhancement to existing systems with no PCB redesign.

ISOM811x opto-emulators offer significant reliability and performance advantages compared to optocouplers, including high bandwidth, low turn-off delay, low power consumption, wider temperature ranges, flat CTR, and tight process controls resulting in small part-to-part skew. Since there is no aging effect or temperature variation to compensate for, the emulated LED input stage consumes less power than optocouplers.

ISOM811x devices are offered in small SOIC-4 packages with 2.54mm and 1.27mm pin pitches, supporting  $3750\text{VRMS}$  and  $5000\text{VRMS}$  isolation ratings with DC (ISOM811[0-3]) and bidirectional DC (ISOM811[5-8]) input options. The high performance and reliability of ISOM811x enables these devices to be used in power supply feedback design, motor drives, I/O modules in industrial controllers, factory automation applications, and more.

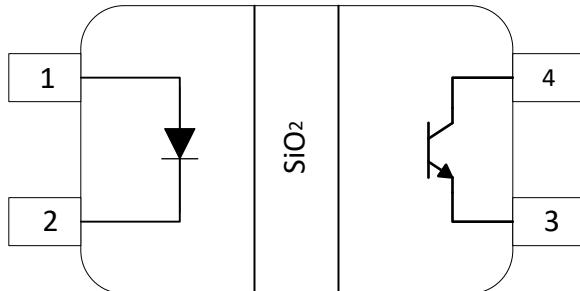
### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE (NOM)
ISOM811x	SO-4 (DFG)	7.0mm × 3.5mm	4.8mm × 3.5mm
	SO-4 (DFH)	7.0mm × 2.7mm	4.8mm × 2.7mm
	SO-4 (DFS)	10.0mm × 3.6mm	7.5mm × 3.6mm

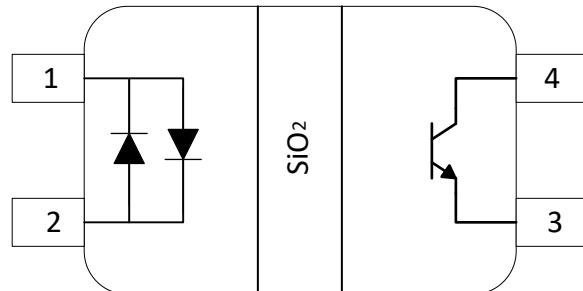
(1) For more information, see [Section 12](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

ISOM811(0-3)



ISOM811(5-8)



Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Device Comparison

Table 4-1. Device Selection

PART NUMBER	CTR ( $I_F = 5\text{mA}$ )	PACKAGE	PIN PITCH
ISOM8110, ISOM8115	100% to 155%	4-pin SOIC (DFG), 4-pin SOIC (DFH), 4-pin SOIC (DFS)	2.54mm, 1.27mm, 2.54mm
ISOM8111, ISOM8116	150% to 230%		
ISOM8112, ISOM8117	255% to 380%		
ISOM8113, ISOM8118	375% to 560%		

## 5 Pin Configuration and Functions

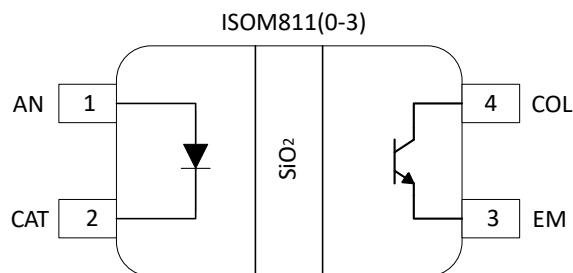


Figure 5-1. ISOM811[0-3] 4-Pin SOIC (Top View)

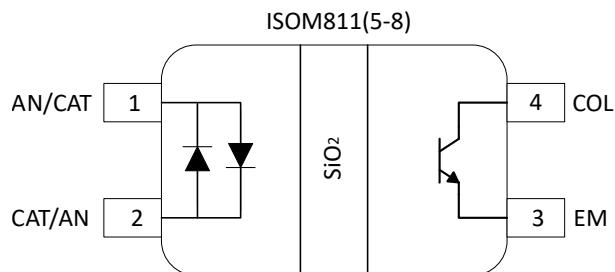


Figure 5-2. ISOM811[5-8] 4-Pin SOIC (Top View)

Table 5-1. Pin Functions

NO.	PIN NAME	TYPE <sup>(1)</sup>	DESCRIPTION
	TYPE <sup>(1)</sup>		
1	AN	I	Anode connection of input LED emulator
2	CAT	I	Cathode connection of input LED emulator
3	EM	O	Emitter for transistor
4	COL	O	Collector for transistor

(1) I = Input, O = Output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

See<sup>(1)</sup> <sup>(2)</sup>

		MIN	MAX	UNIT
I <sub>F(max)</sub>	Maximum Input forward current		50	mA
V <sub>CEO</sub>	Collector-emitter voltage		80	V
V <sub>ECO</sub>	Emitter-collector voltage		7	V
I <sub>FP</sub>	Input pulse forward current (1μs width)		1	A
V <sub>R</sub>	Input reverse voltage at I <sub>R</sub> = 10μA <sup>(3)</sup>		7	V
P <sub>I</sub>	Input power dissipation		140	mW
I <sub>C</sub>	Collector current		50	mA
P <sub>C</sub>	Collector power dissipation		150	mW
P <sub>T</sub>	Total power dissipation		290	mW
T <sub>A</sub>	Ambient temperature	-55	125	°C
T <sub>J</sub>	Operating junction temperature		150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under the operational sections of this document. If used outside the listed operational conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All specifications are at T<sub>A</sub> = 25°C unless otherwise noted
- (3) Only applies to ISOM8110, ISOM8112, and ISOM8113

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ISOM811x			UNIT
		DFS (SOIC)	DFG (SOIC)	DFH (SOIC)	
		4 PINS	4 PINS	4 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	269.1	283.9	288.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	156.7	173.1	173.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	194.2	201.4	192.9	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	128.4	125.1	121.5	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	191.0	198.0	190.0	°C/W

- (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#) application note.

## 6.4 Insulation Specifications

PARAMETER	TEST CONDITIONS	VALUE		UNIT
		4-DFG, 4-DFH	4-DFS	
<b>IEC 60664-1</b>				
CLR	External clearance <sup>(1)</sup>	Side 1 to side 2 distance through air	> 5	> 8 mm
CPG	External creepage <sup>(1)</sup>	Side 1 to side 2 distance across package surface	> 5	> 8 mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	>17 $\mu\text{m}$
CTI	Comparative tracking index	IEC 60112; UL 746A	>400	>400 V
	Material Group	According to IEC 60664-1	II	II
	Overvoltage category per IEC 60664-1	Rated mains voltage $\leq 150\text{V}_{\text{RMS}}$	I-IV	I-IV
		Rated mains voltage $\leq 300\text{V}_{\text{RMS}}$	I-IV	I-IV
		Rated mains voltage $\leq 600\text{V}_{\text{RMS}}$	I-III	I-IV
<b>DIN VDE V 0884-11:2017</b> <sup>(6)</sup>				
$V_{\text{IORM}}$	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	707	1061 $\text{V}_{\text{PK}}$
$V_{\text{IOWM}}$	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test	500	750 $\text{V}_{\text{RMS}}$
		DC voltage	707	1061 $\text{V}_{\text{DC}}$
$V_{\text{IOTM}}$	Maximum transient isolation voltage	$V_{\text{TEST}} = V_{\text{IOTM}}$ , $t = 60\text{s}$ (qualification); $V_{\text{TEST}} = 1.2 \times V_{\text{IOTM}}$ , $t = 1\text{s}$ (100% production)	5303	7071 $\text{V}_{\text{PK}}$
$V_{\text{IMP}}$	Maximum impulse voltage <sup>(2)</sup>	Tested in air, 1.2/50 $\mu\text{s}$ waveform per IEC 62368-1	7200	8000 $\text{V}_{\text{PK}}$
$V_{\text{IOSM}}$	Maximum surge isolation voltage <sup>(3)</sup>	$V_{\text{ISOM}} \geq 1.3 \times V_{\text{IMP}}$ ; tested in oil (qualification test), 1.2/50 $\mu\text{s}$ waveform per IEC 62368-1	10000	10400 $\text{V}_{\text{PK}}$
$q_{\text{pd}}$	Apparent charge <sup>(4)</sup>	Method a: After I/O safety test subgroup 2/3, $V_{\text{ini}} = V_{\text{IOTM}}$ , $t_{\text{ini}} = 60\text{s}$ ; $V_{\text{pd(m)}} = 1.2 \times V_{\text{IORM}}$ , $t_{\text{m}} = 10\text{s}$	$\leq 5$	$\leq 5$
		Method a: After environmental tests subgroup 1, $V_{\text{ini}} = V_{\text{IOTM}}$ , $t_{\text{ini}} = 60\text{s}$ ; $V_{\text{pd(m)}} = 1.6 \times V_{\text{IORM}}$ , $t_{\text{m}} = 10\text{s}$	$\leq 5$	$\leq 5$
		Method b: At routine test (100% production) and preconditioning (type test), $V_{\text{ini}} = 1.2 \times V_{\text{IOTM}}$ , $t_{\text{ini}} = 1\text{s}$ ; $V_{\text{pd(m)}} = 1.875 \times V_{\text{IORM}}$ , $t_{\text{m}} = 1\text{s}$	$\leq 5$	$\leq 5$
$C_{\text{IO}}$	Barrier capacitance, input to output <sup>(5)</sup>	$V_{\text{IO}} = 0.4 \times \sin(2\pi ft)$ , $f = 1\text{MHz}$	1	1 pF
$R_{\text{IO}}$	Insulation resistance, input to output <sup>(5)</sup>	$V_{\text{IO}} = 500\text{V}$ , $T_A = 25^\circ\text{C}$	$> 10^{12}$	$> 10^{12}$ $\Omega$
		$V_{\text{IO}} = 500\text{V}$ , $100^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	$> 10^{11}$	$> 10^{11}$ $\Omega$
		$V_{\text{IO}} = 500\text{V}$ at $T_S = 150^\circ\text{C}$	$> 10^9$	$> 10^9$ $\Omega$
	Pollution degree		2	2
	Climatic category		40/125/2 1	40/125/2 1
<b>UL 1577</b>				
$V_{\text{ISO}}$	Withstand isolation voltage	$V_{\text{TEST}} = V_{\text{ISO}}$ , $t = 60\text{s}$ (qualification); $V_{\text{TEST}} = 1.2 \times V_{\text{ISO}}$ , $t = 1\text{s}$ (100% production)	3750	5000 $\text{V}_{\text{RMS}}$

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
- (2) Testing is carried out in air to determine the surge immunity of the package.
- (3) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-pin device.

- (6) This coupler is suitable for *safe electrical insulation only* within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

## 6.5 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to IEC 61010-1, IEC 62368-1 and IEC 60601-1	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB4943.1-2011	Plan to certify according to EN 61010-1:2010/A1:2019 and EN 62368-1:2014
Certificate planned	Certificate planned	Certificate planned	Certificate planned	Certificate planned

## 6.6 Safety Limiting Values

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SO-4 PACKAGE (DFG)</b>						
Is	Safety limiting input current	R <sub>θJA</sub> = 283.9°C/W, V <sub>F</sub> = 1.4V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		300		mA
		R <sub>θJA</sub> =283.9°C/W, V <sub>CEO</sub> = 40V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		10.5		mA
		R <sub>θJA</sub> = 283.9°C/W, V <sub>CEO</sub> = 24V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		17.5		mA
		R <sub>θJA</sub> = 283.9°C/W, V <sub>CEO</sub> = 15V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		28		mA
P <sub>S</sub>	Safety limiting total power	R <sub>θJA</sub> = 283.9°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		420		mW
T <sub>S</sub>	Maximum safety temperature			150		°C
<b>SO-4 PACKAGE (DFH)</b>						
Is	Safety limiting input current	R <sub>θJA</sub> = 288.8°C/W, V <sub>F</sub> = 1.4V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		300		mA
Is	Safety limiting input current	R <sub>θJA</sub> =288.8°C/W, V <sub>CEO</sub> = 40V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		10.5		mA
Is	Safety limiting input current	R <sub>θJA</sub> = 288.8°C/W, V <sub>CEO</sub> = 24V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		17.5		mA
Is	Safety limiting input current	R <sub>θJA</sub> = 288.8°C/W, V <sub>CEO</sub> = 15V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		28		mA
P <sub>S</sub>	Safety limiting total power	R <sub>θJA</sub> = 288.8°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		420		mW
T <sub>S</sub>	Maximum safety temperature			150		°C
<b>SO-4 PACKAGE (DFS)</b>						
Is	Safety limiting input current	R <sub>θJA</sub> = 269.1°C/W, V <sub>F</sub> = 1.4V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		320		mA
Is	Safety limiting input current	R <sub>θJA</sub> = 269.1°C/W, V <sub>CEO</sub> = 40V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		11		mA
Is	Safety limiting input current	R <sub>θJA</sub> = 269.1°C/W, V <sub>CEO</sub> = 24V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		18		mA
Is	Safety limiting input current	R <sub>θJA</sub> = 269.1°C/W, V <sub>CEO</sub> = 15V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		30		mA
P <sub>S</sub>	Safety limiting total power	R <sub>θJA</sub> = 269.1°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		470		mW
T <sub>S</sub>	Maximum safety temperature			150		°C

- (1) The Is and P<sub>S</sub> parameters represent the safety current and safety power respectively. The maximum limits of Is and P<sub>S</sub> must not be exceeded. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance, R<sub>θJA</sub>, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$$T_J = T_A + R_{\theta JA} \times P, \text{ where } P \text{ is the power dissipated in the device.}$$

$$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S, \text{ where } T_{J(max)} \text{ is the maximum allowed junction temperature.}$$

$P_S = I_S \times V_I$ , where  $V_I$  is the maximum input voltage.

## 6.7 Electrical Characteristics

All specifications are at  $T_A = 25^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	GPN	MIN	TYP	MAX	UNIT
<b>INPUT</b>							
$V_F$	Input forward voltage	$I_F = 5\text{mA}$	ISOM8110, ISOM8111, ISOM8112, ISOM8113		1.2	1.4	V
$V_F$	Input forward voltage	$I_F = 5\text{mA}, T_A = -40 \text{ to } 125^\circ\text{C}$	ISOM8110, ISOM8111, ISOM8112, ISOM8113		1.2	1.6	V
$V_F$	Input forward voltage	$I_F = \pm 5\text{mA}$	ISOM8115, ISOM8116, ISOM8117, ISOM8118		1.2	1.5	V
$V_F$	Input forward voltage	$I_F = \pm 5\text{mA}, T_A = -40 \text{ to } 125^\circ\text{C}$	ISOM8115, ISOM8116, ISOM8117, ISOM8118		1.2	1.5	V
$I_{FT}$	Input forward threshold current		ISOM811x		0.5		mA
$I_R$	Input reverse current	$V_R = 5\text{V}, T_A = -40 \text{ to } 125^\circ\text{C}$	ISOM8110, ISOM8111, ISOM8112, ISOM8113		10		$\mu\text{A}$
$C_{IN}$	Input capacitance	At 1MHz, $V_F = 0\text{V}$	ISOM8110, ISOM8111, ISOM8112, ISOM8113		19		pF
$C_{IN}$	Input capacitance	At 1MHz, $V_F = 0\text{V}$	ISOM8115, ISOM8116, ISOM8117, ISOM8118		6		pF
<b>OUTPUT</b>							
$C_{CE}$	Collector-emitter capacitance	1MHz, $V_F = 0\text{V}$	ISOM811x		10		pF
$V_{CE(\text{SAT})}$	Collector-emitter saturation voltage	$I_F = 20\text{mA}, I_C = 1\text{mA}, T_A = -40 \text{ to } 125^\circ\text{C}$	ISOM811x		0.3		V
$I_{C\_DARK}$	Collector dark current	$V_{CE} = 20\text{V}, I_F = 0\text{mA}, T_A = -40 \text{ to } 125^\circ\text{C}$	ISOM811x		100		nA
$I_{EC}$	Reverse current	$V_{EC} = 7\text{V}, I_F = 0\text{mA}$	ISOM811x		10		$\mu\text{A}$
$I_{EC}$	Reverse current	$V_{EC} = 7\text{V}, I_F = 0\text{mA}, T_A = -40 \text{ to } 125^\circ\text{C}$	ISOM811x		50		$\mu\text{A}$
$I_{C\_OFF}$	OFF_state collector current	$V_F = 0.7\text{V}, V_{CE} = 48\text{V}, T_A = -40 \text{ to } 125^\circ\text{C}$	ISOM811x		10		$\mu\text{A}$
<b>CTR<sup>(1)</sup></b>							

## 6.7 Electrical Characteristics (continued)

All specifications are at  $T_A = 25^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	GPN	MIN	TYP	MAX	UNIT
CTR	Current Transfer Ratio	$I_F = 0.5\text{mA}, V_{CE} = 5\text{V}$	ISOM8110	55	130	195	%
			ISOM8115	55	130	195	%
			ISOM8111	80	180	290	%
			ISOM8116	80	180	290	%
			ISOM8112	135	300	480	%
			ISOM8117	135	300	480	%
			ISOM8113	195	440	710	%
			ISOM8118	195	440	710	%
CTR	Current Transfer Ratio	$I_F = 2\text{mA}, V_{CE} = 5\text{V}$	ISOM8110	70	120	170	%
			ISOM8115	70	120	170	%
			ISOM8111	110	180	260	%
			ISOM8116	110	180	260	%
			ISOM8112	185	300	430	%
			ISOM8117	185	300	430	%
			ISOM8113	265	440	635	%
			ISOM8118	265	440	635	%
CTR	Current Transfer Ratio	$I_F = 2\text{mA}, V_{CE} = 5\text{V}, T_A = -40 \text{ to } 125^\circ\text{C}$	ISOM8110	80	130	180	%
			ISOM8115	80	130	180	%
			ISOM8111	120	180	270	%
			ISOM8116	120	180	270	%
			ISOM8112	200	300	450	%
			ISOM8117	200	300	450	%
			ISOM8113	295	440	655	%
			ISOM8118	295	440	655	%
CTR	Current Transfer Ratio	$I_F = 5\text{mA}, V_{CE} = 5\text{V}$	ISOM8110	100	120	155	%
			ISOM8115	100	120	155	%
			ISOM8111	150	180	230	%
			ISOM8116	150	180	230	%
			ISOM8112	255	300	380	%
			ISOM8117	255	300	380	%
			ISOM8113	375	440	560	%
			ISOM8118	375	440	560	%
CTR	Current Transfer Ratio	$I_F = 5\text{mA}, V_{CE} = 5\text{V}, T_A = -40 \text{ to } 125^\circ\text{C}$	ISOM8110	100	120	155	%
			ISOM8115	100	120	155	%
			ISOM8111	150	180	230	%
			ISOM8116	150	180	230	%
			ISOM8112	255	300	380	%
			ISOM8117	255	300	380	%
			ISOM8113	375	440	560	%
			ISOM8118	375	440	560	%

$$(1) \quad \text{CTR (\%)} = (I_C / I_F) \times 100\%$$

## 6.8 Switching Characteristics

All specifications are at  $T_A = 25^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	GPN	MIN	TYP	MAX	UNIT	
<b>AC</b>								
$t_r$	Rise time, see <a href="#">Figure 7-2</a> and <a href="#">Figure 7-3</a>	$V_{CC} = 10\text{V}, I_C = 2\text{mA}, R_L = 100\Omega, C_L = 50\text{pF}$	ISOM8110	3.2			$\mu\text{s}$	
$t_f$	Fall time, see <a href="#">Figure 7-2</a> and <a href="#">Figure 7-3</a>		ISOM8113	2.5			$\mu\text{s}$	
$T_{ON}$	Turn on time, see <a href="#">Figure 7-2</a> and <a href="#">Figure 7-3</a>		ISOM8110, ISOM8115	4.0			$\mu\text{s}$	
			ISOM8113, ISOM8118	7.5			$\mu\text{s}$	
$T_{OFF}$	Turn off time, see <a href="#">Figure 7-2</a> and <a href="#">Figure 7-3</a>		ISOM8110, ISOM8115	5.7			$\mu\text{s}$	
			ISOM8111, ISOM8116	4.5			$\mu\text{s}$	
			ISOM8112, ISOM8117	6.2			$\mu\text{s}$	
			ISOM8113, ISOM8118	16.7			$\mu\text{s}$	
			ISOM8110, ISOM8115	3.6			$\mu\text{s}$	
$T_{ON}$	Turn on time, see <a href="#">Figure 7-2</a> and <a href="#">Figure 7-3</a>	$V_{CC}=5\text{V}, R_L=4.7\text{k}\Omega, I_F=1.6\text{mA}, C_L=50\text{pF}$	ISOM8111, ISOM8116	2.7			$\mu\text{s}$	
			ISOM8112, ISOM8117	2.1			$\mu\text{s}$	
			ISOM8113, ISOM8118	1.8			$\mu\text{s}$	
			ISOM8110, ISOM8115	3.5			$\mu\text{s}$	
$T_{OFF}$	Turn off time, see <a href="#">Figure 7-2</a> and <a href="#">Figure 7-3</a>		ISOM8111, ISOM8116	8			$\mu\text{s}$	
			ISOM8112, ISOM8117	9			$\mu\text{s}$	
			ISOM8113, ISOM8118	11.5			$\mu\text{s}$	
			ISOM8110, ISOM8115	13.5			$\mu\text{s}$	

## 6.8 Switching Characteristics (continued)

All specifications are at  $T_A = 25^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	GPN	MIN	TYP	MAX	UNIT
$T_{ON}$	Turn on time, see <a href="#">Figure 7-2</a> and <a href="#">Figure 7-3</a>	$V_{CC}=5\text{V}$ , $R_L=1.9\text{k}\Omega$ , $I_F=16\text{mA}$ , $C_L=50\text{pF}$	ISOM8110, ISOM8115	0.62			$\mu\text{s}$
			ISOM8111, ISOM8116	0.56			$\mu\text{s}$
			ISOM8112, ISOM8117	0.48			$\mu\text{s}$
			ISOM8113, ISOM8118	0.44			$\mu\text{s}$
$T_{OFF}$	Turn off time, see <a href="#">Figure 7-2</a> and <a href="#">Figure 7-3</a>		ISOM8110, ISOM8115	10			$\mu\text{s}$
			ISOM8111, ISOM8116	11			$\mu\text{s}$
			ISOM8112, ISOM8117	12.3			$\mu\text{s}$
			ISOM8113, ISOM8118	14.5			$\mu\text{s}$
$t_s$	Storage time; time required for the output waveform to change from 0% (100%) to 10% (90%) when input is turned on and back off, see <a href="#">Figure 7-3</a>	$V_{CC} = 5\text{V}$ , $I_F = 1.6\text{mA}$ , $R_L = 4.7\text{k}\Omega$	ISOM811x		21		$\mu\text{s}$
BW	Bandwidth, see <a href="#">Figure 7-4</a> and <a href="#">Figure 7-5</a>	$V_{IN\_DC} = 5\text{V}$ , $V_{IN\_AC} = 1\text{Vpk}$ , $R_{IN} = 2\text{k}\Omega$ $V_{CC} = 5\text{V}$ , $R_{LOAD} = 100\Omega$ , $C_L = 50\text{pF}$ , measured at $V_{CE} -3\text{dB}$ sinewave	ISOM811x	680			kHz

## 6.9 Typical Characteristics

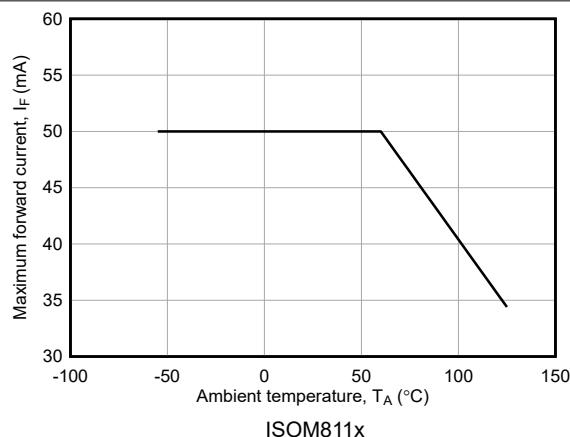


Figure 6-1. Maximum Forward Current vs Ambient Temperature

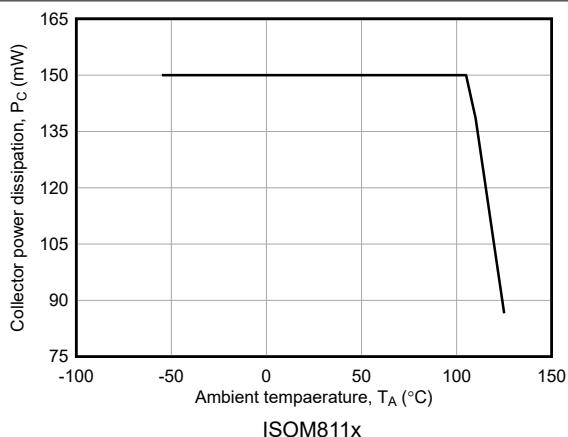


Figure 6-2. Maximum Collector Power Dissipation vs Ambient Temperature

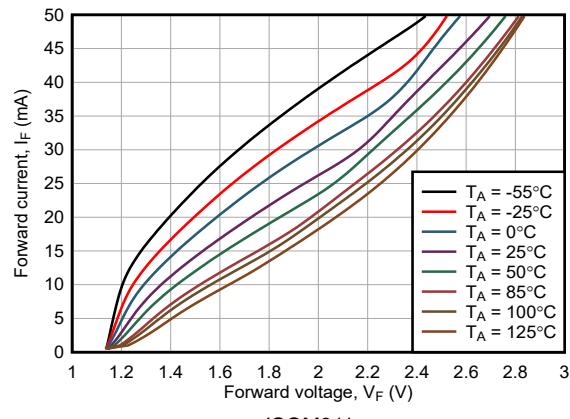


Figure 6-3. Forward Voltage vs Forward Current

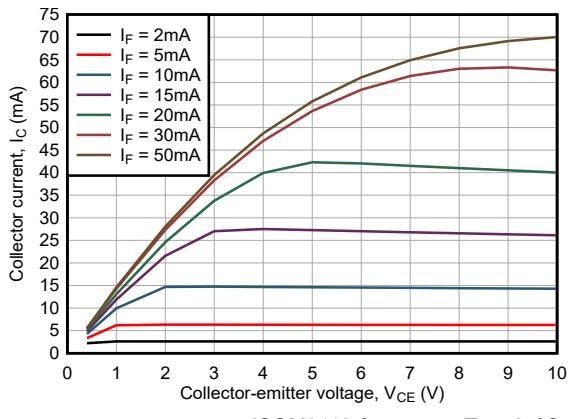


Figure 6-4. Collector Current vs Collector-Emitter Voltage

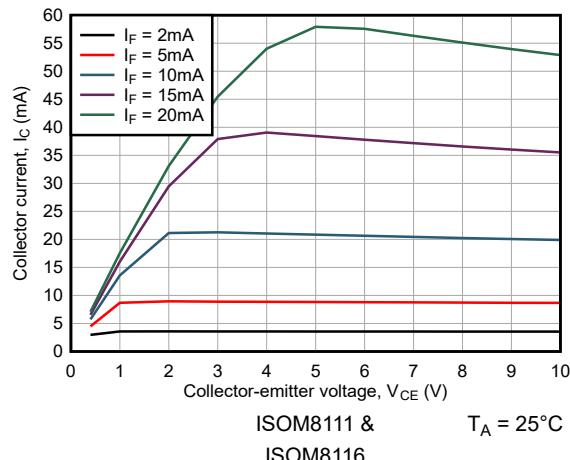


Figure 6-5. Collector Current vs Collector-Emitter Voltage

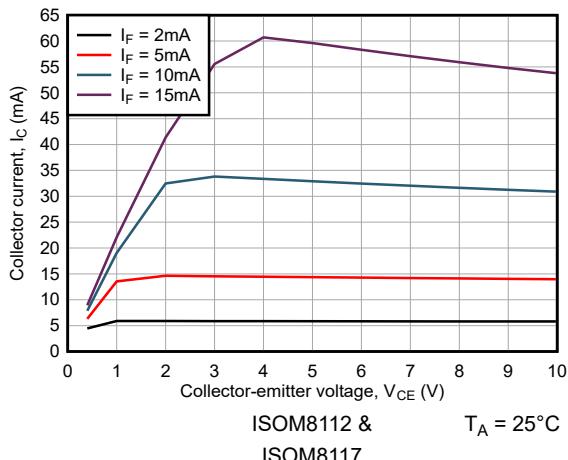
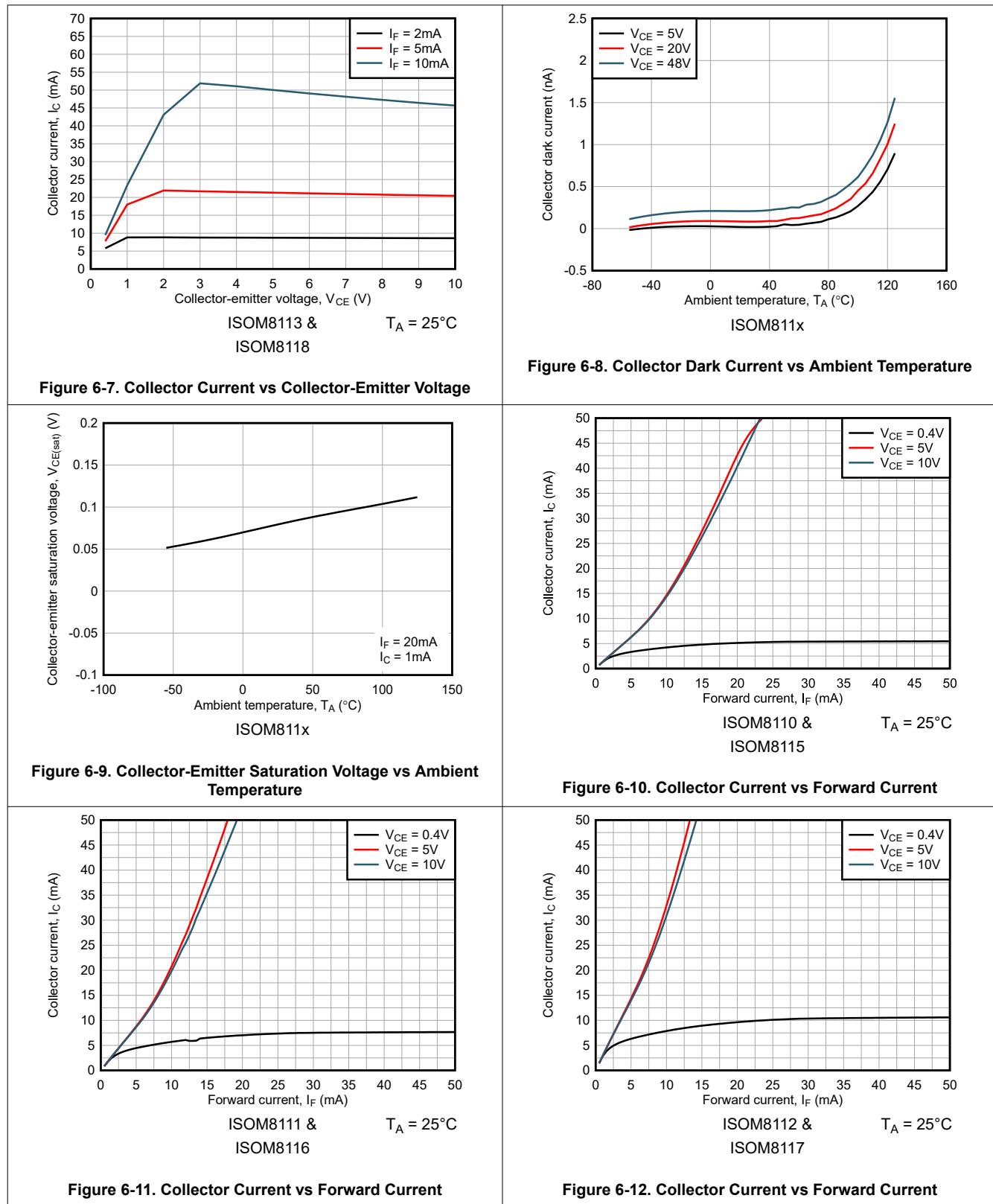
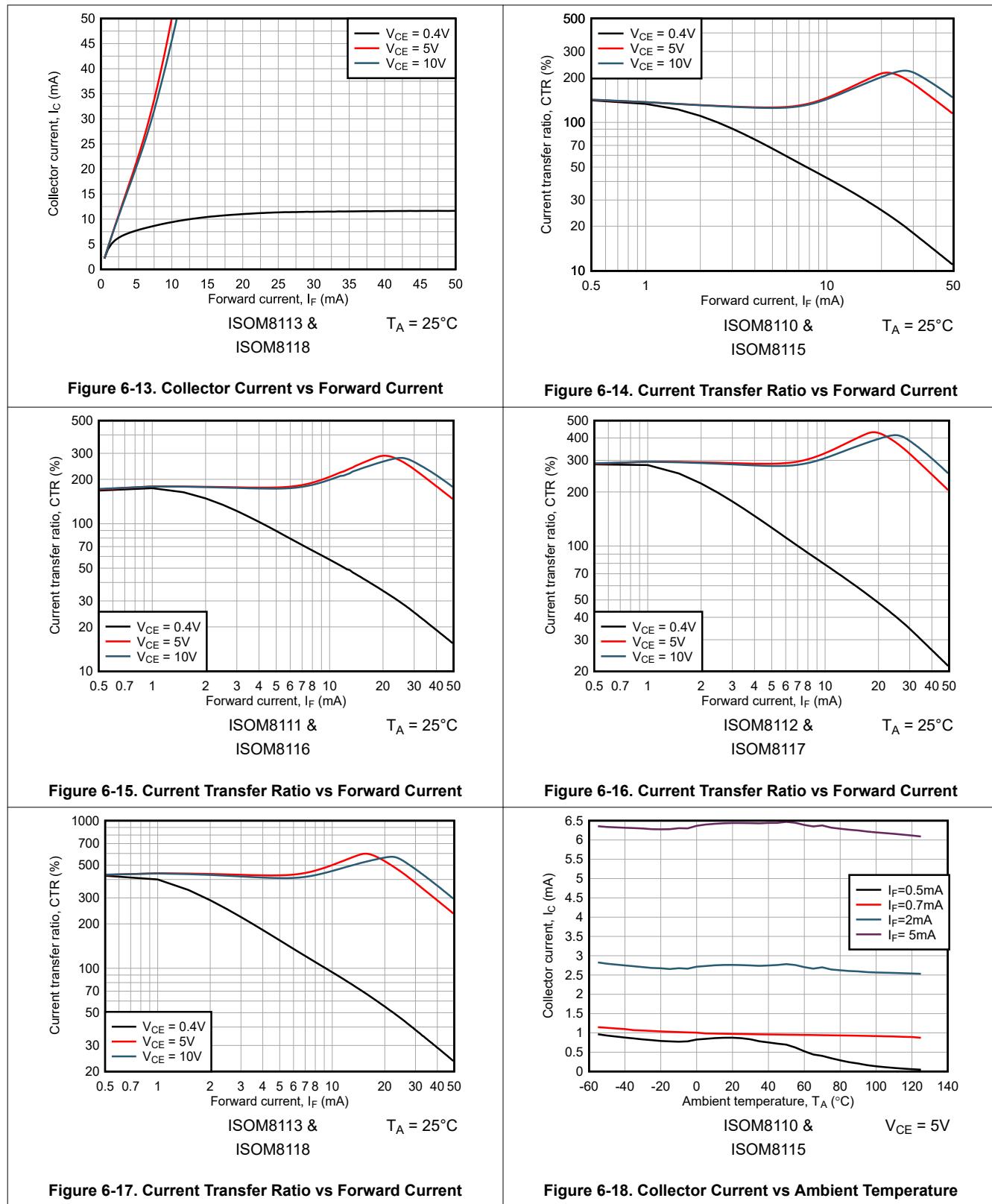


Figure 6-6. Collector Current vs Collector-Emitter Voltage

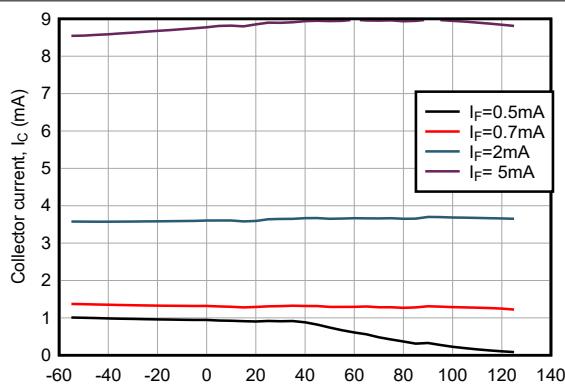
## 6.9 Typical Characteristics (continued)



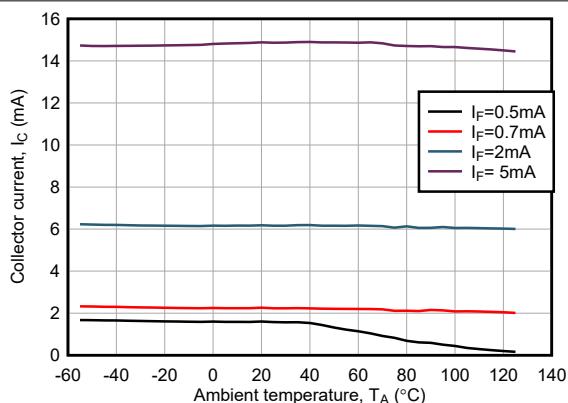
## 6.9 Typical Characteristics (continued)



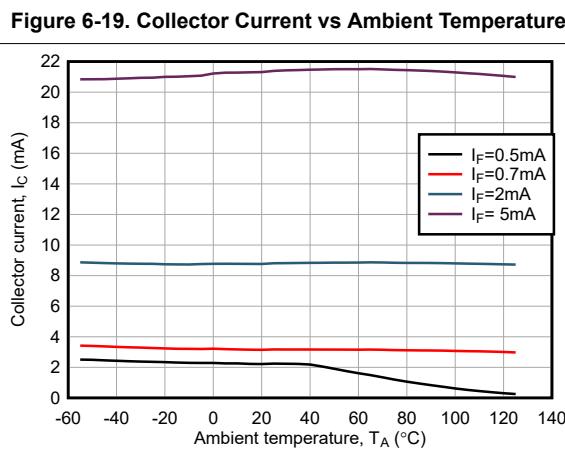
## 6.9 Typical Characteristics (continued)



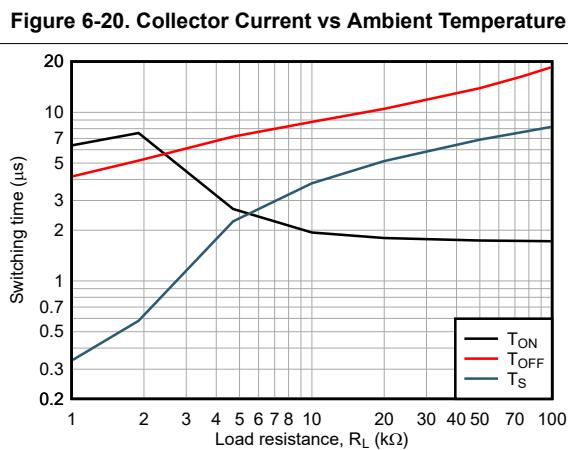
ISOM8111 &  
ISOM8116       $V_{CE} = 5V$



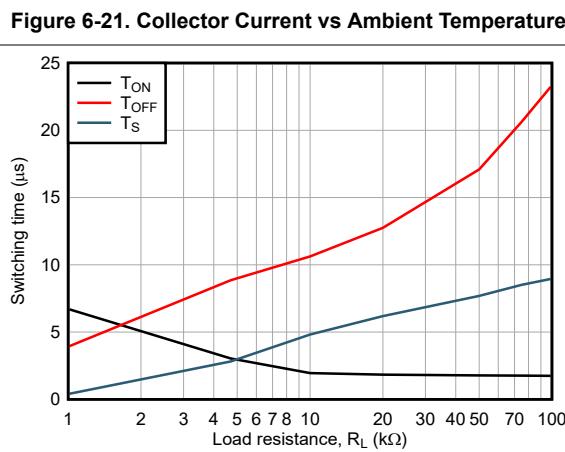
ISOM8112 &  
ISOM8117       $V_{CE} = 5V$



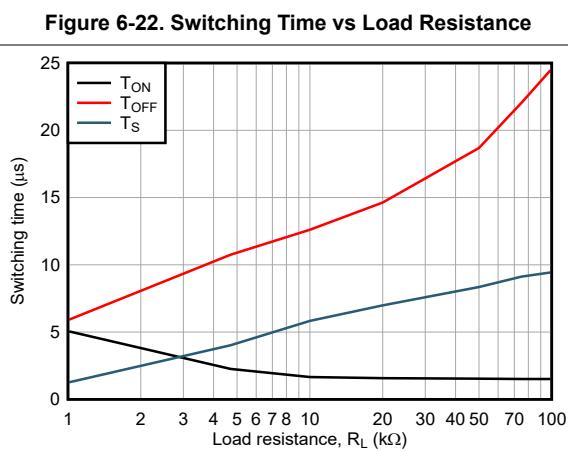
ISOM8113 &  
ISOM8118       $V_{CE} = 5V$



ISOM8110 &  
ISOM8115       $V_{CC} = 5V$



ISOM8111 &  
ISOM8116       $V_{CC} = 5V$



ISOM8112 &  
ISOM8117       $V_{CC} = 5V$

## 6.9 Typical Characteristics (continued)

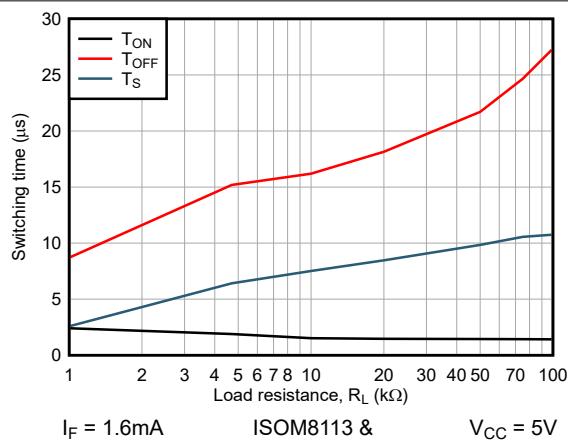


Figure 6-25. Switching Time vs Load Resistance

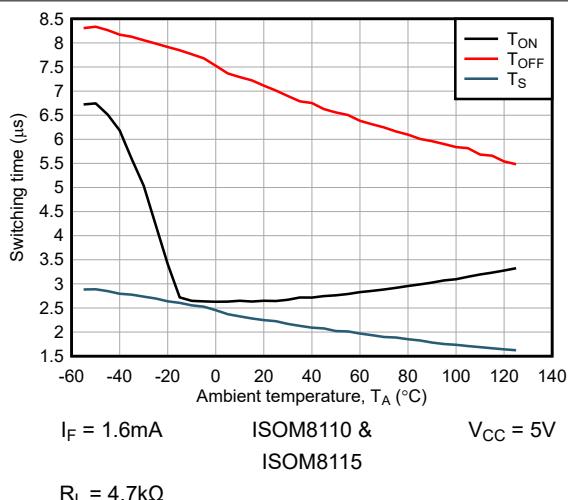


Figure 6-26. Switching Time vs Ambient Temperature

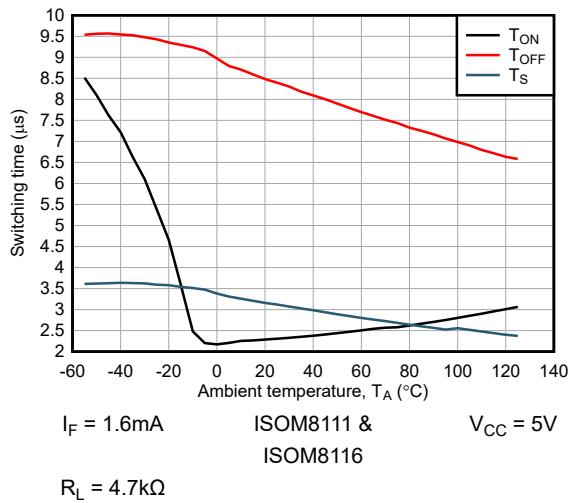


Figure 6-27. Switching Time vs Ambient Temperature

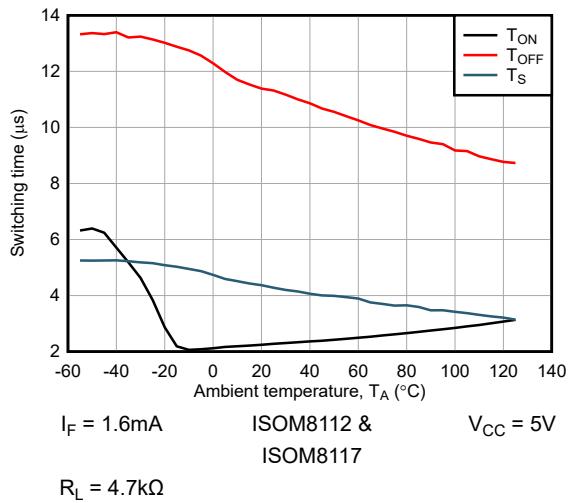


Figure 6-28. Switching Time vs Ambient Temperature

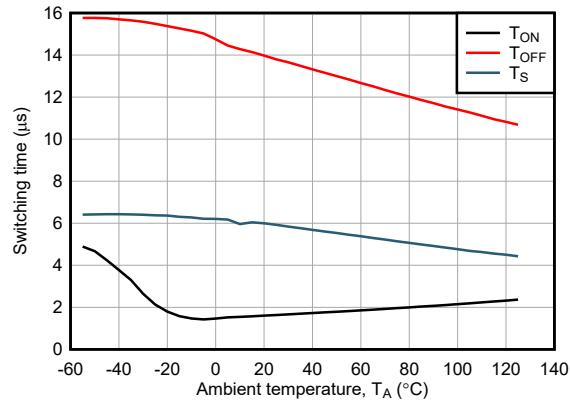


Figure 6-29. Switching Time vs Ambient Temperature

## 7 Parameter Measurement Information

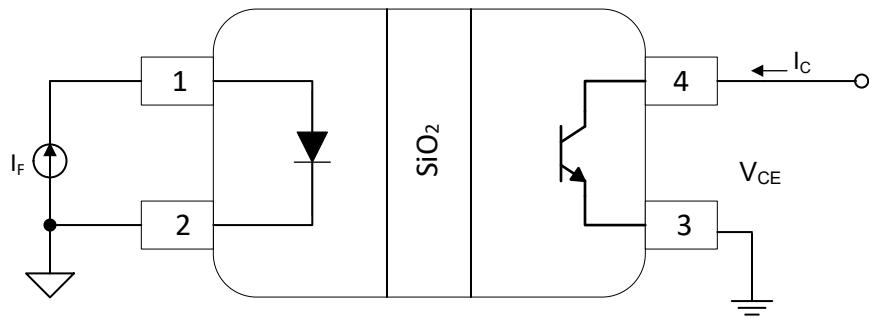


Figure 7-1. ISOM811x Test Circuit for CTR

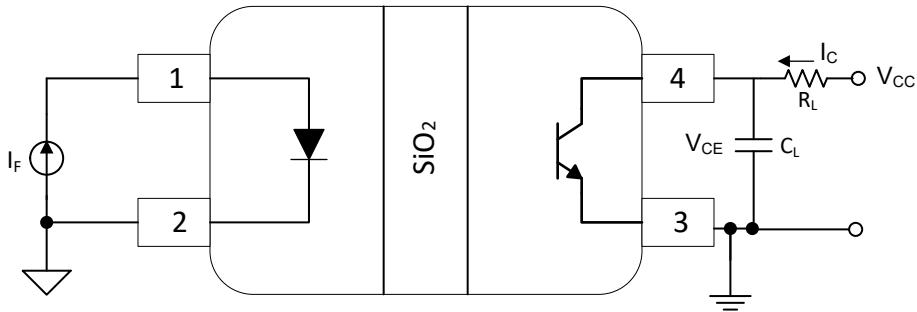


Figure 7-2. ISOM811x Test Circuit for Switching Timing

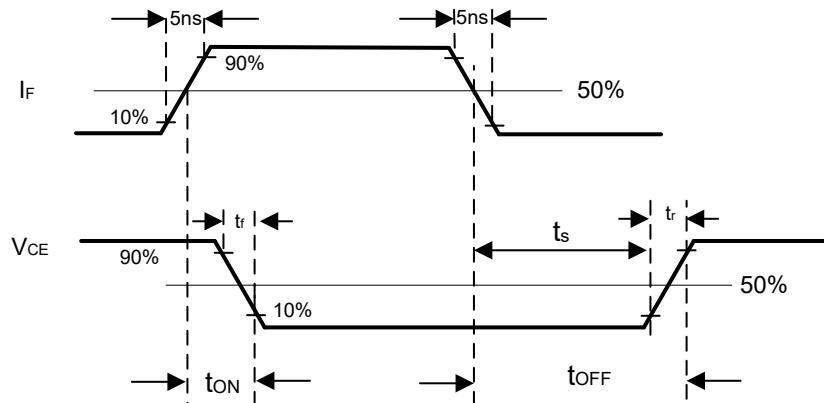


Figure 7-3. ISOM811x Switching Timing Waveforms

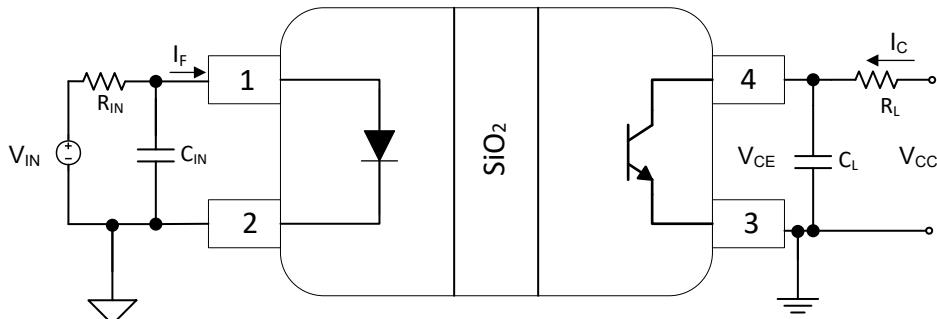


Figure 7-4. ISOM811[0-3] Test Circuit for Bandwidth

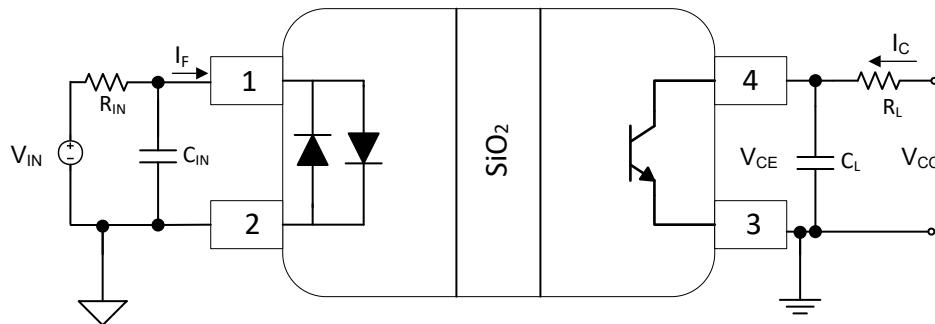


Figure 7-5. ISOM811[5-8] Test Circuit for Bandwidth

## 8 Detailed Description

### 8.1 Overview

The ISOM811x opto-emulators are single-channel, pin-to-pin upgrades for many traditional optocouplers. While standard optocouplers use an LED as the input stage, ISOM811x uses an emulated LED as the input stage. The input and output stages are isolated by TI's proprietary silicon dioxide-based ( $\text{SiO}_2$ ) isolation barrier. This isolation technology makes ISOM811x resistant to the wear-out effects found in optocouplers that degrade performance with increasing temperature, forward current, and device age. Ordering options include four different ranges of current transfer ratio (CTR) and input options supporting uni-polar and bi-polar DC flow.

The ISOM811x family of devices isolate DC and bidirectional DC signals and offer performance, reliability, and flexibility advantages not available with traditional optocouplers.

The functional block diagram of ISOM811x devices are shown in [Section 8.2](#). The input signal is transmitted across the isolation barrier using an on-off keying (OOK) modulation scheme. The transmitter sends a high-frequency carrier across the barrier that contains information on how much current is flowing through the input pins. The receiver demodulates the signal after advanced signal conditioning and produces the signal through the output stage. These devices also incorporate advanced circuit techniques to maximize bandwidth and minimize radiated emissions. [Figure 8-3](#) shows conceptual details of how the OOK scheme works.

### 8.2 Functional Block Diagram

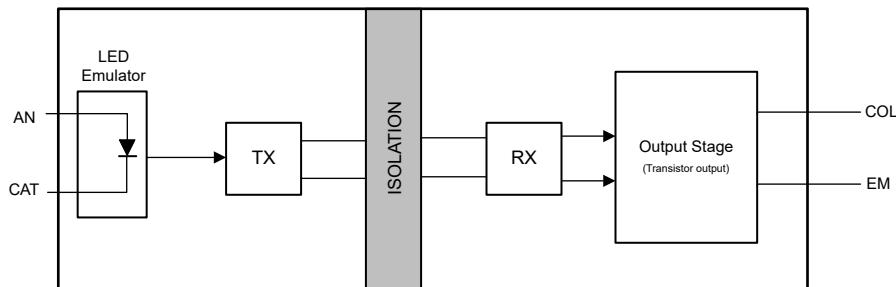


Figure 8-1. Conceptual Block Diagram of an Opto-emulator ISOM811[0-3]

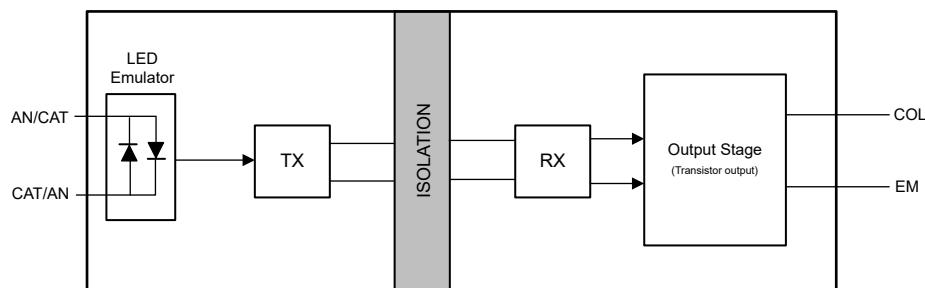
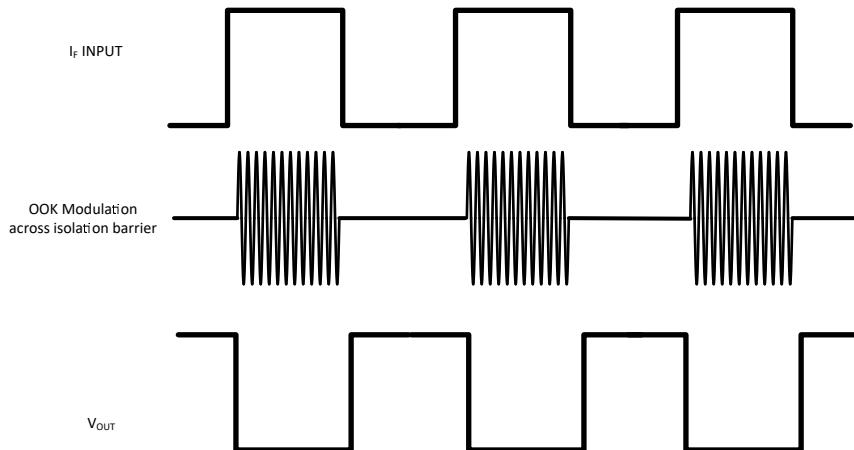


Figure 8-2. Conceptual Block Diagram of an Opto-emulator ISOM811[5-8]



**Figure 8-3. On-off Keying (OOK) Based Modulation Scheme**

### 8.3 Feature Description

The ISOM811x devices isolate DC and bidirectional DC signals. ISOM811x has an open-collector output with multiple CTR options. Depending on the package option being used, these devices can support an isolation withstand voltage ( $V_{ISO}$ ) up to 5000V<sub>RMS</sub> between side 1 and side 2.

### 8.4 Device Functional Modes

Table 8-1 lists the functional modes for the ISOM811x devices.

**Table 8-1. Function Table**

CTR <sup>1</sup>	PART NUMBER	Input type
100% to 155%	ISOM8110	DC
	ISOM8115	Bidirectional DC
150% to 230%	ISOM8111	DC
	ISOM8116	Bidirectional DC
255% to 380%	ISOM8112	DC
	ISOM8117	Bidirectional DC
375% to 560%	ISOM8113	DC
	ISOM8118	Bidirectional DC

1. I<sub>F</sub> = 5mA, T<sub>A</sub> = 25°C, V<sub>CE</sub> = 5V.

## 9 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 9.1 Application Information

The ISOM811x devices are single-channel opto-emulators with LED-emulator input and transistor output. The devices use on-off keying modulation to transmit data across the isolation barrier. The input stage is isolated from the driver stage by TI's proprietary silicon dioxide-based ( $\text{SiO}_2$ ) isolation barrier which provides robust isolation. With wider temperature ratings than traditional optocouplers, ISOM811x opto-emulators can provide reliable signal isolation in harsh environments.

The ISOM811x devices are capable of sinking current when subjected to an external load being connected to the device. Like typical transistor output optocouplers, the output current depends on the input current level ( $I_F$ ) and the current transfer ratio (CTR). With multiple CTR options (100% - 560%), low input current, high bandwidth, low turn-off delay, low power consumption, and wider temperature range, ISOM811x devices are designed for use in a variety of industries such as factory automation, building automation, e-mobility, automotive, avionics, medical, and power delivery.

#### 9.1.1 Typical Application

ISOM811x opto-emulators are commonly used in the feedback control loops of isolated power supplies. These devices are used to solve the problem of feeding back current while isolating the primary and secondary domains to regulate the output voltage.

In power supplies, the output voltage is isolated from main input voltage using a transformer (for example: flyback converter). For analog power supply units, the controller IC is typically on the primary side of the transformer. For closed loop control, measuring the output voltage on the secondary side and feeding the voltage back to the controller on the primary is necessary. The most common method of achieving this design is using an opto-emulator such as ISOM811x, error amplifier (commonly TL431), and a voltage comparator to form a feedback loop across the isolation barrier

**Figure 9-1** illustrates a typical isolated power supply. In this implementation, the output voltage is sensed by an error amplifier using the resistor divider (R1 and R2). Depending on the voltage level that the error amplifier senses, the TL431 can drive the current of the ISOM811x higher or lower which is then compared to a voltage reference. The information is passed across the isolation barrier through ISOM811x to the primary side, where the PWM control circuit modulates the power stage to regulate the output voltage. The TL431 and ISOM811x play an important role for stable feedback and control loop.

The ISOM811x devices enable improvements in transient response, reliability, and stability as compared to commonly used optocoupler as the CTR is stable over wide temperature range providing a small, low-cost, highly reliable, and easy-to-design implementation.

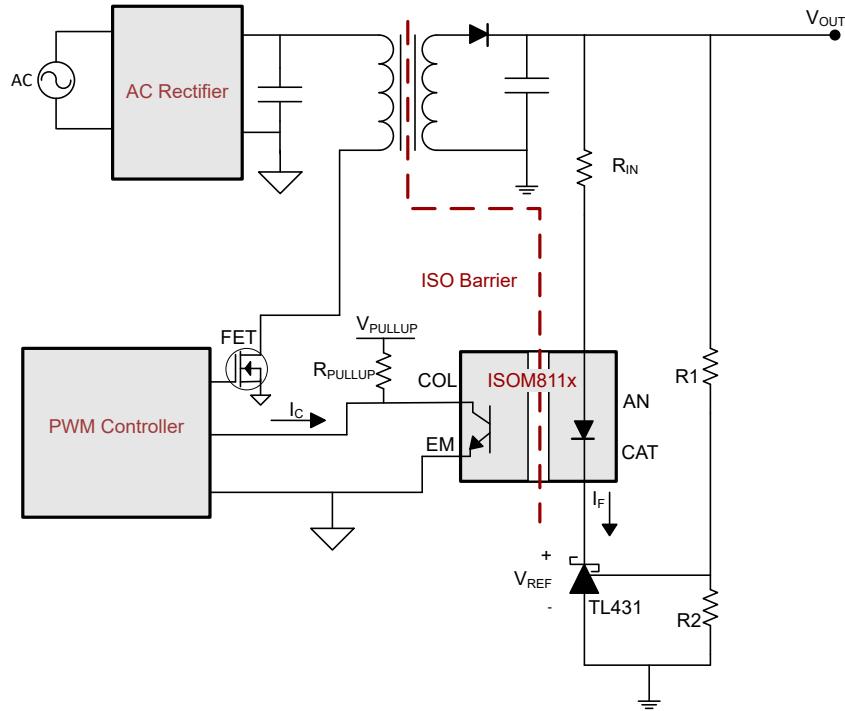


Figure 9-1. Typical Isolated Power Supply Application Using ISOM811x

#### 9.1.1.1 Design Requirements

To design with ISOM811x devices, use the parameters listed in [Table 9-1](#).

Table 9-1. Design Parameters

PARAMETER	VALUE
Input forward current range, $I_F$	0.7mA (min), 20mA (max)
Current transfer ratio at $I_F = 5\text{mA}$ , CTR	100% to 155%
Collector current tolerance, $I_C$	50mA (max)
Collector-emitter voltage (saturation), $V_{CE(SAT)}$	0.3V (max)
Input forward voltage, $V_F$	1.2V (typ)

#### 9.1.1.2 Detailed Design Procedure

This section presents the design procedure for using the ISOM811x opto-emulators. External components must be selected to operate ISOM811x within the *Recommended Operating Conditions*. The following recommendations on component selection focus on the design of a typical feedback control loop for an isolated flyback converter.

When using an optocoupler in a feedback control loop for an isolated power supply, many variables can affect how to properly use the optocoupler, including the output voltage of the power supply and the type of controller the feedback signal is being sent to. For this example, assume that the output voltage of this power supply,  $V_{OUT}$ , is 5V, and the PWM controller being used has an integrated error amplifier with a COMP pin that acts as the output of this amplifier.

##### 9.1.1.2.1 Sizing $R_{PULLUP}$

The transistor output of ISOM811x operates in active, saturation, reverse, and cut-off regions, just like a regular transistor. To verify that the output does not get damaged when the output is saturated, the minimum value of  $R_{PULLUP}$  can be calculated for a given pull-up voltage,  $V_{PULLUP}$ , in [Equation 1](#):

$$R_{PULLUP} > \frac{V_{PULLUP} - V_{CE(SAT)}}{I_C(MAX)} \quad (1)$$

For the example of a feedback loop application, we can calculate the minimum required value for  $R_{PULLUP}$  for a given  $V_{PULLUP}$  of 10V, the maximum output voltage of the error amplifier ( $V_{COMP(MAX)}$ ) of 2.5V, and the maximum output current of the error amplifier is internally clamped at 1.6mA. The equation to calculate  $R_{PULLUP}$  is shown in [Equation 2](#):

$$R_{PULLUP} > \frac{V_{PULLUP} - V_{COMP(MAX)}}{I_{COMP(CLAMP)}} = \frac{10V - 2.5V}{1.6mA} = 4.66k\Omega \quad (2)$$

### 9.1.1.2.2 Sizing $R_{IN}$

The input side of ISOM811x is current-driven. To limit the amount of current flowing into the AN pin, placing a series resistor,  $R_{IN}$ , in series with the input as shown in [Figure 9-1](#) is recommended.

Depending on how the ISOM811x device is being used, the value of  $R_{IN}$  can vary quite a bit. However, at a high level, to make sure the input does not get damaged, the minimum value of  $R_{IN}$  can be calculated for a given input voltage,  $V_{IN}$ , in [Equation 3](#):

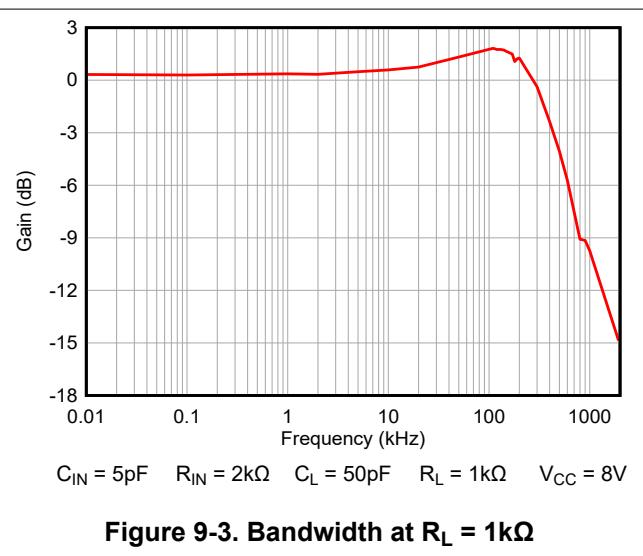
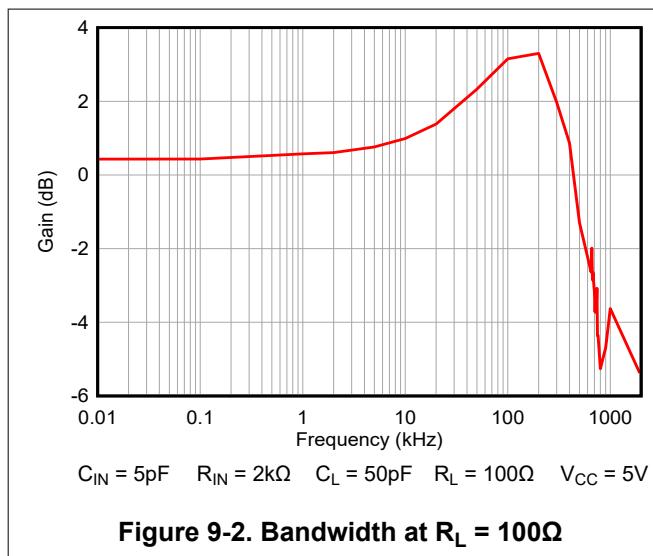
$$R_{IN} > \frac{V_{IN} - V_F}{I_C(MAX)} \quad (3)$$

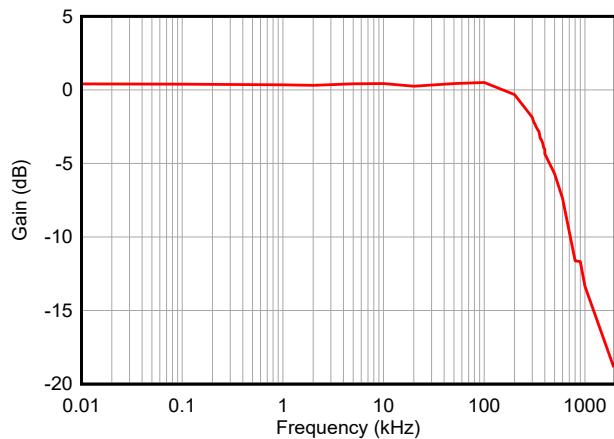
However, in the use case of a feedback loop,  $R_{IN}$  directly affects the mid-band gain of the loop. Assuming that the TL431 has been configured to give a reference voltage,  $V_{REF}$ , of 2.5V and  $R_{PULLUP}$  is 5k $\Omega$ , [Equation 4](#) is used to calculate the maximum value of  $R_{IN}$  verifying that the  $V_{COMP}$  voltage on the primary side can be pulled to the saturation voltage of the ISOM811x,  $V_{CE(SAT)}$ .

$$R_{IN} < \frac{(V_{OUT} - V_{REF} - V_F) \times R_{PULLUP} \times CTR_{MIN}}{V_{PULLUP} - V_{CE(SAT)}} = \frac{(5V - 2.5V - 1.2V) \times 5k\Omega \times 100\%}{10V - 0.3V} = 670\Omega \quad (4)$$

### 9.1.1.3 Application Curves

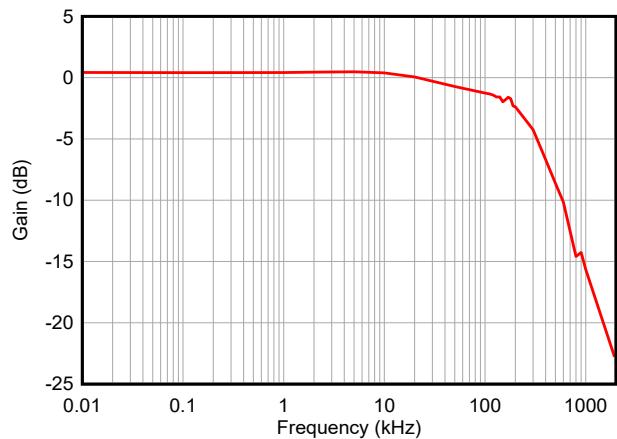
The following curves show ISOM8110 bandwidth performance over different loading conditions where  $V_{IN} = 5V_{DC} + 2V_{PK}$ . See [Figure 7-4](#) for setup details.





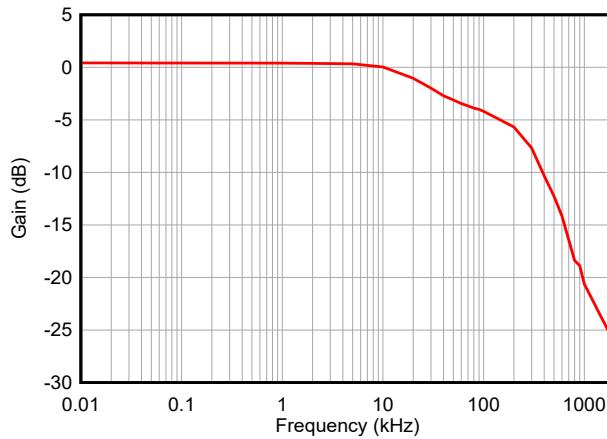
$C_{IN} = 5\text{pF}$     $R_{IN} = 2\text{k}\Omega$     $C_L = 50\text{pF}$     $R_L = 2\text{k}\Omega$     $V_{CC} = 10\text{V}$

**Figure 9-4. Bandwidth at  $R_L = 2\text{k}\Omega$**



$C_{IN} = 5\text{pF}$     $R_{IN} = 2\text{k}\Omega$     $C_L = 50\text{pF}$     $R_L = 4.7\text{k}\Omega$     $V_{CC} = 10\text{V}$

**Figure 9-5. Bandwidth at  $R_L = 4.7\text{k}\Omega$**



$C_{IN} = 5\text{pF}$     $R_{IN} = 2\text{k}\Omega$     $C_L = 50\text{pF}$     $R_L = 10\text{k}\Omega$     $V_{CC} = 45\text{V}$

**Figure 9-6. Bandwidth at  $R_L = 10\text{k}\Omega$**

## 9.2 Power Supply Recommendations

ISOM811x does not require a dedicated power supply to operate since there is no supply pin. Take care to not violate recommended I/O specifications for proper device functionality.

## 9.3 Layout

### 9.3.1 Layout Guidelines

- The device connections to ground must be tied to the PCB ground plane using a direct connection or two vias to help minimize inductance.
- The connections of capacitors and other components to the PCB ground plane must use a direct connection or two vias for minimum inductance.

### 9.3.2 Layout Example

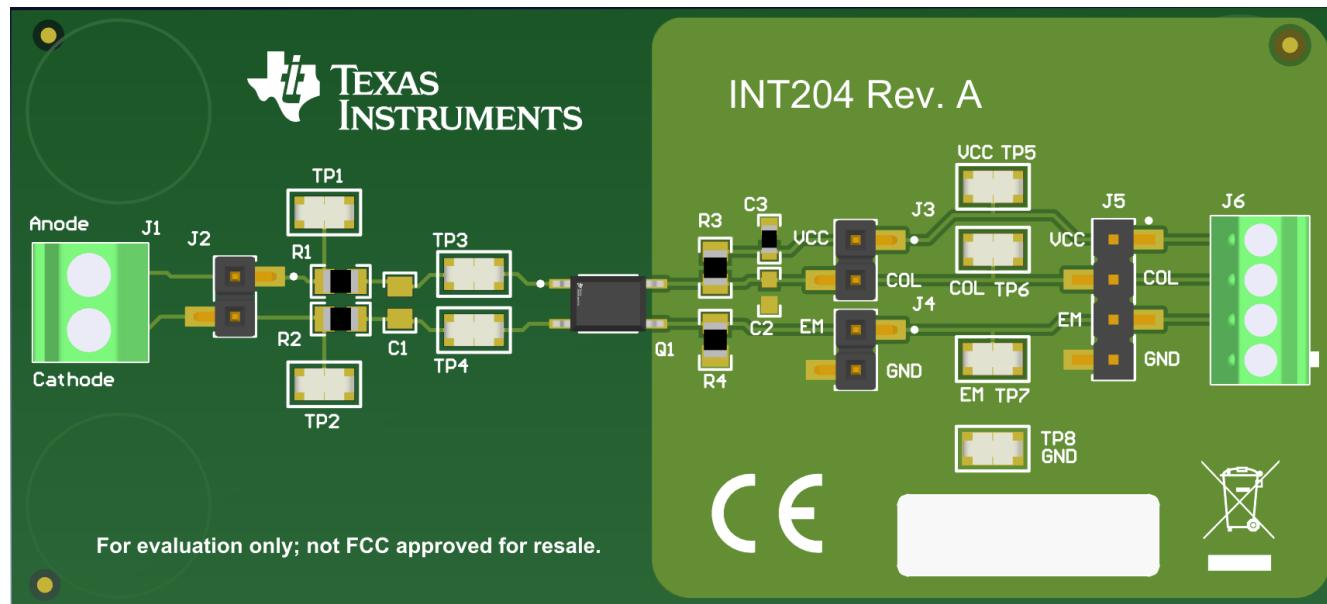


Figure 9-7. Layout Example of ISOM811x With a Single Layer Board

### 9.3.3 Reflow Profile

Many traditional optocouplers have limits on the peak temperature of reflow soldering due to device construction. Opto-emulators benefit from TI's packaging technology and can withstand up to three reflow cycles. These integrated circuit packages are classified for moisture and reflow temperature sensitivity according to the current IPC/JEDEC J-STD-020 standard.

The peak reflow temperature is specified according to the package thickness and plastic volume. The Pb-Free Process-Classification Temperatures ( $T_c$ ) table in the IPC/JEDEC J-STD-020 standard lists the temperatures for lead-free processes, which are shown in [Table 9-2](#).

**Table 9-2. Peak Reflow Classification ( $T_c$ ) Based on Package Dimensions**

Package Thickness	Volume < 350mm <sup>3</sup>	Volume 350 – 2000mm <sup>3</sup>	Volume >2000mm <sup>3</sup>
< 1.6mm	260°C	260°C	260°C
1.6mm – 2.5mm	260°C	250°C	245°C
>2.5mm	250°C	245°C	245°C

The reflow profile shown in [Figure 9-8](#) can be used with a typical range for the customer peak reflow temperature ( $T_p$ ) of 235°C to 250°C. The peak reflow temperature ( $T_p$ ) must not exceed the classification reflow temperature ( $T_c$ ) shown in [Table 9-2](#) and [Figure 9-8](#).

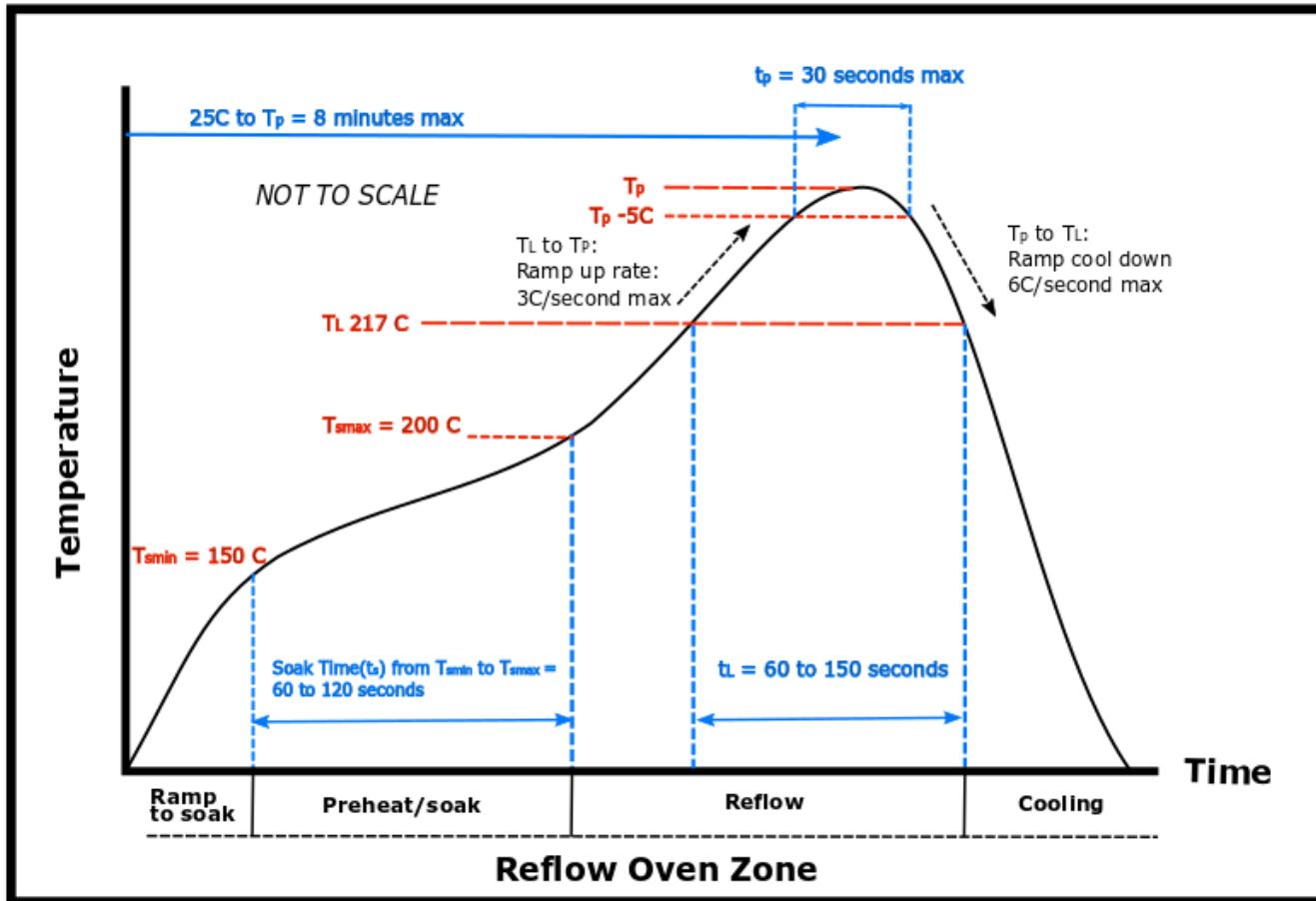


Figure 9-8. TI Representation of the J-STD-020 Classification Profile (not to scale)

For additional details, please refer to [MSL Ratings and Reflow Profiles](#).

## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Isolation Glossary](#), application note
- Texas Instruments, [Introduction to Opto-Emulators](#), application note
- Texas Instruments, [ISOM8110 Single-Channel Opto-Emulator with Analog Transistor Output Evaluation Module](#), EVM user's guide

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision E (April 2025) to Revision F (July 2025)</b>	<b>Page</b>
• Updated the Electrical Characteristics tables test conditions for the Input and Output sections and added information to the CTR section.....	7
• Updated the Switching Characteristics table for better readability.....	9

<b>Changes from Revision D (December 2024) to Revision E (April 2025)</b>	<b>Page</b>
• Updated the number formatting for figures, tables, and cross-references throughout the document .....	1
• Updated with released DFS package information .....	1

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<b>Changes from Revision C (October 2024) to Revision D (December 2024)</b>	<b>Page</b>
• Updated the number formatting for figures, tables, and cross-references throughout the document .....	1
• Updated with preview DFS package information .....	1
• Added DFS package preview information.....	5
• Updated reverse current.....	7

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<b>Changes from Revision B (August 2024) to Revision C (October 2024)</b>	<b>Page</b>
• Updated the number formatting for figures, tables, and cross-references throughout the document .....	1

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<b>Changes from Revision A (December 2023) to Revision B (August 2024)</b>	<b>Page</b>
• Updated the number formatting for figures, tables, and cross-references throughout the document .....	1
• Added <i>Device and Documentation Support</i> section .....	25

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## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">ISOM8110DFGR</a>	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8110
ISOM8110DFGR.A	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8110
ISOM8110DFGR.B	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
<a href="#">ISOM8110DFHR</a>	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8110
ISOM8110DFHR.A	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8110
ISOM8110DFHR.B	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
<a href="#">ISOM8110DFSR</a>	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8110
ISOM8110DFSR.A	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8110
ISOM8110DFSR.B	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8110
<a href="#">ISOM8111DFGR</a>	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8111
ISOM8111DFGR.A	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8111
ISOM8111DFGR.B	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
<a href="#">ISOM8111DFHR</a>	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8111
ISOM8111DFHR.A	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8111
ISOM8111DFHR.B	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
<a href="#">ISOM8111DFSR</a>	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8111
ISOM8111DFSR.A	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8111
ISOM8111DFSR.B	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8111
<a href="#">ISOM8112DFGR</a>	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8112
ISOM8112DFGR.A	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8112
ISOM8112DFGR.B	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
<a href="#">ISOM8112DFHR</a>	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8112
ISOM8112DFHR.A	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8112
ISOM8112DFHR.B	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
<a href="#">ISOM8112DFSR</a>	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8112
ISOM8112DFSR.A	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8112
ISOM8112DFSR.B	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8112
<a href="#">ISOM8113DFGR</a>	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8113
ISOM8113DFGR.A	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8113

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISOM8113DFGR.B	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
<a href="#">ISOM8113DFHR</a>	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8113
ISOM8113DFHR.A	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8113
ISOM8113DFHR.B	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
<a href="#">ISOM8113DFSR</a>	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8113
ISOM8113DFSR.A	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8113
ISOM8113DFSR.B	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8113
<a href="#">ISOM8115DFGR</a>	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8115
ISOM8115DFGR.A	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8115
ISOM8115DFGR.B	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
<a href="#">ISOM8115DFHR</a>	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8115
ISOM8115DFHR.A	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8115
ISOM8115DFHR.B	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
<a href="#">ISOM8115DFSR</a>	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8115
ISOM8115DFSR.A	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8115
ISOM8115DFSR.B	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8115
<a href="#">ISOM8116DFGR</a>	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8116
ISOM8116DFGR.A	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8116
ISOM8116DFGR.B	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
<a href="#">ISOM8116DFHR</a>	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8116
ISOM8116DFHR.A	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8116
ISOM8116DFHR.B	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
<a href="#">ISOM8116DFSR</a>	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8116
ISOM8116DFSR.A	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8116
ISOM8116DFSR.B	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8116
<a href="#">ISOM8117DFGR</a>	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8117
ISOM8117DFGR.A	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8117
ISOM8117DFGR.B	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
<a href="#">ISOM8117DFHR</a>	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8117
ISOM8117DFHR.A	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8117
ISOM8117DFHR.B	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">ISOM8117DFSR</a>	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8117
ISOM8117DFSR.A	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8117
ISOM8117DFSR.B	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8117
<a href="#">ISOM8118DFGR</a>	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8118
ISOM8118DFGR.A	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8118
ISOM8118DFGR.B	Active	Production	SOIC (DFG)   4	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
<a href="#">ISOM8118DFHR</a>	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8118
ISOM8118DFHR.A	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8118
ISOM8118DFHR.B	Active	Production	SOIC (DFH)   4	2000   LARGE T&R	-	Call TI	Call TI	-55 to 125	
<a href="#">ISOM8118DFSR</a>	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8118
ISOM8118DFSR.A	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8118
ISOM8118DFSR.B	Active	Production	SOIC (DFS)   4	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8118

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

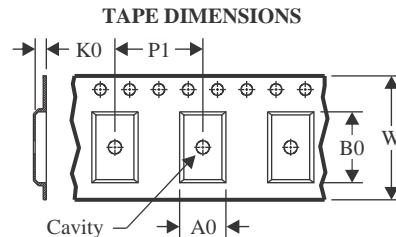
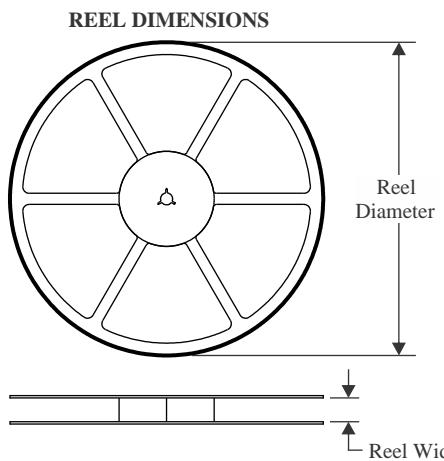
**OTHER QUALIFIED VERSIONS OF ISOM8110, ISOM8111, ISOM8112, ISOM8113, ISOM8115, ISOM8116, ISOM8117, ISOM8118 :**

- Automotive : [ISOM8110-Q1](#), [ISOM8111-Q1](#), [ISOM8112-Q1](#), [ISOM8113-Q1](#), [ISOM8115-Q1](#), [ISOM8116-Q1](#), [ISOM8117-Q1](#), [ISOM8118-Q1](#)

**NOTE: Qualified Version Definitions:**

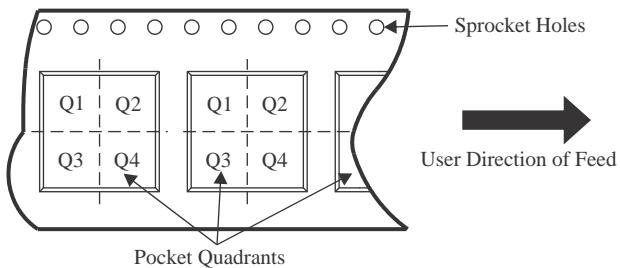
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

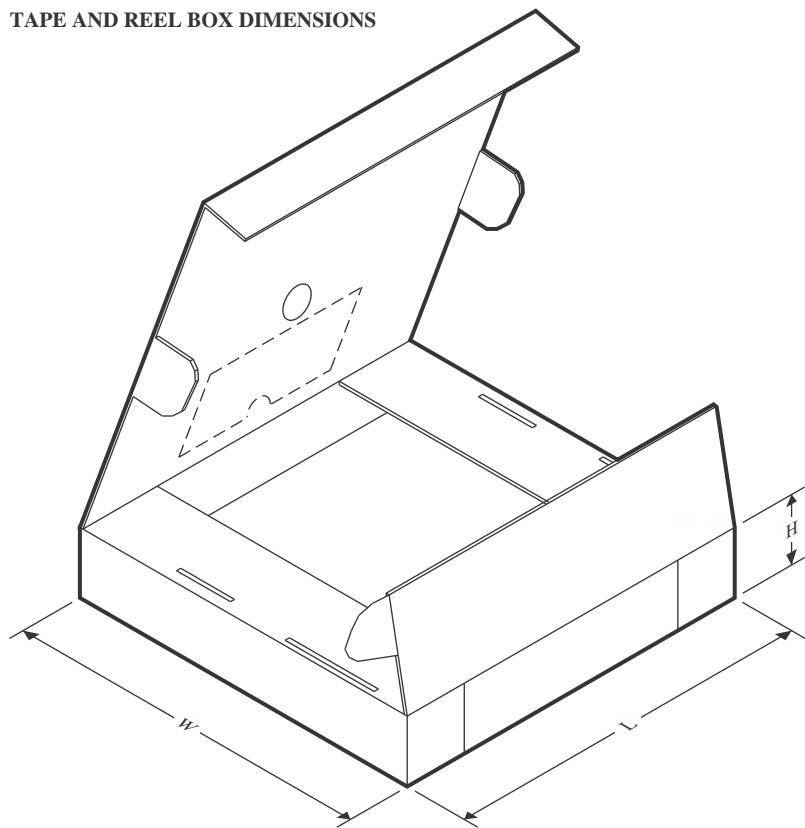
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOM8110DFGR	SOIC	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1
ISOM8110DFHR	SOIC	DFH	4	2000	330.0	12.4	8.0	3.0	2.7	12.0	12.0	Q1
ISOM8110DFSR	SOIC	DFS	4	2000	330.0	12.4	10.9	3.98	2.7	12.0	12.0	Q1
ISOM8111DFGR	SOIC	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1
ISOM8111DFHR	SOIC	DFH	4	2000	330.0	12.4	8.0	3.0	2.7	12.0	12.0	Q1
ISOM8111DFSR	SOIC	DFS	4	2000	330.0	12.4	10.9	3.98	2.7	12.0	12.0	Q1
ISOM8112DFGR	SOIC	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1
ISOM8112DFHR	SOIC	DFH	4	2000	330.0	12.4	8.0	3.0	2.7	12.0	12.0	Q1
ISOM8112DFSR	SOIC	DFS	4	2000	330.0	12.4	10.9	3.98	2.7	12.0	12.0	Q1
ISOM8113DFGR	SOIC	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1
ISOM8113DFHR	SOIC	DFH	4	2000	330.0	12.4	8.0	3.0	2.7	12.0	12.0	Q1
ISOM8113DFSR	SOIC	DFS	4	2000	330.0	12.4	10.9	3.98	2.7	12.0	12.0	Q1
ISOM8115DFGR	SOIC	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1
ISOM8115DFHR	SOIC	DFH	4	2000	330.0	12.4	8.0	3.0	2.7	12.0	12.0	Q1
ISOM8115DFSR	SOIC	DFS	4	2000	330.0	12.4	10.9	3.98	2.7	12.0	12.0	Q1
ISOM8116DFGR	SOIC	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOM8116DFHR	SOIC	DFH	4	2000	330.0	12.4	8.0	3.0	2.7	12.0	12.0	Q1
ISOM8116DFSR	SOIC	DFS	4	2000	330.0	12.4	10.9	3.98	2.7	12.0	12.0	Q1
ISOM8117DFGR	SOIC	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1
ISOM8117DFHR	SOIC	DFH	4	2000	330.0	12.4	8.0	3.0	2.7	12.0	12.0	Q1
ISOM8117DFSR	SOIC	DFS	4	2000	330.0	12.4	10.9	3.98	2.7	12.0	12.0	Q1
ISOM8118DFGR	SOIC	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1
ISOM8118DFHR	SOIC	DFH	4	2000	330.0	12.4	8.0	3.0	2.7	12.0	12.0	Q1
ISOM8118DFSR	SOIC	DFS	4	2000	330.0	12.4	10.9	3.98	2.7	12.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOM8110DFGR	SOIC	DFG	4	2000	353.0	353.0	32.0
ISOM8110DFHR	SOIC	DFH	4	2000	353.0	353.0	32.0
ISOM8110DFSR	SOIC	DFS	4	2000	353.0	353.0	32.0
ISOM8111DFGR	SOIC	DFG	4	2000	353.0	353.0	32.0
ISOM8111DFHR	SOIC	DFH	4	2000	353.0	353.0	32.0
ISOM8111DFSR	SOIC	DFS	4	2000	353.0	353.0	32.0
ISOM8112DFGR	SOIC	DFG	4	2000	353.0	353.0	32.0
ISOM8112DFHR	SOIC	DFH	4	2000	353.0	353.0	32.0
ISOM8112DFSR	SOIC	DFS	4	2000	353.0	353.0	32.0
ISOM8113DFGR	SOIC	DFG	4	2000	353.0	353.0	32.0
ISOM8113DFHR	SOIC	DFH	4	2000	353.0	353.0	32.0
ISOM8113DFSR	SOIC	DFS	4	2000	353.0	353.0	32.0
ISOM8115DFGR	SOIC	DFG	4	2000	353.0	353.0	32.0
ISOM8115DFHR	SOIC	DFH	4	2000	353.0	353.0	32.0
ISOM8115DFSR	SOIC	DFS	4	2000	353.0	353.0	32.0
ISOM8116DFGR	SOIC	DFG	4	2000	353.0	353.0	32.0
ISOM8116DFHR	SOIC	DFH	4	2000	353.0	353.0	32.0
ISOM8116DFSR	SOIC	DFS	4	2000	353.0	353.0	32.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOM8117DFGR	SOIC	DFG	4	2000	353.0	353.0	32.0
ISOM8117DFHR	SOIC	DFH	4	2000	353.0	353.0	32.0
ISOM8117DFSR	SOIC	DFS	4	2000	353.0	353.0	32.0
ISOM8118DFGR	SOIC	DFG	4	2000	353.0	353.0	32.0
ISOM8118DFHR	SOIC	DFH	4	2000	353.0	353.0	32.0
ISOM8118DFSR	SOIC	DFS	4	2000	353.0	353.0	32.0

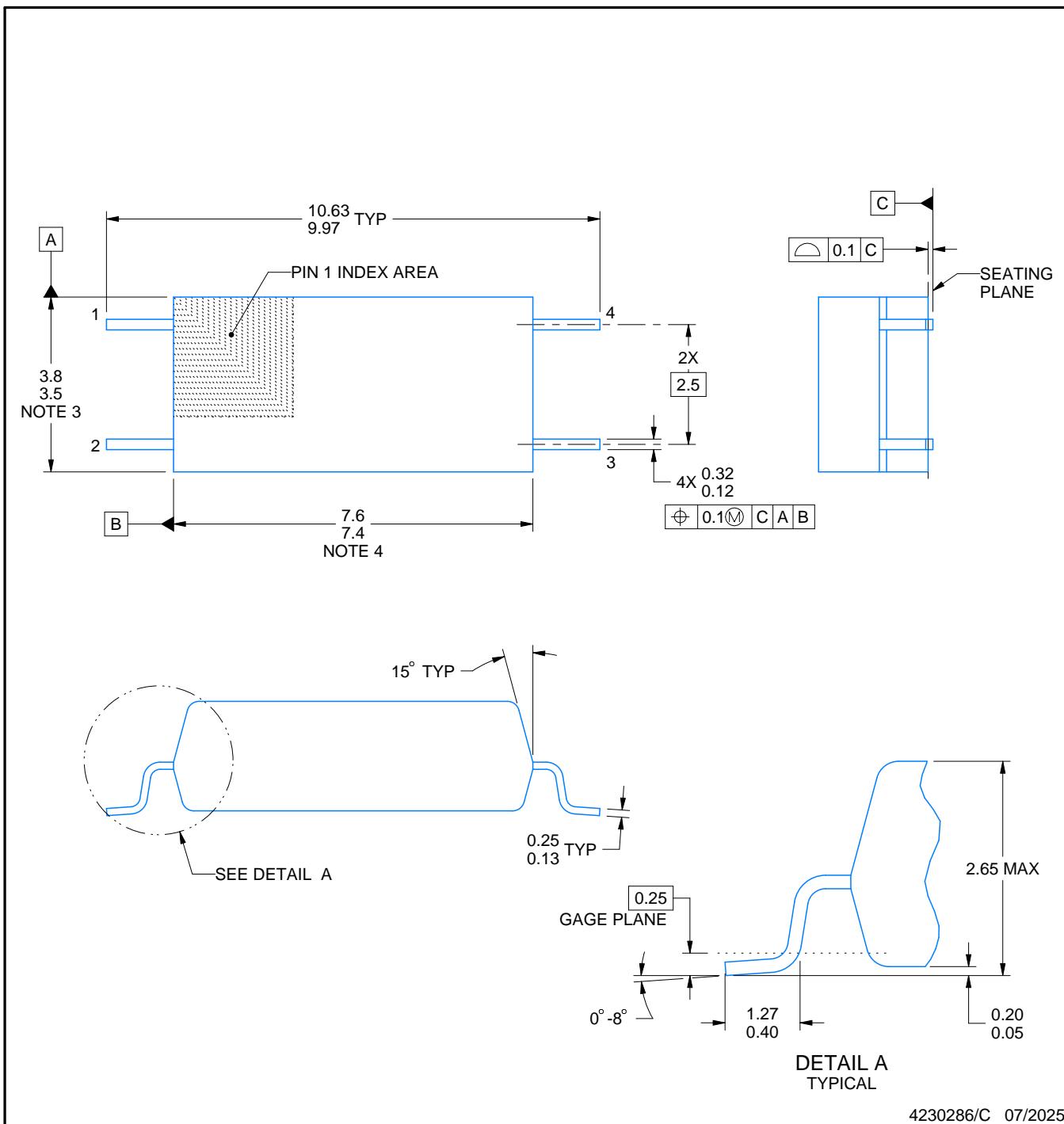
# PACKAGE OUTLINE

**DFS0004A**



**SOIC - 2.65 mm max height**

SMALL OUTLINE PACKAGE



**NOTES:**

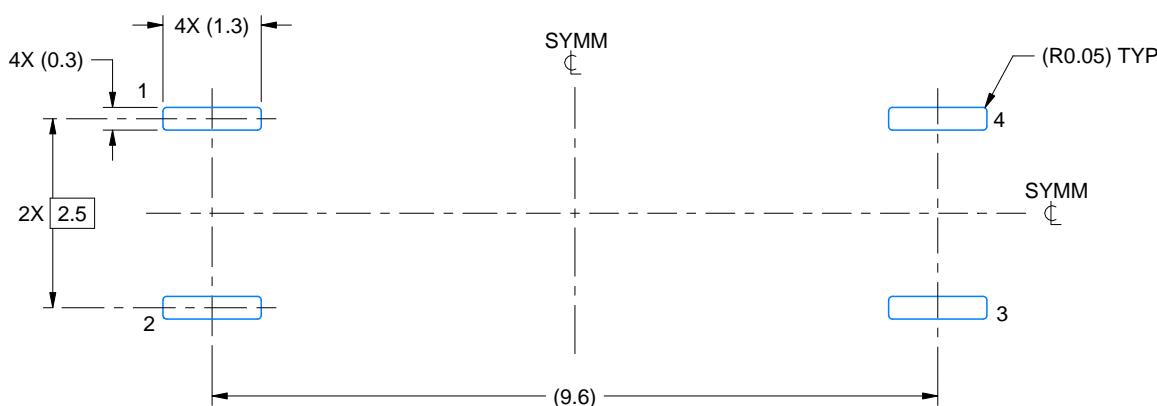
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

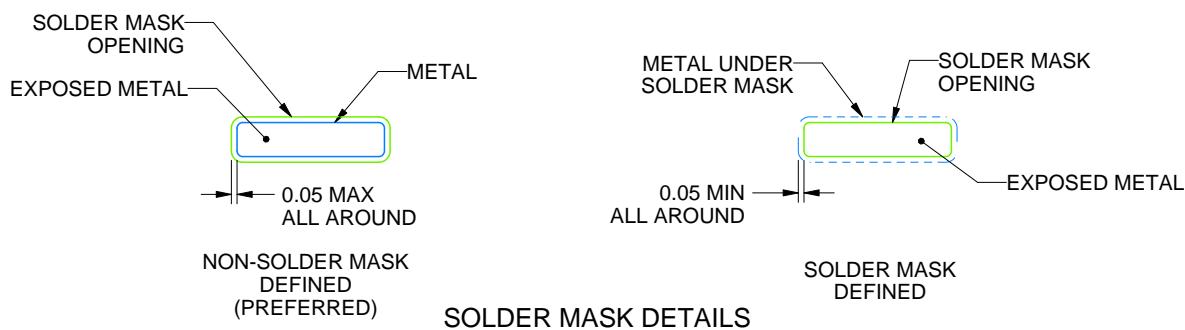
DFS0004A

SOIC - 2.65 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4230286/C 07/2025

NOTES: (continued)

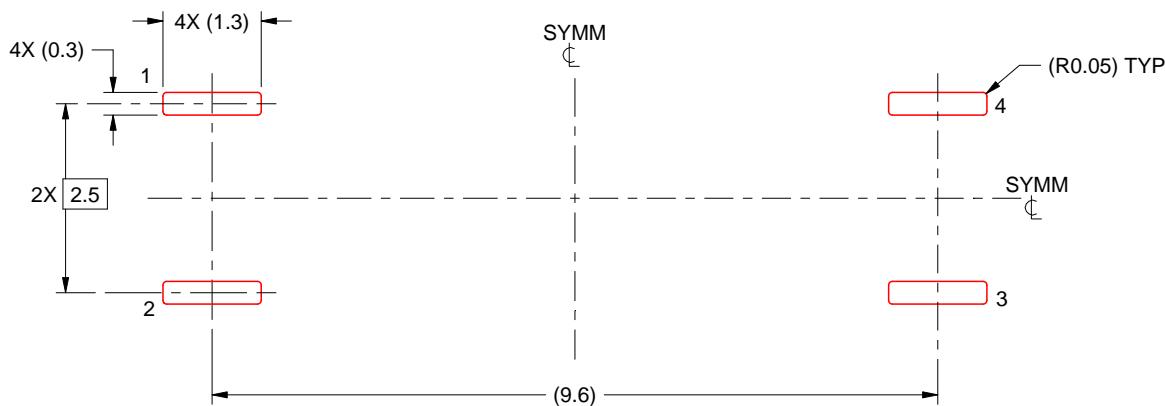
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DFS0004A

SOIC - 2.65 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4230286/C 07/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

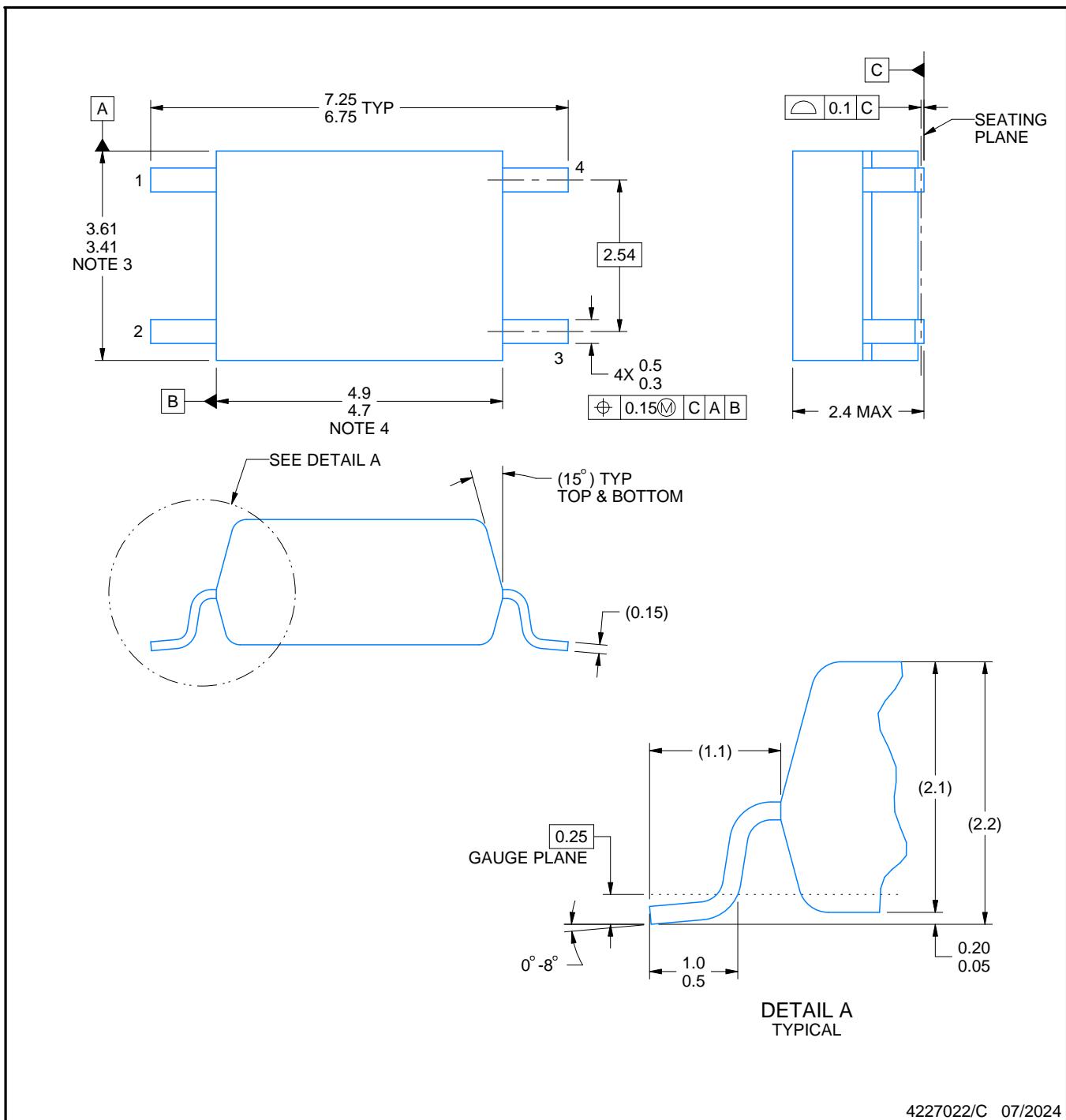
# PACKAGE OUTLINE

**DFG0004A**



**SOIC - 2.4 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

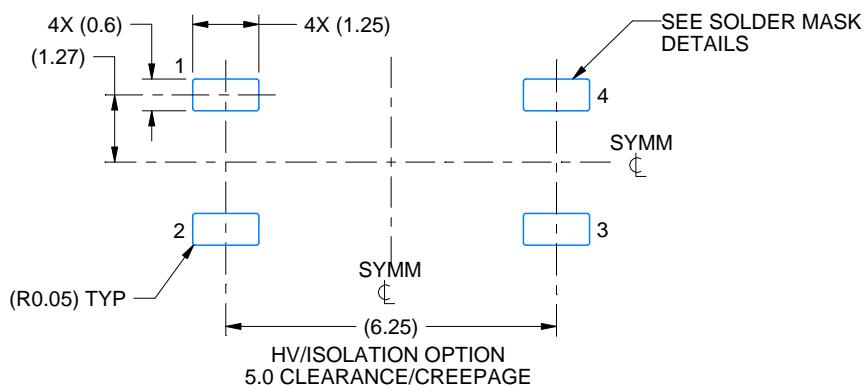
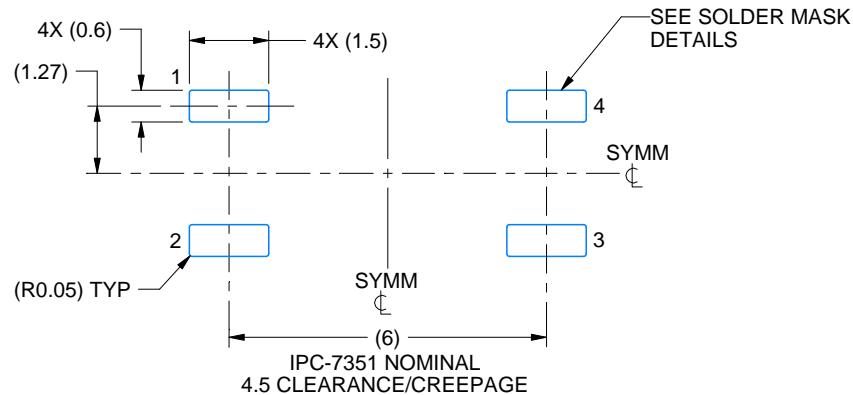
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash.

# EXAMPLE BOARD LAYOUT

DFG0004A

SOIC - 2.4 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 7X



4227022/C 07/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

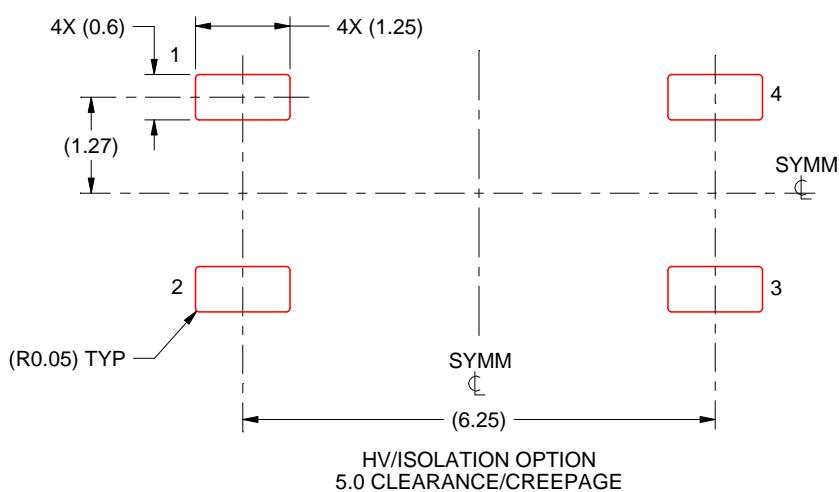
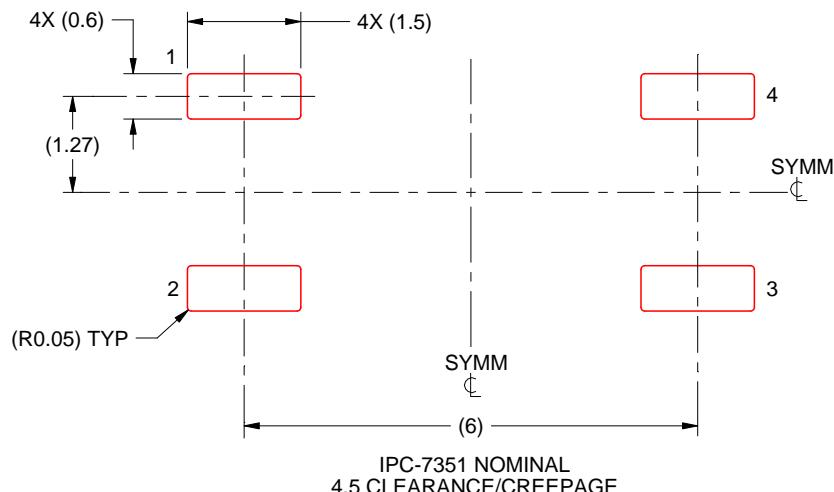
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DFG0004A

SOIC - 2.4 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4227022/C 07/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

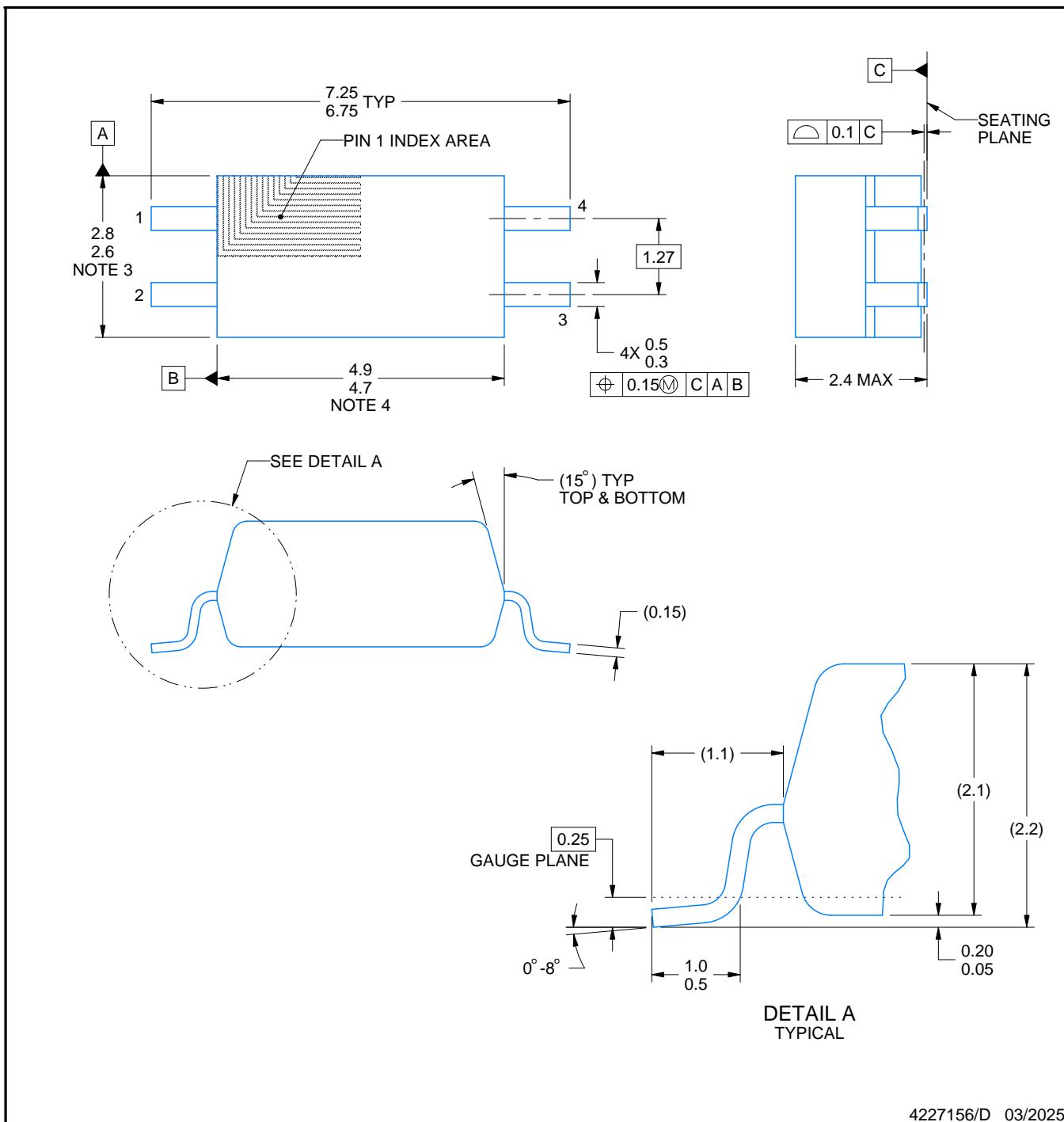
# PACKAGE OUTLINE

**DFH0004A**



**SOIC - 2.4 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4227156/D 03/2025

NOTES:

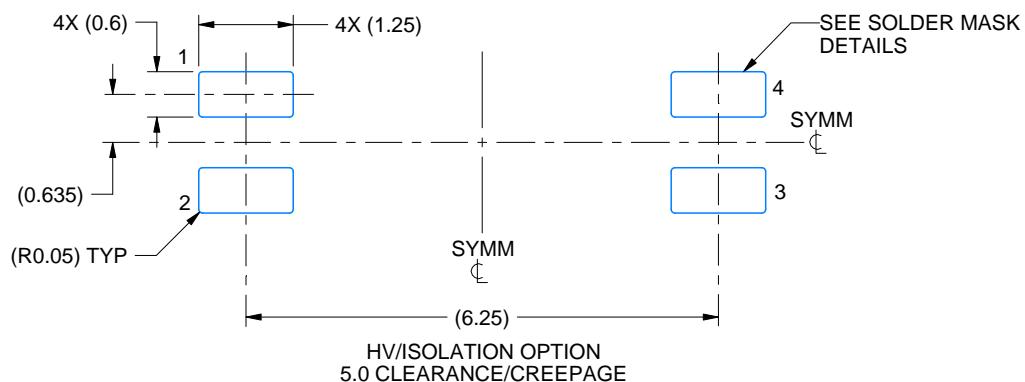
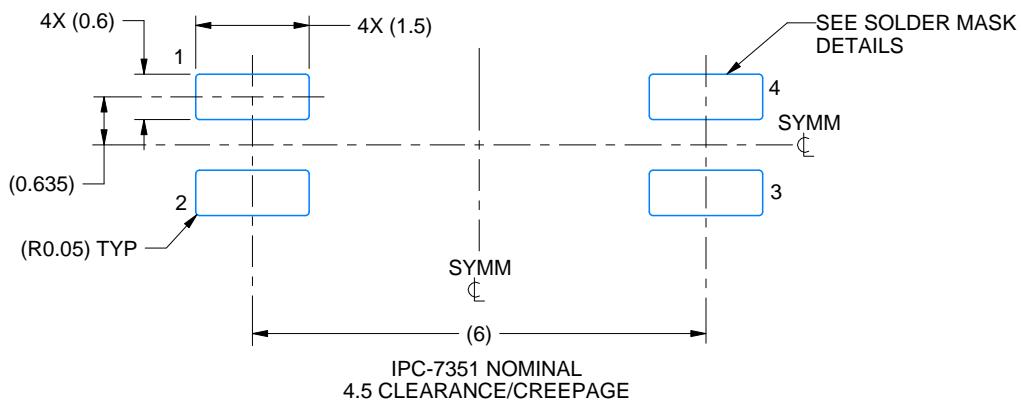
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash.

# EXAMPLE BOARD LAYOUT

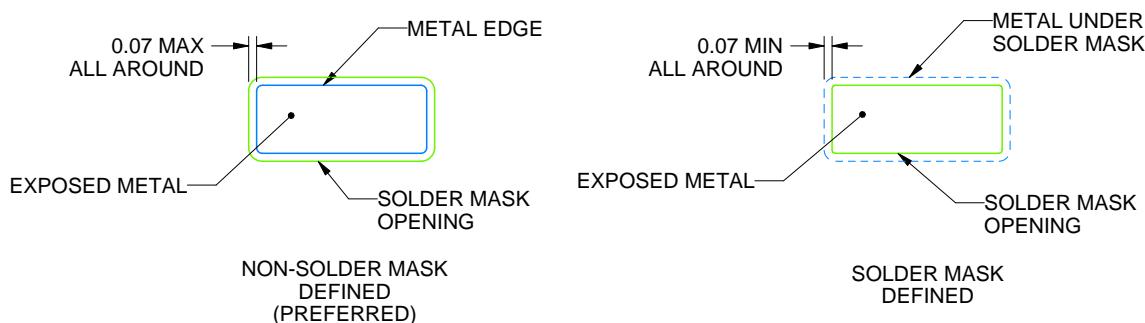
DFH0004A

SOIC - 2.4 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4227156/D 03/2025

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

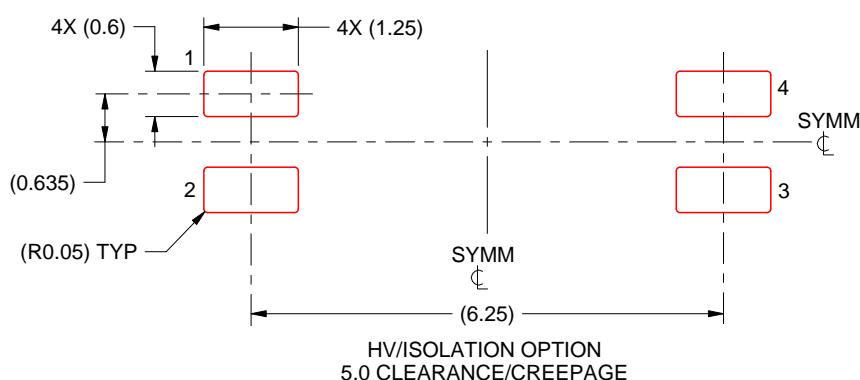
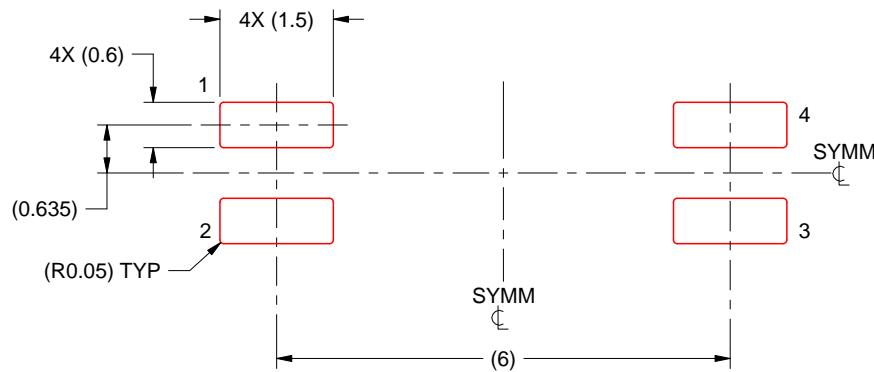
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DFH0004A

SOIC - 2.4 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4227156/D 03/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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