

NP60N06VDK

60 V – 60 A – N-channel Power MOS FET

R07DS1340EJ0200

Rev.2.00

Application: Automotive

May 24, 2018

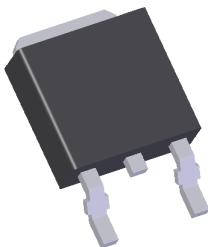
Description

NP60N06VDK is N-channel MOS Field Effect Transistor designed for high current switching applications.

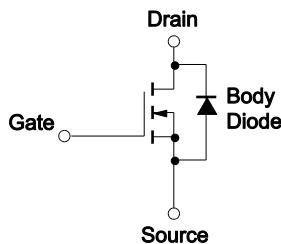
Features

- Super low on-state resistance
 - $R_{DS(on)1} = 7.9 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 10 \text{ V}, I_D = 30 \text{ A}$)
- Low C_{iss} : $C_{iss} = 2400 \text{ pF TYP.}$ ($V_{DS} = 25 \text{ V}$)
- Designed for automotive application and AEC-Q101 qualified

Outline



TO-252(MP-3ZP)



Equivalent circuit

Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Ordering Information

Part No.	Lead Plating	Packing		Package
NP60N06VDK-E1-AY *1	Pure Sn (Tin)	Tape 800 p/reel	Taping (E1 type)	TO-252(MP-3ZP)
NP60N06VDK-E2-AY *1			Taping (E2 type)	

Note: *1. Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	60	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(\text{DC})}$	± 60	A
Drain Current (pulse) ^{*1*3}	$I_{D(\text{pulse})}$	± 240	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	105	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	1.2	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +175	$^\circ\text{C}$
Repetitive Avalanche Current ^{*2*3}	I_{AR}	25	A
Repetitive Avalanche Energy ^{*2*3}	E_{AR}	63	mJ

Thermal Resistance

Channel to Case Thermal Resistance $R_{th(\text{ch-C})}$ ^{*3} 1.43 $^\circ\text{C}/\text{W}$
 Channel to Ambient Thermal Resistance $R_{th(\text{ch-A})}$ ^{*3} 125 $^\circ\text{C}/\text{W}$

Notes: *1. $T_C = 25^\circ\text{C}$, $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

*2. $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

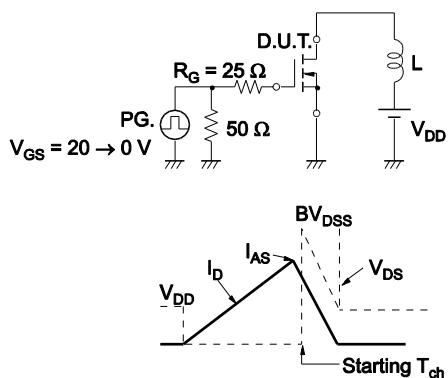
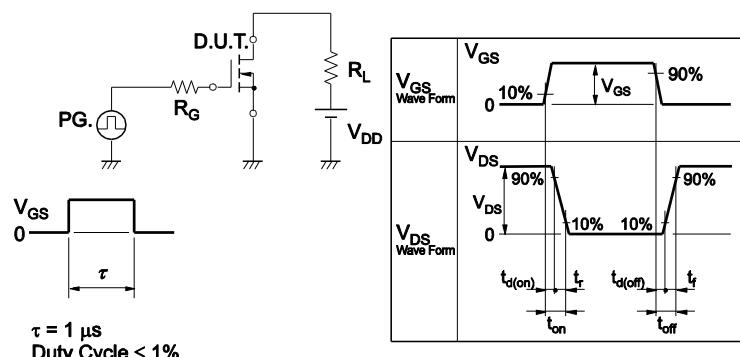
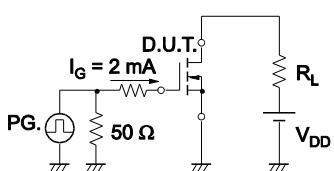
*3. Not subject of production test. Verified by design/characterization.

Electrical Characteristics ($T_A = 25^\circ\text{C}$)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			1	μA	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I_{GSS}			± 100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	$V_{GS(\text{th})}$	1.5	2.1	2.5	V	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$
Forward Transfer Admittance *1	$ y_{fs} $	33	54		S	$V_{DS} = 5 \text{ V}, I_D = 30 \text{ A}$
Drain to Source On-state Resistance *1	$R_{DS(\text{on})1}$		6.1	7.9	$\text{m}\Omega$	$V_{GS} = 10 \text{ V}, I_D = 30 \text{ A}$
	$R_{DS(\text{on})2}$		7.4	12.0	$\text{m}\Omega$	$V_{GS} = 4.5 \text{ V}, I_D = 15 \text{ A}$
Input Capacitance *2	C_{iss}		2400	3600	pF	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$
Output Capacitance *2	C_{oss}		230	350	pF	
Reverse Transfer Capacitance *2	C_{rss}		80	150	pF	
Turn-on Delay Time *2	$t_{d(\text{on})}$		18	40	ns	$V_{DD} = 30 \text{ V}, I_D = 30 \text{ A}, V_{GS} = 10 \text{ V}, R_G = 0 \Omega$
Rise Time *2	t_r		6	20	ns	
Turn-off Delay Time *2	$t_{d(\text{off})}$		45	90	ns	
Fall Time *2	t_f		3	10	ns	
Total Gate Charge *2	Q_G		37	56	nC	$V_{DD} = 48 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 60 \text{ A}$
Gate to Source Charge	Q_{GS}		9		nC	
Gate to Drain Charge	Q_{GD}		8		nC	
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.9	1.5	V	$I_F = 60 \text{ A}, V_{GS} = 0 \text{ V}$
Reverse Recovery Time	t_{rr}		32		ns	$I_F = 60 \text{ A}, V_{GS} = 0 \text{ V}, dI/dt = 100 \text{ A}/\mu\text{s}$
Reverse Recovery Charge	Q_{rr}		30		nC	

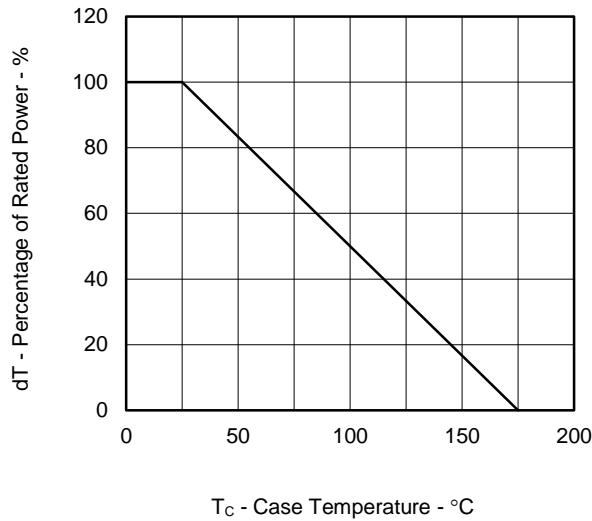
Note: *1. Pulsed test

Note: *2. Not subject of production test. Verified by design/characterization.

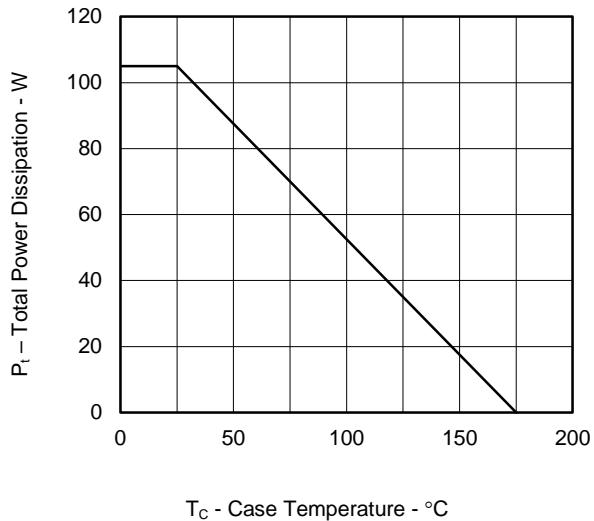
TEST CIRCUIT 1 AVALANCHE CAPABILITY**TEST CIRCUIT 2 SWITCHING TIME****TEST CIRCUIT 3 GATE CHARGE**

Typical Characteristics ($T_A = 25^\circ\text{C}$)

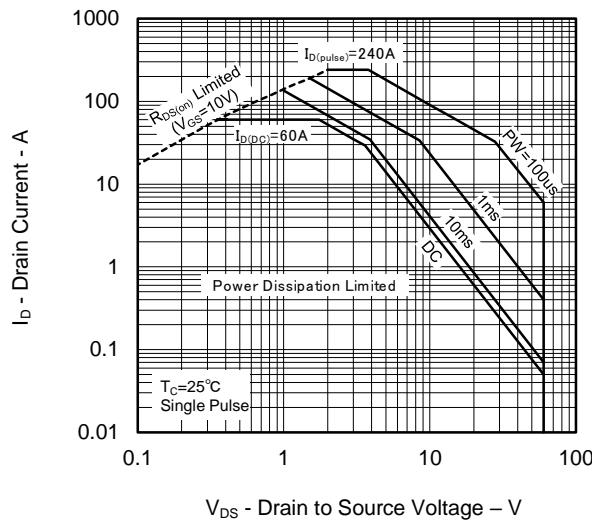
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



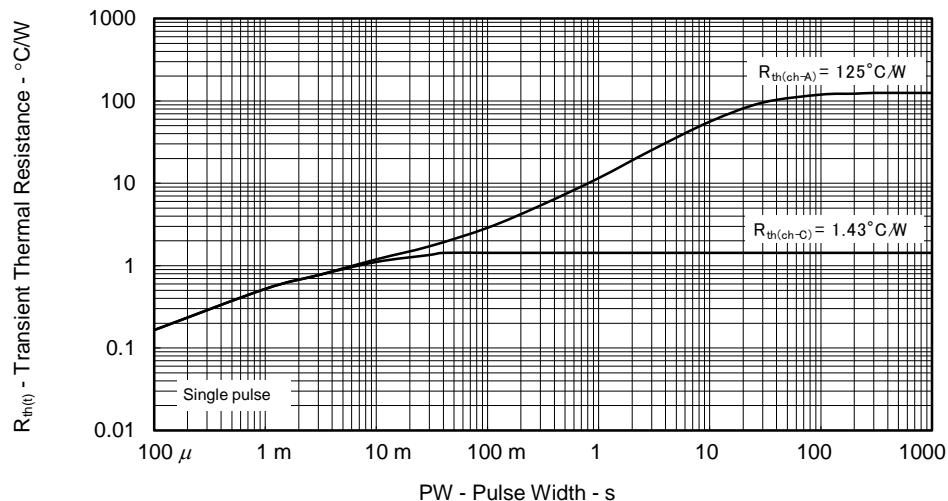
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

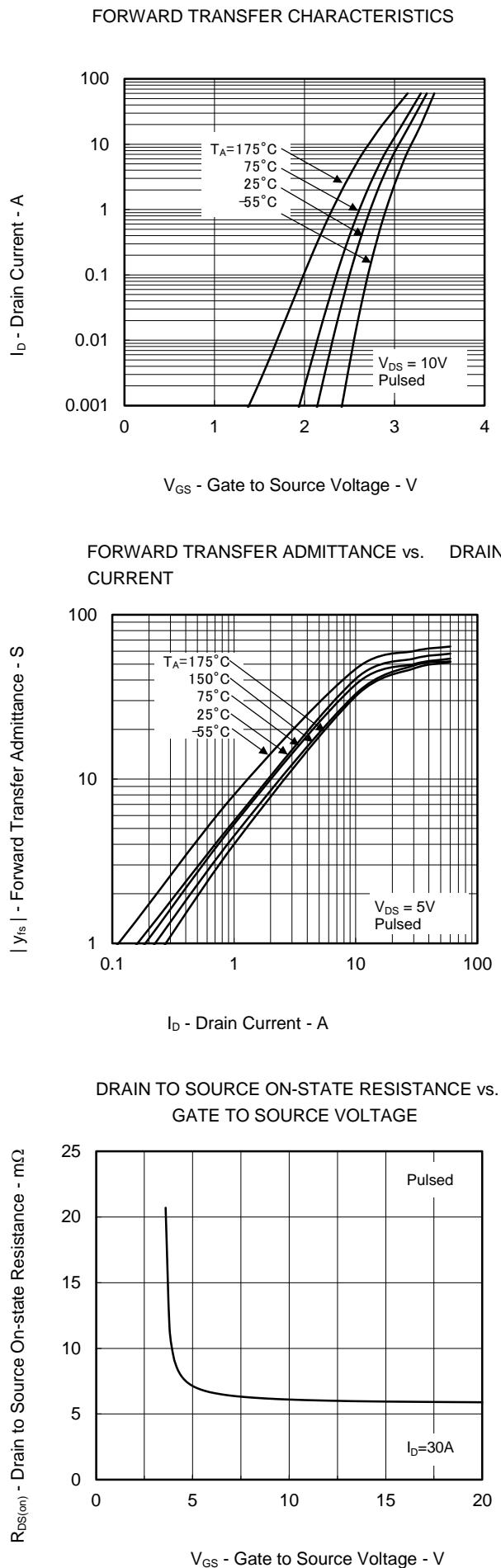
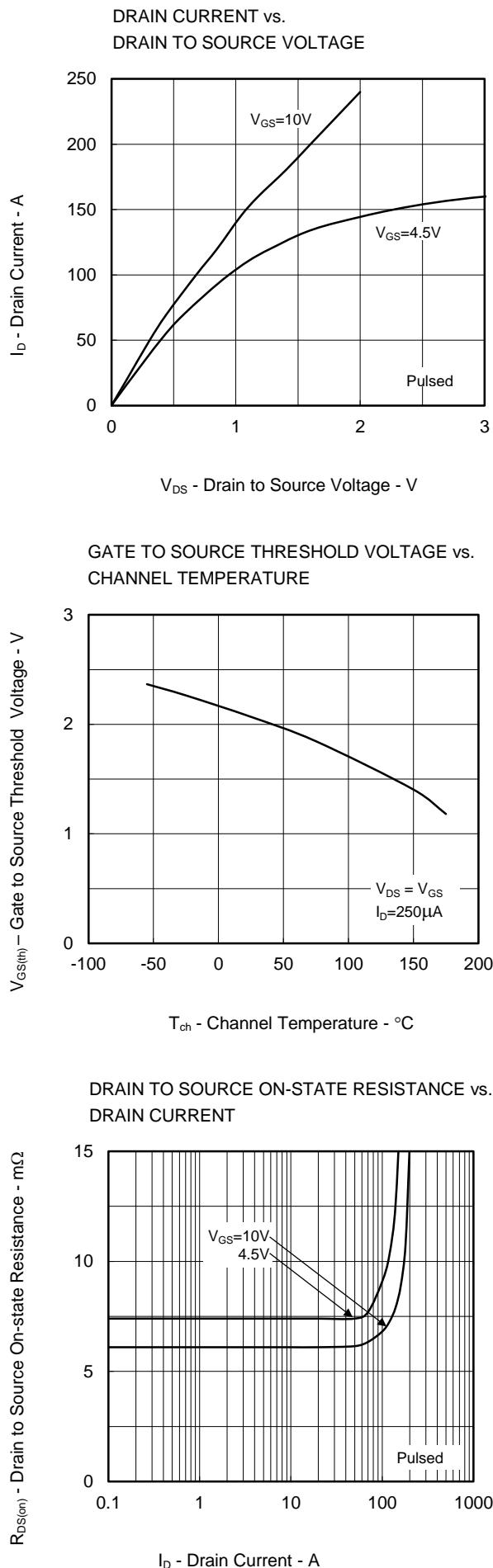


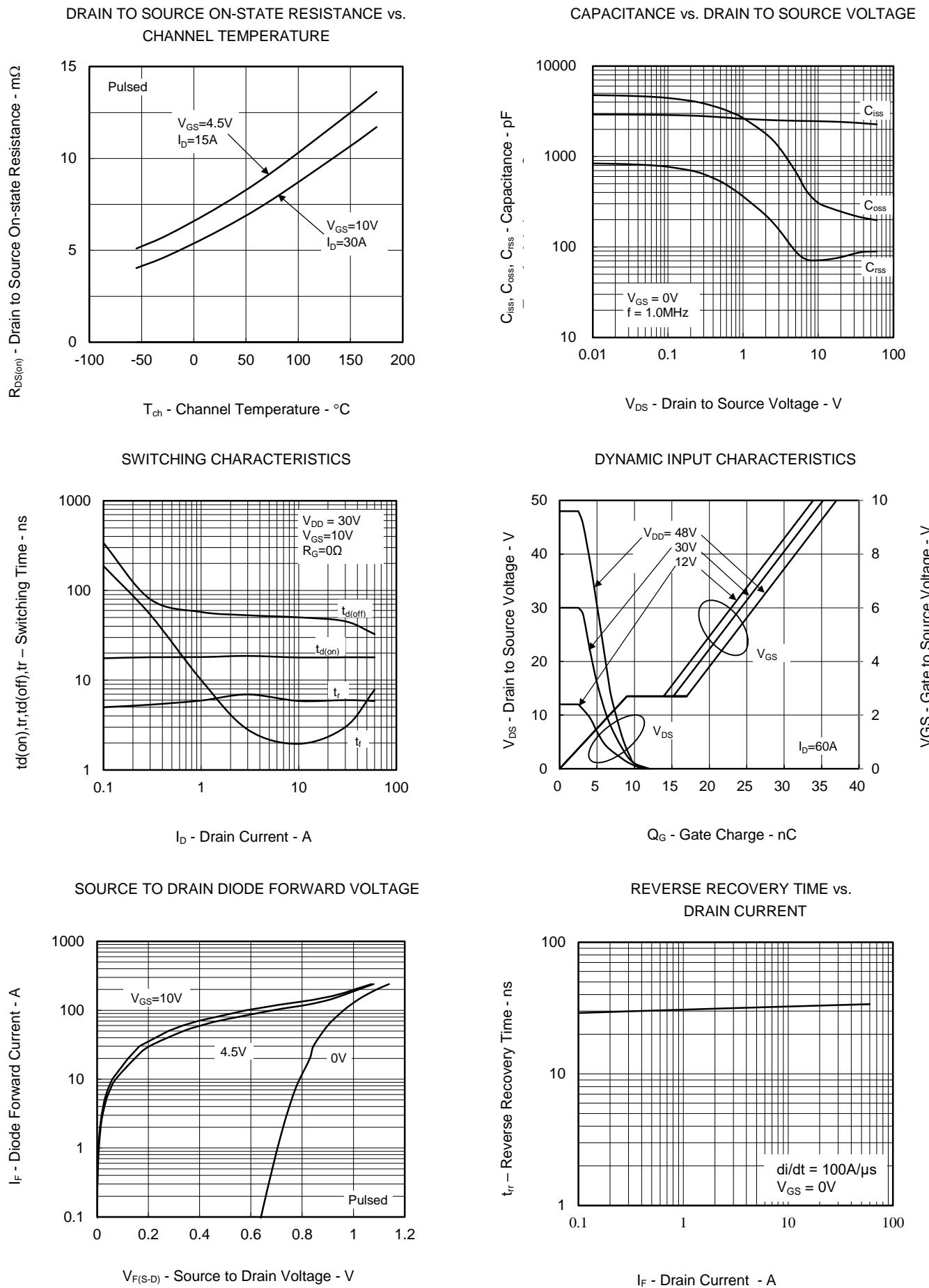
FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

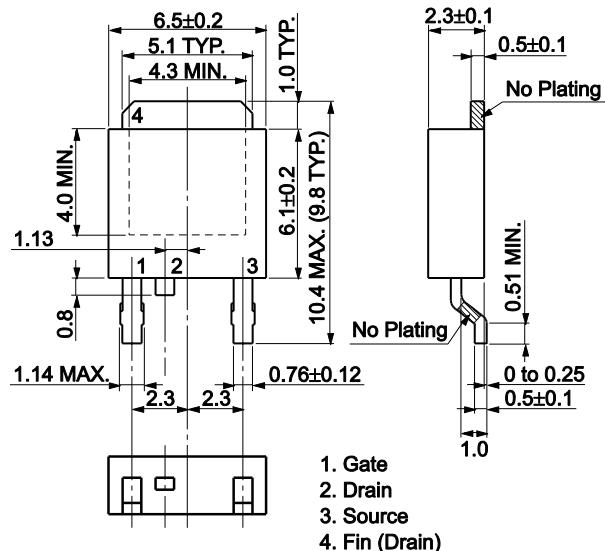






Package Drawings (Unit: mm)**TO-252 (MP-3ZP) (Mass: 1.48 g TYP.)**

Renesas package code: PRSS0004ZP-A



Revision History		NP60N06VDK Data Sheet	
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Rev.	Date	Description	
		Page	Summary
1.00	Apr. 8, 2016	—	First Edition Issued
2.00	May 24 ,2018	2 3	Note 3 was added Note 2 was added

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