Design of a Fully Differential OTA Using 45nm CMOS Technology

Prem Bharath Soundararajan
Electrical Engineering
San Jose State University
prembharath@outlook.com

Shiva Nangi
Electrical Engineering
San Jose State University
shiva.nangi91@gmail.com

Venkata Ranga Sairam Pradyumna Prasad Kondapalli
Electrical Engineering
San Jose State University
pradyumna.kondapalli@gmail.com

Abstract—This paper describes the theory of operation, applications, design considerations, and design methodology of a fully differential Operational Transconductance Amplifier (OTA) using a 45nm CMOS technology. Design synthesis was performed using Cadence Virtuoso. Multiple configurations were created using standard configuration and a cascode differential pair. Gain is primarily dependent upon length of the transistor while bandwidth is dependent upon the width. The design utilized a active Common Mode Feedback Circuit (CMFB) that kept is stable over temperature, voltage and process variations

Keywords - Fully Differntial OTA; Virtuoso; CMFB; 45nm CMOS technology; Telescopic-cascode Operational Amplifier.

I. INTRODUCTION

The main objective of this paper is to illustrate the process for designing a fully differential Operational Transconductance Amplifier (OTA). The process includes the process to create direct current (d. c.), analog current (a. c.), transient and noise simulations to fully characterize the given circuit design. Specifications for the targeted circuit design are shown in Table 1.

Fully differential OTAs are commonly used to drive analog to digital converters (ADCs). Moreover, fully differential OTAs are commonly found in applications such as Differential AD Driver; Networking Interface Drivers; Video over twisted pair; First Stage Line Audio Amplifier; Differential line driver; Single end to differential converter; High speed differential signaling; IF/RF amplifier; and SAW filter buffer/ driver.

TABLE 1 TARGET SPECIFICATIONS

Technology	**gpdk045_RFIC**
Load Capacitance	1 pF
Supply Voltage	1.2 V
Open Loop 3dB Bandwidth	> 2πx20MHz
Closed Loop Unity Gain Bandwidth	> 2πx1GHz
Slew Rate for Positive/ Negative Slopes	> 0.5x10
0.1% Settling Time for Positive/Negative Slopes	< 5nS
Low Frequency Voltage Gain	> 60dB
Power Dissipation	< 10mW
Phase Margin	> 70
Common Mode Rejection Ratio	> 30dB
Power Supply Rejection Ratio	> 40dB
Input Noise	< 1μ
Voltage Swing	> 0.9 V

Since there are many parameters that can vary when sizing each CMOS components, the upcoming sections describes a process to size transistors and the effects such sizing affects parameters such as signal linearity and voltage gain. They show a design that targets specific given requirements and shows limitations of circuit design.

II. OTA CIRCUIT CHARACTERISTICS AND ARCHITECTURE

A. Operation of OTA

A fully differential OTA device amplifies a small differential input voltage signal to create a differential output voltage that drives other circuits. In open loop circuit configuration, a full differential amplifier gain may be as high as 70dB using low voltage operation. When comparing fully differential OTA to a single ended differential OTA, two of the most important advantages seen on a fully differential OTA is that it provides a larger output voltage swing and is less susceptible to input noise.

For purposes of this document, amplification of the input signal is made in two stages. The circuit used in the first stage amplification is designed to minimize the effects of d. c. noise common on the input signal. This noise is amplified but the amplification ratio between the amplified input signal with respect to the amplified noise signal is large. The common mode rejection ratio (CMRR) is achieved by using a common- source p-channel CMOS telescopic-cascode operational amplifier. The second stage of amplification is obtained with a common-source n-channel CMOS amplifier. Both stages of amplification use active loads realized with CMOS transistors operating in the saturation region.

B. Operation of OTA First Stage

Fig. 1 shows a common-source p-channel CMOS telescopic-cascode operational amplifier. Small signal differential input signals vin(+) and vin(-) are connected to both common source amplifiers Q1 and Q2. Inverted output for the first stage amplifier vo1 and vo2 are connected to active loads Q4 and Q3 respectively. The reference current to the circuit is controlled by Q5 which also contributes to set the d.c. bias voltage for the input signal.

The first stage amplifier has a stereoscopic configuration of two common source amplifiers which mirror their electrical and physical parameters. One amplifier leg is formed by Q1, Q3 and Q5, while the other amplifier leg is formed by Q2, Q4 and Q5. As a result, d.c. current for both amplifiers is shared equally through Q5 as long as the intrinsic transistor parameters of width (W) and Length (L) are mirrored.

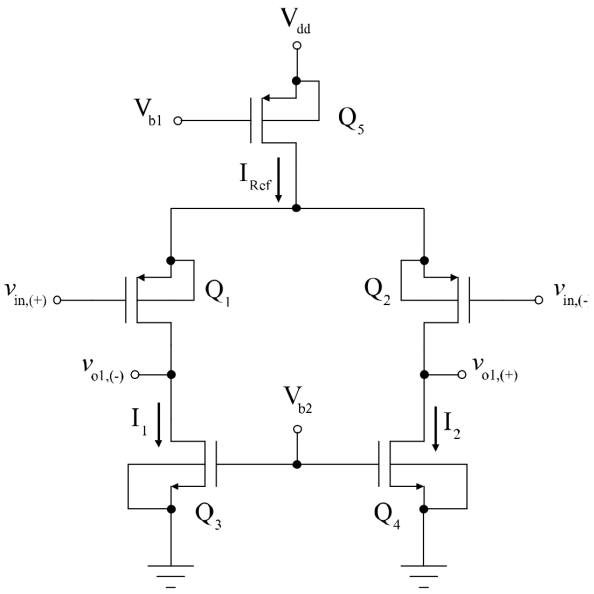


Figure 1. First Stage of OTA

To obtain maximum linear amplification, all transistors must operate in the active region. As a result, the absolute voltage drop between the drain and source of each transistor must be greater than the effective voltage (v_{eff}) of the transistor. This voltage drop is known as over-voltage (v_{ov}). The effective voltage (v_{eff}) of the transistor is defined as the absolute voltage drop value between the transistor's gate and source less the transistor's threshold voltage (v_{th}) which is dependent on MOS technology as well as physical properties of the device. The threshold voltage is the minimum voltage a transistor is required to have before current can be measured between the drain and source of same transistor.

There are two concerns when selecting the correct biasing of the first stage amplifier. The first concern is not allow any of the transistors become cut off when the input signal varies the d. c. bias voltage below a voltage less than the threshold voltage of transistors Q1 and Q2.The second concern is to minimize the amplification distortion of the amplifier by making sure that the bias voltage of either common source amplifiers Q1 and Q2 operate in the transistor's transconductance gain (g_m) linear region.

Transistors Q1 and Q2 which act as common emitter amplifiers need to be biased and sized to allow maximum transconductance gain, maximum input to output linearity or minimum signal distortion, and with

a sufficient large length to increase the bandwidth of the first stage amplifier. The voltage bias depends on the voltage between the source and gate of the PCMOS transistor.

C. Second stage of OTA

The second stage amplifier has two active components:

(1) The common emitter NMOS transistor which acts as the active amplifier; and

(2) The active load realized with a PMOS transistor.

As mentioned in the previous section, one of the most critical parameters of the transistor is to maintain maximum gain while preserving its maximum linearity. The gain of a transistor is affected by the size of the intrinsic semiconductor length (L) and with (W). When a transistor is connected in the diode mode and the output voltage is varied as well as the width and length, the maximum bias voltage for the NMOS transistor can be found for all possible sizes of W and L.

It was assumed that maintaining maximum linearity was needed. Increasing the length parameter of the transistor increases the bandwidth of operation of the amplifier which improves in the gain linearity but lowers the voltage gain of the amplifier. Increasing too much the length parameter caused the voltage gain of the amplifier to drop.

Therefore, to achieve maximum gain, the width value must be the highest value possible, while the length value must be the smallest value possible.

III. Design Process and Selection of Parameters of OTA

There are many electrical parameters associated with transconductance amplifiers. This paper only covers a selected list of the most common parameters as used in the industry. However, the reader should be aware that other parameters such as Enable/Disable Time, Short Circuit Current, and Bias Current are parameters known to be associated with this type of amplifiers.

A. First Stage Parameters

V_{dd} = 1.2V
V_{in}= 1V
V_{b1}= 300mV
V_{b2}=300mV
W_{Q5}=3.6µm

L_{Q5}=45nm
$W_{Q1,Q2}$=1.92µm
$L_{Q1,Q2}$=45nm
$W_{Q3,Q4}$=600nm
$L_{Q3,Q4}$=45nm

B. Second Stage Parameters

V_{dd}=1.2V
V_{PMOS}=635mV
W_{PMOS}=3.6µm
L_{PMOS}=45nm
W_{NMOS}=600nm
L_{NMOS}=45nm
C_C=1fF
C_L=1pF

C. Setting up the test bench.

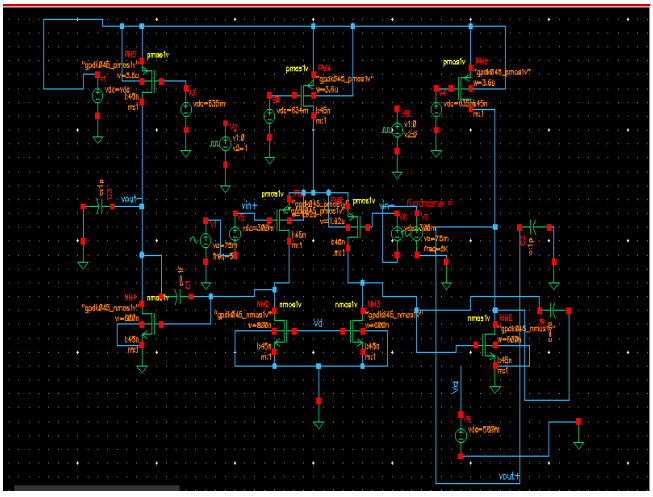


Figure 2. Schematic of the Circuit in Cadence

IV. RESULTS OF SIMULATION

A. Voltage Swing

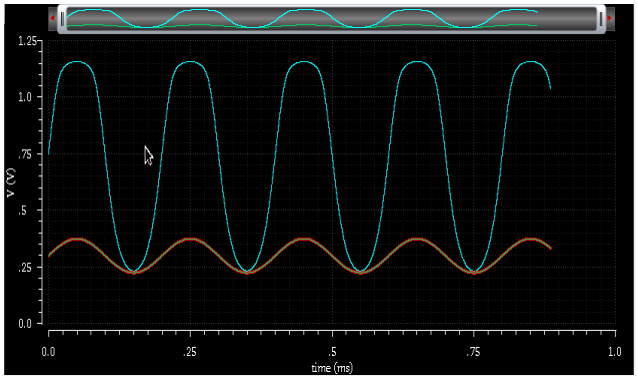


Figure 3. Voltage Swing

Voltage swing is the peak to peak voltage values. The voltage swing observed was 926mV.

B. Gain of the OTA

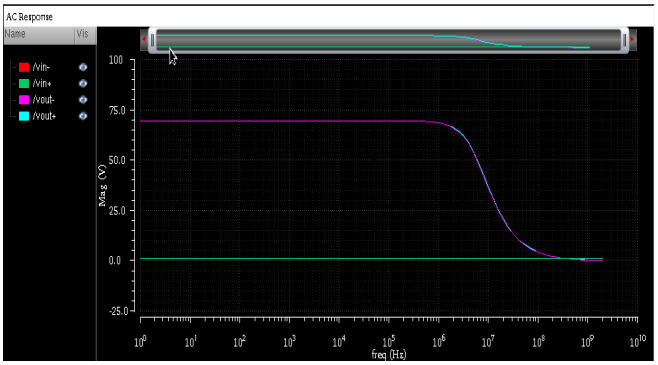


Figure 4. Gain of the OTA in dB

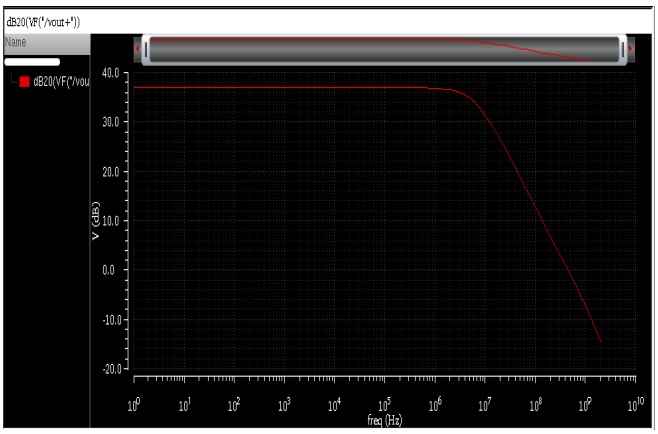


Figure 5. Gain of OTA in Voltage

The low frequency voltage gain of the design was observed to be at 36.78dB.

C. Settling Time

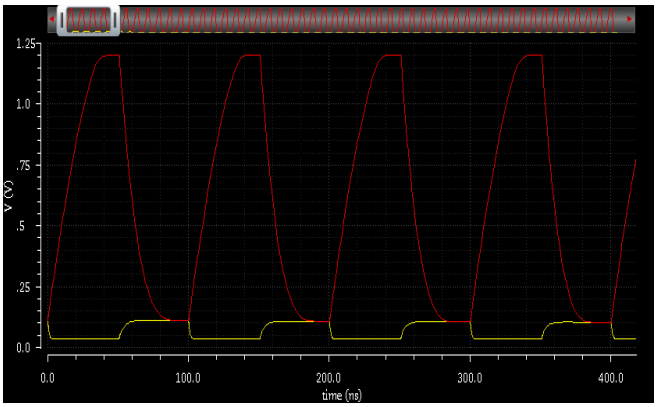


Figure 6. Settling Time

Settling time is the time taken for the voltage to reach from 0 to 99.5% of its maximum value. The rising settling time was 42.41ns and the falling settling time was 38.71ns.

D. Common Mode Rejection Ratio

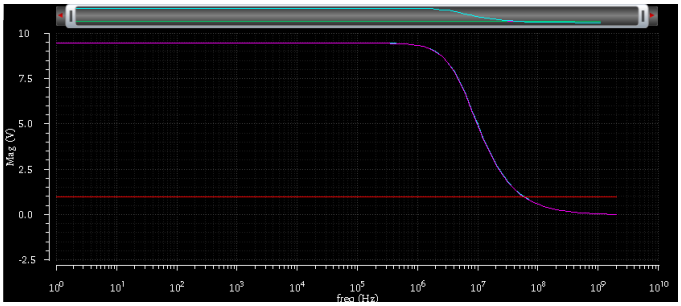


Figure 6. Common Mode Rejection Ratio

The CMRR was measured to be at 17.31dB

E. Power Supply Rejection Ratio

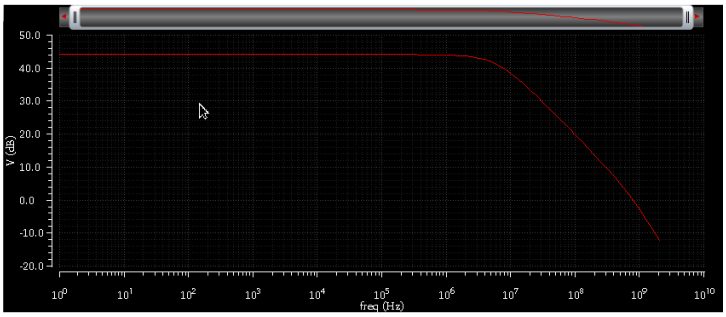


Figure 7. PSRR of OTA

The PSRR of the OTA was measured to be at 47dB.

F. Noise Analysis

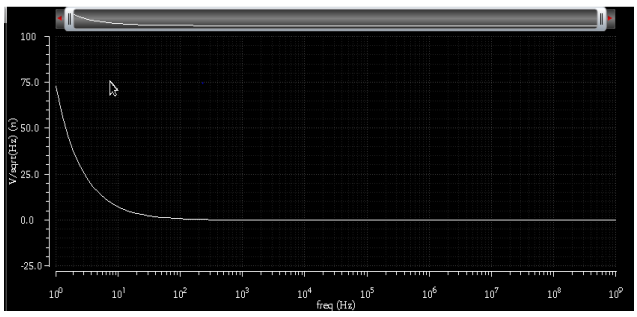


Figure 8. Noise Analysis

The input noise was measured to be at 71.2nV.

G. Phase Margin

Figure 9. Phase Margin of OTA

The phase margin was measured to be 59.54

V. Conclusion

This paper described the use of fully differential OTAs. A design process was described to achieve target specifications. It was shown that changing any given electrical parameters results in affecting the rest of the technical parameters. Therefore, a trial and error process is used to obtain the most desirable requirements. However, it was concluded that obtaining an ideal design is limited by the physical and electrical properties of the 45nm MOS technology.

VI. References

[1]. Sotoudeh Hamedhi-Hagh, Spring 2014, Class Notes.

[2]. Tony Chan Carusone, David A. Johns and Kenneth W. Martin, "ANALOG INTEGRATED CIRCUIT DESIGN," Second Edition, Ed.: WILEY, 2012

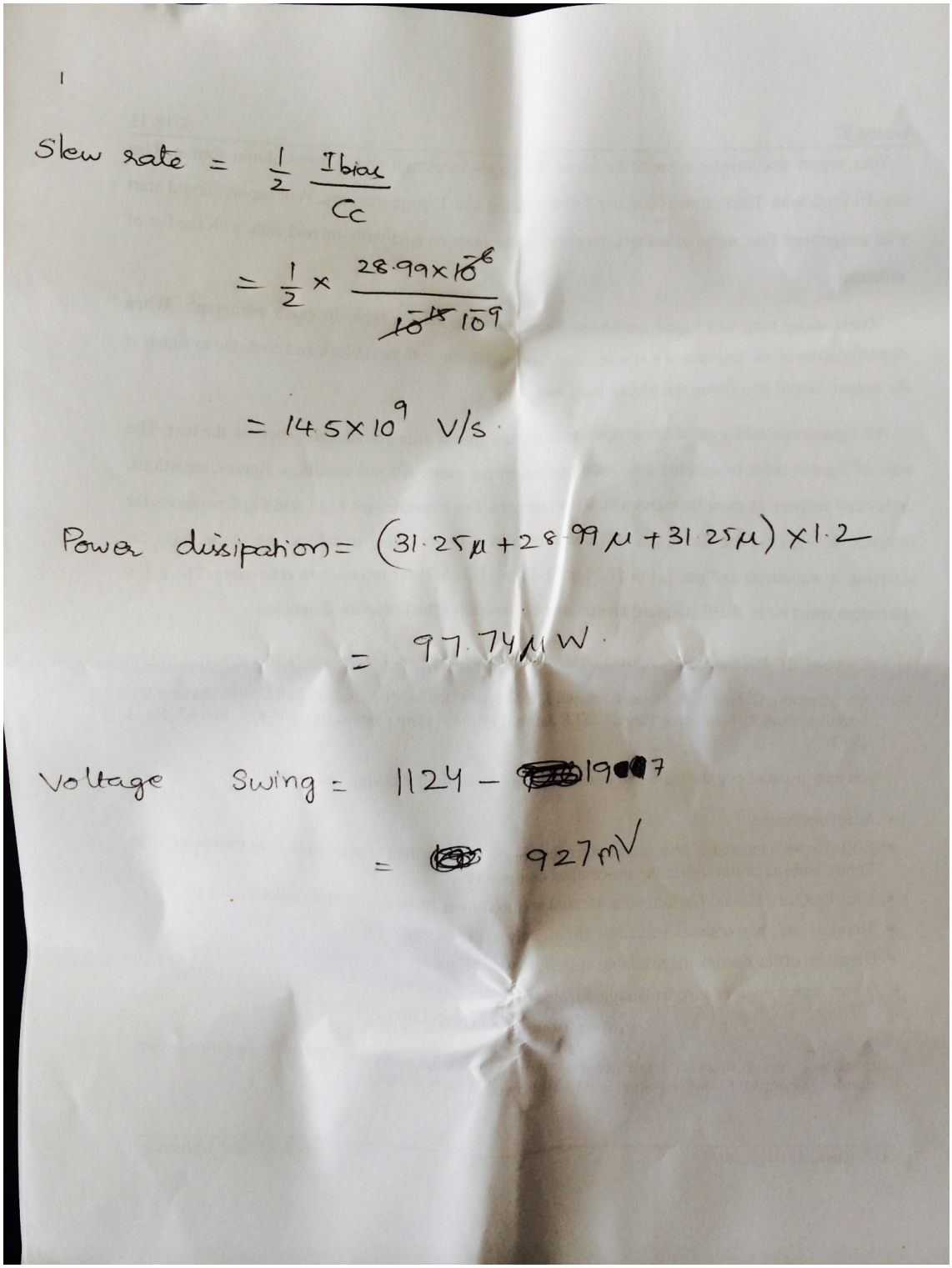
[3]. Behzad Razavi, "Design of Analog CMOS Integrated Circuits," Ed.: McGraw-Hill, 2003

TABLE 2. RESULTS OF THE SIMULATION

Technology	**gpdk045_RFIC**	**Nominal Values**
Load Capacitance	1 pF	1pF
Supply Voltage	1.2 V	1.2V
Open Loop 3dB Bandwidth	> 2πx20MHz	2πx6.22MHz
Closed Loop Unity Gain Bandwidth	> 2πx1GHz	2πx445MHz
Slew Rate for Positive/ Negative Slopes	> 0.5x10	14.5x10
0.1% Settling Time for Positive/ Negative Slopes	< 5nS	Positive = 42.41ns Negative = 38.71ns
Low Frequency Voltage Gain	> 60dB	36.78dB
Power Dissipation	< 10mW	97.25µW
Phase Margin	> 70	59.54
Common Mode Rejection Ratio	> 30dB	17.31dB
Power Supply Rejection Ratio	> 40dB	47dB
Input Noise	< 1µ	71.2075 nV
Voltage Swing	> 0.9 V	927mV

APPENDIX

HAND CALCULATIONS



1

Slew rate = $\frac{1}{2}\frac{I_{bias}}{C_c}$

$= \frac{1}{2} \times \frac{28.99 \times 10^{-6}}{10^{-9}}$

$= 14.5 \times 10^{9}$ V/s

Power dissipation = $(31.25\mu + 28.99\mu + 31.25\mu) \times 1.2$

$= 97.74\mu W$

Voltage Swing = $1124 - [illegible]$

$= [illegible]\ 927mV$