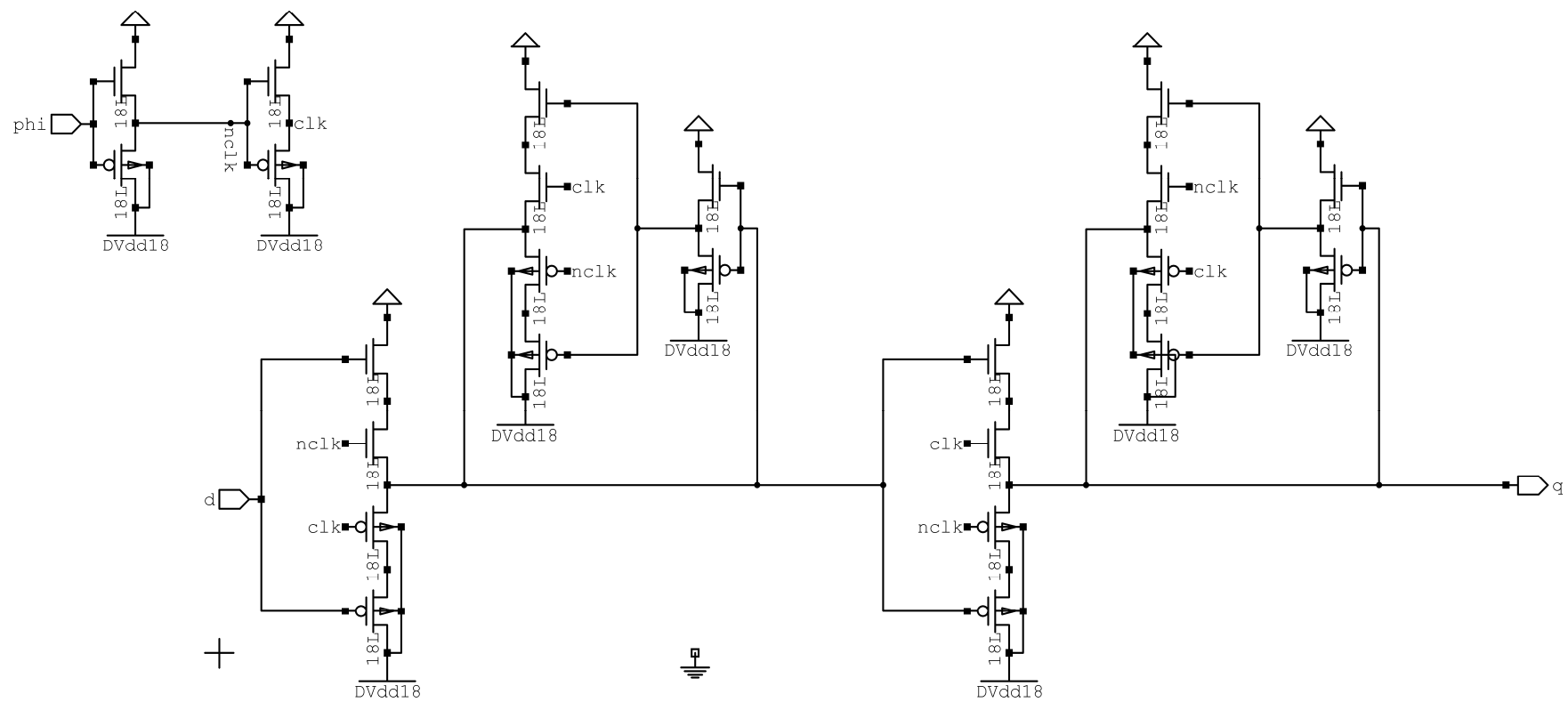
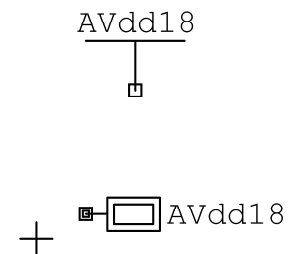
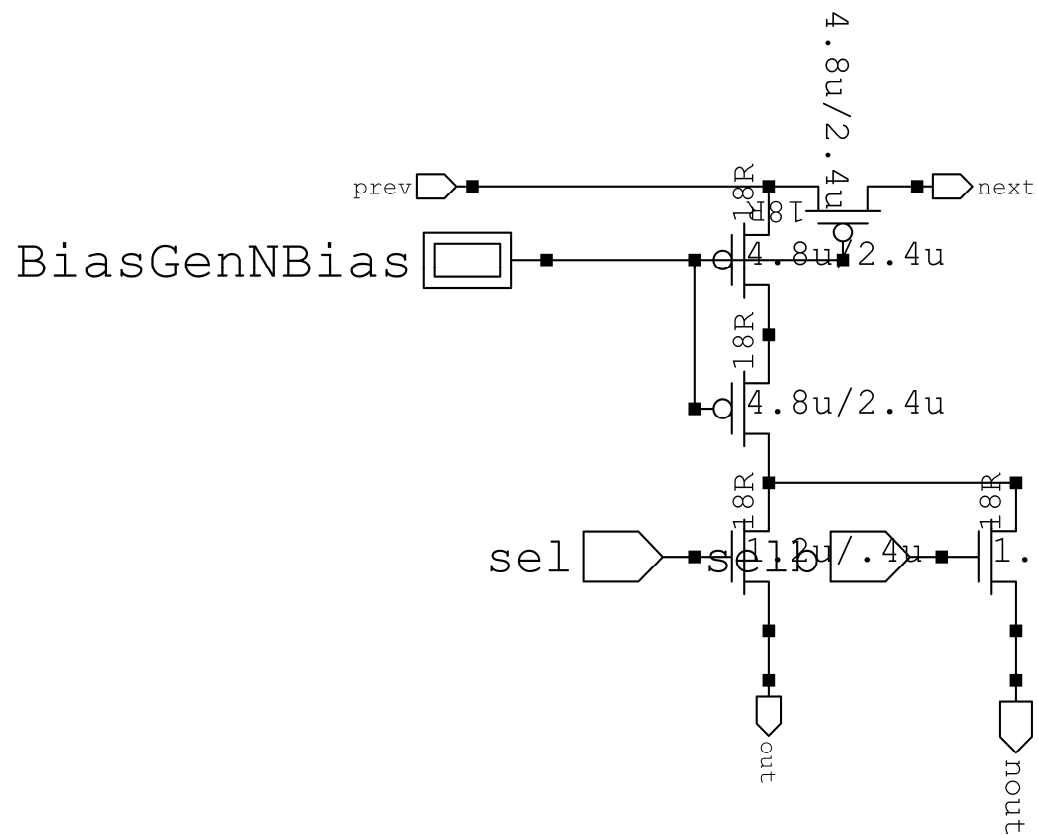
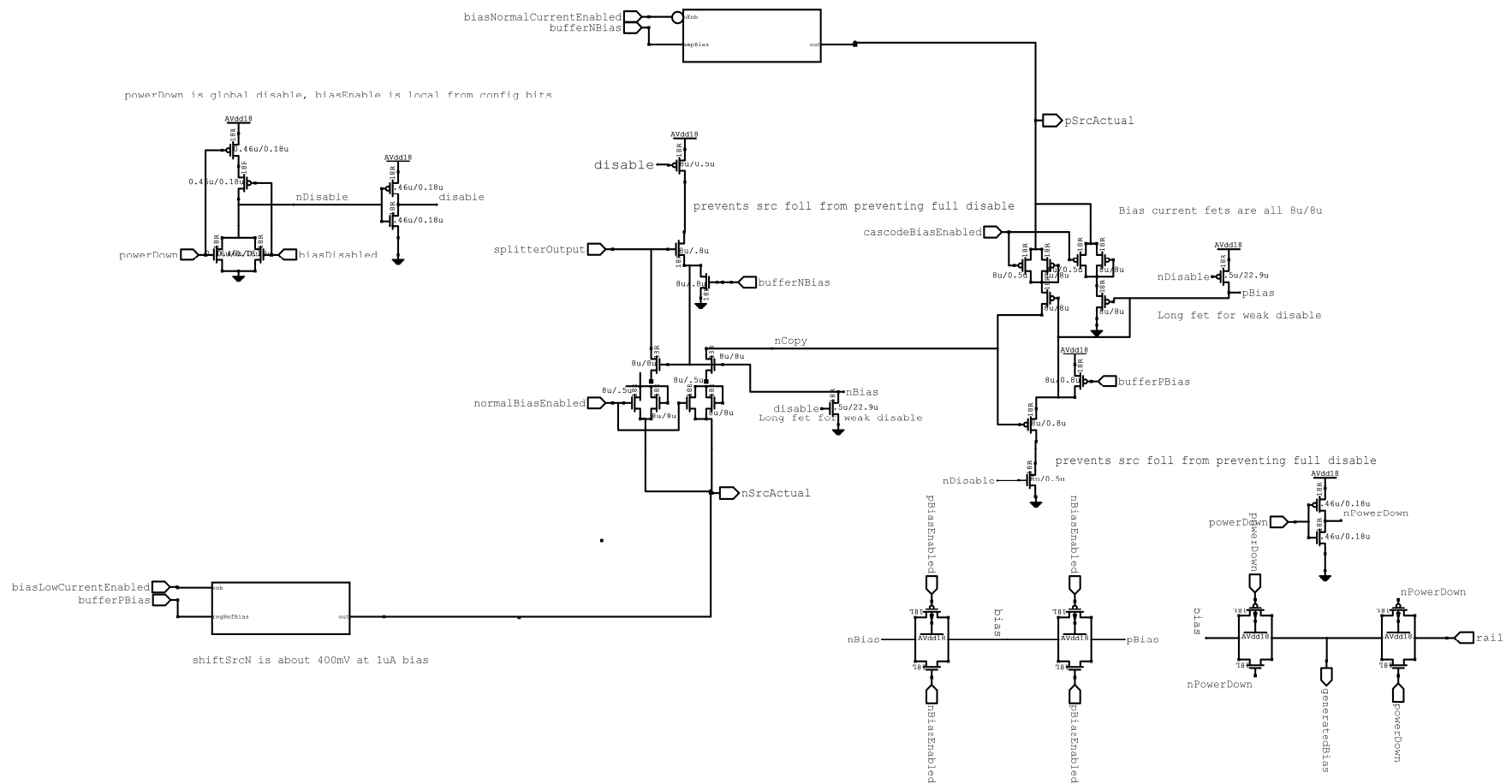


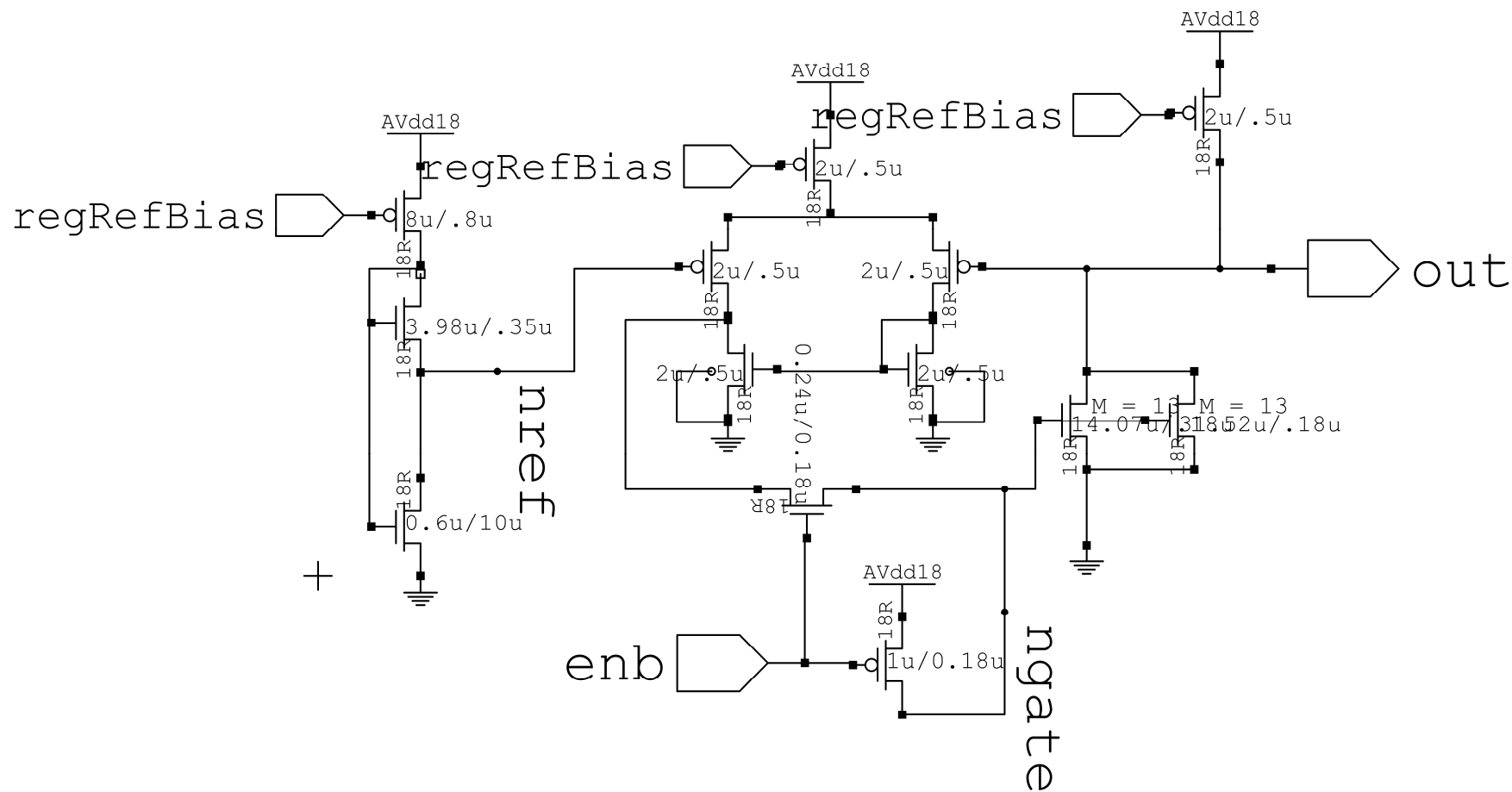
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	Modified = 8/6/2008 12:54:59 AM
Info - a level sensitive latch for storing the biasShiftRegister outputs	
Author = tobi	
File = DVS320Biasgen	

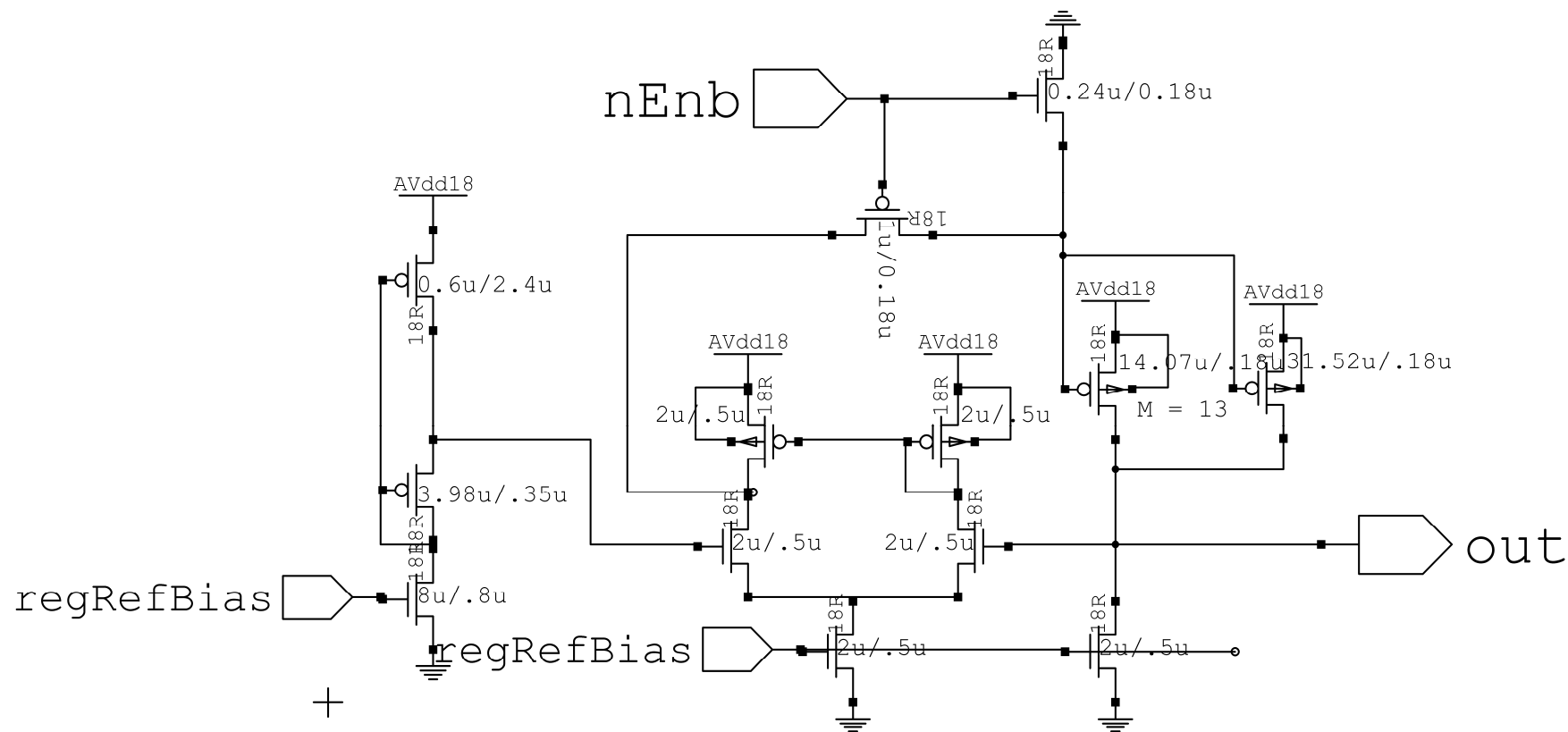


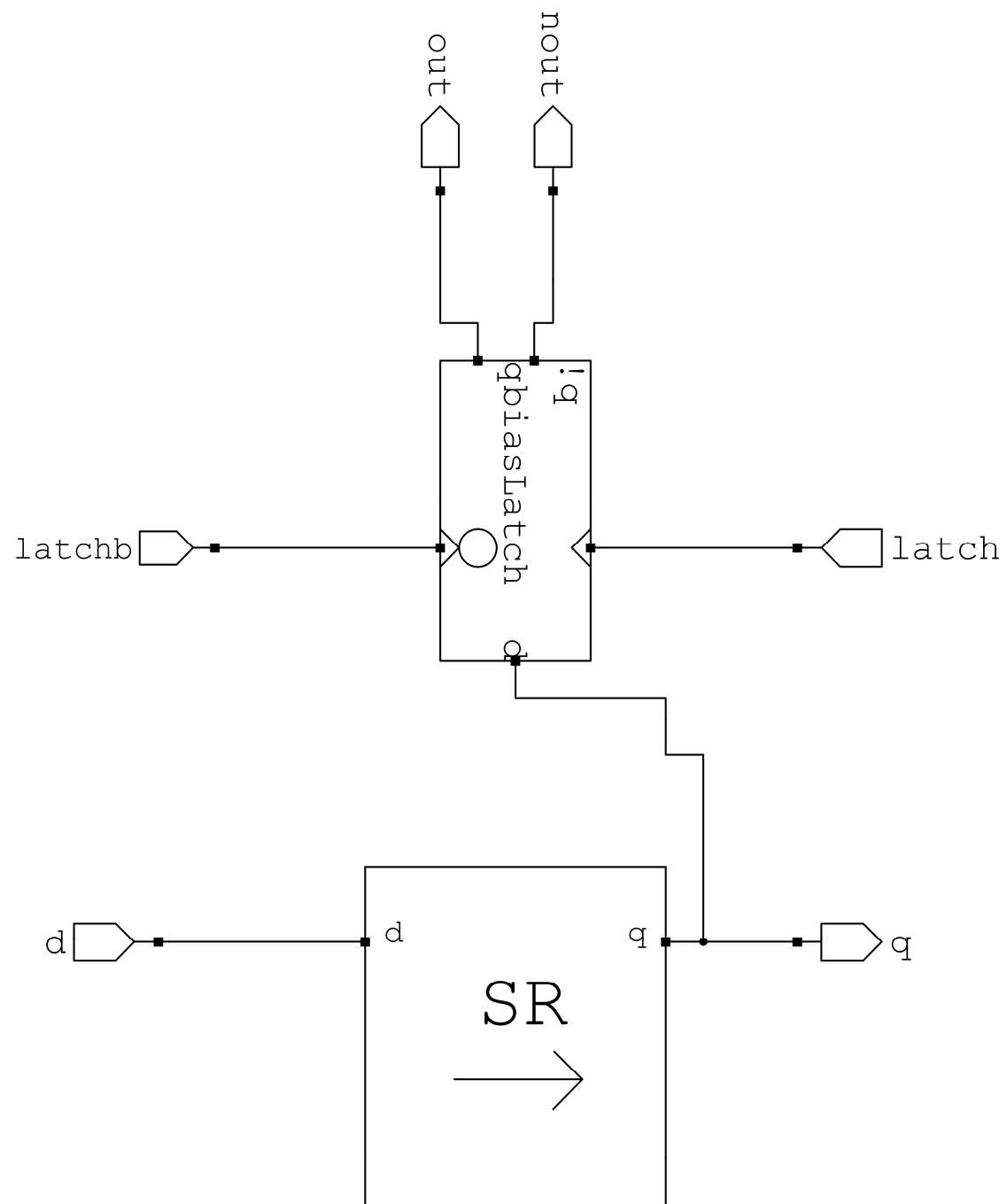


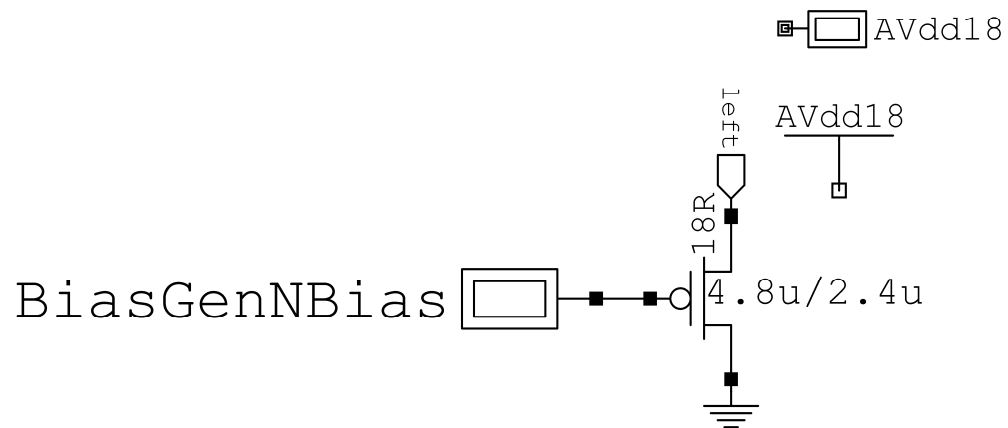
Module = biasSplitter08save	Created = 1998 10 19 15 39 21
	Modified = 8/8/2008 7:33:00 P
Info = one cell of psuedo-resistive R/2R divider	
Author = tobi/andre von shaik	
File = DVS320Biasgen	











Module = biasSplitterOctave	Created = 1998 10 19 15:39:21
Info = last cell of divider, R/R only	Modified = 8/6/2008 12:54:59
Author = tobi/andre von shaik	
File = DVS320Biasgen	