



天钰科技股份有限公司

*Fitipower Integrated Technology Inc.*

# JD9161Z

## Data Sheet

480RGB x 960(Max:1334) dot, 16.7M color,  
without internal GRAM, a-Si TFT LCD Single Chip Driver

Version 0.01  
2018/8/3

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## 1. Revision History

## 2. General Description

The JD9161Z supports WVGA resolution driving controller. The JD9161Z is designed to provide a single-chip solution that combines a source driver, gate driver control, power supply circuit to drive a-Si TFT dot matrix LCD with 480RGBx960 dots.

The JD9161Z can be operated in low-voltage condition for the interface and integrated internal boosters that produce the liquid crystal voltage and the voltage follower circuit for liquid crystal driver. In addition, The JD9161Z also supports various driving functions to reduce the power consumption of a LCD system via software control.

The JD9161Z is suitable for any small portable battery-driven and long-term driving products, such as handheld PDAs, digital cellular phones and bi-directional pagers.

### 3. Features

#### 3.1. Display

- Single chip solution for a WVGA a-Si type LCD display
- Resolution:
  - 480RGB x LN\*2(Max:1334)
  - 360RGB x LN\*2(Max:1000)
- Display color modes
  - Full color mode:
    - 16.7M colors (24-bit 8(R):8(G):8(B))
  - Reduce color mode:
    - 262k colors (18-bit 6(R):6(G):6(B))
    - 65k colors (16-bit 5(R):6(G):5(B))
    - 8 colors (Idle mode on): 8 colors (3-bit binary mode)

#### 3.2. Display interface

- Display interface types supported
  - MIPI-DSI (Display Serial Interface) interface
    - Support DSI Version 1.1
    - Support D-PHY version 1.00

#### 3.3. Input voltage ranges

- I/O and interface power supply (IOVCC): 1.65V to 3.3V
- High speed interface power supply (VCCH): 1.65V to 3.3V
- Analog power supply (VCI): 2.5V to 3.3V
- DC/DC set-up supply (VCIP): 2.5V to 3.3V
- OTP programming voltage (VPP): 8.3V ± 0.1V

#### 3.4. Output voltage ranges

- On module DC/DC converter
  - AVDD= +4.375V to +6.6V
  - AVEE= -3.75V to -6.0V
  - Positive source output voltage level: VGMP= +3.85V to +6.5V
  - Negative source output voltage level: VGMN= -1.85V to -4.5V
  - Positive gate driver output voltage level: VGH= 7 to 18V
  - Negative gate driver output voltage level: VGL=-7V to -16V
  - VCOM = -3.3V ~ 0V

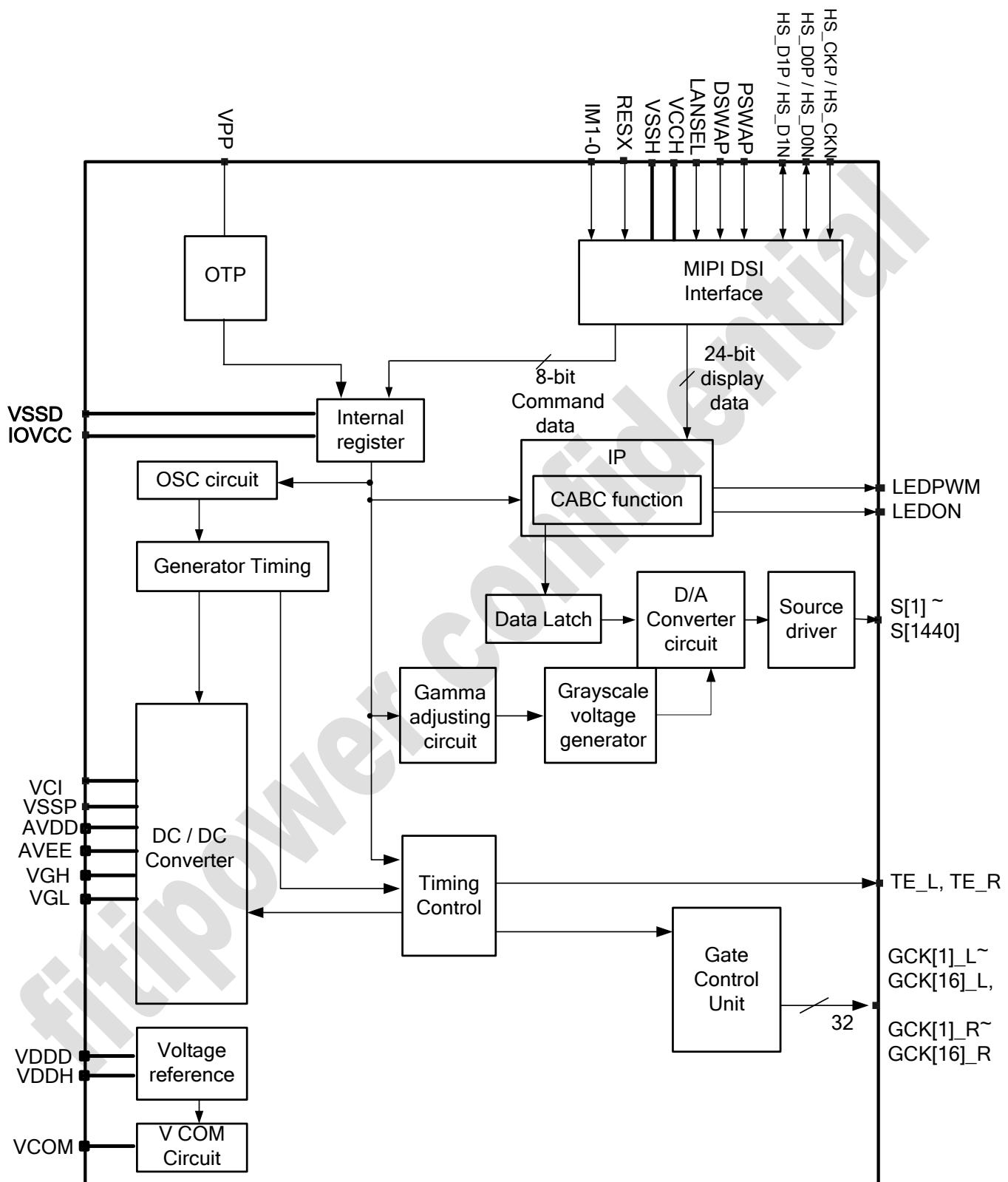
### 3.5. Miscellaneous of chip

- Internal level shifter for Gate Driver control
- Supports column / 1-dot / 1+2-dot / 2-dot / 4-dot inversion
- Gamma correction (1 preset gamma curve)
- Internal Oscillator generation
- CMOS compatible inputs
- Proprietary multi phase driving for lower power consumption
- GAS function for preventing image sticking when abnormal power off
- Temperature range: -40 to +85 °C
- On-chip OTP program voltage generator
- OTP memory to store initialization register settings
- Support CABC (Content Adaptive Brightness Control) function

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## 4. Device Overview

### 4.1. Device Block Diagram



#### 4.2. LCD power generation scheme

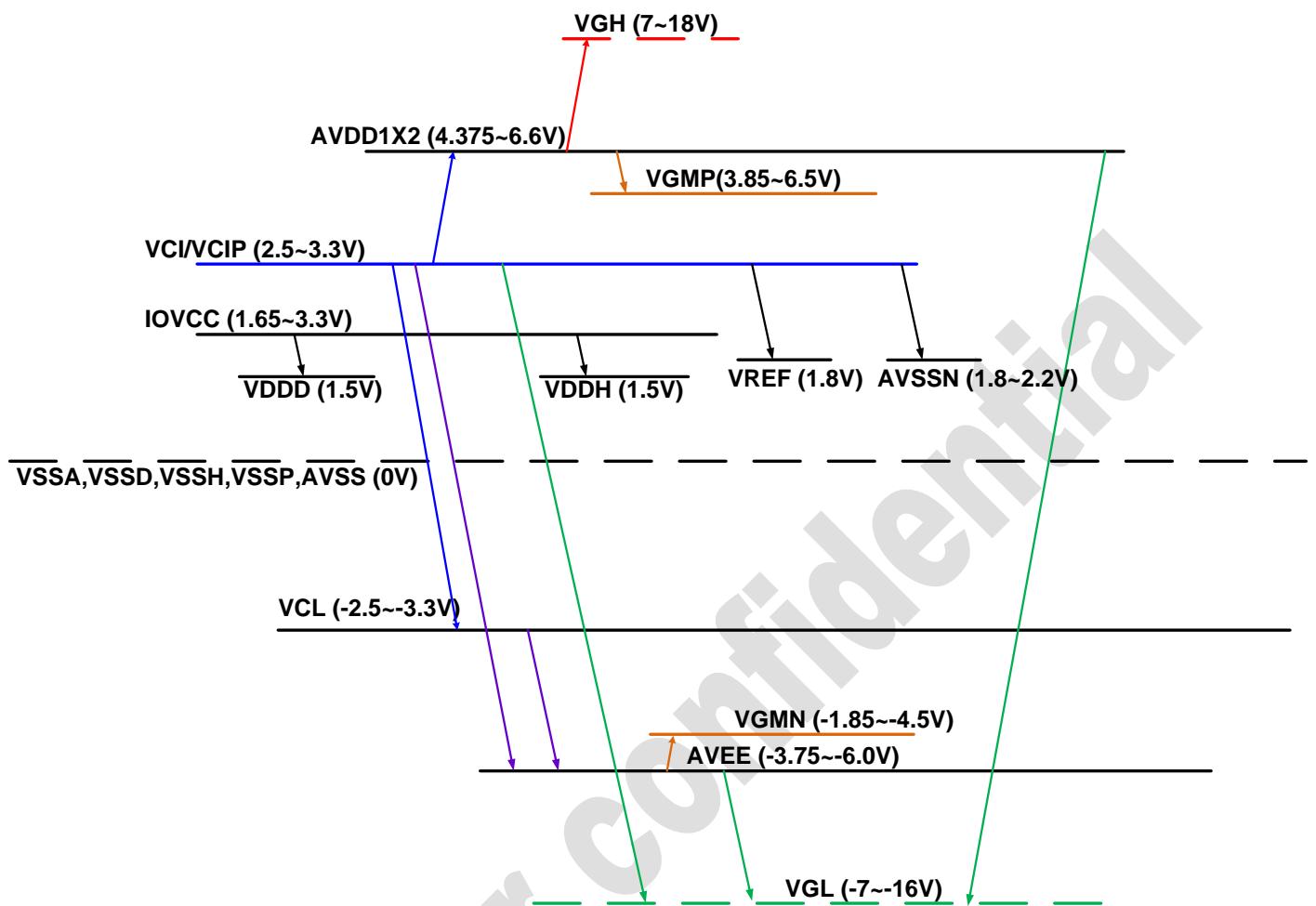


Figure 4.1: LCD power generation scheme

#### 4.3. Output voltage range

JD9161Z generates corresponding voltage with a-Si TFT LCD panel by internal power supply circuit. Please set up each voltage output according to the LCD panel.

Name	Function	Set up value	Note
AVDD	DC/DC converter circuit output	+4.375V ~ +6.6V	Do not exceed 6.6V
AVEE	DC/DC converter circuit output	-3.75V ~ -6.0V	Do not exceed -6V
VGMP	Reference voltage for gamma circuit	+3.85V ~ +6.5V	Reference register
VGMN	Reference voltage for gamma circuit	-1.85V ~ -4.5V	Reference register
VGH	Positive gate driver output voltage level	+7V ~ +18V	Depend on AVDD & AVEE
VGL	Negative gate driver output voltage level	-7V ~ -16V	Depend on AVDD & AVEE
VCOM	VCOM DC voltage	-3.3V ~ 0V	-
VDDH	Analog power for High speed interface circuit	1.5V	Depend on DSI I/F
VDDD	Digital power for internal digital circuit.	1.5V	-

Table 4.1: Voltage configuration

## 5. Maximum layout resistance

Name	Pin Definition	Maximum series resistance	Unit
IOVCC, VCCH	Power supply	5	Ω
VCI, VCIR, VCIP, VCIP2, VCIP3	Power supply	5	Ω
VSSD, VSSA, AVSS, VSSH, VSSP, VSSP2, VSSP3	Power supply	5	Ω
VPP	OTP Power supply	20	Ω
TEST_OSC, TESTP, TESTP1, TESTP2, TESTN, TESTI[3:0], TESTS[1:0]	Input	100	Ω
CSX, WRX_SCL, RESX, SDI	Input	100	Ω
LANSEL, DSWAP, PSWAP, IM[1:0], NBWSEL	Input	100	Ω
SDO, TE_L, TE_R, LEDPWM, LEDON	Output	100	Ω
HS_D0P, HS_D0N	Input + Output	6	Ω
HS_D1P, HS_D1N	Input	6	Ω
HS_CP, HS_CN	Input	6	Ω
VDDD, VDDH	Output	5	Ω
AVDD, AVEE	Output	10	Ω
VGH, VGH1_L, VGH1_R, VGH2_L, VGH2_R, VGL	Output	10	Ω
HTEST1	output	100	Ω
D_TEST_N	output	100	Ω
COGTESTA[2:1], COGTESTB[2:1], COGTESTC2[2:1], COGTESTD[2:1], COGTESTE[2:1], COGTESTF[2:1],	Input + Output	100	Ω

Table 5.1: Maximum Layout Resistance

## 6. Pin description

Host interface pins												
Pin name	I/O type	Connected with	Description									
IM1 ~ IM0	I	VSSD / IOVCC	Select the Interface mode as listed below:									
			IM1	IM0	Command	Display data						
			0	1	DSI	DSI interface						
Other setting			Not used									
Must be connected to VSSD or IOVCC.												
LANSEL	I	VSSD / IOVCC	Select number for MIPI DSI data lane.									
			LANSEL	DSI Data lane								
			0	1 Lane								
DSWAP, PSWAP	I	VSSD / IOVCC	Select for DSI data lane sequence and polarity.									
			PSWAP	DSWAP	HS_D1P	HS_D1N	HS_CP					
			0	0	D1+	D1-	CLK+					
NBWSEL	I	VSSD / IOVCC	Normal Black/ Normal White panel select. Must be connected to VSSD or IOVCC.									
			NBWSEL	Panel type								
			0	Normal White								
RESX	I	Host or reset circuit	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied (Must be connected to VSSD or IOVCC).									
LEDPWM	O	Host or LED Driver	Backlight PWM control output pin. If use CABC function, the pin can connect to external LED driver IC. The output voltage range=0 to IOVCC.									
LEDON	O	Host or LED Driver	Backlight on/off control output pin. The output voltage range=0 to IOVCC.									
Panel driver output												
S[1] ~ S[1440]	O	LCD	Output voltages applied to the liquid crystal.									
GCK[1]_L ~ GCK[16]_L	O	LCD	These pins are used for Panel control signal. If not use, let it open.									
GCK[1]_R ~ GCK[16]_R	O	LCD	These pins are used for Panel control signal. If not use, let it open.									

<b>Power supply pins</b>			
IOVCC	I	External power	A power supply for the I/O circuit. IOVCC=1.65 to 3.3V
VCI	I	External power	A power supply for DC/DC circuit. VCI=2.5V to 3.3V VCI input level should be same as VCIP input level to avoid the level-mismatching at internal level shifter circuit.
VCIP/ VCIP2/ VCIP3	I	External power	A power supply for DC/DC circuit. VCIP=2.5V to 3.3V VCIP input level should be same as VCI input level to avoid the level-mismatching at internal level shifter circuit.
AVSS	P	System ground	Analog ground. AVSS=0V. When using the COG method, connect to VSSD on the FPC to prevent noise.
VSSA	P	System ground	Analog ground. Must connect to AVSS on the FPC.
VSSD	P	System ground	Ground for the internal logic. VSSD=0V. When using the COG method, connect to AVSS on the FPC to prevent noise.
VSSP/ VSSP2/ VSSP3	P	System ground	Ground for the DC/DC circuit. VSSP=0V. When using the COG method, connect to AVSS on the FPC to prevent noise.
VPP	I	External power or Open	External high voltage pin used in OTP mode and operates at 8.3V. If not used, let it open.
AVDD	O	Internal power	Analog positive power.
AVEE	O	Internal power	Analog negative power.
VGH/VGH1_L/VGH1_R/ VGH2_L/VGH2_R	O	Internal power	Output voltage from the step-up circuit.
VGL	O	Internal power	Output voltage from the step-up circuit.
VDDD	O	Internal power	Internal logic voltage output
VCOM	O	Internal power	The power supply of common voltage in DC com driving.
<b>High speed interface parts</b>			
HS_D0P, HS_D0N	I/O	DSI Host	MIPI-DSI Data differential signal input pins. (Data lane 0) if not used , Please connected to VSSH or .open
HS_CP, HSI_CN	I	DSI Host	MIPI-DSI CLOCK differential signal input pins. if not used , Please connected to VSSH or open.
HS_D1P, HS_D1N	I/O	DSI Host	MIPI-DSI Data differential signal input pins. (Data lane 1) If not used , Please connected to VSSH or open.
VCCH	I/O	Internal power	Power supply for the MIPI DSI analog power. VCCH=1.65 to 3.3V

VSSH	P	System ground	MIPI DSI analogy ground. VSSH=0V. When using the COG method, connect to AVSS on the FPC to prevent noise.
VDDH	O	Internal power	DSI I/F: DSI regulator output pin. (1.5V) Connect to a stabilizing capacitor between VDDH and VSSH If not used, please open these pins.
<b>Other Pins</b>			
TEST_OSC	I	Open	A test pin. This pin is by internal logic function test. This pin can output on FPC. If not used, let it open or connected to VSSD.(weak pull low)
TESTI[3:0]	I	Open	A test pin. This pin is by internal logic function test. This pin can output on FPC. If not used, let it open
TESTS[1:0]	I	Open	A test pin. This pin is by internal logic function test. This pin can output on FPC. If not used, let it open
TEST_P / TEST_P1/ TEST_P2	O	Open	A test pin. Disconnect it. This pin will output Gamma voltage. This pin can output on FPC.
TEST_N	O	Open	A test pin. Disconnect it. This pin will output Gamma voltage. This pin can output on FPC.
D_TEST_N	O	Open	A test pin. Disconnect it. This pin will output Gamma voltage. This pin can output on FPC.
HTEST1	O	Open	A test pin. Disconnect it. This pin will output Gamma voltage. This pin can output on FPC.
DUMMY	-	Open	Not used. Let it open.
COGTESTA[1:2]	-	Open	Test pin for bonding resistance measurement. COGTESTA1 and COGTESTA2 are short in IC inside.
COGTESTB[1:2]	I	Open	Test pin for bonding resistance measurement. COGTESTB1 and COGTESTB2 are short in IC inside.
COGTESTC[1:2]	-	Open	Test pin for bonding resistance measurement. COGTESTC1 and COGTESTC2 are short in IC inside.
COGTESTD[1:2]	I	Open	Test pin for bonding resistance measurement. COGTESTD1 and COGTESTD2 are short in IC inside.
COGTESTE[1:2]	I	Open	Test pin for bonding resistance measurement. COGTESTE1 and COGTESTE2 are short in IC inside.
COGTESTF[1:2]	I	Open	Test pin for bonding resistance measurement. COGTESTF1 and COGTESTF2 are short in IC inside.

## 7. Interface

The JD9161Z supports DSI (Display Serial Interface). The IM1-0 pins setting are fixed as “01”.

### 7.1. DSI system interface

The Display Serial Interface (DSI) specifies the interface between a host processor and a peripheral. DSI builds on existing MIPI Alliance specifications by adopting pixel formats and command set specified in DCS standards.

Figure 7.16 shows a simplified DSI interface. DSI sends display data or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that, in traditional or legacy interfaces, are normally conveyed to and from the peripheral on a parallel data bus with additional control signals.

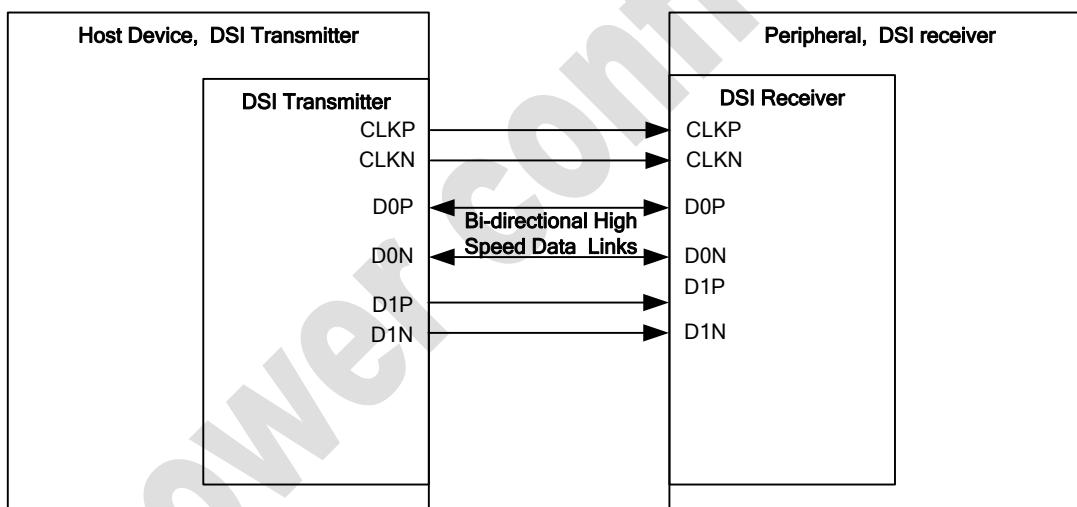


Figure 7.1: DSI transmitter and receiver interface

A conceptual view of DSI organizes the interface into several functional layers. A description of the layers follows and is also shown in Figure 7.17.

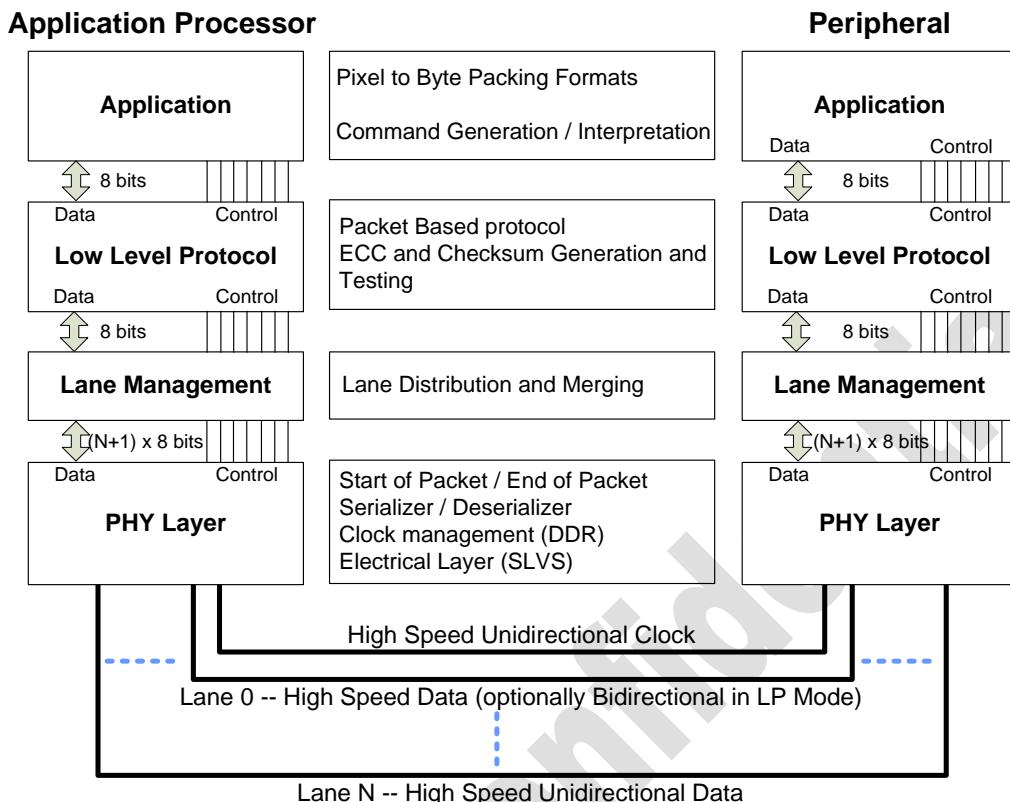


Figure 7.2: DSI Layer

**PHY Layer:** The PHY Layer specifies transmission medium (electrical conductors), the input/output circuitry and the clocking mechanism that captures “ones” and “zeroes” from the serial bit stream. Bit-level and byte-level synchronization mechanisms are included as part of the PHY.

**Lane Management Layer:** DSI is Lane-scalable for increased performance. The number of data signals may be 1 or 2 depending on the bandwidth requirements of the application. The transmitter side of the interface distributes the outgoing data stream to one or more Lanes (“distributor” function). On the receiving end, the interface collects bytes from the Lanes and merges them together into a recombined data stream that restores the original stream sequence (“merger” function).

**Protocol Layer:** At the lowest level, DSI protocol specifies the sequence and value of bits and bytes traversing the interface. It specifies how bytes are organized into defined groups called packets. The protocol defines required headers for each packet, and how header information is generated and interpreted. The transmitting side of the interface appends header and error-checking information to data being transmitted. On the receiving side, the header is stripped off and interpreted by corresponding logic in the receiver. Error-checking information may be used to test the integrity of

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incoming data. DSI protocol also documents how packets may be tagged for interleaving multiple command or data streams to separate destinations using a single DSI.

**Application Layer:** This layer describes higher-level encoding and interpretation of data contained in the data stream. Depending on the display subsystem architecture, it may consist of pixels having a prescribed format, or of commands that are interpreted by the display controller inside a display module. The DSI specification describes the mapping of pixel values, commands and command parameters to bytes in the packet assembly.

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### 7.1.1. Command mode, Video mode and Virtual Channel

DSI-compliant peripheral support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral.

Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

#### **Command Mode**

Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface.

#### **Video Mode**

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode.

Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

#### **Virtual Channel Capability**

While this specification only addresses the connection of a host processor to a single peripheral, DSI incorporates a virtual channel capability for communication between a host processor and multiple, physical display modules. Since interface bandwidth is

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shared between peripherals, there are constraints that limit the physical extent and performance of multiple-peripheral systems. The DSI protocol permits up to four virtual channels, enabling traffic for multiple peripherals to share a common DSI Link. The DSI specification makes no requirements on the specific value assigned to each virtual channel used to designate interlaced fields. For clarity, the first interlaced video field may be assigned as DI[7:6] = 2'b00 and the second interlaced video field may be assigned DI[7:6] = 2'b01.

Note1: JD9161Z support video mode.

Note2: For JD9161, DI[7:6] for virtual channel should be set as 2'b00.

### 7.1.2. Power-up Sequence Example

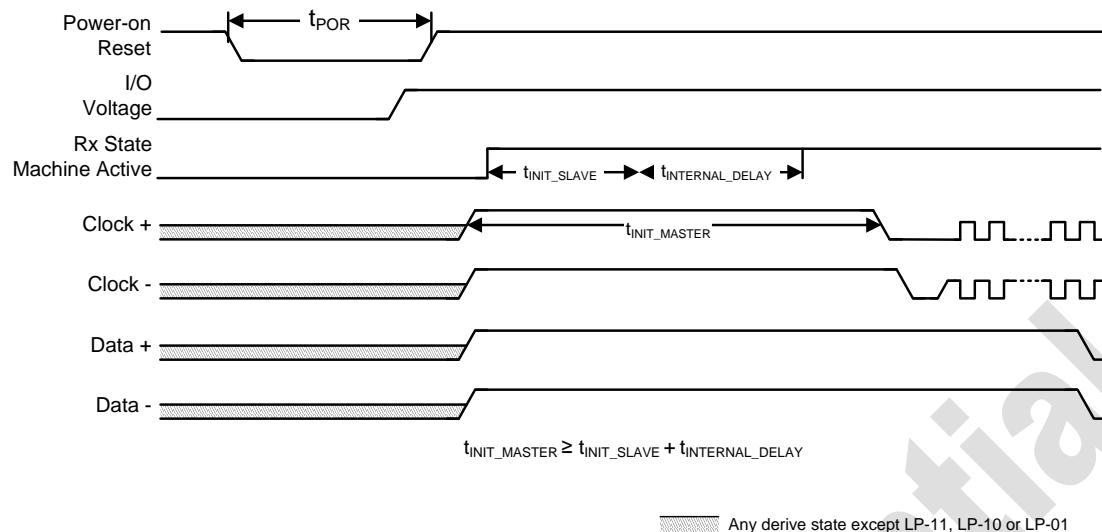
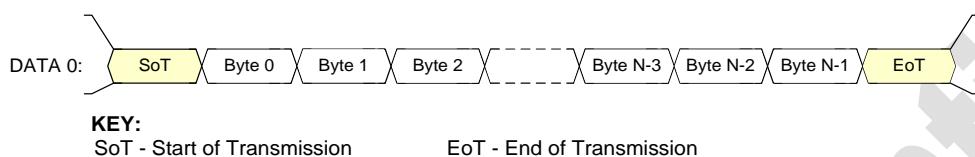


Figure 7.3: Peripheral Power-Up Sequencing Example

### 7.1.3. DSI Format

Information is transferred between host processor and peripheral using one or more serial data signals and accompanying serial clock. The action of sending high-speed serial data across the bus is called a HS transmission or burst. Between transmissions, the differential data signal or Lane goes to a low-power state (LPS). Interfaces should be in LPS when they are not actively transmitting or receiving high-speed data. Figure 7.19 shows the basic structure of a HS transmission. N is the total number of bytes sent in the transmission



**Figure 7.4: Basic HS Transmission Structure**

### Multi Lane Distribution and Merging

DSI is a Lane-scalable interface. Applications requiring more bandwidth than that provided by one Data Lane may expand the data path to two, three, or four Lanes wide and obtain approximately linear increases in peak bus bandwidth.

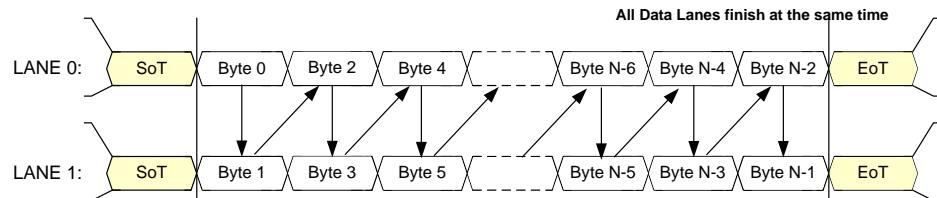
Multi-Lane implementations shall use a single common clock signal, shared by all Data Lanes. Conceptually, between the PHY and higher functional blocks is a layer that enables multi-Lane operation.

Since a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of Lanes, some Lanes may run out of data before others. Therefore, the Lane Management layer, as it buffers up the final set of less-than-N bytes, de-asserts its “valid data” signal into all Lanes for which there is no further data.

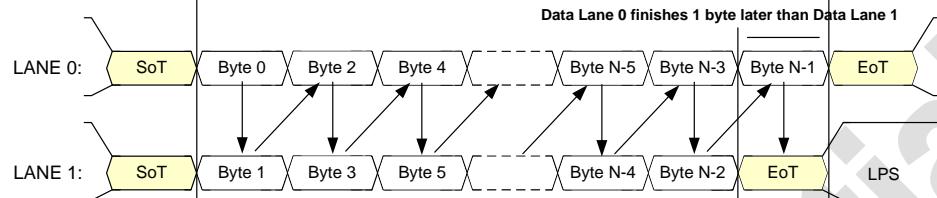
Although all Lanes start simultaneously with parallel SoTs, each Lane operates independently and may complete the HS transmission before the other Lanes, sending an EoT one cycle (byte) earlier.

The N PHYs on the receiving end of the Link collect bytes in parallel and feed them into the Lane Management layer. The Lane Management layer reconstructs the original sequence of bytes in the transmission. Figure 7.20 & 7.21 illustrate a variety of ways a HS transmission can terminate for different number of Lanes and packet lengths.

Number of Bytes, N transmitted is an integer multiple of the number of lanes:



Number of Bytes, N transmitted is NOT an integer multiple of the number of lanes:



**KEY:**

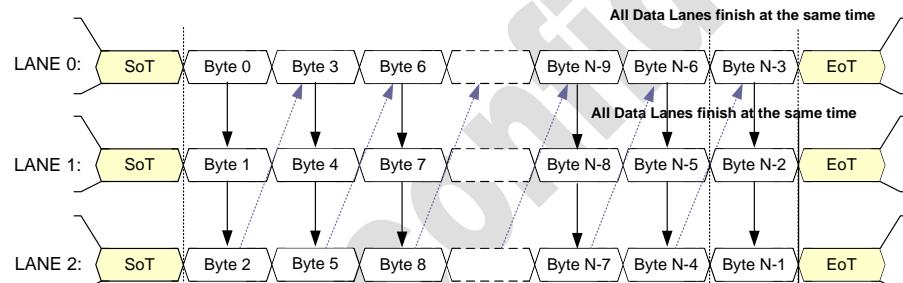
LPS - Low Power State

SoT - Start of Transmission

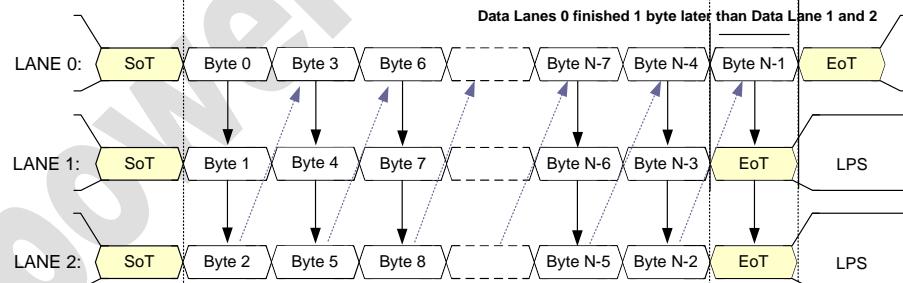
EoT - End of Transmission

**Figure 7.5: Two Lane HS Transmission Example**

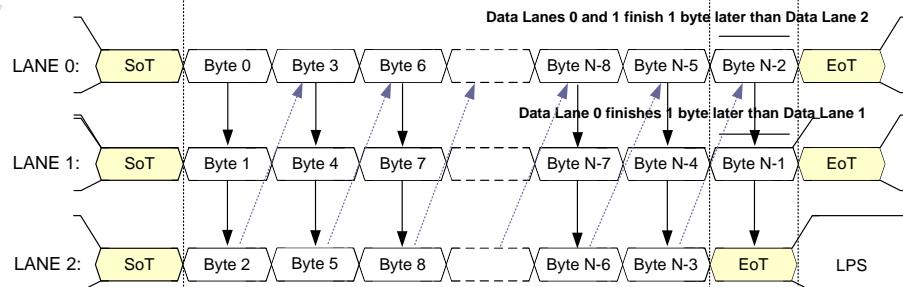
Number of Bytes, N transmitted is an integer multiple of the number of lanes:



Number of Bytes, N transmitted is NOT an integer multiple of the number of lanes (Example 1):



Number of Bytes, N transmitted is NOT an integer multiple of the number of lanes (Example 2):



**KEY:**

LPS - Low Power State

SoT - Start of Transmission

EoT - End of Transmission

**Figure 7.6: Three Lane HS Transmission Example**

## 7.1.4. DSI Protocol

On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted in the Protocol layer to packets, following the packet organization documented in this section. The Protocol layer appends packet-protocol information and headers, and then sends complete bytes through the Lane Management layer to the PHY.

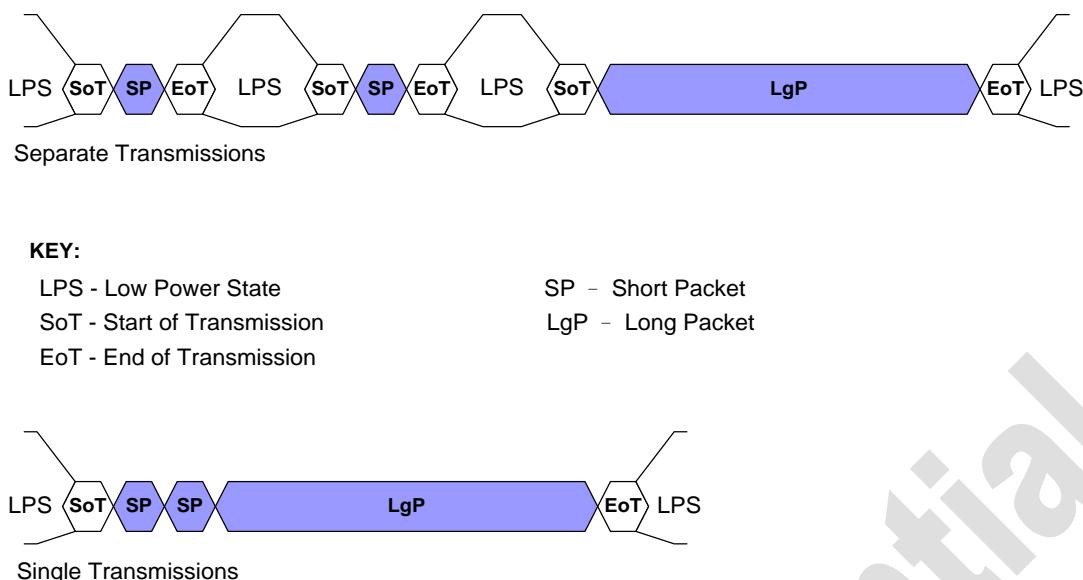
### 7.1.4.1. Multiple Packets per Transmission

In its simplest form, a transmission may contain one packet. If many packets are to be transmitted, the overhead of frequent switching between LPS and High-Speed Mode will severely limit bandwidth if packets are sent separately, e.g. one packet per transmission.

The DSI protocol permits multiple packets to be concatenated, which substantially boosts effective bandwidth. This is useful for events such as peripheral initialization, where many registers may be loaded with separate write commands at system startup.

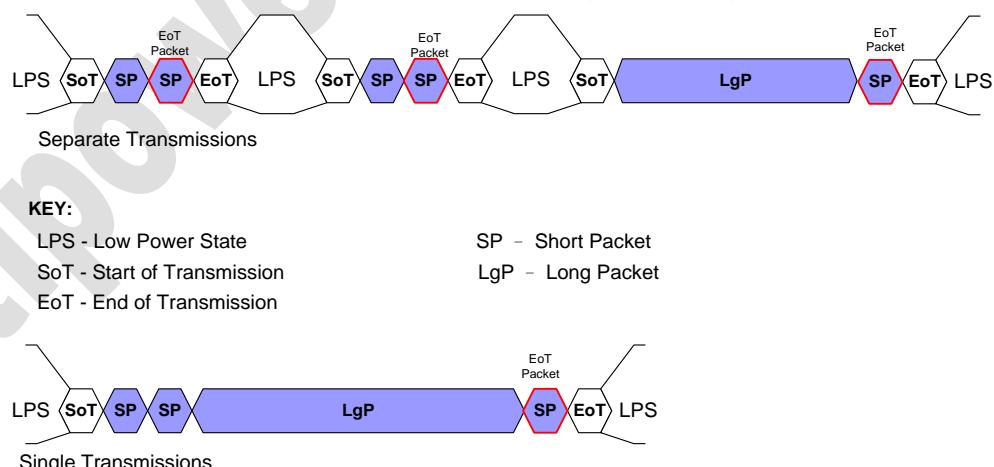
There are two modes of data transmission, HS and LP transmission modes, at the PHY layer. Before a HS transmission can be started, the transmitter PHY issues a SoT sequence to the receiver. After that, data or command packets can be transmitted in HS mode. Multiple packets may exist within a single HS transmission and the end of transmission is always signaled at the PHY layer using a dedicated EoT sequence. In order to enhance the overall robustness of the system, DSI defines a dedicated EoT packet (EoTp) at the protocol layer for signaling the end of HS transmission. For backwards compatibility with earlier DSI systems, the capability of generating and interpreting this EoTp can be enabled or disabled. The method of enabling or disabling this capability is out of scope for this document.

The top diagram in Figure 7.22 illustrates a case where multiple packets are being sent separately with EoTp support disabled. In HS mode, time gaps between packets shall result in separate HS transmissions for each packet, with a SoT, LPS, and EoT issued by the PHY layer between packets. This constraint does not apply to LP transmissions. The bottom diagram in Figure 7.22 demonstrates a case where multiple packets are concatenated within a single HS transmission.



**Figure 7.7: HS Transmission Examples with EoTp disabled**

Figure 7.23 depicts HS transmission cases where EoTp generation is enabled. In the figure, EoT short packets are highlighted in red. The top diagram illustrates a case where a host is intending to send a short packet followed by a long packet using two separate transmissions. In this case, an additional EoT short packet is generated before each transmission ends. This mechanism provides a more robust environment, at the expense of increased overhead (four extra bytes per transmission) compared to cases where EoTp generation is disabled, i.e. the system only relies on the PHY layer EoT sequence for signaling the end of HS transmission. The overhead imposed by enabling EoTp can be minimized by sending multiple long and short packets within a single transmission as illustrated by the bottom diagram in Figure 7.23.



**Figure 7.8: HS Transmission Examples with EoTp enabled**

#### **7.1.4.2. Endian Policy**

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified. Figure 7.24 shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

**Figure 7.9: Endian Example (Long Packet)**

### 7.1.4.3. Packet Structure

The first byte of the packet, the Data Identifier (DI), includes information specifying the type of the packet. Packet sizes fall into two categories:

- **Long packets** specify the payload length using a two-byte Word Count field. Payloads may be from 0 to 216-1 bytes long. Therefore, a Long packet may be up to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data.
- **Short packets** are four bytes in length including the ECC. Short packets are used for most Command Mode commands and associated parameters. Other Short packets convey events like H Sync and V Sync edges. Because they are Short packets they can convey accurate timing information to logic at the peripheral.

The Set Maximum Return Packet Size command allows the host processor to limit the size of response packets coming from a peripheral.

### 7.1.4.3.1. Long Packet

Figure 7.25 shows the structure of the Long packet. A Long packet shall consist of three elements: a 32-bit Packet Header (PH), an application-specific Data Payload with a variable number of bytes, and a 16-bit Packet Footer (PF). The Packet Header is further composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

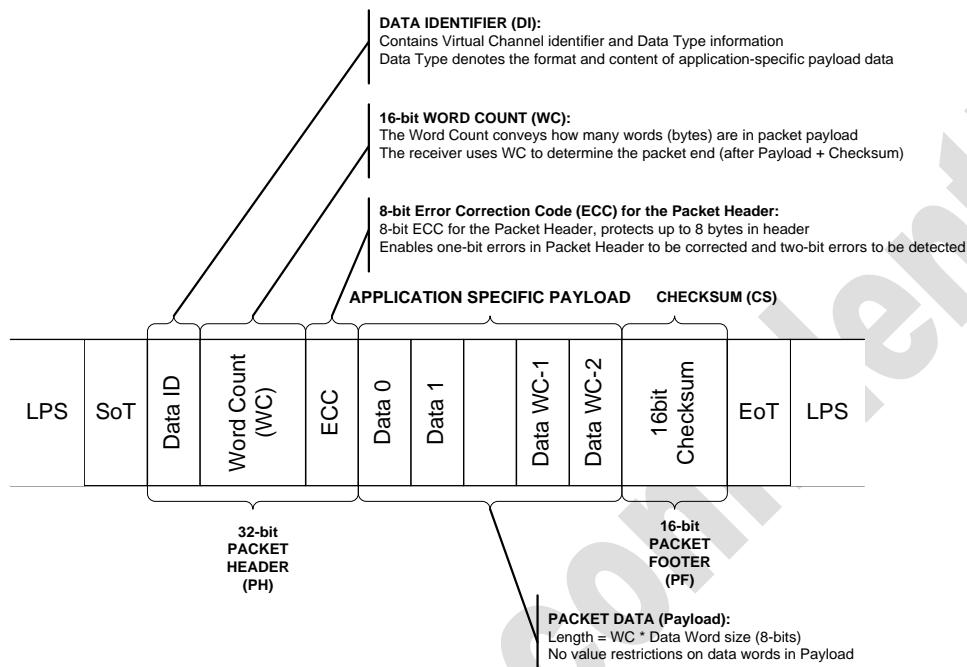


Figure 7.10: Long Packet Structure

The Data Identifier defines the Virtual Channel for the data and the Data Type for the application specific payload data.

The Word Count defines the number of bytes in the Data Payload between the end of the Packet Header and the start of the Packet Footer. Neither the Packet Header nor the Packet Footer shall be included in the Word Count.

The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. This includes both the Data Identifier and Word Count fields.

After the end of the Packet Header, the receiver reads the next  $WC \times$  bytes of the Data Payload. Within the Data Payload block, there are no limitations on the value of a data word, i.e. no embedded codes are used.

Once the receiver has read the Data Payload it reads the Checksum in the Packet Footer. The host processor shall always calculate and transmit a Checksum in the Packet Footer. Peripherals are not required to calculate a Checksum. Also note the

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special case of zero-byte Data Payload: if the payload has length 0, then the Checksum calculation results in (0xFFFF). If the Checksum is not calculated, the Packet Footer shall consist of two bytes of all zeros (0x0000). In the generic case, the length of the Data Payload shall be a multiple of bytes.

Each byte shall be transmitted least significant bit first. Payload data may be transmitted in any byte order restricted only by data format requirements. Multi-byte elements such as Word Count and Checksum shall be transmitted least significant byte first.

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### 7.1.4.3.2. Short Packet

Figure 7.26 shows the structure of the Short packet. A Short packet shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC; a Packet Footer shall not be present. Short packets shall be four bytes in length. The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Short packet.

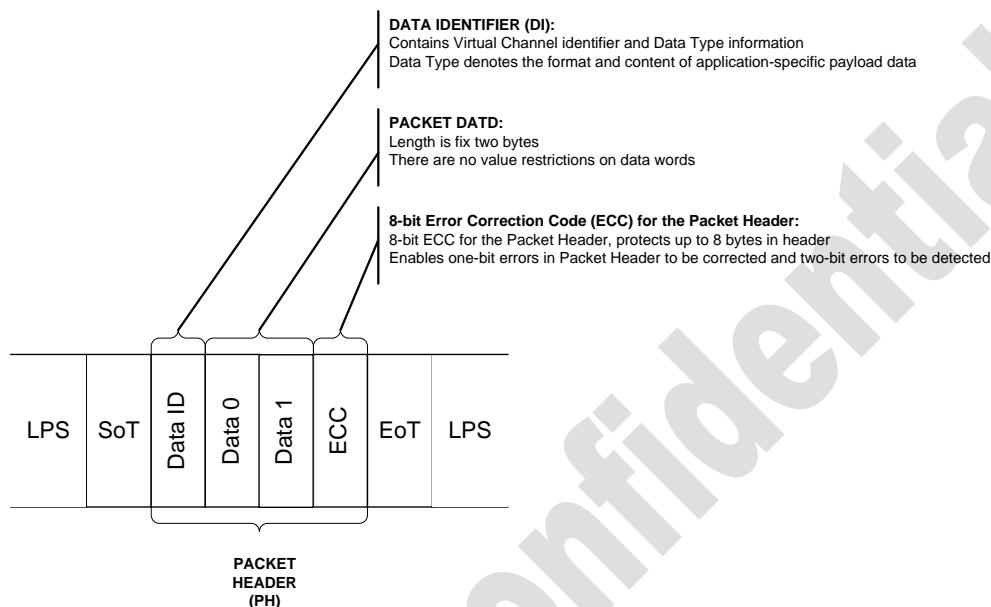


Figure 7.11: Short Packet Structure

## 7.1.5. Common Packet Elements

Long and Short packets have several common elements that are described in this section.

### 7.1.5.1. Data Identifier Byte

The first byte of any packet is the DI (Data Identifier) byte. Figure 7.27 shows the composition of the Data Identifier (DI) byte. DI[7:6]: These two bits identify the data as directed to one of four virtual channels. DI[5:0]: These six bits specify the Data Type.

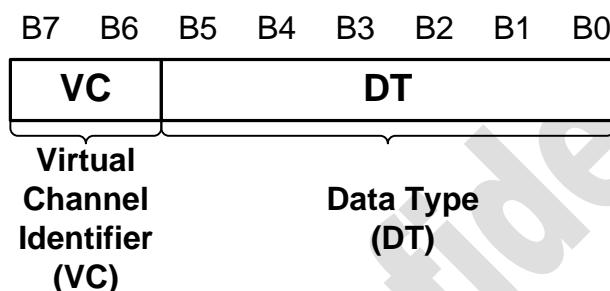


Figure 7.12: Data Identifier Byte

### 7.1.5.2. Virtual Channel Identifier – VC field, DI[7:6]

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals. The Virtual Channel ID enables one serial stream to service two or more virtual peripherals by multiplexing packets onto a common transmission channel.

### 7.1.5.3. Data Type Field DT[5:0]

The Data Type field specifies if the packet is a Long or Short packet type and the packet format. The Data Type field, along with the Word Count field for Long packets, informs the receiver of how many bytes to expect in the remainder of the packet. This is necessary because there are no special packet start / end sync codes to indicate the beginning and end of a packet. This permits packets to convey arbitrary data, but it also requires the packet header to explicitly specify the size of the packet. When the receiving logic has counted down to the end of a packet, it shall assume the next data is either the header of a new packet or the EoT (End of Transmission) sequence.

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#### 7.1.5.4. ECC

The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. The host processor shall always calculate and transmit an ECC byte. Peripherals shall support ECC in both forward- and reverse-direction communications.

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## 7.1.6. DSI packet

### 7.1.6.1. Processor-sourced Packets

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 7.4.

Data Type (Hex)	Data Type (Binary)	Description	Packet Size
0x01	00 0001	Sync Event, V Sync Start	Short
0x11	01 0001	Sync Event, V Sync End	Short
0x21	10 0001	Sync Event, H Sync Start	Short
0x31	11 0001	Sync Event, H Sync End	Short
0x08	00 1000	End of Transmission packet (EoTp)	Short
0x02	00 0010	Color Mode (CM) Off Command	Short
0x12	01 0010	Color Mode (CM) On Command	Short
0x22	10 0010	Shut Down Peripheral Command	Short
0x32	11 0010	Turn On Peripheral Command	Short
0x03	00 0011	Generic Short WRITE, no parameters	Short
0x13	01 0011	Generic Short WRITE, 1 parameter	Short
0x23	10 0011	Generic Short WRITE, 2 parameters	Short
0x04	00 0100	Generic READ, no parameters	Short
0x14	01 0100	Generic READ, 1 parameter	Short
0x24	10 0100	Generic READ, 2 parameters	Short
0x05	00 0101	DCS Short WRITE, no parameters	Short
0x15	01 0101	DCS Short WRITE, 1 parameter	Short
0x06	00 0110	DCS READ, no parameters	Short
0x37	11 0111	Set Maximum Return Packet Size	Short
0x09	00 1001	Null Packet, no data	Long
0x19	01 1001	Blanking Packet, no data	Long
0x29	10 1001	Generic Long Write	Long
0x39	11 1001	DCS Long Write/write_LUT Command Packet	Long
0x0E	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
0x1E	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x2E	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x3E	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
0xX0 and 0xF unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	

Table 7.1: Data Types for supported Processor-sourced Packets

### 7.1.6.2. Packed Pixel Stream, 16-bit Format, Long Packet

Packed Pixel Stream 16-Bit Format shown in Figure 7.28 is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is five bits red, six bits green, five bits blue, in that order. Within a color component, the LSB is sent first, the MSB last. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

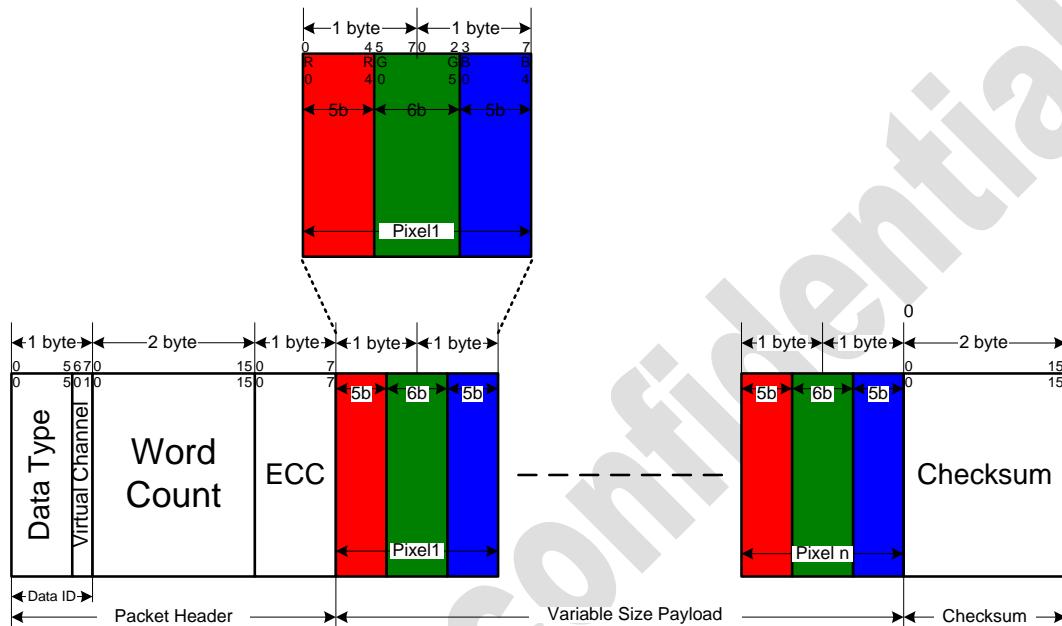


Figure 7.13: 16-bit per Pixel – RGB Color Format, Long Packet

### 7.1.6.3. Packed Pixel Stream, 18-bit Format, Long Packet

Packed Pixel Stream 18-Bit Format (Packed) shown in Figure 7.29 is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. Peripheral will not display the fill pixels when refreshing the display device.

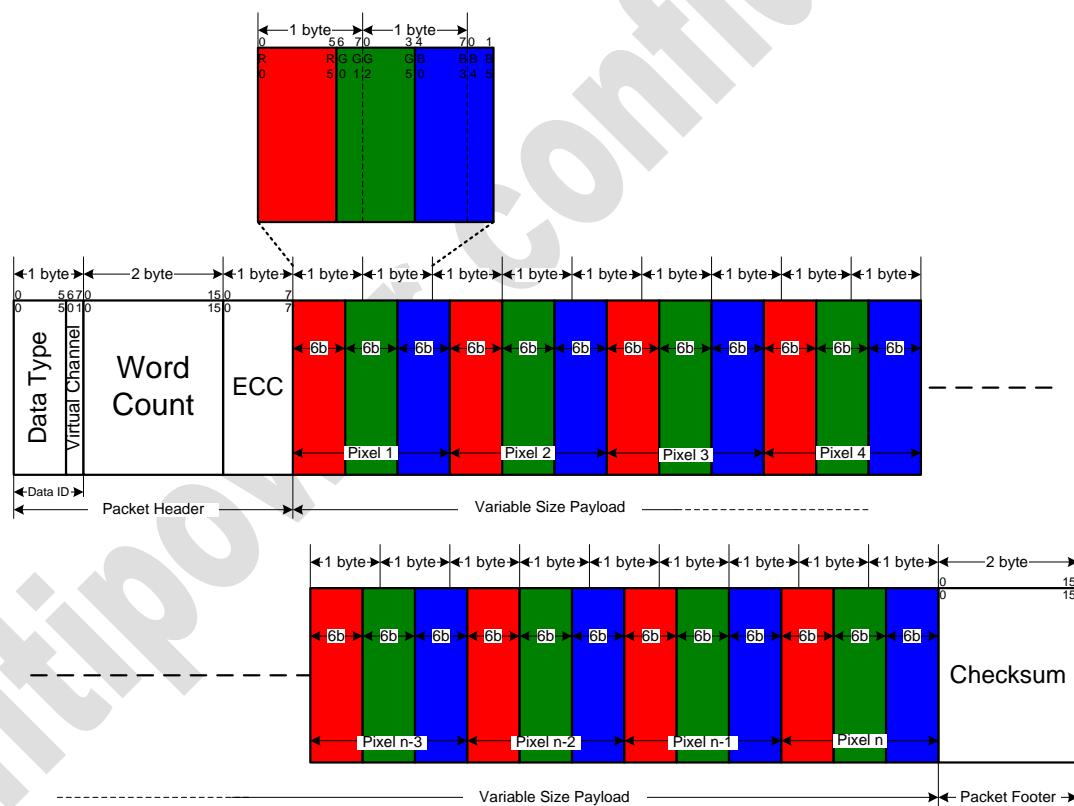


Figure 7.14: 18-bit per Pixel (Packed) – RGB Color Format, Long Packet

#### 7.1.6.4. Pixel Stream, 18-bit Loosely Format, Long Packet

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits, but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte as shown in Figure 7.30. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link. With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

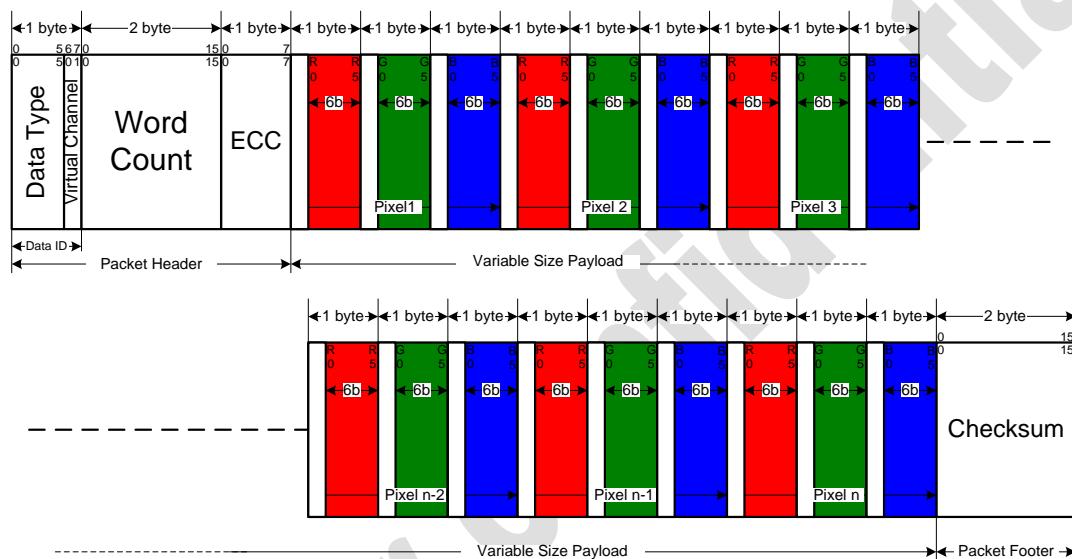


Figure 7.15: 18-bit per Pixel (Loosely Packed) – RGB Color Format, Long Packet

### 7.1.6.5. Packed Pixel Stream, 24-bit Format, Long Packet

Packed Pixel Stream 24-Bit Format shown in Figure 7.31 is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last. With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

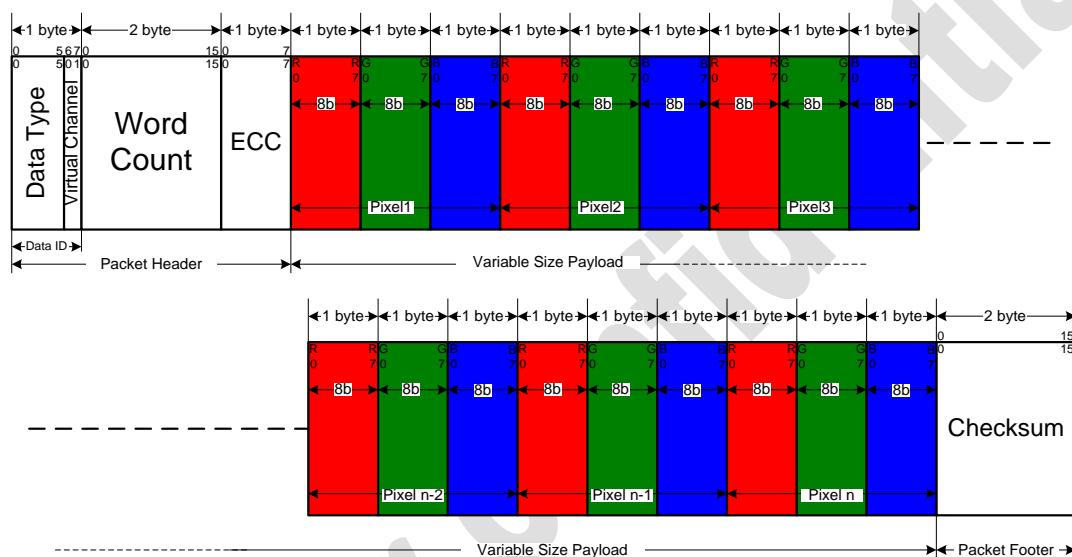


Figure 7.16: 24-bit per Pixel – RGB Color Format, Long Packet

### 7.1.7. Peripheral to Processor Transmission

JD9161Z has bidirectional capability for returning READ data, acknowledge, or error information to the host processor. BTA shall take place after every peripheral-to-processor transaction. This returns bus control to the host processor following the completion of the LP transmission from the peripheral.

Peripheral-to-processor transactions are of four basic types:

- **Tearing Effect (TE)** is a Trigger message sent to convey display timing information to the host processor. Trigger messages are single byte packets sent by a peripheral's PHY layer in response to a signal from the DSI protocol layer.
- **Acknowledge** is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication, i.e. either triggers or packets, is received by the peripheral with no errors.
- **Acknowledge and Error Report** is a Short packet sent if any errors were detected in preceding transmissions from the host processor. Once reported, accumulated errors in the error register are cleared.
- **Response to Read Request** may be a Short or Long packet that returns data requested by the preceding READ command from the processor.

### 7.1.7.1. Appropriate Responses to Commands and ACK Requests

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host processor. If BTA is not asserted following a transmission from the host processor, the peripheral shall not communicate an Acknowledge or error information back to the host processor.

Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:

- Following a non-Read command, the peripheral shall respond with Acknowledge if no errors were detected and stored since the last peripheral to host communication, i.e. either triggers or packets.
- Following a Read request, the peripheral shall send the requested READ data if no errors were detected and stored since the last peripheral to host communication, i.e. either triggers or packets.
- Following a Read request if only a single-bit ECC error was detected and corrected, the peripheral shall send the requested READ data in a Long or Short packet, followed by a 4-byte Acknowledge and Error Report packet in the same LP transmission. The Error Report shall have the ECC Error – Single Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.
- Following a non-Read command if only a single-bit ECC error was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte Acknowledge and Error Report packet. The Error Report shall have the ECC Error – Single Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.
- Following a Read request, if multi-bit ECC errors were detected and not corrected, the peripheral shall send a 4-byte Acknowledge and Error Report packet without sending Read data. The Error Report shall have the ECC Error – Multi-Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.
- Following a non-Read command, if multi-bit ECC errors were detected and not corrected, the peripheral shall not execute the command, and shall send a 4-byte Acknowledge and Error Report packet. The Error Report shall have the ECC Error – Multi-Bit flag set, as well as any error bits from any preceding transmissions stored

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since the last peripheral to host communication.

- Following any command, if SoT Error, SoT Sync Error or DSI VC ID Invalid or DSI protocol violation was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge and Error Report response, with the appropriate error flags set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication, in the two-byte error field. Only the Acknowledge and Error Report packet shall be transmitted; no read or write accesses shall take place on the peripheral in response.
- Following any command, if EoT Sync Error or LP Transmit Sync Error is detected, or a checksum error is detected in the payload, the peripheral shall send a 4-byte Acknowledge and Error Report packet with the appropriate error flags set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication. For a read command, only the Acknowledge and Error Report packet shall be transmitted; no read data shall be sent by the peripheral in response.

Once reported to the host processor, all errors documented in this section are cleared from the Error Register.

#### 7.1.7.2. Peripheral-to-Processor Packet Description

Table 7.5 presents the complete set of peripheral-to-processor Data Types.

Data Type (Hex)	Data Type (Binary)	Description	Packet Size
0x02	00 0010	Acknowledge and Error Report	Short
0x08	00 1000	End of Transmission packet	Short
0x1C	01 1100	DCS Long READ Response	Long

Table 7.2: Data Types for Peripheral-sourced Packets

### 7.1.8. Format of Acknowledge and Error Report and Read Response Data Type

**Acknowledge** is sent using a Trigger message.

- Byte 0: 00100001 (shown here in first bit [left] to last bit [right] sequence)

**Response to Read Request** returns data requested by the preceding READ command from the processor. These may be short or Long packets. The format for short READ packet responses is:

- Byte 0: Data Identifier (Virtual Channel ID + Data Type)
- Bytes 1, 2: READ data, may be one or two bytes. For single byte parameters, the parameter shall be returned in Byte 1 and Byte 2 shall be set to 0x00.
- ECC byte covering the header

**Acknowledge and Error Report** confirms that the preceding command or data sent from the host processor to a peripheral was received, and indicates what types of error were detected on the transmission and any preceding transmissions. Note that if errors accumulate from multiple preceding transmissions, it may be difficult or impossible to identify which transmission contained the error. This message is a Short packet of four bytes, taking the form:

- Byte 0: Data Identifier (Virtual Channel ID + Acknowledge Data Type)
- Byte 1: Error Report bits 0-7
- Byte 2: Error Report bits 8-15
- ECC byte covering the header

An error report is a Short packet comprised of two bytes following the DI byte, with an ECC byte following the Error Report bytes. By convention, detection and reporting of each error type is signified by setting the corresponding bit to “1”. Table 7.6 shows the bit assignment for all error reporting.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Peripheral Timeout Error
6	False Control Error
7	Contention Detected
8	ECC Error, Single-bit (detected and corrected)
9	ECC Error, Multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
14	Reserved
15	DSI Protocol Violation

Table 7.3: Error Report Bit Definitions

The first eight bits, bit 0 through bit 7, are related to the physical layer errors. Bits 8 and 9 are related to single-bit and multi-bit ECC errors. The remaining bits indicate DSI protocol-specific errors.

## 7.1.9. Video Mode Interface Timing

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

### 7.1.9.1. Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. In the following sections, Burst Mode refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

- **Non-Burst Mode with Sync Pulses** – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- **Non-Burst Mode with Sync Events** – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- **Burst mode** – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral.

To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. The host processor should return to LP state once per scanline during the horizontal blanking time.

During the BLLP the DSI Link may do any of the following:

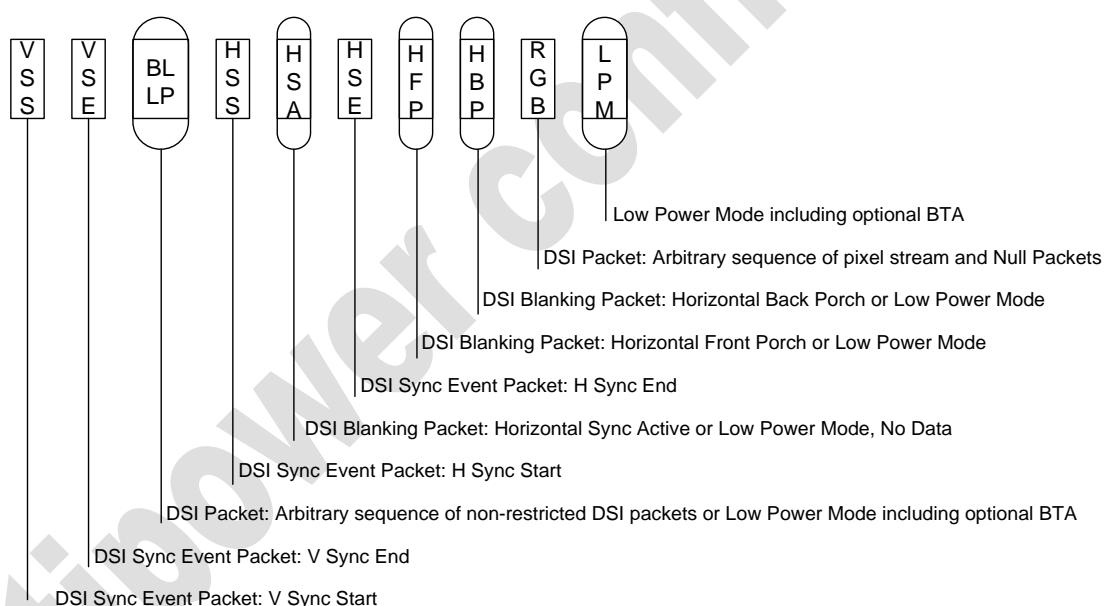
- Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX
- Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode
- Transmit one or more non-video packets from the host processor to the peripheral using HS Mode

- If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode
- Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VSS; all other lines shall start with VSE or HSS. Note that the position of synchronization packets, such as VSS and HSS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet.

Transmission packet components used in the figures in this section are defined in Figure 7.32 unless otherwise specified.

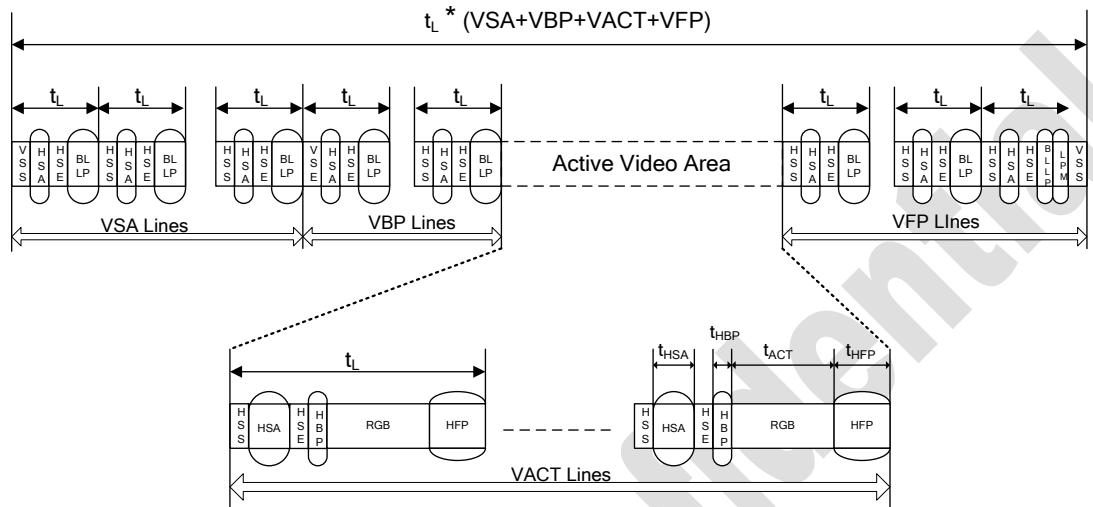


**Figure 7.17: Video Mode Interface Timing Legend**

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

### 7.1.9.2. Non-Burst sync pulse mode

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure 7.33.

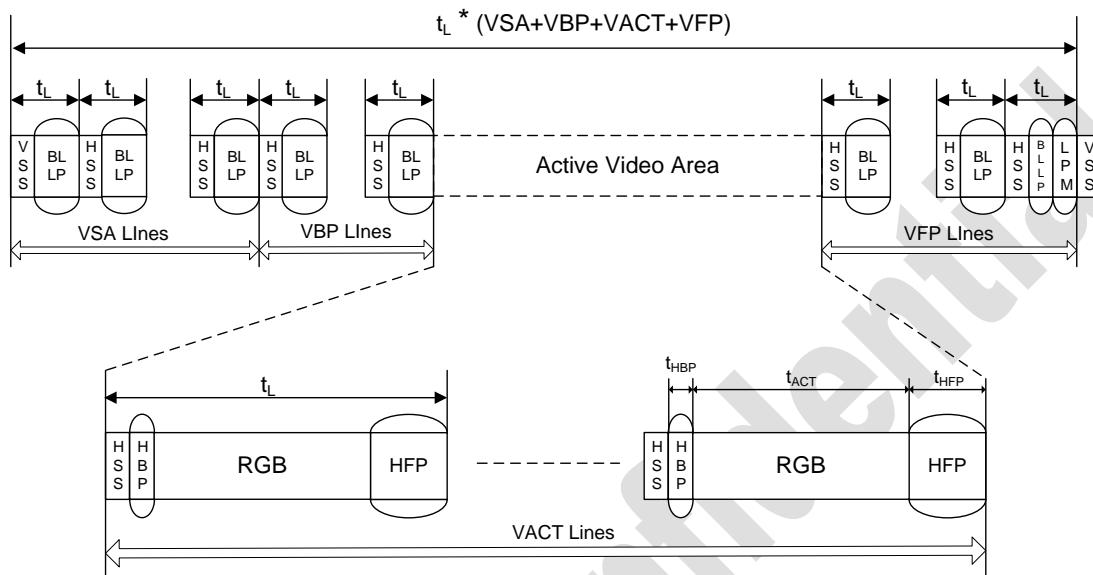


**Figure 7.18: Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End**

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power. During HSA, HBP and HFP periods, the bus should stay in the LP-11 state.

### 7.1.9.3. Non-Burst sync event mode

This mode is a simplification of the “Non-Burst Mode with Sync Pulses” format. Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. An example of this mode is shown in Figure 7.34.



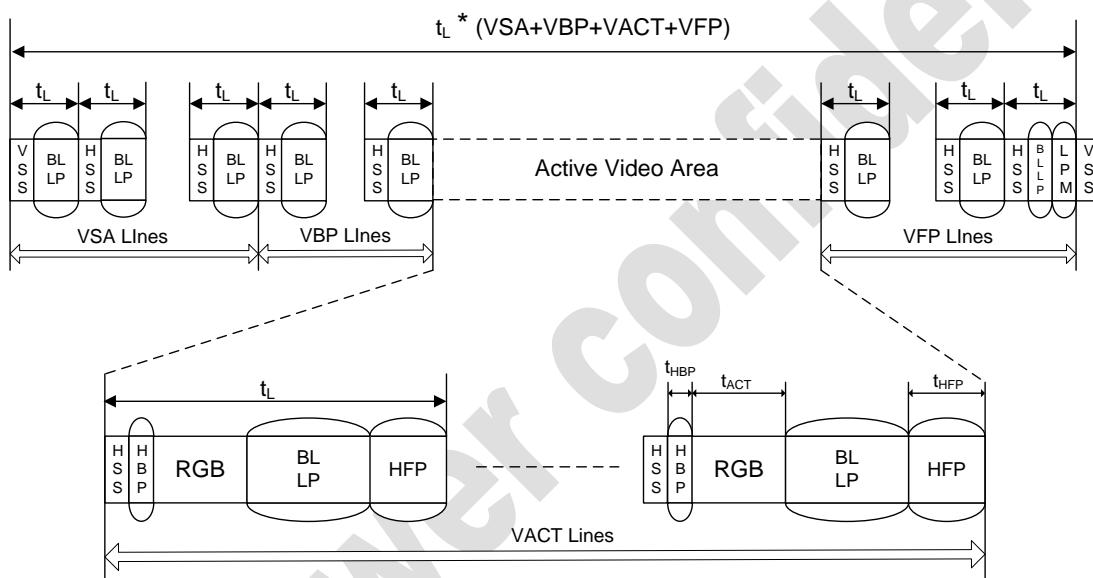
**Figure 7.19: Video Mode Interface Timing: Non-burst Transmission with Sync Events**

As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

### 7.1.9.4. Burst mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction.

Following HS pixel data transmission, the bus may stay in HS Mode for sending blanking packets or go to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure 7.35.



**Figure 7.20: Video Mode Interface Timing: Burst Transmission**

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

## 7.1.10.Error-Correcting Code and Checksum

### 7.1.10.1.Error-Correcting Code(ECC)

MIPI DSI uses Hamming Code Theory as ECC generate rule. The parity of each bits in ECC are showed as below.

$$P7=0$$

$$P6=0$$

$$P5=D10 \wedge D11 \wedge D12 \wedge D13 \wedge D14 \wedge D15 \wedge D16 \wedge D17 \wedge D18 \wedge D19 \wedge D21 \wedge D22 \wedge D23$$

$$P4=D4 \wedge D5 \wedge D6 \wedge D7 \wedge D8 \wedge D9 \wedge D16 \wedge D17 \wedge D18 \wedge D19 \wedge D20 \wedge D22 \wedge D23$$

$$P3=D1 \wedge D2 \wedge D3 \wedge D7 \wedge D8 \wedge D9 \wedge D13 \wedge D14 \wedge D15 \wedge D19 \wedge D20 \wedge D21 \wedge D23$$

$$P2=D0 \wedge D2 \wedge D3 \wedge D5 \wedge D6 \wedge D9 \wedge D11 \wedge D12 \wedge D15 \wedge D18 \wedge D20 \wedge D21 \wedge D22$$

$$P1=D0 \wedge D1 \wedge D3 \wedge D4 \wedge D6 \wedge D8 \wedge D10 \wedge D12 \wedge D14 \wedge D17 \wedge D20 \wedge D21 \wedge D22 \wedge D23$$

$$P0=D0 \wedge D1 \wedge D2 \wedge D4 \wedge D5 \wedge D7 \wedge D10 \wedge D11 \wedge D13 \wedge D16 \wedge D20 \wedge D21 \wedge D22 \wedge D23$$

ECC is generated from the twenty-four bits with in the Packet Header as illustrated in Figure 7.36, which also serves as an ECC calculation example.

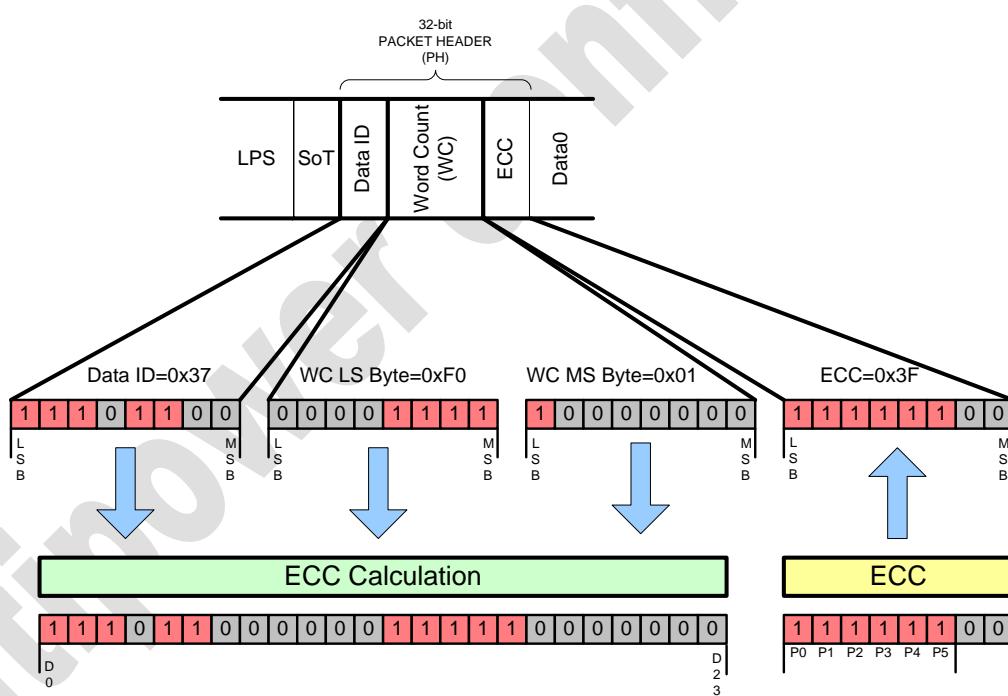
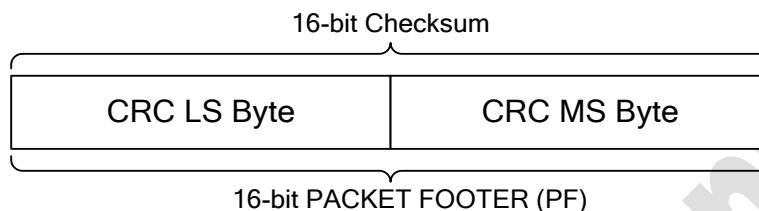


Figure 7.21: 24-bit ECC generation Example

### 7.1.10.2. Checksum Generation for Long Packet Payloads

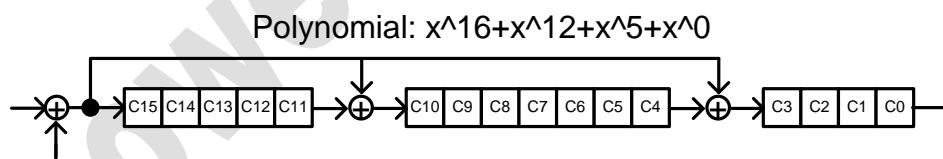
To detect errors in transmission of Long packets, a checksum is calculated over the payload portion of the data packet. Note that, for the special case of a zero-length payload, the 2-byte checksum is set to 0xFFFF. The checksum shall be realized as a 16-bit CRC with a generator polynomial of  $x^{16}+x^{12}+x^5+x^0$

The transmission of the checksum is illustrated in Figure 7.37. The LS byte is sent first, followed by the MS byte. Note that within the byte, the LS bit is sent first.



**Figure 7.22: Checksum Transmission**

The CRC implementation is presented in Figure 7.38. The CRC shift register shall be initialized to 0xFFFF before packet data enters. Packet data not including the Packet Header then enters as a bitwise data stream from the left, LS bit first. Each bit is fed through the CRC shift register before it is passed to the output for transmission to the peripheral. After all bytes in the packet payload have passed through the CRC shift register, the shift register contains the checksum. C15 contains the checksum's MSB and C0 the LSB of the 16-bit checksum. The checksum is then appended to the data stream and sent to the receiver. The receiver uses its own generated CRC to verify that no errors have occurred in transmission.



**Figure 7.23: 16-bit CRC Generation Using a Shift Register**

## 7.1.11.DPHY

### 7.1.11.1.Lane Module

A PHY configuration contains a Clock Lane Module and one or more Data Lane Modules. Each of these PHY Lane Modules communicates via two Lines to a complementary part at the other side of the Lane Interconnect. Each Lane Module consists of one or more differential High-Speed functions utilizing both interconnect wires simultaneously, one or more single-ended Low-Power functions operating on each of the interconnect wires individually, and control & interface logic. For proper operation, the set of functions in the Lane Modules on both sides of the Lane Interconnect has to be matched.

#### 7.1.11.1.1. Lane Module Type of Clock Lane, Data0, Data1 and Data2

The required functions in a Lane Module depend on the Lane type and which side (master or slave) of the Lane Interconnect the Lane Module is located. There are three main Lane types: Clock Lane, Unidirectional Data Lane and Bi-directional Data Lane. Several PHY configurations can be constructed with these Lane types. In JD9161Z Below show the lane module architecture of each lane.

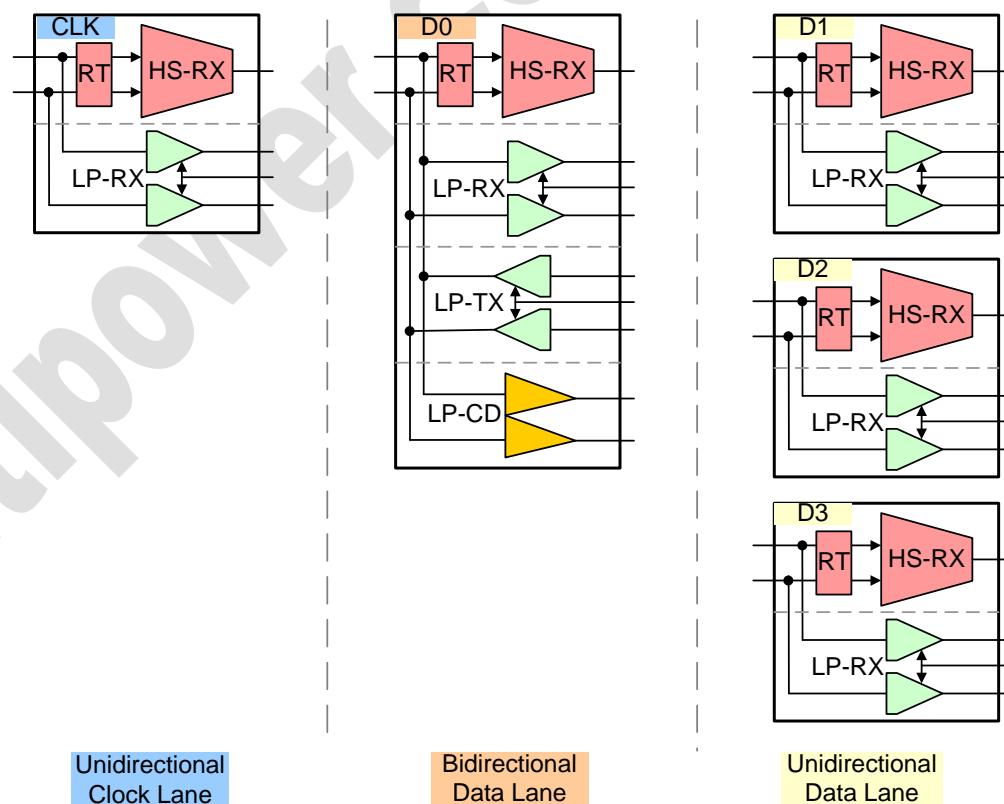


Figure 7.24: Lane Module Type

### 7.1.11.2. Master and Slave

Each Link has a Master and a Slave side. The Master provides the High-Speed DDR Clock signal to the Clock Lane and is the main data source. The Slave receives the clock signal at the Clock Lane and is the main data sink. The main direction of data communication, from source to sink, is denoted as the Forward direction. Data communication in the opposite direction is called Reverse transmission. Only bi-directional Data Lanes can transmit in the Reverse direction. In all cases, the Clock Lane remains in the Forward direction, but bi-directional Data Lane(s) can be turned around, sourcing data from the Slave side.

JD9161Z serves as Slave side.

### 7.1.11.3. Lane States and Line Levels

Transmitter functions determine the Lane state by driving certain Line levels. During normal operation either a HS-TX or a LP-TX is driving a Lane. A HS-TX always drives the Lane differentially. The two LP-TX's drive the two Lines of a Lane independently and single-ended. This results in two possible High-Speed Lane states and four possible Low-Power Lane states. The High-Speed Lane states are Differential-0 and Differential-1. The interpretation of Low-Power Lane states depends on the mode of operation. The LP-Receiver shall always interpret both High-Speed differential states as LP-00.

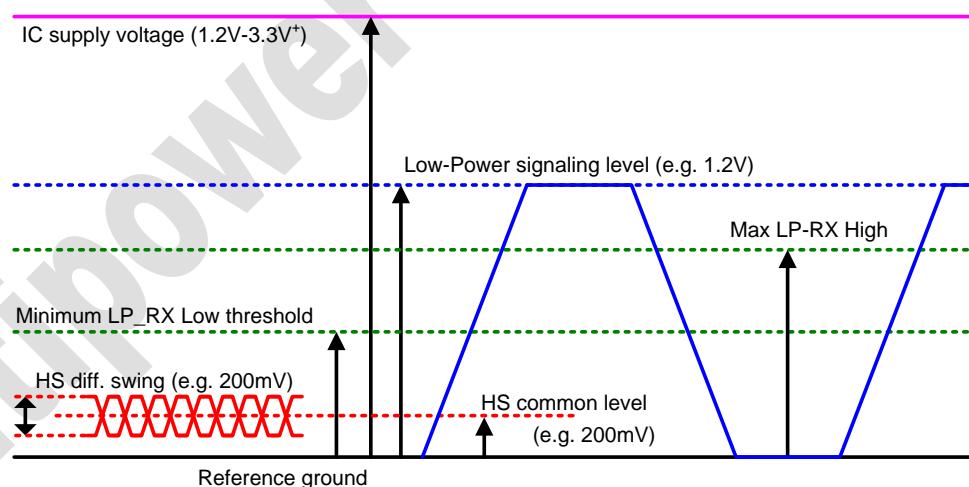


Figure 7.25: Line Levels

The Stop state has a very exclusive and central function. If the Line levels show a Stop state for the minimum required time, the PHY state machine shall return to the Stop state regardless of the previous state. This can be in RX or TX mode depending on the most recent operating direction. Table 7.7 lists all the states that can appear on a Lane during normal operation. All LP state periods shall be at least TLPX in duration. State

transitions shall be smooth and exclude glitch effects. A clock signal can be reconstructed by exclusive-ORing the Dp and Dn Lines. Ideally, the reconstructed clock has a duration of at least  $2 \times T_{LPX}$ , but may have a duty cycle other than 50% due to signal slope and trip levels effects.

Start Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

Table 7.4: Lane State Descriptions

#### 7.1.11.4. Bi-directional Data Lane Turnaround

The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction. Notice that Master and Slave side shall not be changed by Turnaround.

Figure 7.41 shows the Turnaround procedure graphically.

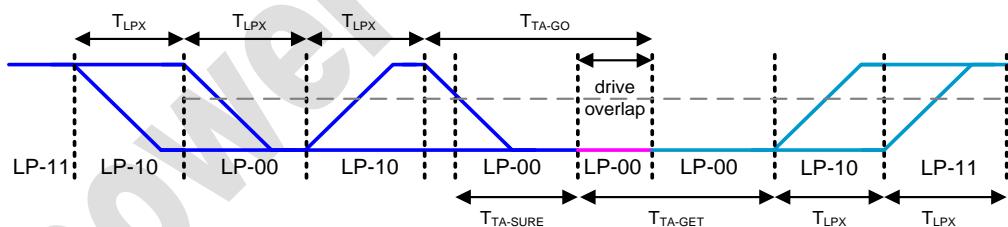


Figure 7.26: Turnaround Procedure

### 7.1.11.5. Escape Mode

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. A Data Lane shall enter Escape mode via an Escape mode Entry procedure (LP-11, LP-10, LP-00, LP-01, LP-00). As soon as the final Bridge state (LP-00) is observed on the Lines the Lane shall enter Escape mode in Space state (LP-00). If an LP-11 is detected at any time before the final Bridge state (LP-00), the Escape mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state.

For Data Lanes, once Escape mode is entered, the transmitter shall send an 8-bit entry command, by Spaced-One-Hot coding, to indicate the requested action. Table 7.8 lists all supported Escape mode commands and actions.

Spaced-One-Hot coding means that each Mark state is interleaved with a Space state. Each symbol consists therefore of two parts: a One-Hot phase (Mark-0 or Mark-1) and a Space phase. The TX shall send Mark-0 followed by a Space to transmit a ‘zero-bit’ and it shall send a Mark-1 followed by a Space to transmit a ‘one-bit’. A Mark that is not followed by a Space does not represent a bit. The last phase before exiting Escape mode with a Stop state shall be a Mark-1 state that is not part of the communicated bits, as it is not followed by a Space state.

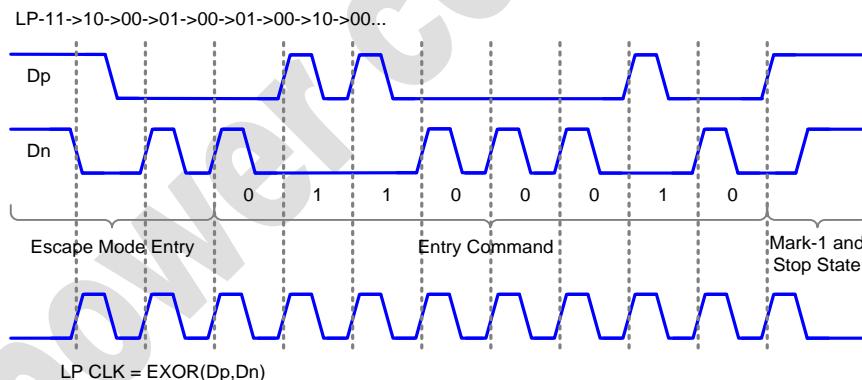


Figure 7.27: Trigger-Reset Command in Escape Mode

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low power State	mode	00011110
Reset-Trigger	Trigger	01100010
TE-Trigger	Trigger	01011101
Acknowledge	Trigger	00100001

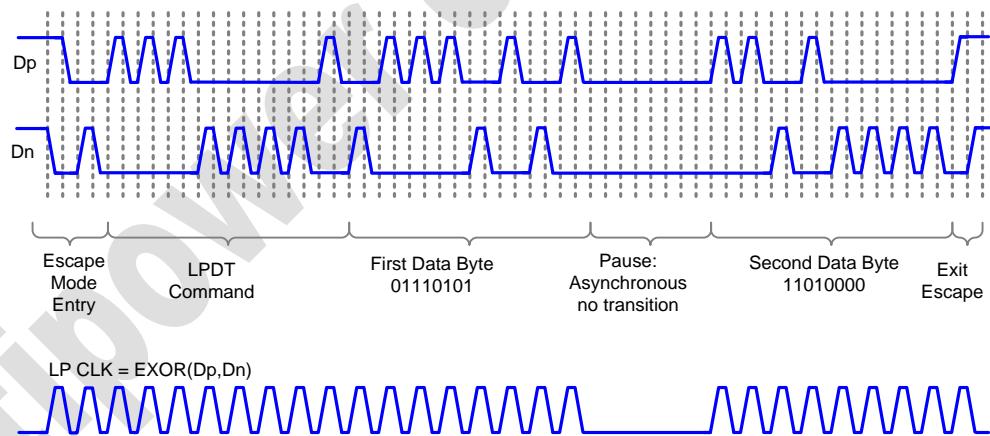
Table 7.5: Escape Entry Codes

### **7.1.11.5.1. Remote Trigger**

Trigger signaling is the mechanism to send a flag to the protocol at the receiving side, on request of the protocol on the transmitting side. This can be either in the Forward or Reverse direction depending on the direction of operation and available Escape mode functionality. Trigger signaling requires Escape mode capability and at least one matching Trigger Escape Entry Command on both sides of the interface. Any bit received after a Trigger Command but before the Lines go to Stop state shall be ignored. Therefore, dummy bytes can be concatenated in order to provide Clock information to the receive side.

#### **7.1.11.5.2. Low-Power Data Transmission(LPDT)**

If the Escape mode Entry procedure is followed-up by the Entry Command for Low-Power Data Transmission (LPDT), Data can be communicated by the protocol at low speed, while the Lane remains in Low-Power mode. Data shall be encoded on the lines with the same Spaced-One-Hot code as used for the Entry Commands. The data is self-coded by the applied bit encoding and does not rely on the Clock Lane. The Lane can pause while using LPDT by maintaining a Space state on the Lines. A Stop state on the Lines stops LPDT, exits Escape mode, and switches the Lane to Control mode. The last phase before Stop state shall be a Mark-1 state, which does not represent a data-bit. At the end of LPDT the Lane shall return to the Stop state.



**Figure 7.28: Two Data Byte Low-Power Data Transmission Example**

### **7.1.11.5.3. Ultra-Low Power State(ULPS)**

If the Ultra-Low Power State Entry Command is sent after an Escape mode Entry command, the Lane shall enter the Ultra-Low Power State (ULPS). This command shall be flagged to the receive side Protocol. During this state, the Lines are in the Space state (LP-00). Ultra-Low Power State is exited by means of a Mark-1 state with a length TWAKEUP followed by a Stop state.

#### 7.1.11.5.4. TE Trigger

A Command Mode display module has its own timing controller and local frame buffer for display refresh. In some cases the host processor needs to be notified of timing events on the display module, e.g. the start of vertical blanking or similar timing information. In a traditional parallel-bus interface like DBI-2, a dedicated signal wire labeled TE (Tearing Effect) is provided to convey such timing information to the host processor. In a DSI system, the same information, with reasonably low latency, shall be transmitted from the display module to the host processor when requested, using the bidirectional Data Lane.

For polling to the display module, the host processor shall detect the current scan line information with a DCS command such as get\_scan\_line to avoid Tearing Effects. For TE-reporting from the display module, the TE-reporting function is enabled and disabled by three DCS commands to the display module's controller: set\_tear\_on, set\_tear\_scanline, and set\_tear\_off.

set\_tear\_on and set\_tear\_scanline are sent to the display module as DSI Data Type 0x15 (DCS Short Write, one parameter) and DSI Data Type 0x39 (DCS Long Write/write\_LUT), respectively. The host processor ends the transmission with Bus Turn-Around asserted, giving bus possession to the display module. Since the display module's DSI Protocol layer does not interpret DCS commands, but only passes them through to the display controller, it responds with a normal Acknowledge and returns bus possession to the host processor. In this state, the display module cannot report TE events to the host processor since it does not have bus possession.

To enable TE-reporting, the host processor shall give bus possession to the display module without an accompanying DSI command transmission after TE reporting has been enabled. This is accomplished by the host processor's protocol logic asserting (internal) Bus Turn-Around signal to its D-PHY functional block. The PHY layer will then initiate a Bus Turn-Around sequence in LP mode, which gives bus possession to the display module.

Since the timing of a TE event is, by definition, unknown to the host processor, the host processor shall give bus possession to the display module and then wait for up to one video frame period for the TE response. During this time, the host processor cannot send new commands, or requests to the display module, because it does not have bus possession.

When the TE event takes place the display module shall send TE event information in LP mode using a specified trigger message available with D-PHY protocol via the following sequence:

- The display module shall send the LP Escape Mode sequence
- The display module shall then send the trigger message byte 01011101 (shown here in first bit to last bit sequence)
- The display module shall then return bus possession to the host processor

This Trigger Message is reserved by DSI for TE signaling only and shall not be used for any other purpose in a DSI-compliant interface.

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## 7.1.12.High Speed Transmission

### 7.1.12.1.1. Burst Payload Data

The payload data of a burst shall always represent an integer number of payload data bytes with a minimum length of one byte. Note that for short bursts the Start and End overhead consumes much more time than the actual transfer of the payload data.

There is no maximum number of bytes implied by the PHY. However, in the PHY there is no autonomous way of error recovery during a HS data burst and the practical BER will not be zero. Therefore, it is important to consider for every individual protocol what the best choice is for maximum burst length.

### 7.1.12.1.2. Start-of-Transmission

After a Transmit request, a Data Lane leaves the Stop state and prepares for High-Speed mode by means of a Start-of-Transmission (SoT) procedure. Table 7.9 describes the sequence of events on TX and RX side.

TX Side	RX Side
Drives Stop state (LP-11)	Observes Stop state
Drives HS-Rqst state (LP-01) for time $T_{LPX}$	Observes transition from LP-11 to LP-01 on the Lines
Drives Bridge state (LP-00) for time $T_{HS-PREPARE}$	Observes transition from LP-01 to LP-00 on the Lines, enables Line Termination after time $T_{D-TERM-EN}$
Enables High-Speed driver and disables Low-Powerdrivers simultaneously.	
Drives HS-0 for a time $T_{HS-ZERO}$	Enables HS-RX and waits for timer $T_{HS-SETTLE}$ to expire in order to neglect transition effects
	Starts looking for Leader-Sequence
Inserts the HS Sync-Sequence '00011101' beginning on a rising Clock edge	
	Synchronizes upon recognition of Leader Sequence '011101'
Continues to Transmit High-Speed payload data	
	Receives payload data

Table 7.6: Start-of-Transmission Sequence

### 7.1.12.1.3. End-of-Transmission

At the end of a Data Burst, a Data Lane leaves High-Speed Transmission mode and enters the Stop state by means of an End-of-Transmission (EoT) procedure. Table 7.10 shows a possible sequence of events during the EoT procedure. Note, EoT processing may be handled by the protocol or by the D-PHY.

TX Side	RX Side
Completes Transmission of payload data	Receives payload data
Toggles differential state immediately after last payload data bit and keeps that state for a time $T_{HS-TRAIL}$	
Disables the HS-TX, enables the LP-TX, and drives Stop state (LP-11) for a time $T_{HS-EXIT}$	Detects the Lines leaving LP-00 state and entering Stop state (LP-11) and disables Termination
	Neglect bits of last period $T_{HS-SKIP}$ to hide transition effects
	Detect last transition in valid Data, determine last valid Data byte and skip trailer sequence

Table 7.7: End-of-Transmission Sequence

#### 7.1.12.1.4. High Speed Data Transmission

Figure 7.44 shows the sequence of events during the transmission of a Data Burst. Transmission can be started and ended independently for any Lane by the protocol. However, for most applications the Lanes will start synchronously but may end at different times due to an unequal amount of transmitted bytes per Lane.

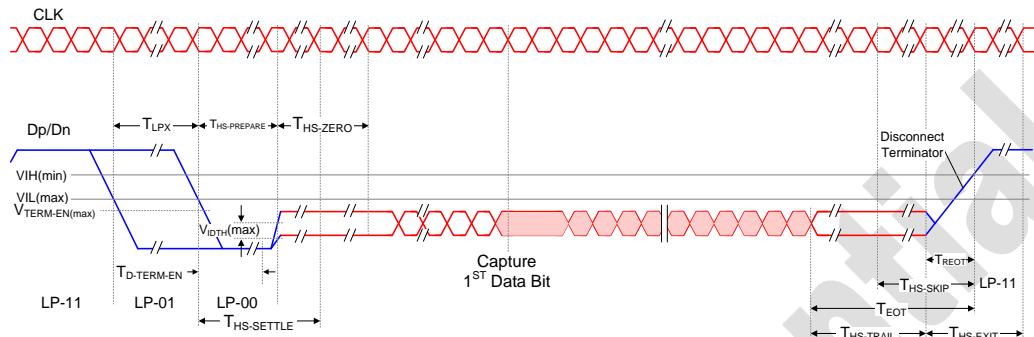


Figure 7.29: High-Speed Data Transmission in Bursts

#### 7.1.12.1.5. High Speed Clock Transmission

In High-Speed mode the Clock Lane provides a low-swing, differential DDR (half-rate) clock signal from Master to Slave for High-Speed Data Transmission. The Clock signal shall have quadrature-phase with respect to a toggling bit sequence on a Data Lane in the Forward direction and a rising edge in the center of the first transmitted bit of a burst. The detail Clock Start and Stop procedures are shown in Figure 7.45.

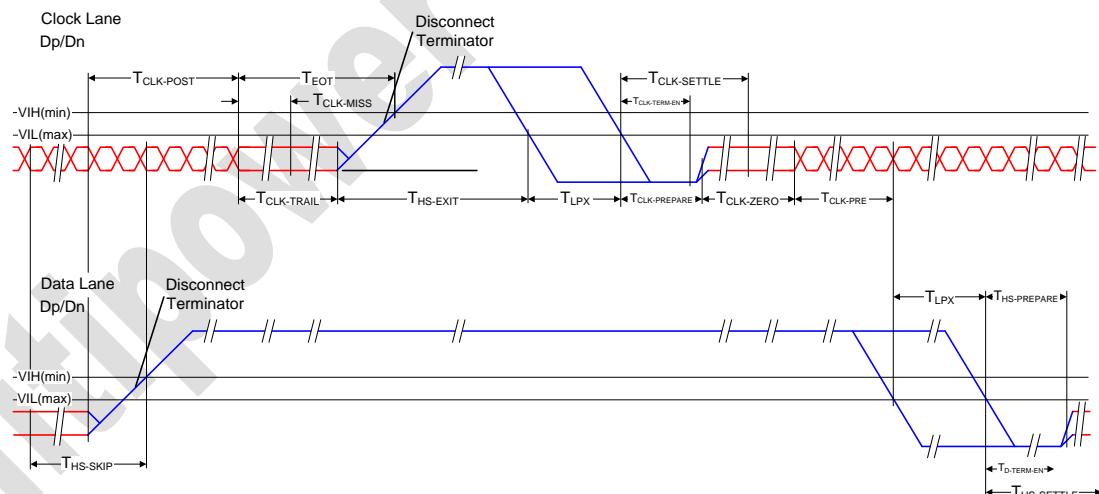


Figure 7.30: Switching the Clock Lane between Clock Transmission and Low-Power Mode

### 7.1.13. System Power state

Each Lane within a PHY configuration, that is powered and enabled, has potentially three different power consumption levels: High-Speed Transmission mode, Low-Power mode and Ultra-Low Power State.

#### 7.1.13.1.1. Initialization

After power-up, the Slave side PHY shall be initialized when the Master PHY drives a Stop State (LP-11) for a period longer than TINIT. The first Stop state longer than the specified TINIT is called the Initialization period. The Master side shall ensure that a Stop State longer than TINIT does not occur on the Lines before the Master is initialized.

TINIT must be larger than 500us.

#### 7.1.13.1.2. Global Operation Flow Diagram

Figure 7.46 shows the operational flow diagram for a Data Lane Module. Within both TX and RX four main processes can be distinguished: High-Speed Transmission, Escape mode, Turnaround, and Initialization.

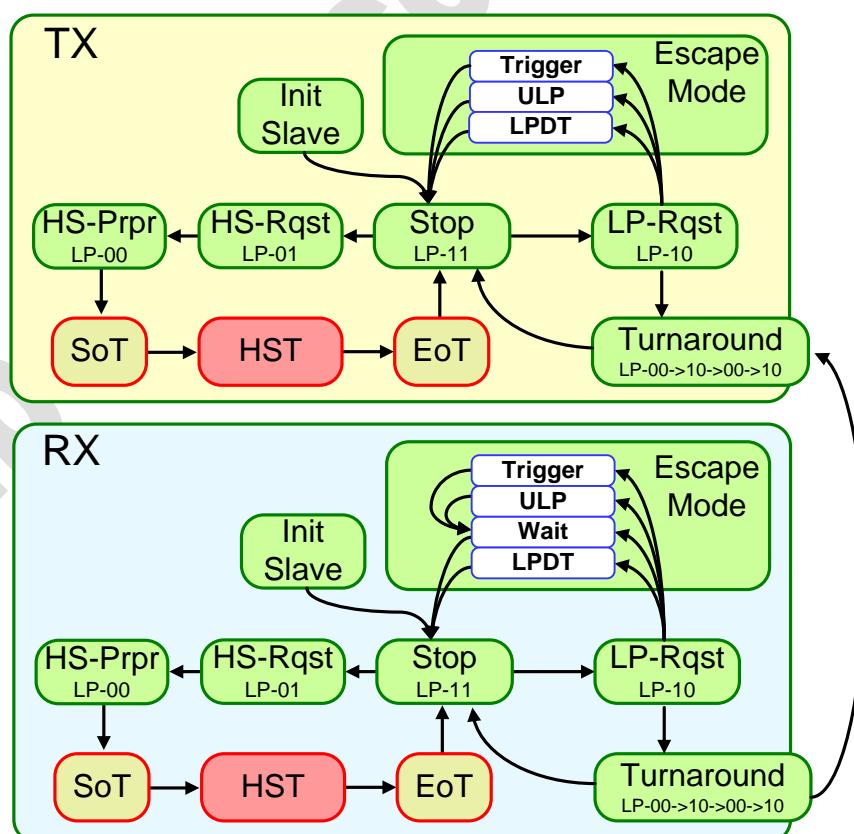
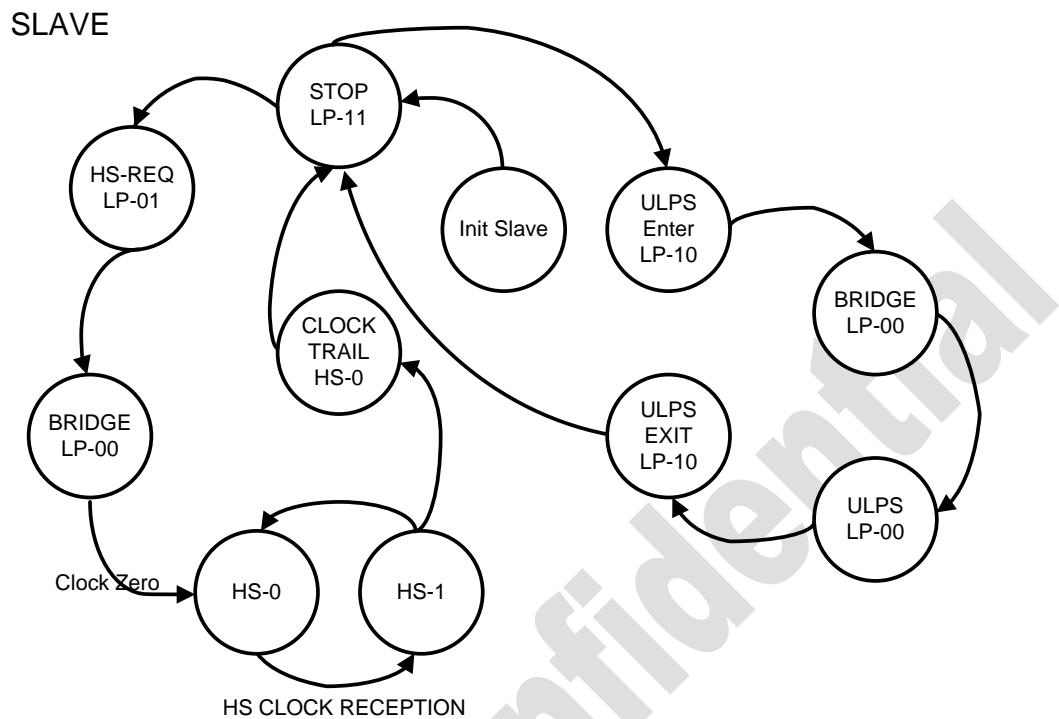


Figure 7.31: Data Lane Module State Diagram

Figure 7.47 shows the state diagram for a Clock Lane Module. The Clock Lane Module has four major operational states: Init (of unspecified duration), Low-Power Stop state, Ultra-Low Power state, and High-Speed clock transmission.



**Figure 7.32: Clock Lane Module State Diagram**

## 8. Gamma Structure Description

### 8.1. Adjustable gamma characteristic

The JD9161Z includes gamma adjustment function for the 16.7M colors display (256 grayscale for R/G/B- color). Gamma adjustment operation is implemented by 19 gamma adjustment control registers to meet the characteristic of LCD panel. Then total 512 grayscale levels are generated in Positive-/Negative- grayscale voltage. These registers are available for both polarities.

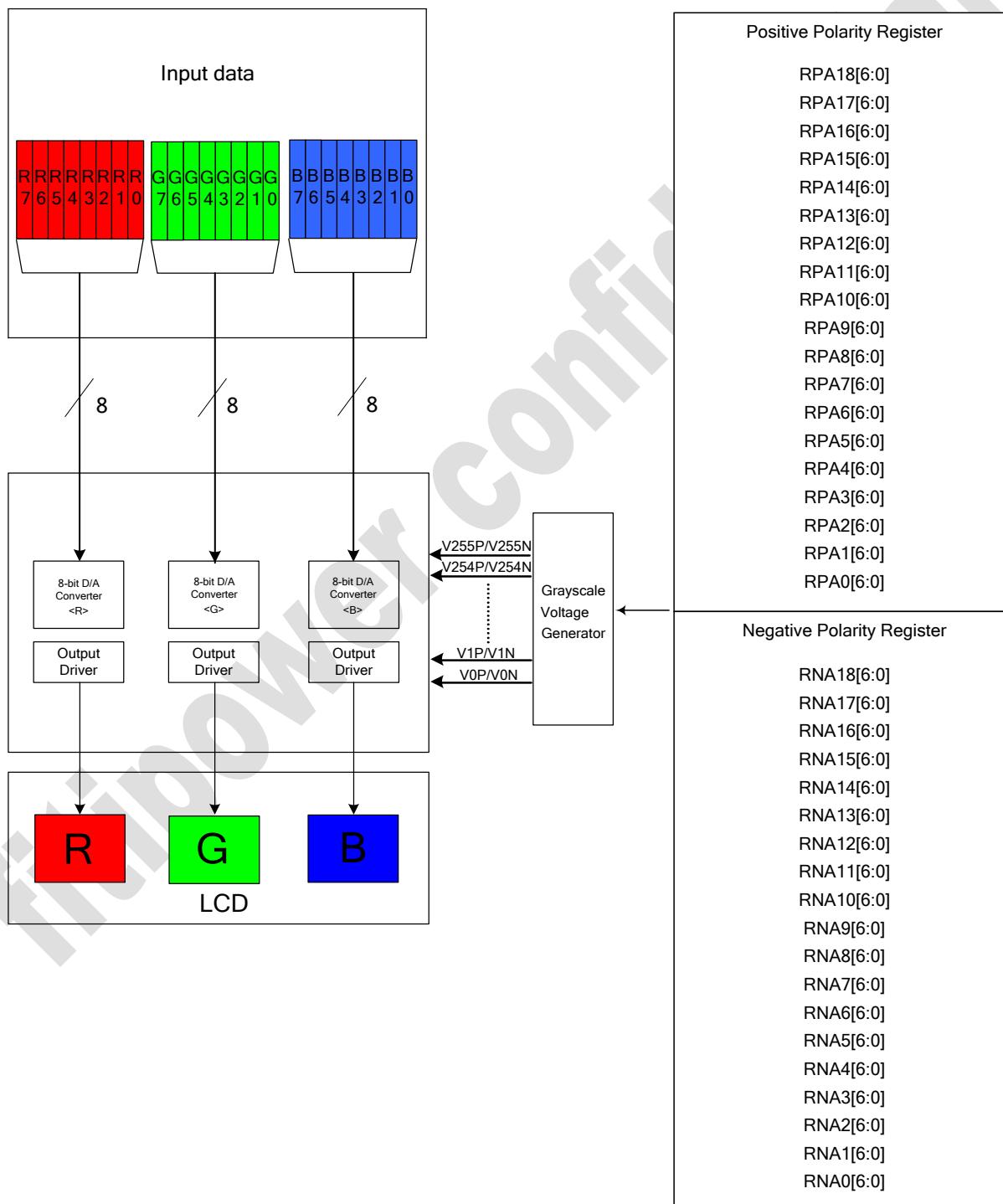


Figure 8.1: Grayscale control

## 8.2. Grayscale-Level adjustment control

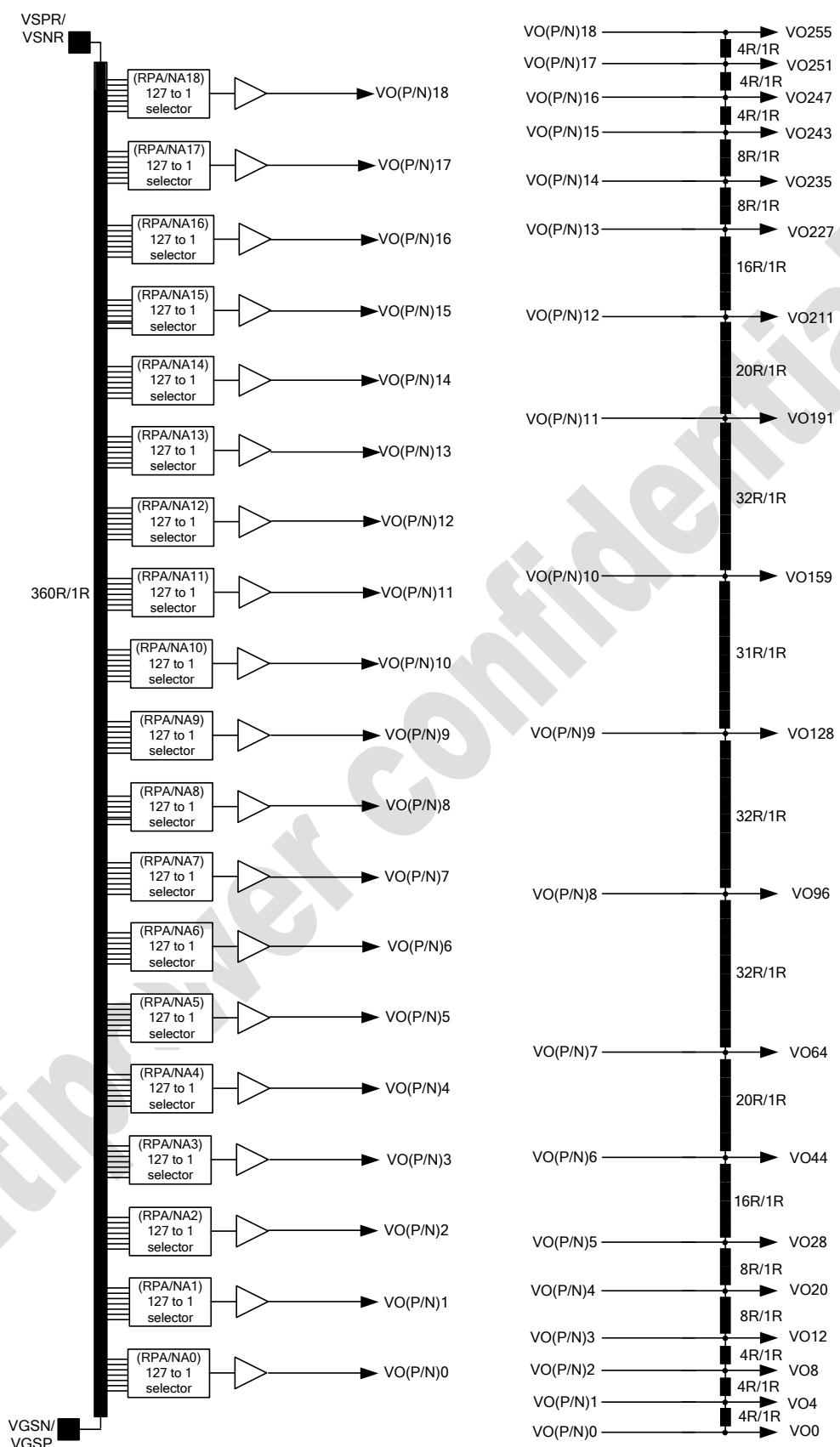
The JD9161Z has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel. These registers are belong amplitude adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently.

### Amplitude adjustment registers

The amplitude adjustment variable registers are used to adjust the amplitude of the grayscale voltage. his function is implemented by controlling the 127-to-1 selectors (RPA/RNA0~18), each one of whole has 7 bits and generates one reference voltage output (VO(P/N)0, 4, 8, 12, 20, 28, 44, 64, 96, 128, 159, 191, 211, 227, 235, 243, 247, 251, 255). These registers are available for both positive and negative polarities.

Register Groups	Positive Polarity	Negative Polarity	Description
Amplitude Adjustment	RPA18 6-0	RNA18 6-0	Variable resistor(RPA/RNA18) for VO(P/N)255
	RPA17 6-0	RNA17 6-0	Variable resistor(RPA/RNA17) for VO(P/N)251
	RPA16 6-0	RNA16 6-0	Variable resistor(RPA/RNA16) for VO(P/N)247
	RPA15 6-0	RNA15 6-0	Variable resistor(RPA/RNA15) for VO(P/N)243
	RPA14 6-0	RNA14 6-0	Variable resistor(RPA/RNA14) for VO(P/N)235
	RPA13 6-0	RNA13 6-0	Variable resistor(RPA/RNA13) for VO(P/N)227
	RPA12 6-0	RNA12 6-0	Variable resistor(RPA/RNA12) for VO(P/N)211
	RPA11 6-0	RNA11 6-0	Variable resistor(RPA/RNA11) for VO(P/N)191
	RPA10 6-0	RNA10 6-0	Variable resistor(RPA/RNA10) for VO(P/N)159
	RPA9 6-0	RNA9 6-0	Variable resistor(RPA/RNA9) for VO(P/N)128
	RPA8 6-0	RNA8 6-0	Variable resistor(RPA/RNA8) for VO(P/N)96
	RPA7 6-0	RNA7 6-0	Variable resistor(RPA/RNA7) for VO(P/N)64
	RPA6 6-0	RNA6 6-0	Variable resistor(RPA/RNA6) for VO(P/N)44
	RPA5 6-0	RNA5 6-0	Variable resistor(RPA/RNA5) for VO(P/N)28
	RPA4 6-0	RNA4 6-0	Variable resistor(RPA/RNA4) for VO(P/N)20
	RPA3 6-0	RNA3 6-0	Variable resistor(RPA/RNA3) for VO(P/N)12
	RPA2 6-0	RNA2 6-0	Variable resistor(RPA/RNA2) for VO(P/N)8
	RPA1 6-0	RNA1 6-0	Variable resistor(RPA/RNA1) for VO(P/N)4
	RPA0 6-0	RNA0 6-0	Variable resistor(RPA/RNA0) for VO(P/N)0

Table 8.1: Gamma-Adjustment registers

**Gamma resister stream and 127 to 1 selector****Figure 8.2: Gamma resister stream and gamma reference voltage**

### 8.2.1. Variable resistor ratio & Voltage levels

The resistances are decided by setting values in the Amplitude adjustment register.

The relationships are the same for RPA/RNA 0 ~18, shown below.

Value in Register RPA/RNA 0~18 (6-0)	Resistance RPA/RNA 0~18
0000000	0R
0000001	1R
0000010	2R
0000011	3R
:	:
1000000	64R
1000001	65R
1000010	66R
1000011	67R
:	:
1111100	124R
1111101	125R
1111110	126R
1111111	127R

The voltage levels are determined by the following formulas:

Reference voltage	Amplitude adjustment value	VOP15~18 formula
VOP15~18	RPA15~18 6-0 = 0000000	$((360R-128R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA15~18 6-0 = 0000001	$((360R-127R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA15~18 6-0 = 0000010	$((360R-126R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA15~18 6-0 = 0000011	$((360R-125R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA15~18 6-0 = 0000100	$((360R-124R) / 360R) * (VGMP - VGSP) + VGSP$
	:	:
	RPA15~18 6-0 = 1000000	$((360R-64R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA15~18 6-0 = 1000001	$((360R-63R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA15~18 6-0 = 1000010	$((360R-62R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA15~18 6-0 = 1000011	$((360R-61R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA15~18 6-0 = 1000100	$((360R-60R) / 360R) * (VGMP - VGSP) + VGSP$
	:	:
	RPA15~18 6-0 = 1111011	$((360R-5R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA15~18 6-0 = 1111100	$((360R-4R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA15~18 6-0 = 1111101	$((360R-3R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA15~18 6-0 = 1111110	$((360R-2R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA15~18 6-0 = 1111111	$((360R-1R) / 360R) * (VGMP - VGSP) + VGSP$

Table 8.2: VOP15~18

Reference voltage	Amplitude adjustment value	VOP13/VOP14 formula
VOP13/VOP14	RPA13/14 6-0 = 0000000	$((344R-128R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA13/14 6-0 = 0000001	$((344R-127R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA13/14 6-0 = 0000010	$((344R-126R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA13/14 6-0 = 0000011	$((344R-125R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA13/14 6-0 = 0000100	$((344R-124R) / 360R) * (VGMP - VGSP) + VGSP$
	:	:
	RPA13/14 6-0 = 1000000	$((344R-64R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA13/14 6-0 = 1000001	$((344R-63R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA13/14 6-0 = 1000010	$((344R-62R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA13/14 6-0 = 1000011	$((344R-61R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA13/14 6-0 = 1000100	$((344R-60R) / 360R) * (VGMP - VGSP) + VGSP$
	:	:
	RPA13/14 6-0 = 1111011	$((344R-5R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA13/14 6-0 = 1111100	$((344R-4R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA13/14 6-0 = 1111101	$((344R-3R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA13/14 6-0 = 1111110	$((344R-2R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA13/14 6-0 = 1111111	$((344R-1R) / 360R) * (VGMP - VGSP) + VGSP$

Table 8.3: VOP13/VOP14

Reference voltage	Amplitude adjustment value	VOP11/VOP12 formula
VOP11/VOP12	RPA11/12 6-0 = 0000000	$((316R-128R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA11/12 6-0 = 0000001	$((316R-127R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA11/12 6-0 = 0000010	$((316R-126R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA11/12 6-0 = 0000011	$((316R-125R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA11/12 6-0 = 0000100	$((316R-124R) / 360R) * (VGMP - VGSP) + VGSP$
	:	:
	RPA11/12 6-0 = 1000000	$((316R-64R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA11/12 6-0 = 1000001	$((316R-63R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA11/12 6-0 = 1000010	$((316R-62R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA11/12 6-0 = 1000011	$((316R-61R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA11/12 6-0 = 1000100	$((316R-60R) / 360R) * (VGMP - VGSP) + VGSP$
	:	:
	RPA11/12 6-0 = 1111011	$((316R-5R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA11/12 6-0 = 1111100	$((316R-4R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA11/12 6-0 = 1111101	$((316R-3R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA11/12 6-0 = 1111110	$((316R-2R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA11/12 6-0 = 1111111	$((316R-1R) / 360R) * (VGMP - VGSP) + VGSP$

Table 8.4: VOP11/VOP12

Reference voltage	Amplitude adjustment value	VOP10 formula
VOP10	RPA10 6-0 = 0000000	$((264R-128R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA10 6-0 = 0000001	$((264R-127R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA10 6-0 = 0000010	$((264R-126R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA10 6-0 = 0000011	$((264R-125R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA10 6-0 = 0000100	$((264R-124R) / 360R) * (VGMP - VGSP) + VGSP$
	:	:
	RPA10 6-0 = 1000000	$((264R-64R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA10 6-0 = 1000001	$((264R-63R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA10 6-0 = 1000010	$((264R-62R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA10 6-0 = 1000011	$((264R-61R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA10 6-0 = 1000100	$((264R-60R) / 360R) * (VGMP - VGSP) + VGSP$
	:	:
	RPA10 6-0 = 1111011	$((264R-5R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA10 6-0 = 1111100	$((264R-4R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA10 6-0 = 1111101	$((264R-3R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA10 6-0 = 1111110	$((264R-2R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA10 6-0 = 1111111	$((264R-1R) / 360R) * (VGMP - VGSP) + VGSP$

Table 8.5: VOP10

Reference voltage	Amplitude adjustment value	VOP9 formula
VOP9	RPA9 6-0 = 0000000	$((244R-128R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA9 6-0 = 0000001	$((244R-127R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA9 6-0 = 0000010	$((244R-126R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA9 6-0 = 0000011	$((244R-125R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA9 6-0 = 0000100	$((244R-124R) / 360R) * (VGMP - VGSP) + VGSP$
	:	:
	RPA9 6-0 = 1000000	$((244R-64R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA9 6-0 = 1000001	$((244R-63R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA9 6-0 = 1000010	$((244R-62R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA9 6-0 = 1000011	$((244R-61R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA9 6-0 = 1000100	$((244R-60R) / 360R) * (VGMP - VGSP) + VGSP$
	:	:
	RPA9 6-0 = 1111011	$((244R-5R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA9 6-0 = 1111100	$((244R-4R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA9 6-0 = 1111101	$((244R-3R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA9 6-0 = 1111110	$((244R-2R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA9 6-0 = 1111111	$((244R-1R) / 360R) * (VGMP - VGSP) + VGSP$

Table 8.6: VOP9

Reference voltage	Amplitude adjustment value	VOP8 formula
VOP8	RPA8 6-0 = 0000000	$((224R-128R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA8 6-0 = 0000001	$((224R-127R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA8 6-0 = 0000010	$((224R-126R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA8 6-0 = 0000011	$((224R-125R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA8 6-0 = 0000100	$((224R-124R) / 360R) * (VGMP - VGSP) + VGSP$
	:	:
	RPA8 6-0 = 1000000	$((224R-64R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA8 6-0 = 1000001	$((224R-63R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA8 6-0 = 1000010	$((224R-62R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA8 6-0 = 1000011	$((224R-61R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA8 6-0 = 1000100	$((224R-60R) / 360R) * (VGMP - VGSP) + VGSP$
	:	:
	RPA8 6-0 = 1111011	$((224R-5R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA8 6-0 = 1111100	$((224R-4R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA8 6-0 = 1111101	$((224R-3R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA8 6-0 = 1111110	$((224R-2R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA8 6-0 = 1111111	$((224R-1R) / 360R) * (VGMP - VGSP) + VGSP$

Table 8.7: VOP8

Reference voltage	Amplitude adjustment value	VOP6/ VOP7 formula
VOP6/ VOP7	RPA6/7 6-0 = 0000000	$((172R-128R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA6/7 6-0 = 0000001	$((172R-127R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA6/7 6-0 = 0000010	$((172R-126R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA6/7 6-0 = 0000011	$((172R-125R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA6/7 6-0 = 0000100	$((172R-124R) / 360R) * (VGMP - VGSP) + VGSP$
	:	:
	RPA6/7 6-0 = 1000000	$((172R-64R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA6/7 6-0 = 1000001	$((172R-63R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA6/7 6-0 = 1000010	$((172R-62R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA6/7 6-0 = 1000011	$((172R-61R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA6/7 6-0 = 1000100	$((172R-60R) / 360R) * (VGMP - VGSP) + VGSP$
	:	:
	RPA6/7 6-0 = 1111011	$((172R-5R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA6/7 6-0 = 1111100	$((172R-4R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA6/7 6-0 = 1111101	$((172R-3R) / 360R) * (VGMP - VGSP) + VGSP$
	VRP6/7 6-0 = 1111110	$((172R-2R) / 360R) * (VGMP - VGSP) + VGSP$
	VRP6/7 6-0 = 1111111	$((172R-1R) / 360R) * (VGMP - VGSP) + VGSP$

Table 8.8: VOP6/ VOP7

Reference voltage	Amplitude adjustment value	VOP4/ VOP5 formula
VOP4/ VOP5	RPA4/5 6-0 = 0000000	$((144R-128R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA4/5 6-0 = 0000001	$((144R-127R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA4/5 6-0 = 0000010	$((144R-126R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA4/5 6-0 = 0000011	$((144R-125R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA4/5 6-0 = 0000100	$((144R-124R) / 360R) * (VGMP - VGSP) + VGSP$
	:	:
	RPA4/5 6-0 = 1000000	$((144R-64R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA4/5 6-0 = 1000001	$((144R-63R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA4/5 6-0 = 1000010	$((144R-62R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA4/5 6-0 = 1000011	$((144R-61R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA4/5 6-0 = 1000100	$((144R-60R) / 360R) * (VGMP - VGSP) + VGSP$
	:	:
	RPA4/5 6-0 = 1111011	$((144R-5R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA4/5 6-0 = 1111100	$((144R-4R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA4/5 6-0 = 1111101	$((144R-3R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA4/5 6-0 = 1111110	$((144R-2R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA4/5 6-0 = 1111111	$((144R-1R) / 360R) * (VGMP - VGSP) + VGSP$

Table 8.9: VOP4/ VOP5

Reference voltage	Amplitude adjustment value	VOP0~3 formula
VOP0~3	RPA0~3 6-0 = 0000000	$((128R-128R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA0~3 6-0 = 0000001	$((128R-127R) / 360R) * (VGMP - VGSP) + VGSP$
	VRP0~3 6-0 = 0000010	$((128R-126R) / 360R) * (VGMP - VGSP) + VGSP$
	VRP0~3 6-0 = 0000011	$((128R-125R) / 360R) * (VGMP - VGSP) + VGSP$
	VRP0~3 6-0 = 0000100	$((128R-124R) / 360R) * (VGMP - VGSP) + VGSP$
	:	:
	RPA0~3 6-0 = 1000000	$((128R-64R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA0~3 6-0 = 1000001	$((128R-63R) / 360R) * (VGMP - VGSP) + VGSP$
	VRP0~3 6-0 = 1000010	$((128R-62R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA0~3 6-0 = 1000011	$((128R-61R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA0~3 6-0 = 1000100	$((128R-60R) / 360R) * (VGMP - VGSP) + VGSP$
	:	:
	RPA0~3 6-0 = 1111011	$((128R-5R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA0~3 6-0 = 1111100	$((128R-4R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA0~3 6-0 = 1111101	$((128R-3R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA0~3 6-0 = 1111110	$((128R-2R) / 360R) * (VGMP - VGSP) + VGSP$
	RPA0~3 6-0 = 1111111	$((128R-1R) / 360R) * (VGMP - VGSP) + VGSP$

Table 8.10: VOP0~3

Reference voltage	Amplitude adjustment value	VON15~18 formula
VON15~18	RNA15~18 6-0 = 0000000	$((360R-128R) / 360R) * (VGNN - VGSN) + VGSN$
	RNA15~18 6-0 = 0000001	$((360R-127R) / 360R) * (VGNN - VGSN) + VGSN$
	RNA15~18 6-0 = 0000010	$((360R-126R) / 360R) * (VGNN - VGSN) + VGSN$
	RNA15~18 6-0 = 0000011	$((360R-125R) / 360R) * (VGNN - VGSN) + VGSN$
	RNA15~18 6-0 = 0000100	$((360R-124R) / 360R) * (VGNN - VGSN) + VGSN$
	:	:
	RNA15~18 6-0 = 1000000	$((360R-64R) / 360R) * (VGNN - VGSN) + VGSN$
	RNA15~18 6-0 = 1000001	$((360R-63R) / 360R) * (VGNN - VGSN) + VGSN$
	RNA15~18 6-0 = 1000010	$((360R-62R) / 360R) * (VGNN - VGSN) + VGSN$
	RNA15~18 6-0 = 1000011	$((360R-61R) / 360R) * (VGNN - VGSN) + VGSN$
	RNA15~18 6-0 = 1000100	$((360R-60R) / 360R) * (VGNN - VGSN) + VGSN$
	:	:
	RNA15~18 6-0 = 1111011	$((360R-5R) / 360R) * (VGNN - VGSN) + VGSN$
	RNA15~18 6-0 = 1111100	$((360R-4R) / 360R) * (VGNN - VGSN) + VGSN$
	RNA15~18 6-0 = 1111101	$((360R-3R) / 360R) * (VGNN - VGSN) + VGSN$
	RNA15~18 6-0 = 1111110	$((360R-2R) / 360R) * (VGNN - VGSN) + VGSN$
	RNA15~18 6-0 = 1111111	$((360R-1R) / 360R) * (VGNN - VGSN) + VGSN$

Table 8.11: VON15~18

Reference voltage	Amplitude adjustment value	VON13/VON14 formula
VON13/VON14	RNA13/14 6-0 = 0000000	$((344R-128R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA13/14 6-0 = 0000001	$((344R-127R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA13/14 6-0 = 0000010	$((344R-126R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA13/14 6-0 = 0000011	$((344R-125R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA13/14 6-0 = 0000100	$((344R-124R) / 360R) * (VGMN - VGSN) + VGSN$
	:	:
	RNA13/14 6-0 = 1000000	$((344R-64R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA13/14 6-0 = 1000001	$((344R-63R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA13/14 6-0 = 1000010	$((344R-62R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA13/14 6-0 = 1000011	$((344R-61R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA13/14 6-0 = 1000100	$((344R-60R) / 360R) * (VGMN - VGSN) + VGSN$
	:	:
	RNA13/14 6-0 = 1111011	$((344R-5R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA13/14 6-0 = 1111100	$((344R-4R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA13/14 6-0 = 1111101	$((344R-3R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA13/14 6-0 = 1111110	$((344R-2R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA13/14 6-0 = 1111111	$((344R-1R) / 360R) * (VGMN - VGSN) + VGSN$

Table 8.12: VON13/VON14

Reference voltage	Amplitude adjustment value	VON11/VON12 formula
VON11/VON12	RNA11/12 6-0 = 0000000	$((316R-128R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA11/12 6-0 = 0000001	$((316R-127R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA11/12 6-0 = 0000010	$((316R-126R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA11/12 6-0 = 0000011	$((316R-125R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA11/12 6-0 = 0000100	$((316R-124R) / 360R) * (VGMN - VGSN) + VGSN$
	:	:
	RNA11/12 6-0 = 1000000	$((316R-64R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA11/12 6-0 = 1000001	$((316R-63R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA11/12 6-0 = 1000010	$((316R-62R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA11/12 6-0 = 1000011	$((316R-61R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA11/12 6-0 = 1000100	$((316R-60R) / 360R) * (VGMN - VGSN) + VGSN$
	:	:
	RNA11/12 6-0 = 1111011	$((316R-5R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA11/12 6-0 = 1111100	$((316R-4R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA11/12 6-0 = 1111101	$((316R-3R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA11/12 6-0 = 1111110	$((316R-2R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA11/12 6-0 = 1111111	$((316R-1R) / 360R) * (VGMN - VGSN) + VGSN$

Table 8.13: VON11/VON12

Reference voltage	Amplitude adjustment value	VON10 formula
VON10	RNA10 6-0 = 0000000	$((264R-128R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA10 6-0 = 0000001	$((264R-127R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA10 6-0 = 0000010	$((264R-126R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA10 6-0 = 0000011	$((264R-125R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA10 6-0 = 0000100	$((264R-124R) / 360R) * (VGMN - VGSN) + VGSN$
	:	:
	RNA10 6-0 = 1000000	$((264R-64R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA10 6-0 = 1000001	$((264R-63R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA10 6-0 = 1000010	$((264R-62R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA10 6-0 = 1000011	$((264R-61R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA10 6-0 = 1000100	$((264R-60R) / 360R) * (VGMN - VGSN) + VGSN$
	:	:
	RNA10 6-0 = 1111011	$((264R-5R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA10 6-0 = 1111100	$((264R-4R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA10 6-0 = 1111101	$((264R-3R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA10 6-0 = 1111110	$((264R-2R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA10 6-0 = 1111111	$((264R-1R) / 360R) * (VGMN - VGSN) + VGSN$

Table 8.14: VON10

Reference voltage	Amplitude adjustment value	VON9 formula
VON9	RNA9 6-0 = 0000000	$((244R-128R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA9 6-0 = 0000001	$((244R-127R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA9 6-0 = 0000010	$((244R-126R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA9 6-0 = 0000011	$((244R-125R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA9 6-0 = 0000100	$((244R-124R) / 360R) * (VGMN - VGSN) + VGSN$
	:	:
	RNA9 6-0 = 1000000	$((244R-64R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA9 6-0 = 1000001	$((244R-63R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA9 6-0 = 1000010	$((244R-62R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA9 6-0 = 1000011	$((244R-61R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA9 6-0 = 1000100	$((244R-60R) / 360R) * (VGMN - VGSN) + VGSN$
	:	:
	RNA9 6-0 = 1111011	$((244R-5R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA9 6-0 = 1111100	$((244R-4R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA9 6-0 = 1111101	$((244R-3R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA9 6-0 = 1111110	$((244R-2R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA9 6-0 = 1111111	$((244R-1R) / 360R) * (VGMN - VGSN) + VGSN$

Table 8.15: VON9

Reference voltage	Amplitude adjustment value	VON8 formula
VON8	RNA8 6-0 = 0000000	$((224R-128R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA8 6-0 = 0000001	$((224R-127R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA8 6-0 = 0000010	$((224R-126R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA8 6-0 = 0000011	$((224R-125R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA8 6-0 = 0000100	$((224R-124R) / 360R) * (VGMN - VGSN) + VGSN$
	:	:
	RNA8 6-0 = 1000000	$((224R-64R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA8 6-0 = 1000001	$((224R-63R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA8 6-0 = 1000010	$((224R-62R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA8 6-0 = 1000011	$((224R-61R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA8 6-0 = 1000100	$((224R-60R) / 360R) * (VGMN - VGSN) + VGSN$
	:	:
	RNA8 6-0 = 1111011	$((224R-5R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA8 6-0 = 1111100	$((224R-4R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA8 6-0 = 1111101	$((224R-3R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA8 6-0 = 1111110	$((224R-2R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA8 6-0 = 1111111	$((224R-1R) / 360R) * (VGMN - VGSN) + VGSN$

Table 8.16: VON8

Reference voltage	Amplitude adjustment value	VON6/ VON7 formula
VON6/ VON7	RNA6/7 6-0 = 0000000	$((172R-128R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA6/7 6-0 = 0000001	$((172R-127R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA6/7 6-0 = 0000010	$((172R-126R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA6/7 6-0 = 0000011	$((172R-125R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA6/7 6-0 = 0000100	$((172R-124R) / 360R) * (VGMN - VGSN) + VGSN$
	:	:
	RNA6/7 6-0 = 1000000	$((172R-64R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA6/7 6-0 = 1000001	$((172R-63R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA6/7 6-0 = 1000010	$((172R-62R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA6/7 6-0 = 1000011	$((172R-61R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA6/7 6-0 = 1000100	$((172R-60R) / 360R) * (VGMN - VGSN) + VGSN$
	:	:
	RNA6/7 6-0 = 1111011	$((172R-5R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA6/7 6-0 = 1111100	$((172R-4R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA6/7 6-0 = 1111101	$((172R-3R) / 360R) * (VGMN - VGSN) + VGSN$
	VRN6/7 6-0 = 1111110	$((172R-2R) / 360R) * (VGMN - VGSN) + VGSN$
	VRN6/7 6-0 = 1111111	$((172R-1R) / 360R) * (VGMN - VGSN) + VGSN$

Table 8.17: VON6/ VON7

Reference voltage	Amplitude adjustment value	VON4/ VON5 formula
VON4/ VON5	RNA4/5 6-0 = 0000000	$((144R-128R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA4/5 6-0 = 0000001	$((144R-127R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA4/5 6-0 = 0000010	$((144R-126R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA4/5 6-0 = 0000011	$((144R-125R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA4/5 6-0 = 0000100	$((144R-124R) / 360R) * (VGMN - VGSN) + VGSN$
	:	:
	RNA4/5 6-0 = 1000000	$((144R-64R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA4/5 6-0 = 1000001	$((144R-63R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA4/5 6-0 = 1000010	$((144R-62R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA4/5 6-0 = 1000011	$((144R-61R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA4/5 6-0 = 1000100	$((144R-60R) / 360R) * (VGMN - VGSN) + VGSN$
	:	:
	RNA4/5 6-0 = 1111011	$((144R-5R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA4/5 6-0 = 1111100	$((144R-4R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA4/5 6-0 = 1111101	$((144R-3R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA4/5 6-0 = 1111110	$((144R-2R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA4/5 6-0 = 1111111	$((144R-1R) / 360R) * (VGMN - VGSN) + VGSN$

Table 8.18: VON4/ VON5

Reference voltage	Amplitude adjustment value	VON0~3 formula
VON0~3	RNA0~3 6-0 = 0000000	$((128R-128R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA0~3 6-0 = 0000001	$((128R-127R) / 360R) * (VGMN - VGSN) + VGSN$
	VRN0~3 6-0 = 0000010	$((128R-126R) / 360R) * (VGMN - VGSN) + VGSN$
	VRN0~3 6-0 = 0000011	$((128R-125R) / 360R) * (VGMN - VGSN) + VGSN$
	VRN0~3 6-0 = 0000100	$((128R-124R) / 360R) * (VGMN - VGSN) + VGSN$
	:	:
	RNA0~3 6-0 = 1000000	$((128R-64R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA0~3 6-0 = 1000001	$((128R-63R) / 360R) * (VGMN - VGSN) + VGSN$
	VRN0~3 6-0 = 1000010	$((128R-62R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA0~3 6-0 = 1000011	$((128R-61R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA0~3 6-0 = 1000100	$((128R-60R) / 360R) * (VGMN - VGSN) + VGSN$
	:	:
	RNA0~3 6-0 = 1111011	$((128R-5R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA0~3 6-0 = 1111100	$((128R-4R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA0~3 6-0 = 1111101	$((128R-3R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA0~3 6-0 = 1111110	$((128R-2R) / 360R) * (VGMN - VGSN) + VGSN$
	RNA0~3 6-0 = 1111111	$((128R-1R) / 360R) * (VGMN - VGSN) + VGSN$

Table 8.19: VON0~3

## 9. Function Description

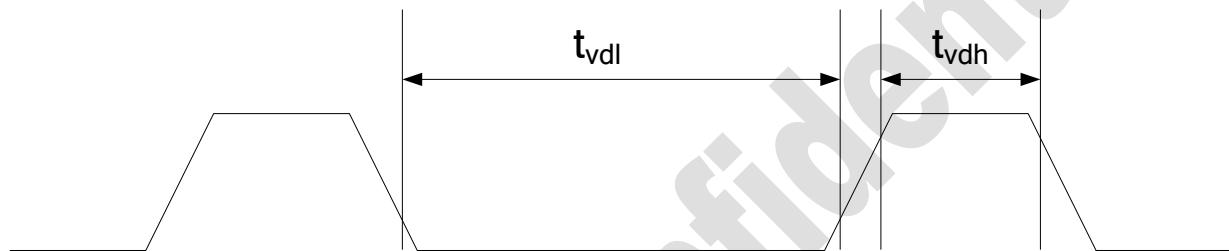
### 9.1. Tearing effect Line

#### 9.1.1. Tearing effect Line mode

The Tearing Effect line supplies to the MPU a Panel synchronization signal and this signal can be enabled or disabled by the Tearing Effect Line Off & On commands. It can be used by the MPU to synchronize GRAM Writing when displaying video images. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command.

#### Tearing Effect Line Modes

**Mode 1**, the Tearing Effect Output signal consists of V-Blanking Information only:



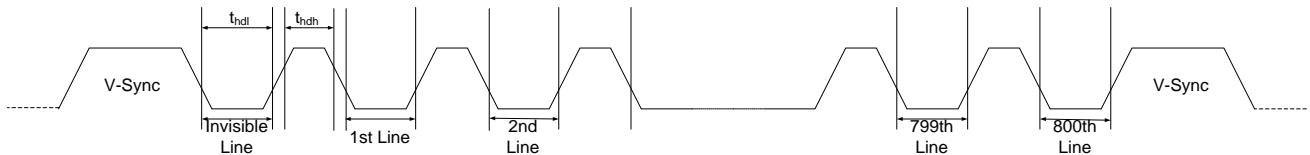
**Figure 9.1: Tearing Effect Line mode 1**

$t_{vdh}$ = The LCD display is not updated from the Frame Memory

$t_{vdl}$ = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

**Mode 2**, the Tearing Effect Output signal consists of V-sync and H-sync Information, there is one V-sync and N H-sync pulses per field.

N: If the resolution is 480 RGB X 800, the N=800.



**Figure 9.2: Tearing Effect Line mode 2**

t<sub>vh</sub>= The LCD display is not updated from the Frame Memory

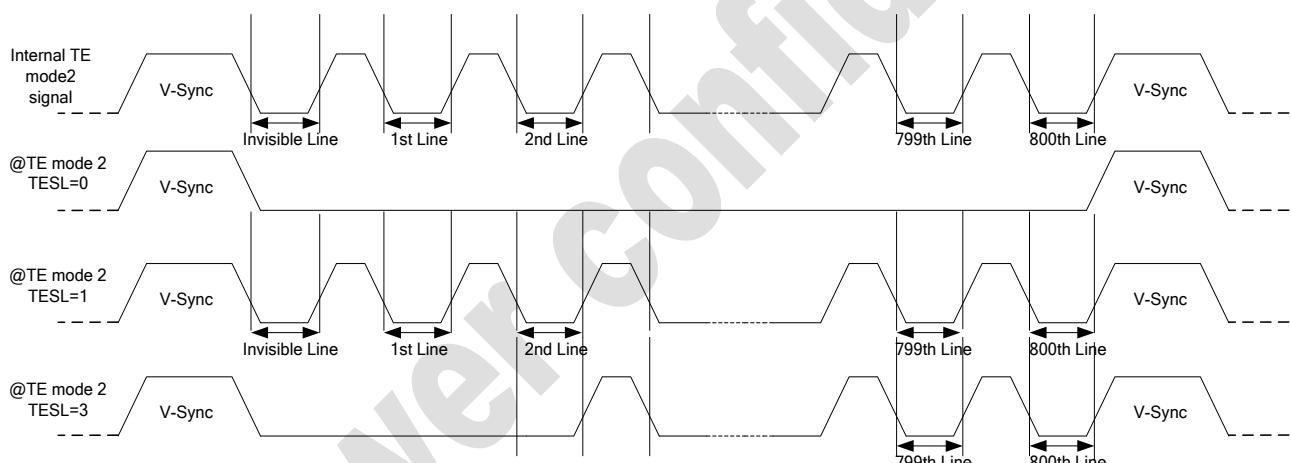
t<sub>thd</sub>= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

The H-sync pulses output amount will be defined by TESL [15:0] setting under Mode2.

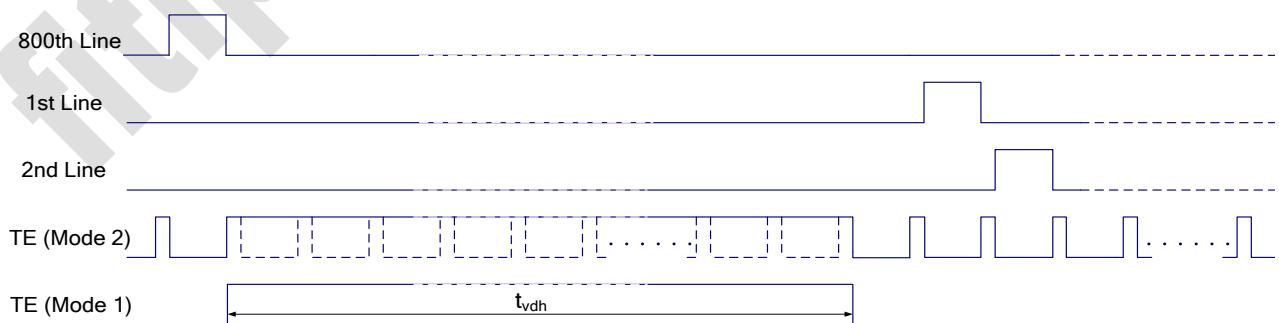
Ex: 1. TESL [15:0]=0, then TE signal will the same as TE mode 1.

TESL [15:0]=1, then TE signal will output 800 H-sync.

TESL [15:0]=3, then TE signal will output 798 H-sync.



**Figure 9.3: TE Line Output for TELINE setting**

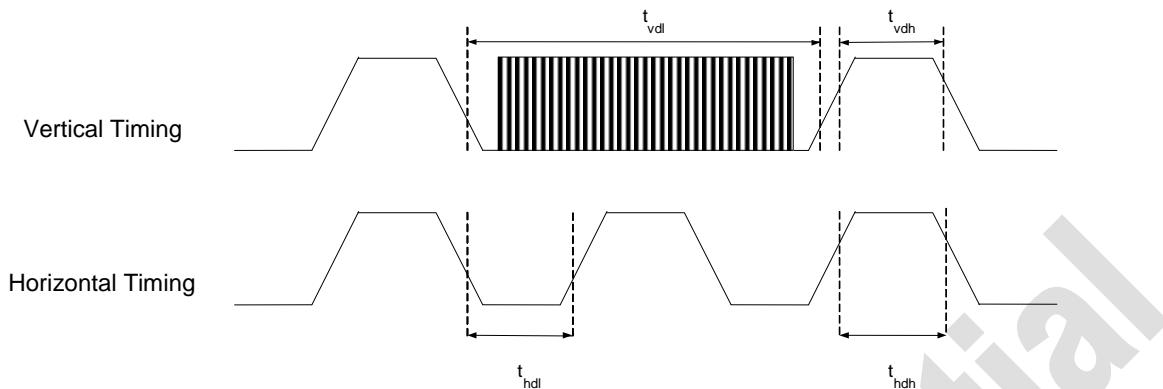


**Figure 9.4: Tearing Effect Line Output signal**

Note: During Sleep In Mode, the Tearing Output Pin is active Low

### 9.1.2. Tearing effect line timing

The Tearing Effect signal is described below:



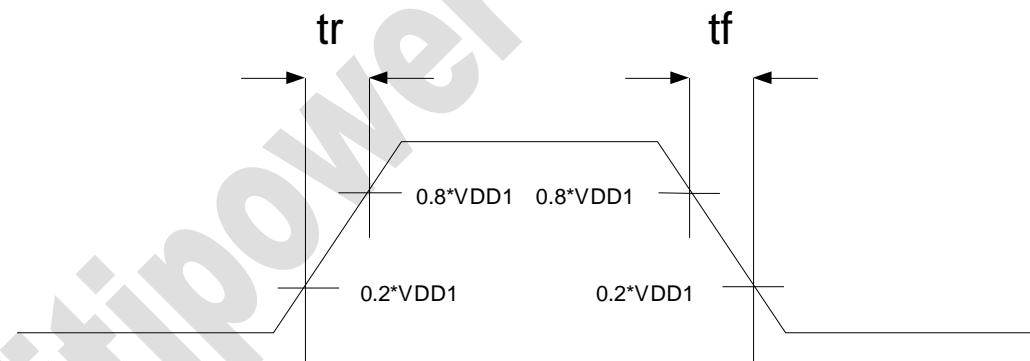
**Figure 9.5: Tearing Effect Line timing**

Idle Mode Off/On (Resolution 480x800 RGB, Frame Rate = 60 Hz)

Symbol	Parameter	Min.	Max.	Unit
tvd़l	Vertical Timing Low Duration	TBD	-	ms
tvd़h	Vertical Timing High Duration	1000	-	us
thd़l	Horizontal Timing Low Duration	TBD	-	us
thd़h	Horizontal Timing High Duration	TBD	500	us
tr	Rise time	-	15	ns
tf	Fall time	-	15	Ns

**Table 9.1: AC characteristics of Tearing Effect Line**

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



**Figure 9.6: Tearing Effect Line definition of tf, tr**

## 9.2. Oscillator

The JD9161Z has an internal R-C oscillator. The oscillator frequency is 32MHz and tolerance is 5%. The oscillation frequency can be adjusted according to internal register setting.

## 9.3. Output pins Characteristics

Pin name	After power on	After hardware reset	After software reset
TE_L, TE_R	Low	Low	Low
LEDPWM, LEDON	Low	Low	Low

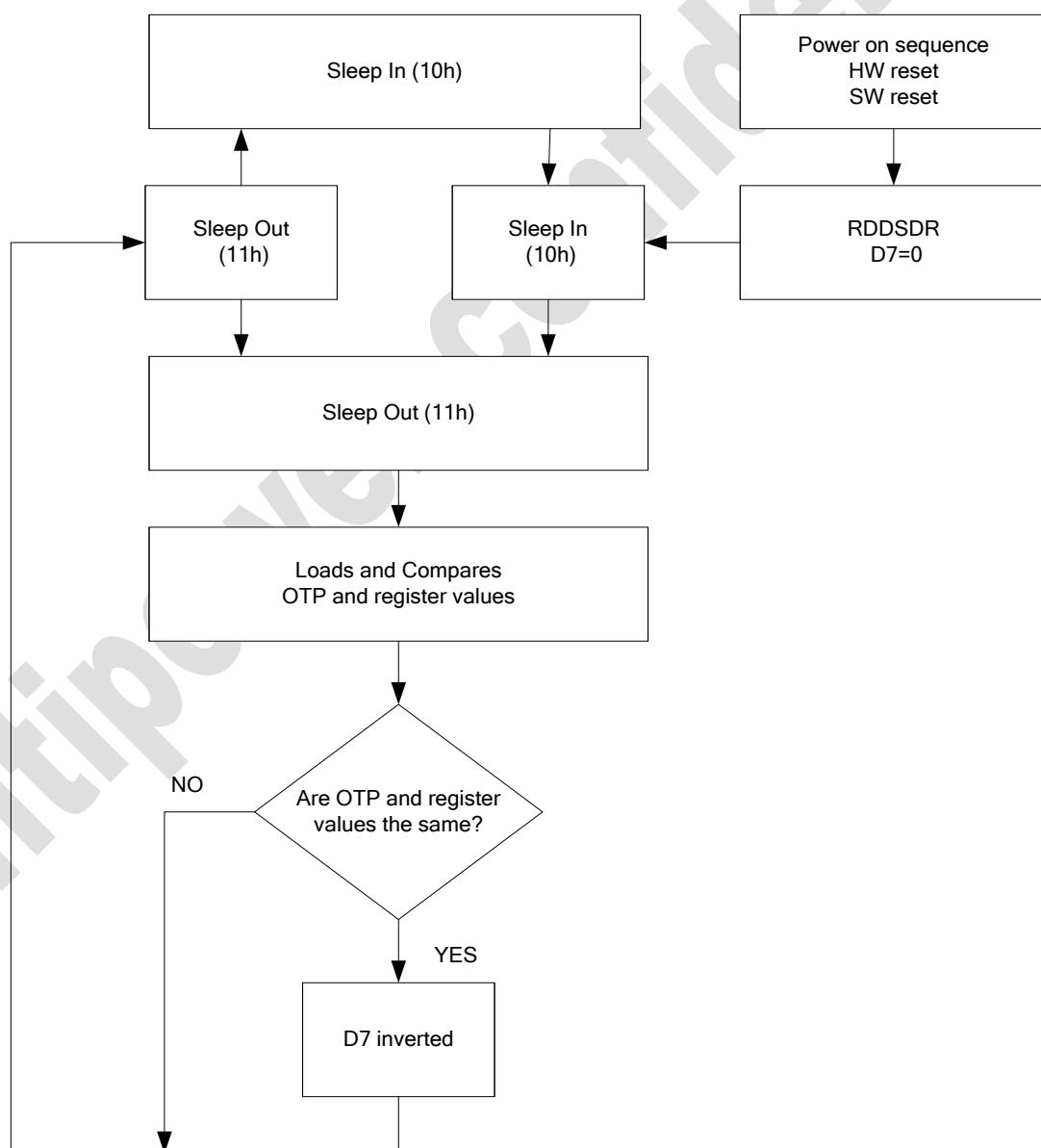
Table 9.2: Output and I/O pins Characteristics

## 9.4. Self-diagnostic Functions

The display module shall support all the self-diagnostic functions in this section except those functions indicated as optional. Optional functions can be implemented in the display module at the manufacturer's discretion.

### 9.4.1. Register loading detection

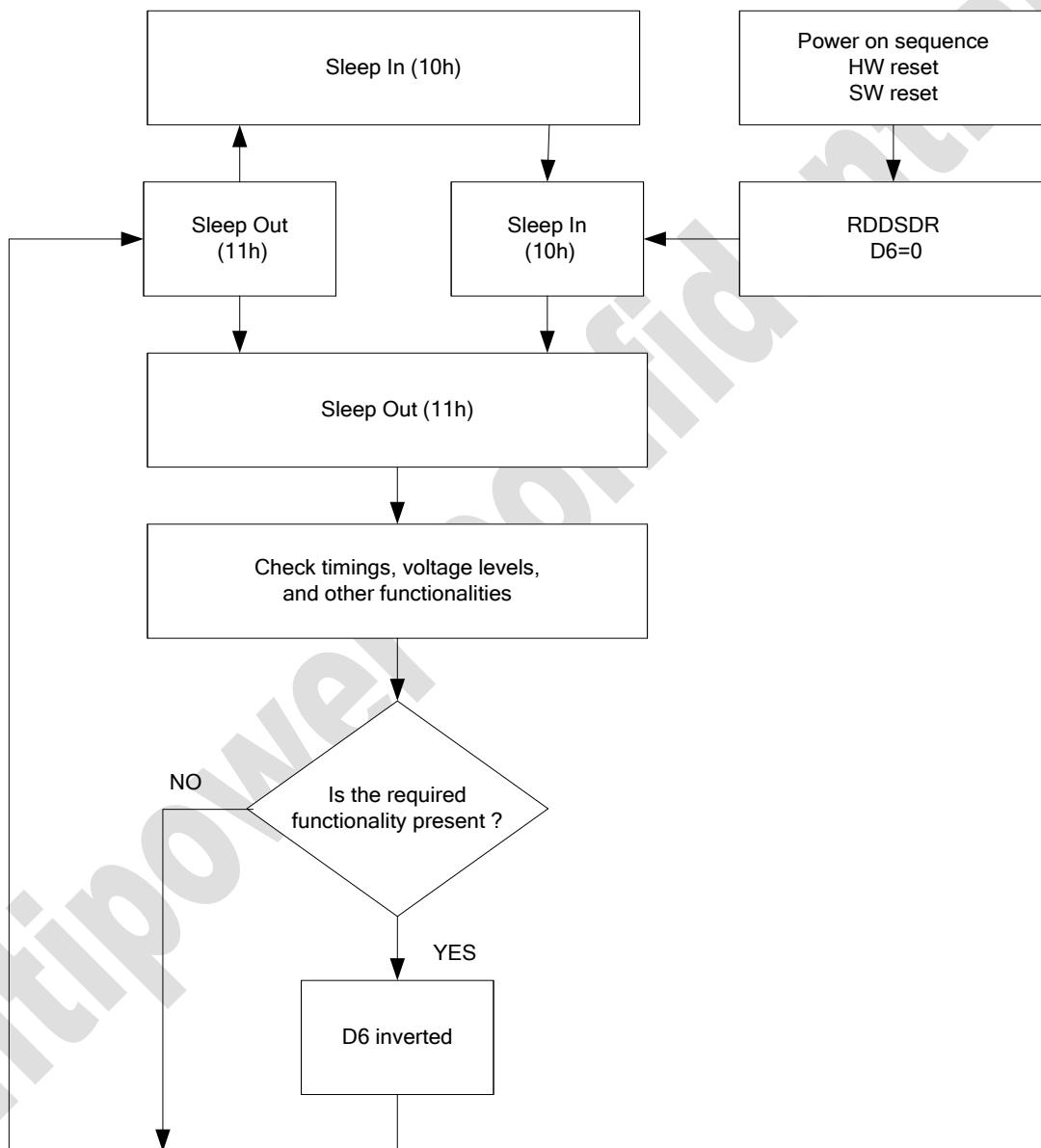
The SLPOUT command (See "SLPOUT: Exit Sleep In Mode (11h)") is a trigger for the Register Loading Detection function. This function indicates if the display module correctly loaded the factory default values from Non-volatile memory to the registers. If the registers were loaded properly then bit D7 of the SDR register is inverted, otherwise the value is unchanged. See RDDSDR: Read Display Self-Diagnostic Result (0Fh) for a description of the RDDSDR register. The flow chart for the Register Loading Detection function is shown in Figure 9.8.



**Figure 9.7: Register loading detection flow chart**

#### 9.4.2. Functionality Detection

The SLPOUT command (see SLPOUT: Exit Sleep In Mode (11h)) is a trigger for the Functionality Detection function. This function indicates if the display module functional blocks, e.g. power supply, clock generator, etc. are operating correctly. If the functional blocks are operating properly then bit D6 of the RDDSDR register is inverted, otherwise the value is unchanged. See RDDSDR: Read Display Self-Diagnostic Result (0Fh) for a description of the RDDSDR register. The flow chart for the Functionality Detection function is shown in Figure 9.8.



**Note:** There is needed 120msec after SLPOUT command, when there is changing from SLPIN mode to SLPOUT mode, before there is possible to check if Customer's functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when SLIPOT command is sent in SLPOUT mode.

**Figure 9.8: Functionality detection flow chart**

## **9.5. Power on/off sequence**

### **9.5.1. General**

During power off, if the display module is in the SLPOUT mode, VCI, VCIP and IOVCC must be powered down minimum 120msec after RESX has been released.

During power off, if the display module is in the SLPIN mode, VCI, VCIP and IOVCC can be powered down minimum 0msec after RESX has been released.

There will be no damage to the display module if the power sequences are not met.

There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

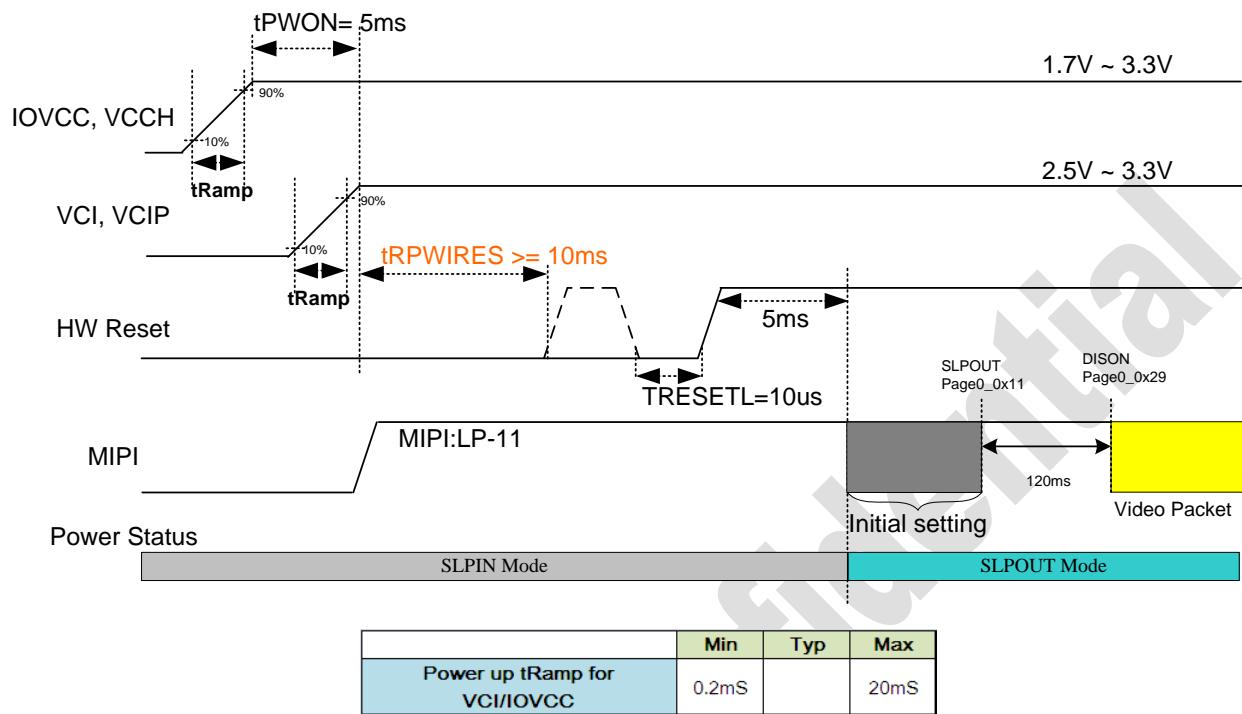
There will be no abnormal visible effects on the display panel between end of Power On Sequence and before receiving SLPOUT command. Also between receiving SLPOUT command and Power Off Sequence.

If RESX line is not held stable by host during Power On Sequence as defined in Sections 9.5.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

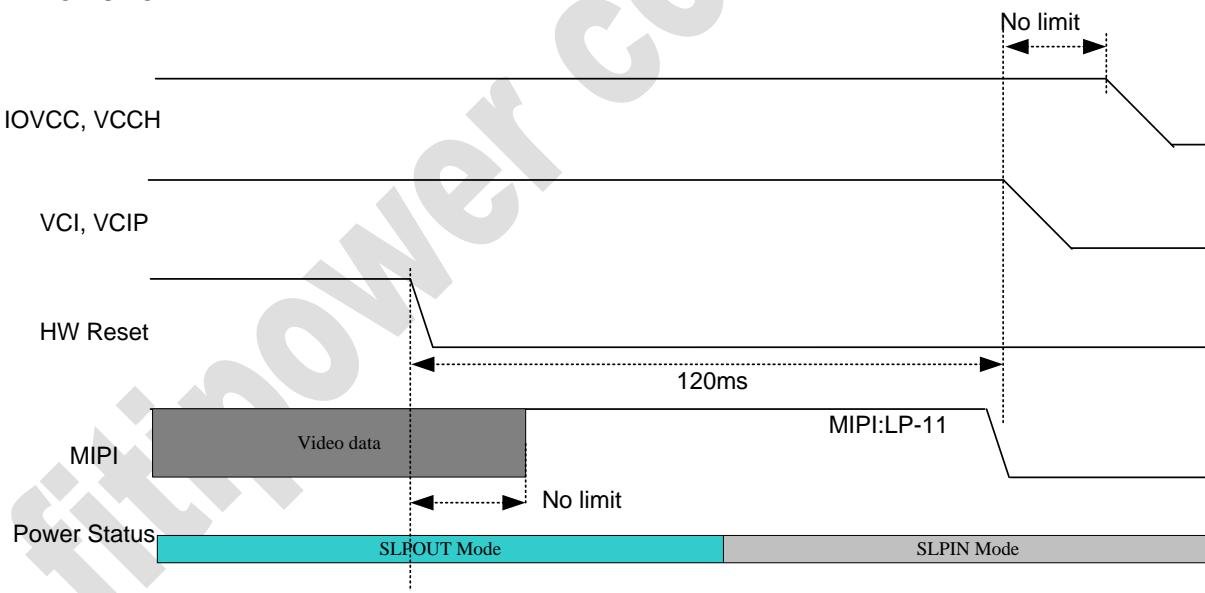
There is not a limit for Rise/Fall time on VCI, VCIP and IOVCC.

### 9.5.2. Power on/off sequence

Internal DC/DC power mode IOVCC=VCCH=1.65V ~ 3.3V, VCI=VCIP=2.5V ~ 3.3V.



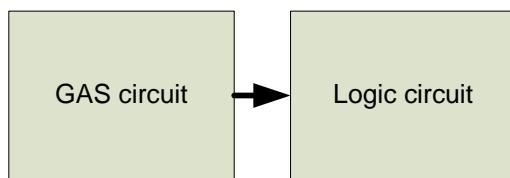
Power off:



## 9.6. Uncontrolled power off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. The display module must meet following requirements:

- There cannot be any damages for the display module or the display module cannot cause any damages for the host or lines of the interface.
- There cannot be any abnormal visible effects (= display must be blank) with in 1 second on the display and remains blank until "Power On Sequence" powers it up



## 9.7. Content adaptive brightness control (CABC) function

### 9.7.1. Definition of the CABC

A Content Adaptive Brightness Control function can be used to reduce the power consumption of the luminance source. Content adaptation means that content grey level scale can be increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted grey level scale and thus the power consumption reduction depend on the content of the image.

This function and its four different modes can be controlled. See chapter “10.2.39 Write Content Adaptive

Brightness Control (55h)” (bits: C1 and C0) for more information.

Definition of These Four Modes and Target Power Reduction Ration:

1. Off mode: Content Adaptive Brightness Control functionality is totally off.
2. UI [User interface] image mode: Optimized for UI image. It is kept image quality as much as possible. Target power consumption reduction ratio: 10% or less
3. Still picture mode: Optimized for still picture. Some image quality degradation would be acceptable. Target power consumption reduction ratio: more than 30%
4. Moving image mode: Optimized for moving image e.g. Video clip. It is focused on the biggest power reduction with image quality degradation. Target power consumption reduction ratio: more than 30% Limits of image degradation are needed to agree with Nokia and module supplier. Nokia provides test images to the module supplier.

Notes:

1. Partial area updating of the image data is supported by the CABC function.
2. Power consumption of the CABC processing is minimized.

### 9.7.2. Transition Time of the CABC

Content Adaptive Brightness Control (CABC) is a dimming function where two different dimming functions are implemented in the ABC system:

- Image content based dimming function
- Manual Setting based dimming function

Both functions have to combine without any abnormal visible effect, e.g. flicker problem.

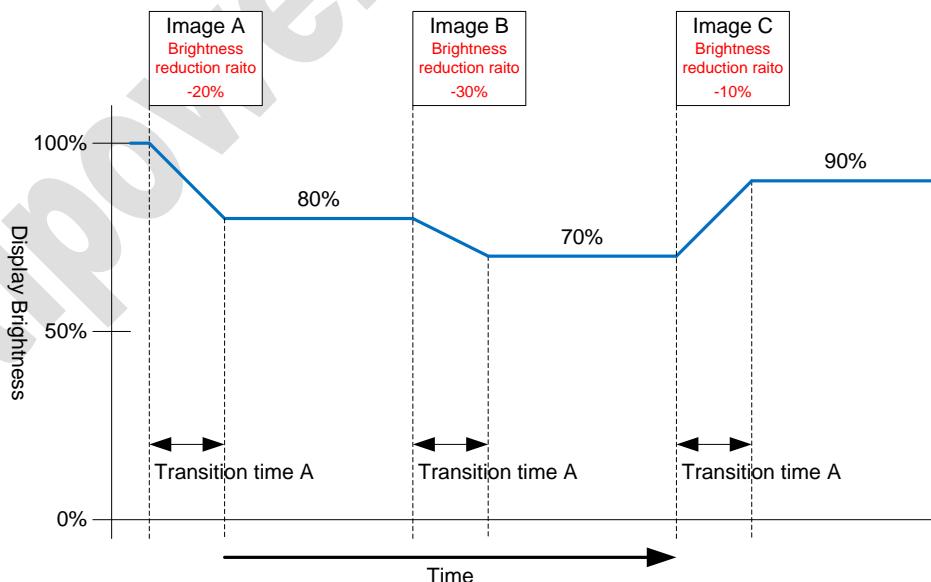
The transition time for dimming function is illustrated below.

- Image content based dimming function

Display brightness is changed, according to the image contents. The following graph mentions the case of displaying three different images.

- Image A: -20% brightness reduction
- Image B: -30% brightness reduction
- Image C: -10% brightness reduction

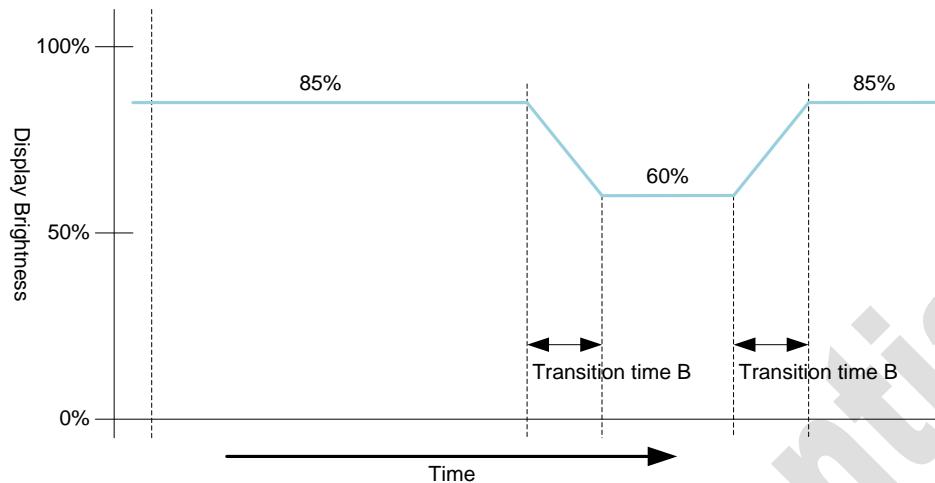
Transition time from the previous image to the current displayed image is “Transition time A”. “Transition time A” is not specified in this specification because it is depending on CABC algorithm, which is defined by the display module supplier.



**Figure 9.9: Transition Time on Content Adaptive Brightness Control**

- Manual Setting based dimming function

Transition time from the previous display brightness to the current display brightness is “Transition time B”.



**Figure 9.10: Transition Time on Manual Setting**

- Combined display brightness

Green line in the following graph is for the output brightness of display. It is combined with both display brightness, which are defined in the above graphs.

Maximum transition time is transition time A + B.

The brightness level of the display is calculated with the following formula.

Display Output Brightness = Manual Setting \* CABC Brightness Ratio.

Case	Brightness	Brightness ratio	Display Output brightness
Case 1	85%	80%	68%
Case 2	60%	70%	42%
Case 3	85%	90%	76.5%

**Table 9.3: Display Output Brightness Calculations**

Notes:

1. “Transition Time A” is based on CABC algorithm.
2. “Transition Time B” is controlled by bit DD of “11.2.45 Write CTRL Display (53h)” command.
3. The worst case transition time (A+B) is from a current to target brightness

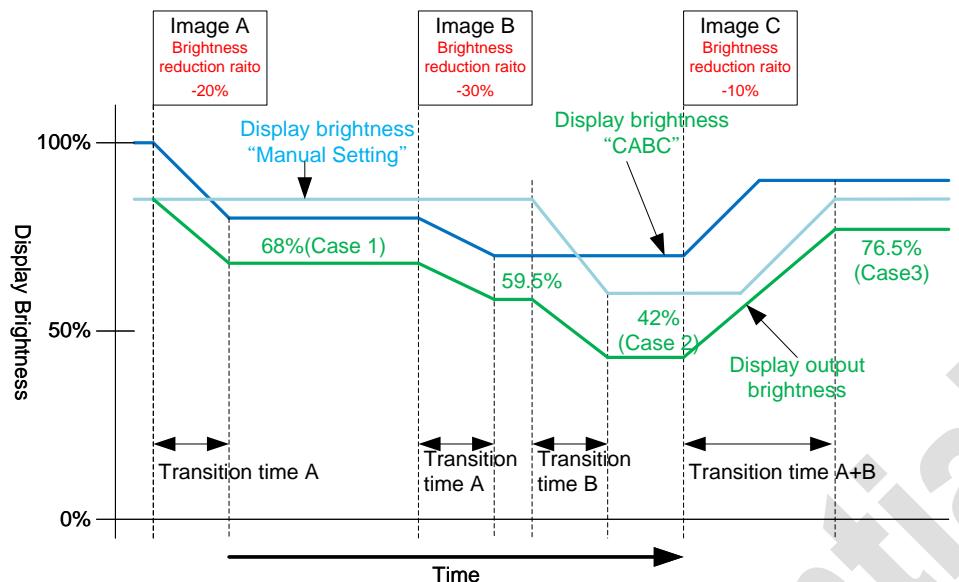


Figure 9.11: Transition Time on Combined Display Brightness

### 9.7.3. Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting is to avoid too much brightness reduction. When CABC is active, CABC cannot reduce the display brightness to less than CABC minimum brightness setting. If CABC algorithm works without any abnormal visual effect, image processing function can operate even when the brightness cannot be changed.

When display brightness is turned off (BCTRL=0 of “10.2.37 Write CTRL Display (53h)”), CABC minimum brightness setting is ignored. “10.2.42 Read CABC Minimum Brightness (5Fh)” always read the setting value of “10.2.41 Write CABC Minimum Brightness (5Eh)”.

Example:

CABC minimum brightness value = 51d (33h: 20% display brightness)

Case	A	B	C	Real Display Output Brightness
	Brightness (Manual Setting)	Brightness Ratio (CABC)	Calculation Result: Display Output Brightness Value	
Case 1	50%	70%	35%	35%
Case 2	20%	70%	14%	20%
Case 3	50%	70%	35%	35%

Table 9.4: Minimum Brightness Setting of the CABC Function - Example

## 10. Command

### 10.1. Command List

#### 10.1.1. Standard command

Address	Operation code	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Function	
00	NOP	W	0	0	0	0	0	0	0	0	No Operation	
01	SWRESET	W	0	0	0	0	0	0	0	1	Software Reset	
04	RDDIDIF	W	0	0	0	0	0	1	0	0	Read Display Identification Information	
		R	ID1[7:0]									
		R	ID2[7:0]									
		R	ID3[7:0]									
05	RDNUMPE	W	0	0	0	0	0	1	0	1	Read Number of DSI Parity Error	
		R	P[7:0]									
06	RDRED	W	0	0	0	0	0	1	1	0	Read Red Color	
		R	R[7:0]									
07	RDGREEN	W	0	0	0	0	0	1	1	1	Read Green Color	
		R	G[7:0]									
08	RDBLUE	W	0	0	0	0	1	0	0	0	Read Blue Color	
		R	B[7:0]									
09	RDDST	W	0	0	0	0	1	0	0	1	Read Display Status	
		R	D[31:24]									
		R	D[23:16]									
		R	D[15:8]									
		R	D[7:0]									
0A	RDDPM	W	0	0	0	0	1	0	1	0	Read display power mode	
		R	D7	D6	D5	D4	D3	D2	0	0		
0B	RDDMADCTL	W	0	0	0	0	1	0	1	1	Read display MADCTL	
		R	D7	D6	D5	D4	D3	D2	D1	D0		
0C	RDDCOLMOD	W	0	0	0	0	1	1	0	0	Read display pixel format	
		R	0	D6	D5	D4	0	D2	D1	D0		
0D	RDDIM	W	0	0	0	0	1	1	0	1	Read display image mode	
		R	D7	D6	D5	D4	D3	D2	D1	D0		
0E	RDDSM	W	0	0	0	0	1	1	1	0	Read display signal mode	
		R	D7	D6	D5	D4	D3	D2	D1	D0		
0F	RDDSDR	W	0	0	0	0	1	1	1	1	Read display self-diagnostic result	
		R	D7	D6	D5	D4	0	0	0	0		
10	SLPIN	W	0	0	0	1	0	0	0	0	Sleep In	
11	SLPOUT	R	0	0	0	1	0	0	0	1	Sleep Out	
13	NORON	W	0	0	0	1	0	0	1	1	Normal display mode on	
20	INVOFF	W	0	0	1	0	0	0	0	0	Display inversion off	
21	INVON	W	0	0	1	0	0	0	0	1	Display inversion on	
22	ALLPOFF	W	0	0	1	0	0	0	1	0	All Pixel Off	

23	ALLPON	W	0	0	1	0	0	0	1	1	All Pixel On	
26	GAMSET	W	0	0	1	0	0	1	1	0	Gamma set-	
		W	CG[7:0]									
28	DISPOFF	W	0	0	1	0	1	0	0	0	Display off	
29	DISPON	W	0	0	1	0	1	0	0	1	Display on	
34	TEOFF	W	0	0	1	1	0	1	0	0	Tearing Effect Line OFF	
35	TEON	W	0	0	1	1	0	1	0	1	Tearing Effect Line ON	
		W	X	X	X	X	X	X	X	M		
36	MADCTL	W	0	0	1	1	0	1	1	0	Memory Access Control	
		W	B7	B6	B5	B4	B3	B2	X	X		
38	IDMOFF	W	0	0	1	1	1	0	0	0	Idle mode off	
39	IDMON	W	0	0	1	1	1	0	0	1	Idle mode on	
3A	COLMOD	W	0	0	1	1	1	0	1	0	Interface Pixel Format	
		W	X	D6	D5	D4	X	D2	D1	D0		
44	TESL	W	0	1	0	0	0	1	0	0	Set Tear Effect Scan Lines	
		W	TELIN[15:8]									
		W	TELIN[7:0]									
45	GETSCAN	W	0	1	0	0	0	1	0	1	Return the current scanline	
		R	SLN[15:8]									
		R	SLN[7:0]									
51	WRDISBV	W	0	1	0	1	0	0	0	1	Write Display Brightness	
		W	DBV[7:0]								-	
52	RDDISBV	W	0	1	0	1	0	0	1	0	Read Display Brightness Value	
		R	DBV[7:0]									
53	WRCTRLD	W	0	1	0	1	0	0	1	1	Write CTRL Display	
		W	X	X	BCTRL	X	DD	BL	X	X		
54	RDCTRLD	W	0	1	0	1	0	0	1	1	Read Control Value Display-	
		R	0	0	BCTRL	0	DD	BL	0	0		
55	WRCABC	W	0	1	0	1	0	1	0	1	Write Adaptive Brightness Control	
		W	X	X	X	X	X	X	CABC[1:0]			
56	RDCABC	W	0	1	0	1	0	1	1	0	Read Adaptive Brightness Control Content	
		R	0	0	0	0	0	0	CABC[1:0]			
5E	WRCABCMB	W	0	1	0	1	1	1	1	0	Write CABC minimum brightness	
		W	CMB[7:0]									
5F	RDCABCMB	W	0	1	0	1	1	1	1	1	Read CABC minimum brightness	
		R	CMB[7:0]									
DA	RDID1	W	1	1	0	1	1	0	1	0	Read ID1	
		R	module's manufacturer[7:0]									
DB	RDID2	W	1	1	0	1	1	0	1	1	Read ID2	
		R	LCD module/driver version [7:0]									

DC	RDID3	W	1	1	0	1	1	1	0	0	Read ID3
		R	LCD module/driver ID[7:0]								
A1	RDDDB	W	1	0	1	0	0	0	0	1	Read the DDB from the provided location.
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
A8	RDDDBCON	W	1	0	1	0	1	0	0	0	Continue reading the DDB from the last read location.
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	

Table 10.1: Standard command list

### 10.1.2. Standard Command Accessibility

Hex Code	Operation code	Normal Mode On, Idle Mode Off, Sleep Mode Off	Normal Mode On, Idle Mode On, Sleep Mode Off	Sleep Mode On
00	NOP	Yes	Yes	Yes
01	SWRESET	Yes	Yes	Yes
04	RDDIDIF	Yes	Yes	Yes
05	RDNUMPE	Yes	Yes	Yes
06	RDRED	Yes	Yes	Yes
07	RDGREEN	Yes	Yes	Yes
08	RDBLUE	Yes	Yes	Yes
09	RDDST	Yes	Yes	Yes
0A	RDDPM	Yes	Yes	Yes
0B	RDDMADCTL	Yes	Yes	Yes
0C	RDDCOLMOD	Yes	Yes	Yes
0D	RDDIM	Yes	Yes	Yes
0E	RDDSM	Yes	Yes	Yes
0F	RDDSDR	Yes	Yes	Yes
10	SLPIN	Yes	Yes	Yes
11	SLPOUT	Yes	Yes	Yes
13	NORON	Yes	Yes	Yes
20	INVOFF	Yes	Yes	Yes
21	INVON	Yes	Yes	Yes
22	ALLPOFF	Yes	Yes	Yes
23	ALLPON	Yes	Yes	Yes
26	GAMSET	Yes	Yes	Yes
28	DISPOFF	Yes	Yes	Yes
29	DISPON	Yes	Yes	Yes
34	TEOFF	Yes	Yes	Yes
35	TEON	Yes	Yes	Yes
36	MADCTL	Yes	Yes	Yes
38	IDMOFF	Yes	Yes	Yes
39	IDMON	Yes	Yes	Yes
3A	COLMOD	Yes	Yes	Yes
44	TESL	Yes	Yes	Yes
45	GETSCAN	Yes	Yes	Yes
51	WRDISBV	Yes	Yes	Yes
52	RDDISBV	Yes	Yes	Yes
53	WRCTRLD	Yes	Yes	Yes
54	RDCTRLD	Yes	Yes	Yes
55	WRCABC	Yes	Yes	Yes
56	RDCABC	Yes	Yes	Yes
5E	WRCABCMB	Yes	Yes	Yes
5F	RDCABCMB	Yes	Yes	Yes
DA	RDID1	Yes	Yes	Yes
DB	RDID2	Yes	Yes	Yes
DC	RDID3	Yes	Yes	Yes
A1	RDDDB	Yes	Yes	Yes
A8	RDDDBCON	Yes	Yes	Yes

Table 10.2: Standard Command Accessibility

### 10.1.3. Standard Command Default Modes and Values

Hex Code	Operation code	Parameters	Power-on Sequence	SW Reset	HW Reset
00	NOP	None	N/A	N/A	N/A
01	SWRESET	None	N/A	N/A	N/A
04	RDDIDIF	3	OTP Value	OTP Value	OTP Value
05	RDNUMPE	1	00h	00h	00h
06	RDRED	1	00h	00h	00h
07	RDGREEN	1	00h	00h	00h
08	RDBLUE	1	00h	00h	00h
09	RDDST	1	Refer to corresponding command parameters	Refer to corresponding command parameters	Refer to corresponding command parameters
0A	RDDPM	1	08h	08h	08h
0B	RDDMADCTL	1	00h	Refer to corresponding command parameters	00h
0C	RDDCOLMOD	1	07h	07h	07h
0D	RDDIM	1	00h	00h	00h
0E	RDDSM	1	00h	00h	00h
0F	RDDSDR	1	00h	00h	00h
10	SLPIN	None	Sleep In Mode	Sleep In Mode	Sleep In Mode
11	SLPOUT	None	Sleep In Mode	Sleep In Mode	Sleep In Mode
13	NORON	None	Normal Display mode On	Normal Display mode On	Normal Display mode On
20	INVOFF	None	Display Inversion Off	Display Inversion Off	Display Inversion Off
21	INVON	None	Display Inversion Off	Display Inversion Off	Display Inversion Off
22	ALLPOFF	None	All Pixel Off	All Pixel Off	All Pixel Off
23	ALLPON	None	All Pixel Off	All Pixel Off	All Pixel Off
26	GAMSET	1	01h	01h	01h
28	DISPOFF	None	Display Off	Display Off	Display Off
29	DISPON	None	Display Off	Display Off	Display Off
34	TEOFF	None	TE Off	TE Off	TE Off
35	TEON	1	TE Off	TE Off	TE Off
36	MADCTL	1	00h	No Change	00h
38	IDMOFF	None	Idle Mode Off	Idle Mode Off	Idle Mode Off
39	IDMON	None	Idle Mode Off	Idle Mode Off	Idle Mode Off
3A	COLMOD	1	07h	No Change	07h
44	TESL	2	0000h	0000h	0000h
45	GETSCAN	2	0000h	0000h	0000h
51	WRDISBV	1	00h	00h	00h
52	RDDISBV	1	00h	00h	00h
53	WRCTRLD	1	00h	00h	00h
54	RDCTRLD	1	00h	00h	00h
55	WRCABC	1	00h	00h	00h
56	RDCABC	1	00h	00h	00h
5E	WRCABCM	1	00h	00h	00h
5F	RDCABCM	1	00h	00h	00h
DA	RDID1	1	OTP Value	OTP Value	OTP Value
DB	RDID2	1	OTP Value	OTP Value	OTP Value
DC	RDID3	1	OTP Value	OTP Value	OTP Value
A1	RDDDB	All	OTP Value	OTP Value	OTP Value
A8	RDDDBCON	All	OTP Value	OTP Value	OTP Value

Table 10.3: Standard Command Default Modes and Value

**10.2. Command Description****10.2.1.NOP (00h)**

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	<b>W</b>	0	0	0	0	0	0	0	0	00
Description	This command does not have any effect on the display module. The NOP command may be used to terminate a Frame Memory Read or Frame Memory Write.									
Restriction	-									
Flow Chart	-									

### 10.2.2. SWRESET: Software Reset (01h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	0	0	0	0	1	01
Description	The display module performs a software reset. Registers are written with their SW Reset default values. The Frame Memory contents are unaffected by this command									
Restriction	The host processor must wait 5 milliseconds before sending any new commands to a display module following this command. The display module updates the registers during this time. If a SWRESET is sent when the display module is in SLPIN Mode, the host processor must wait 120 milliseconds before sending an SLPOUT command. SWRESET should not be sent when the display module is not in SLPIN mode.									
Flow Chart	<pre> graph TD     SWRESET[SWRESET] --&gt; BlankDisplay([Blank Display])     BlankDisplay --&gt; LoadSWD[Load S/W Defaults]     LoadSWD --&gt; SLPINMode([SLPIN Mode])   </pre>									

### 10.2.3.RDDIDIF: Read Display Identification Information (04h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX																						
Command	W	0	0	0	0	0	1	0	0	04																						
Parameter 1	R					ID1[7:0]																										
Parameter 2	R					ID2[7:0]																										
Parameter 3	R					ID3[7:0]																										
Description		<p>This read byte returns 24-bit display identification information. The 1<sup>st</sup> Parameter identifies the LCD module's manufacturer. It is specified by display supplier and for xx is defined as xxHEX.</p> <p>The 2<sup>nd</sup> Parameter has 2 purposes. Bit7 (MSB) defines the type of panel. 0=Driver (STN B/W), 1=Module (Color). Bits 6~0 are used to track the LCD module/driver version. It is defined by display supplier and it changes each time a revision is made to the display, material or construction specifications. See Table:</p> <table border="1"> <thead> <tr> <th>ID Byte Value V[7:0]</th> <th>Version</th> <th>Changes</th> </tr> </thead> <tbody> <tr> <td>80h</td> <td></td> <td></td> </tr> <tr> <td>81h</td> <td></td> <td></td> </tr> <tr> <td>82h</td> <td></td> <td></td> </tr> <tr> <td>83h</td> <td></td> <td></td> </tr> <tr> <td>84h</td> <td></td> <td></td> </tr> <tr> <td>85h</td> <td></td> <td></td> </tr> </tbody> </table> <p>The 3<sup>rd</sup> parameter identifies the LCD module/driver. It is specified by display supplier and for this LCD project module is defined as xxHEX.</p>										ID Byte Value V[7:0]	Version	Changes	80h			81h			82h			83h			84h			85h		
ID Byte Value V[7:0]	Version	Changes																														
80h																																
81h																																
82h																																
83h																																
84h																																
85h																																
Restriction	-																															
Flow Chart		<pre> graph TD     A[RDDIDIF (04h)] --&gt; B[/Send ID1[7:0]/]     B --&gt; C[/Send ID2[7:0]/]     C --&gt; D[/Send ID3[7:0]/]   </pre>																														

## 10.2.4.RDNUMPE: Read number of the parity errors (05h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	0	0	1	0	1	05
Parameter 1	R	P7	P6	P5	P4	P3	P2	P1	P0	
Description	<p>The first parameter is telling a number of the errors on DSI. The more detailed description of the bits is below.</p> <p>P[6:0] bits are telling a number of the errors.</p> <p>P[7] is set to '1' if there is overflow with P[6..0] bits.</p> <p>P[7:0] bits are set to '0's (as well as RDDSM(0Eh)'s D0 is set '0' at the same time) after there is sent the second parameter information (=The read function is completed).</p>									
Restriction	-									
Flow Chart	<p>DSI I/F Mode</p> <pre> graph TD     RDNUMPE["RDNUMPE (R05h)"] --&gt; HostDriver[Host Driver]     HostDriver --&gt; SendParam[/Send 1st parameter/]     SendParam --&gt; RDDSM["RDDSM (R0Eh) 's D0 = '0' P[7:0] = \"00\"h"]   </pre>									

### 10.2.5.REDRD: Read Red Color (06h)

CMD/PAs	R/W	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	-	0	0	0	0	0	1	1	0	06
Parameter 1	R	-	R7	R6	R5	R4	R3	R2	R1	R0	
Description	<p>The first parameter is telling red color value of the first pixel of the frame when there is used DPI I/F.</p> <p>16 bit format: R5 is MSB and R1 is LSB. R7, R6 and R0 are set to '0'.</p> <p>18 bit format: R5 is MSB and R0 is LSB. R7 and R6 are set to '0'.</p> <p>24 bit format: R7 is MSB and R0 is LSB. All bits are used.</p>										
Restriction	-										
Flow Chart	<pre> graph TD     RDREAD[RDREAD(06h)] --&gt; Host[Host]     Host -.-&gt; Driver[Driver]     Driver -- "Send D[7:0]" --&gt; Response[Response]   </pre>										

### 10.2.6.RDGREEN: Read Green Color (07h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	0	0	1	1	1	07
Parameter 1	R	G7	G6	G5	G4	G3	G2	G1	G0	
Description	<p>The first parameter is telling green color value of the first pixel of the frame when there is used DPI I/F.</p> <p>16 bit format: G5 is MSB and G0 is LSB. G7 and G6 are set to '0'.</p> <p>18 bit format: G5 is MSB and G0 is LSB. G7 and G6 are set to '0'.</p> <p>24 bit format: G7 is MSB and G0 is LSB. All bits are used.</p>									
Restriction	-									
Flow Chart	<pre> graph TD     RDGREEN[RDGREEN (07h)] --&gt; Host[Host]     Host -.-&gt; Driver[Driver]     Host -- "Send D[7:0]" --&gt; Driver   </pre> <p>The flow chart illustrates the communication between the Host and the Driver. It starts with a box labeled 'RDGREEN (07h)' which has an arrow pointing down to a dashed horizontal line representing the interface. Below this line, the word 'Host' is positioned above the word 'Driver'. A second arrow originates from the 'Host' label and points down to a trapezoidal shape labeled 'Send D[7:0]' located within the 'Driver' area.</p>									

## 10.2.7.REDBLUE: Read Blue Color (08h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	0	1	0	0	0	08
Parameter 1	R	B7	B6	B5	B4	B3	B2	B1	B0	
Description	<p>The first parameter is telling blue color value of the first pixel of the frame when there is used DPI I/F.</p> <p>16 bit format: B5 is MSB and B1 is LSB. B7, B6 and B0 are set to '0'.</p> <p>18 bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to '0'.</p> <p>24 bit format: B7 is MSB and B0 is LSB. All bits are used.</p>									
Restriction	-									
Flow Chart	<pre> graph TD     A[RDBLUE (08h)] --&gt; B[Send D[7:0]]     subgraph Host [Host]         A     end     subgraph Driver [Driver]         B     end     A -.-&gt; B   </pre> <p>The flow chart illustrates the communication between the Host and the Driver. At the top, a rectangular box labeled "RDBLUE (08h)" represents the command being sent. An arrow points downwards from this box to a trapezoidal box below it, which is labeled "Send D[7:0]". This trapezoidal box represents the data being transmitted. The entire process is enclosed within two dashed horizontal lines labeled "Host" on the left and "Driver" on the right, indicating the boundaries of these two components.</p>									

## 10.2.8.RDDST: Read Display Status (09h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX																															
Command	W	0	0	0	0	1	0	0	1	09																															
Parameter 1	R					D[31:24]																																			
Parameter 2	R					D[23:16]																																			
Parameter 3	R					D[15:8]																																			
Parameter 4	R					D[7:0]																																			
Description	This command indicates the current status of the display as described in the table below:																																								
	Bit	Description			Value																																				
	D31	Booster Voltage Status			'0' = Booster Off. '1' = Booster On.																																				
	D30	Page Address Order			'0' = Top to Bottom (MADCTL B7='0'). '1' = Bottom to Top (MADCTL B7='1').																																				
	D29	Column Address Order			'0' = Left to Right (MADCTL B6='0'). '1' = Right to Left (MADCTL B6='1')																																				
	D28	Page/Column Order			This bit is not applicable for this project, set it to '0'																																				
	D27	Display Device Line Refresh Order			This bit is not applicable for this project, set it to '0'																																				
	D26	RGB/BGR Order			'0' = RGB (MADCTL B3='0'). '1' = BGR (MADCTL B3='1').																																				
	D25	Display Data Latch Data Order			This bit is not applicable for this project, so it is set to '0'																																				
	D24	Source san sequence			'0' = Source output Left to Right (MADCTL B1='0'). '1' = Source output Right to Left (MADCTL B1='1')																																				
	D23	Gate san sequence			'0' = Gate output Top to Bottom (MADCTL B0='0'). '1' = Gate output Bottom to Top (MADCTL B0='1')																																				
	D22	Interface Colo Pixel Format Definition			<table border="1"> <thead> <tr> <th>Interface Format</th> <th>D22</th> <th>D21</th> <th>D20</th> </tr> </thead> <tbody> <tr> <td>Not Defined</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Not Defined</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>Not Defined</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>Not Defined</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>16 Bit/Pixel</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>18 Bit/Pixel</td> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>						Interface Format	D22	D21	D20	Not Defined	0	0	0	Not Defined	0	0	1	Not Defined	0	1	0	Not Defined	0	1	1	Not Defined	1	0	0	16 Bit/Pixel	1	0	1	18 Bit/Pixel	1	1
Interface Format	D22	D21	D20																																						
Not Defined	0	0	0																																						
Not Defined	0	0	1																																						
Not Defined	0	1	0																																						
Not Defined	0	1	1																																						
Not Defined	1	0	0																																						
16 Bit/Pixel	1	0	1																																						
18 Bit/Pixel	1	1	0																																						
D21																																									
D20																																									
D19	Idle Mode On/Off			'0' = Idle Mode Off. '1' = Idle Mode On.																																					
D18	Partial Mode On/Off			'0' = Partial Mode Off, '1' = Partial Mode On.																																					
D17	Sleep In/Out			'0' = Sleep In Mode. '1' = Sleep Out Mode.																																					
D16	Display Normal Mode On/Off			'0' = Partial or Scrolling Mode. '1' = Normal Mode.																																					
D15	Vertical Scrolling Status			This bit is not applicable for this project, set it to '0'																																					
D14	Horizontal Scrolling Status			This bit is not applicable for this project, set it to '0'																																					
D13	Inversion Status			'0' = Inversion is Off. '1' = Inversion is On.																																					
D12	All Pixels On			'0' = Normal mode. '1' = All Pixels On.																																					
D11	All Pixels Off			'0' = Normal mode. '1' = All Pixels Off.																																					
D10	Display On/Off			'0' = Display is Off. '1' = Display is On.																																					
D9	Tearing Effect Line On/Off			'0' =Tearing Effect Line Off. '1' = Tearing Effect On.																																					

	D8	Gamma Curve Selection	Gamma Curve Selected	B8	B7	B6
	D7		Gamma Curve 1	0	0	0
	D6		Gamma Curve 2	0	0	1
	D5		Gamma Curve 3	0	1	0
	D4		Gamma Curve 4	0	1	1
	D3		Not Defined	1	0	0
	D2		Not Defined	1	0	1
	D1		Not Defined	1	1	0
	D0		Not Defined	1	1	1
Restriction	-		'0' = Mode 1, V-Blanking only. '1' = Mode 2, both H-Blanking and V-Blanking.			
Flow Chart			<pre> graph TD     RDDST["RDDST (09h)"] --&gt; SendD31[Send D[31:24]]     SendD31 --&gt; SendD23[Send D[23:16]]     SendD23 --&gt; SendD15[Send D[15:8]]     SendD15 --&gt; SendD7[Send D[7:0]]   </pre>			

**Note:** This bit indicates current status of the line when this command has been sent.

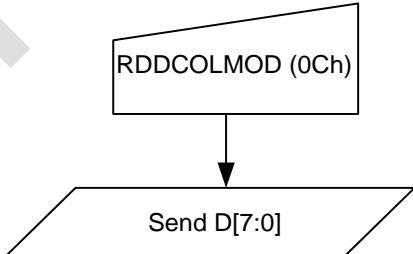
## 10.2.9.RDDPM: Read Display Power Mode (0Ah)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	W	0	0	0	0	1	0	1	0	0A									
Parameter 1	R	D7	D6	D5	D4	D3	D2	D1	D0										
Description	This command indicates the current status of the display as described in the table below:																		
Description	Bit	Description			Value														
	D7	Booster Voltage Status			„0“ = Booster Off. „1“ = Booster On.														
	D6	Idle Mode On/Off			‘0’ = Idle Mode Off. ‘1’ = Idle Mode On.														
	D5	Partial Mode On/Off			‘0’ = Partial Mode Off. ‘1’ = Partial Mode On.														
	D4	Sleep In/Out			‘0’ = Sleep In Mode. ‘1’ = Sleep Out Mode.														
	D3	Display Normal Mode On/Off			‘0’ = Display Normal Mode Off. ‘1’ = Display Normal Mode On.														
	D2	Display On/Off			‘0’ = Display is Off. ‘1’ = Display is On.														
	D1	Not Defined			Set to ‘0’														
	D0	Not Defined			Set to ‘0’														
Restriction	-																		
Flow Chart	<pre> graph TD     A[RDDMP(0Ah)] --&gt; B[/Send D[7:0]/]   </pre>																		

### 10.2.10. RDDMATCDL: Read Display MADCTL (0Bh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	W	0	0	0	0	1	0	1	1	0B									
Parameter 1	R	D7	D6	D5	D4	D3	D2	D1	D0										
Description	This command indicates the current status of the display as described in the table below:																		
	Bit	Description		Value															
	D7	Page Address Order		'0' = Top to Bottom (When MADCTL B7='0'). '1' = Bottom to Top (When MADCTL B7='1').															
	D6	Column Address Order		'0' = Left to Right (When MADCTL B6='0'). '1' = Right to Left (When MADCTL B6='1').															
	D5	Page/Column Order		This bit is not applicable for this project, set it to '0'															
	D4	Display Device Line Refresh Order		This bit is not applicable for this project, set it to '0'															
	D3	RGB/BGR Order		'0' = RGB (When MADCTL B3='0'). '1' = BGR (When MADCTL B3='1').															
	D2	Display Data Latch Data Order		This bit is not applicable for this project, set it to '0'															
	D1	Source san sequence		'0' = Source output Left to Right (When MADCTL B1='0'). '1' = Source output Right to Left (When MADCTL B1='1').															
	D0	Gate san sequence		'0' = Gate output Top to Bottom (When MADCTL B0='0'). '1' = Gate output Bottom to Top (When MADCTL B0='1').															
Restriction	-																		
Flow Chart	<pre> graph TD     A[RDDMADCTR (0Bh)] --&gt; B[/Send D[7:0]/]   </pre>																		

### 10.2.11. RDDCOLMOD: Read Display COLMOD (0Ch)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
Command	W	0	0	0	0	1	1	0	0	0C																																				
Parameter 1	R	0	D6	D5	D4	0	D2	D1	D0																																					
Description																																														
<p>This command gets the pixel format for the RGB image data used by the interface.</p> <p>D[6:4] – DPI Interface Color Pixel Format Definition</p> <p>D[2:0] – DBI Interface Color Pixel Format Definition.</p> <p>For Setting pixel format, see section “COLMOD: Interface Pixel Format (3Ah)”.</p> <table border="1"> <thead> <tr> <th>Pixel Format</th><th>D6/D2</th><th>D5/D1</th><th>D4/D0</th></tr> </thead> <tbody> <tr> <td>Not Defined</td><td>0</td><td>0</td><td>0</td></tr> <tr> <td>Not Defined</td><td>0</td><td>0</td><td>1</td></tr> <tr> <td>Not Defined</td><td>0</td><td>1</td><td>0</td></tr> <tr> <td>Not Defined</td><td>0</td><td>1</td><td>1</td></tr> <tr> <td>Not Defined</td><td>1</td><td>0</td><td>0</td></tr> <tr> <td>16 bit/pixel</td><td>1</td><td>0</td><td>1</td></tr> <tr> <td>18 bit/pixel</td><td>1</td><td>1</td><td>0</td></tr> <tr> <td>24 bit/pixel</td><td>1</td><td>1</td><td>1</td></tr> </tbody> </table> <p>If a particular interface, either DBI or DPI, is not used then the corresponding bits in the parameter returned from the display module are undefined.</p> <p>Therefore, for a DBI display module, the Host shall ignore D[6:4] and for a DPI display module, the Host shall ignore D[2:0].</p>											Pixel Format	D6/D2	D5/D1	D4/D0	Not Defined	0	0	0	Not Defined	0	0	1	Not Defined	0	1	0	Not Defined	0	1	1	Not Defined	1	0	0	16 bit/pixel	1	0	1	18 bit/pixel	1	1	0	24 bit/pixel	1	1	1
Pixel Format	D6/D2	D5/D1	D4/D0																																											
Not Defined	0	0	0																																											
Not Defined	0	0	1																																											
Not Defined	0	1	0																																											
Not Defined	0	1	1																																											
Not Defined	1	0	0																																											
16 bit/pixel	1	0	1																																											
18 bit/pixel	1	1	0																																											
24 bit/pixel	1	1	1																																											
Restriction	-																																													
Flow Chart	 <pre> graph TD     A[RDDCOLMOD (0Ch)] --&gt; B[/Send D[7:0]/]   </pre>																																													

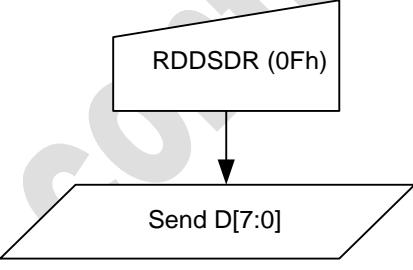
### 10.2.12. Read Display Image Mode (0Dh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX			
Command	W	0	0	0	0	1	1	0	1	0D			
Parameter 1	R	D7	D6	D5	D4	D3	D2	D1	D0				
This command indicates the current status of the display as described in the table below:													
Description	Bit	Description			Value								
	D7	Vertical Scrolling On/Off			This bit is not applicable for this project, set it to '0'								
	D6	Horizontal Scrolling Status			This bit is not applicable for this project, set it to '0'								
	D5	Inversion On/Off			'0' = Inversion is Off. '1' = Inversion is On.								
	D4	All Pixels On			'0' = Normal Display '1' = White Display								
	D3	All Pixels Off			'0' = Normal Display '1' = Black Display								
	D2	Gamma Curve Selection			Gamma Curve Selected	D2	D1	D0	Gamma Set (26h)				
					Gamma Curve 1	0	0	0	CG0				
	D1				Gamma Curve 2	0	0	1	CG1				
					Gamma Curve 3	0	1	0	CG2				
	D0				Gamma Curve 4	0	1	1	CG3				
					Not Defined	1	0	0					
					Not Defined	1	0	1					
					Not Defined	1	1	0					
					Not Defined	1	1	1					
Restriction	-												
Flow Chart	<pre> graph TD     A[RDDIM (0Dh)] --&gt; B[Send D[7:0]]   </pre>												

### 10.2.13. RDDSM: Read Display Signal Mode (0Eh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	W	0	0	0	0	1	1	1	0	0E									
Parameter 1	R	D7	D6	D5	D4	D3	D2	D1	D0										
This command indicates the current status of the display as described in the table below:																			
Description	Bit	Description			Value														
	D7	Tearing Effect Line On/Off			'0' = Tearing Effect Line Off. '1' = Tearing Effect On.														
	D6	Tearing Effect Line Output Mode			'0' = Mode 1. '1' = Mode 2.														
	D5	Horizontal Sync. (RGB I/F) On/Off.			'0' = Horizontal Sync. Line is Off ("Low"). '1' = Horizontal Sync. Line is On ("High").														
	D4	Vertical Sync. (RGB I/F) On/Off.			'0' = Vertical Sync. Line is Off ("Low"). '1' = Vertical Sync. Line is On ("High").														
	D3	Pixel Clock (PCLK, RGB I/F) On/Off.			'0' = PCLK line is Off ("Low"). '1' = PCLK line is On ("High").														
	D2	Data Enable (DE, RGB I/F) On/Off.			'0' = DE line is Off ("Low"). '1' = DE line is On ("High").														
	D1	Not Defined			For future use and are set to '0'.														
	D0	Parity Error on DSI			'0'=No Parity Error. '1'=Parity Error.														
Restriction	-																		
Flow Chart	<pre> graph TD     A[RDDSM (0Eh)] --&gt; B[/Send D[7:0]/]   </pre>																		

### 10.2.14. RDDSDR: Read Display Self-Diagnostic Result (0Fh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	W	0	0	0	0	1	1	1	1	0F									
Parameter 1	R	D7	D6	D5	D4	0	0	0	0										
Description The display module returns the self-diagnostic results following a SLPOUT command. See section “9.4 Self-diagnostic Functions” for a description																			
Description	Bit	Description			Value														
	D7	Register Loading Detection			See section “Sleep Out –command and self-diagnostic functions of the display module”														
	D6	Functionality Detection																	
	D5	Chip Attachment Detection			Set to ‘0’ if feature unimplemented.														
	D4	Display Glass Break Detection			Set to ‘0’ if feature unimplemented.														
	D3	Reserved			Set to ‘0’.														
	D2				Set to ‘0’.														
	D1				Set to ‘0’.														
	D0				Set to ‘0’.														
Restriction	-																		
Flow Chart	 <pre> graph TD     A[RDDSDR (0Fh)] --&gt; B[/Send D[7:0]/]     </pre>																		

### 10.2.15. SLPIN: Enter Sleep In Mode (10h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	1	0	0	0	0	10
This command causes the LCD module to enter the minimum power consumption mode.										
In this mode, all unnecessary blocks inside the display module are disabled except interface communication. This is the lowest power mode the display module supports.										
DBI or DSI Command Mode remains operational and the frame memory maintains its contents. The host processor continues to send PCLK, HS and VS information to DPI IF for two frames after this command is sent when the display module is in Normal mode.										
Description	In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.									
Restriction	<p>This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h).</p> <p>It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.</p> <p>It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</p>									
Flow Chart	<p>It takes 120msec to get into Sleep In mode after SLPIN command issued.</p> <pre> graph TD     S[SLPIN] --&gt; D1{Display whole blank screen Automatic No effect to DISP ON/OFF Commands}     D1 --&gt; D2{Drain charge from LCD panel}     D2 --&gt; S2[Sleep In Mode]          S2 --&gt; S3{Stop DC/DC Converter}     S3 --&gt; S4{Stop Internal Oscillator}     S4 --&gt; S5[Sleep In Mode]   </pre>									

### 10.2.16. SLPOUT: Exit Sleep In Mode (11h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	1	0	0	0	1	11
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.									
	<p>User can start to send PCLK, HS and VS information on DPI IF before Sleep Out command and this information is valid at least 2 frames before Sleep Out command, if there is left Sleep In -mode to Sleep Out-mode in Normal Mode On. There is used an internal oscillator for blank display.</p>									
Restriction	<p>This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h).</p> <p>It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.</p> <p>The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode.</p> <p>The display module is doing self-diagnostic functions during this 5msec. It will be necessary to alit 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</p>									
Flow Chart	<p>It takes 120msec to become Sleep Out mode after SLPOUT command issued.</p> <pre> graph TD     SLPOUT[SLPOUT] --&gt; StartOsc[Start Internal Oscillator]     StartOsc --&gt; StartDCDC[Start up DC:DC Converter]     StartDCDC --&gt; ChargeLCD[Charge Offset voltage for LCD Panel]     ChargeLCD --&gt; BlankScreen{Display whole blank screen for 2 frames (Automatic No effect to DISP ON/OFF Commands)}     BlankScreen --&gt; MemoryContent{Display Memory contents In accordance with the current command table settings}     MemoryContent --&gt; SleepOutMode([Sleep Out mode])   </pre>									

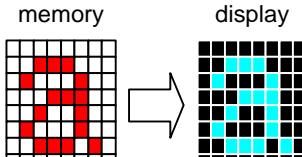
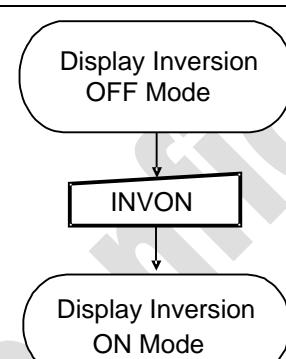
**10.2.17. NORON: Enter Normal Mode (13h)**

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	0	1	0	0	1	1	13
Description	<p>This command returns the display to normal mode. Normal display mode is means Partial mode off, Scroll mode Off. There is no abnormal visual effect during mode change from Partial mode On to Normal mode On.</p>									
Restriction	This command has no effect when Normal Display mode is active.									
Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command.									

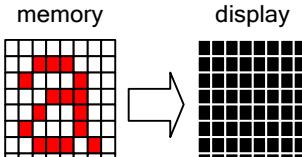
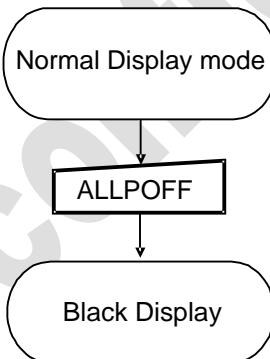
### 10.2.18. INVOFF: Display Inversion Off (20h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	0	0	0	0	0	20
Description	<p>This command is used to recover from display inversion mode.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p>									
Restriction	<p>This command has no effect when module is already in inversion off mode.</p>									
Flow Chart	<pre> graph TD     A([Display Inversion On Mode]) --&gt; B[INVOFF]     B --&gt; C([Display Inversion OFF Mode])     </pre>									

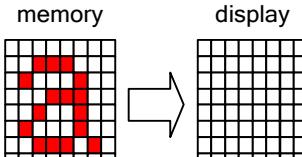
### 10.2.19. INVON: Display Inversion On (21h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	0	0	0	0	1	21
Description	<p>This command is used to enter into display inversion mode.</p> <p>This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.</p> <p>This command does not change any other status.</p> <p style="text-align: center;">(Example)</p> 									
Restriction	This command has no effect when module is already in inversion on mode.									
Flow Chart	 <pre> graph TD     A([Display Inversion OFF Mode]) --&gt; B[INVON]     B --&gt; C([Display Inversion ON Mode])   </pre>									

### 10.2.20. ALLPOFF: All Pixel Off (22h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	0	0	0	1	0	22
This command turns the display panel black in 'Sleep Out' –mode and a status of the 'Display On/Off' –register can be 'on' or 'off'. This command makes no change of contents of frame memory. This command does not change any other status										
(Example)										
Description	<p style="text-align: center;">memory                          display</p>  <p>'All Pixels On', 'Normal Display Mode On' or 'Partial Mode On' – commands are used to leave this mode. The display panel is showing the content of the frame memory after 'Normal Display Mode On' and 'Partial Mode On' -commands.</p>									
Restriction	This command has no effect when module is already in All Pixel Off mode.									
Flow Chart	<pre> graph TD     A([Normal Display mode]) --&gt; B[ALLPOFF]     B --&gt; C([Black Display])     </pre> 									

### 10.2.21. ALLPON: All Pixel On (23h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	0	0	0	1	1	23
This command turns the display panel white in 'Sleep out' –mode and a status of the 'Display On/Off' –register can be 'on' or 'off'. This command makes no change of contents of frame memory. This command does not change any other status.										
(Example)										
Description	<p style="text-align: center;">memory                          display</p>  <p>'All Pixels Off', 'Normal Display Mode On' or 'Partial Mode On' – commands are used to leave this mode. The display is showing the content of the frame memory after 'Normal Display Mode On' and 'Partial Mode On' –commands.</p>									
Restriction	This command has no effect when module is already in all Pixel On mode.									
Flow Chart	<pre> graph TD     A([Normal Display mode]) --&gt; B[ALLPON]     B --&gt; C([White Display])     </pre>									

### 10.2.22. GAMSET: Gamma Set (26h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	W	0	0	1	0	0	1	1	0	26															
Description	<p>This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curves are defined in Curve Correction Power Supply Circuit. The curve is selected by setting the appropriate bit in the parameter as described in the Table:</p> <table border="1"> <thead> <tr> <th>GC[7..0]</th><th>Parameter</th><th>Curve selected</th></tr> </thead> <tbody> <tr> <td>01h</td><td>GC0</td><td>Gamma Curve 1</td></tr> <tr> <td>02h</td><td>GC1</td><td>Gamma Curve 2</td></tr> <tr> <td>04h</td><td>GC2</td><td>Gamma Curve 3</td></tr> <tr> <td>08h</td><td>GC3</td><td>Gamma Curve 4</td></tr> </tbody> </table> <p><b>Note:</b> All other values are undefined.</p>										GC[7..0]	Parameter	Curve selected	01h	GC0	Gamma Curve 1	02h	GC1	Gamma Curve 2	04h	GC2	Gamma Curve 3	08h	GC3	Gamma Curve 4
GC[7..0]	Parameter	Curve selected																							
01h	GC0	Gamma Curve 1																							
02h	GC1	Gamma Curve 2																							
04h	GC2	Gamma Curve 3																							
08h	GC3	Gamma Curve 4																							
Restriction	Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.																								
Flow Chart	<pre> graph TD     A[GAMSET] --&gt; B[GC [7:0]]     B --&gt; C{New Gamma Curve Loaded}   </pre>																								

### 10.2.23. DISPOFF: Display Off (28h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	0	1	0	0	0	28
Description	<p>This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p> <p>There will be no abnormal visible effect on the display.</p>									
	<p>Example</p>									
Restriction	<p>This command has no effect when module is already in display off mode.</p>									
Flow Chart	<pre> graph TD     A([Display On Mode]) --&gt; B[DISPOFF]     B --&gt; C([Display Off Mode])   </pre>									

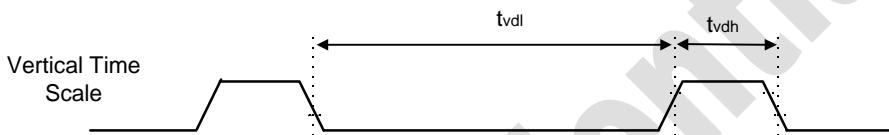
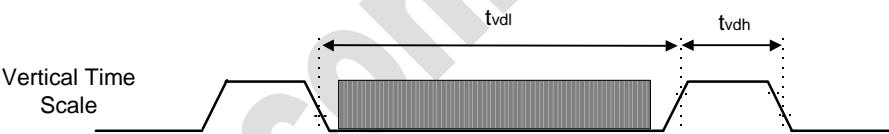
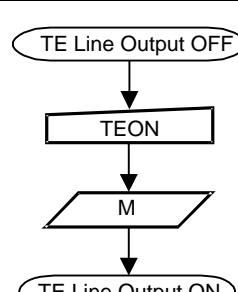
### 10.2.24. DISPON: Display On (29h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	0	1	0	0	1	29
Description	<p>This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p>									
	(Example)									
Restriction	This command has no effect when module is already in display on mode.									
Flow Chart	<pre> graph TD     A([Display Off Mode]) --&gt; B[DISPON]     B --&gt; C([Display On Mode])     </pre>									

**10.2.25. TEOFF: Tearing Effect Line OFF (34h)**

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	1	0	1	0	0	34
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.									
Restriction	This command has no effect when Tearing Effect output is already OFF.									
Flow Chart	<pre>graph TD; A([TE Line Output ON]) --&gt; B[TEOFF]; B --&gt; C([TE Line Output OFF]);</pre>									

### 10.2.26. TEON: Tearing Effect Line ON (35h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	0	1	1	0	1	0	1	35
Parameter 1	W	X	X	X	X	X	X	X	M	
Description		<p>This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4.</p> <p>The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).</p> <p>When M=0:</p> <p>The Tearing Effect Output line consists of V-Blanking information only:</p>  <p>Vertical Time Scale</p> <p>tvdl</p> <p>tvdh</p>								
Restriction		<p>When M=1:</p> <p>The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:</p>  <p>Vertical Time Scale</p> <p>tvdl</p> <p>tvdh</p>								
Flow Chart		 <pre> graph TD     A([TE Line Output OFF]) --&gt; B[TEON]     B --&gt; C[/M/]     C --&gt; D([TE Line Output ON])   </pre>								

## 10.2.27. MADCTL: Memory Access Control(36h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX																													
Command	W	0	0	1	1	0	1	1	0	36																													
Parameter 1	W	B7	B6	B5	B4	B3	B2	B1	B0																														
Description		<p>This command defines read/write scanning direction of frame memory.</p> <p>This command makes no change on the other driver status.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Bit</th><th style="text-align: center;">NAME</th><th style="text-align: center;">DESCRIPTION</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">B7</td><td>PAGE ADDRESS ORDER (MY)</td><td>Select the Source driver scan direction on panel module. Same as GS.</td></tr> <tr> <td style="text-align: center;">B6</td><td>COLUMN ADDRESS ORDER (MX)</td><td>Select the Gate driver scan direction on panel module. Same as SS.</td></tr> <tr> <td style="text-align: center;">B5</td><td>PAGE/COLUMN SELECTION (MV)</td><td>This bit is not applicable for this project, set it to '0'</td></tr> <tr> <td style="text-align: center;">B4</td><td>Vertical ORDER (ML)</td><td>LCD vertical refresh direction control</td></tr> <tr> <td style="text-align: center;">B3</td><td>RGB-BGR ORDER (BGR)</td><td>Color selector switch control 0=RGB color filter panel 1=BGR color filter panel</td></tr> <tr> <td style="text-align: center;">B2</td><td>Horizontal ORDER (MH)</td><td>This bit is not applicable for this project, set it to '0'</td></tr> <tr> <td style="text-align: center;">B1</td><td>Flip Horizontal (SS)</td><td>Select the Source driver scan direction on panel module</td></tr> <tr> <td style="text-align: center;">B0</td><td>Flip Vertical (GS)</td><td>Select the Gate driver scan direction on panel module</td></tr> </tbody> </table>		Bit	NAME	DESCRIPTION	B7	PAGE ADDRESS ORDER (MY)	Select the Source driver scan direction on panel module. Same as GS.	B6	COLUMN ADDRESS ORDER (MX)	Select the Gate driver scan direction on panel module. Same as SS.	B5	PAGE/COLUMN SELECTION (MV)	This bit is not applicable for this project, set it to '0'	B4	Vertical ORDER (ML)	LCD vertical refresh direction control	B3	RGB-BGR ORDER (BGR)	Color selector switch control 0=RGB color filter panel 1=BGR color filter panel	B2	Horizontal ORDER (MH)	This bit is not applicable for this project, set it to '0'	B1	Flip Horizontal (SS)	Select the Source driver scan direction on panel module	B0	Flip Vertical (GS)	Select the Gate driver scan direction on panel module									
Bit	NAME	DESCRIPTION																																					
B7	PAGE ADDRESS ORDER (MY)	Select the Source driver scan direction on panel module. Same as GS.																																					
B6	COLUMN ADDRESS ORDER (MX)	Select the Gate driver scan direction on panel module. Same as SS.																																					
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B2	Horizontal ORDER (MH)	This bit is not applicable for this project, set it to '0'																																					
B1	Flip Horizontal (SS)	Select the Source driver scan direction on panel module																																					
B0	Flip Vertical (GS)	Select the Gate driver scan direction on panel module																																					
Diagram		<p>RGB-BGR Order</p> <p>B3= 0</p> <p>B3= 1</p> <p>Source scan sequence (SS)</p> <p>SS=0</p> <p>SS=1</p>																																					

	Gate scan sequence (GS)			
	GS=0	Display Device	GS=1	Display Device
	Frame Memory	Top Left	Frame Memory	Top Left
Note: Top-Left (0,0) means a physical memory location.				
Restriction	-			
Flow Chart	<pre>MADCTL ↓ 1st parameter B[7:0]</pre>			

**10.2.28. IDMOFF: Idle Mode Off (38h)**

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	<b>W</b>	0	0	1	1	1	0	0	0	38
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 16.7M colors.									
Restriction	This command has no effect when module is already in idle off mode.									
Flow Chart	<pre>graph TD; A([Idle on mode]) --&gt; B[IDMOFF]; B --&gt; C([Idle off mode]);</pre> The flowchart illustrates the process of transitioning from an 'Idle on mode' to an 'Idle off mode'. It begins with an oval labeled 'Idle on mode', which points down to a rectangular box labeled 'IDMOFF'. From the 'IDMOFF' box, an arrow points down to another oval labeled 'Idle off mode'.									

### 10.2.29. IDMON: Idle Mode On (39h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																			
Command	W	0	0	1	1	1	0	0	0	38																																			
										This command is used to enter into Idle mode on. In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.																																			
										(Example)																																			
<p style="text-align: center;">Memory                          Display</p>																																													
Description	Memory contents vs. Display Color																																												
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th></th><th>R7 - R0</th><th>G7 - G0</th><th>B7 - B0</th></tr> </thead> <tbody> <tr> <td>Black</td><td>0XXXXXX</td><td>0XXXXXX</td><td>0XXXXXX</td></tr> <tr> <td>Blue</td><td>0XXXXXX</td><td>0XXXXXX</td><td>1XXXXXX</td></tr> <tr> <td>Red</td><td>1XXXXXX</td><td>0XXXXXX</td><td>0XXXXXX</td></tr> <tr> <td>Magenta</td><td>1XXXXXX</td><td>0XXXXXX</td><td>1XXXXXX</td></tr> <tr> <td>Green</td><td>0XXXXXX</td><td>1XXXXXX</td><td>0XXXXXX</td></tr> <tr> <td>Cyan</td><td>0XXXXXX</td><td>1XXXXXX</td><td>1XXXXXX</td></tr> <tr> <td>Yellow</td><td>1XXXXXX</td><td>1XXXXXX</td><td>0XXXXXX</td></tr> <tr> <td>White</td><td>1XXXXXX</td><td>1XXXXXX</td><td>1XXXXXX</td></tr> </tbody> </table>											R7 - R0	G7 - G0	B7 - B0	Black	0XXXXXX	0XXXXXX	0XXXXXX	Blue	0XXXXXX	0XXXXXX	1XXXXXX	Red	1XXXXXX	0XXXXXX	0XXXXXX	Magenta	1XXXXXX	0XXXXXX	1XXXXXX	Green	0XXXXXX	1XXXXXX	0XXXXXX	Cyan	0XXXXXX	1XXXXXX	1XXXXXX	Yellow	1XXXXXX	1XXXXXX	0XXXXXX	White	1XXXXXX	1XXXXXX	1XXXXXX
	R7 - R0	G7 - G0	B7 - B0																																										
Black	0XXXXXX	0XXXXXX	0XXXXXX																																										
Blue	0XXXXXX	0XXXXXX	1XXXXXX																																										
Red	1XXXXXX	0XXXXXX	0XXXXXX																																										
Magenta	1XXXXXX	0XXXXXX	1XXXXXX																																										
Green	0XXXXXX	1XXXXXX	0XXXXXX																																										
Cyan	0XXXXXX	1XXXXXX	1XXXXXX																																										
Yellow	1XXXXXX	1XXXXXX	0XXXXXX																																										
White	1XXXXXX	1XXXXXX	1XXXXXX																																										
X=don't care																																													
Restriction	This command has no effect when module is already in idle on mode.																																												
Flow Chart	<pre> graph TD     A([Idle off mode]) --&gt; B[IDMON]     B --&gt; C([Idle on mode])     </pre>																																												

## 10.2.30. COLMOD: Interface Pixel Format (3Ah)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																			
Command	W	0	0	1	1	1	0	1	0	3A																																			
Parameter 1	W	X	D6	D5	D4	X	D2	D1	D0																																				
Description										This command is used to define the format of RGB picture data. D6~D4 : DPI Pixel format Definition. D2~D0 : DBI Pixel format Definition. The formats are shown in the table:																																			
<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Pixel Format</th><th>D6/D2</th><th>D5/D1</th><th>D4/D0</th></tr> </thead> <tbody> <tr><td>Not Defined</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>Not Defined</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>Not Defined</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>Not Defined</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>Not Defined</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>16 Bit/Pixel</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>18 Bit/Pixel</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>24 Bit/Pixel</td><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>										Pixel Format	D6/D2	D5/D1	D4/D0	Not Defined	0	0	0	Not Defined	0	0	1	Not Defined	0	1	0	Not Defined	0	1	1	Not Defined	1	0	0	16 Bit/Pixel	1	0	1	18 Bit/Pixel	1	1	0	24 Bit/Pixel	1	1	1
Pixel Format	D6/D2	D5/D1	D4/D0																																										
Not Defined	0	0	0																																										
Not Defined	0	0	1																																										
Not Defined	0	1	0																																										
Not Defined	0	1	1																																										
Not Defined	1	0	0																																										
16 Bit/Pixel	1	0	1																																										
18 Bit/Pixel	1	1	0																																										
24 Bit/Pixel	1	1	1																																										
If a particular interface, enter DBI or DPI, is not used then the corresponding bits in the parameter returned from the display module undefined.																																													
Restriction	There is no visible effect until the Frame Memory is written to.																																												
Flow Chart	<pre> graph TD     A([Bit/Pixel Mode]) --&gt; B[Set Pixel Format]     B --&gt; C{Parameter}     C --&gt; D([New n Bit/Pixel Mode])     </pre>																																												

### 10.2.31. TESL: Set Tear Effect Scanline (44h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	W	0	1	0	0	0	1	0	0	44	
Parameter 1	W	TELINE[15:8]									
Parameter 2	W	TELINE[7:0]									
Description	<p>This command turns on the display module's Tearing Effect output signal on the TE signal</p> <p>Line when the display module reaches line TELINE. The TE signal is not affected by changing MADCTL bit B4.</p> <p>The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.</p> <p>The Tearing Effect Output line consists of V-Blanking information only:</p> <p><b>Note:</b> That TELINE=0 is equivalent to TEMODE=0. The Tearing Effect Output Line shall be active low when the display module is in Sleep mode.</p>										
Restriction	The command has no effect when Tearing Effect output is already ON.										
Flow Chart	<pre>     graph TD       A([TE output On or Off]) --&gt; B[Set TE On]       B --&gt; C[/Line N (LSB)]       C --&gt; D[/Line N (MSB)]       D --&gt; E([TE output On])   </pre>										

### 10.2.32. GETSCAN: Get the Current Scanline (45h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	W	0	1	0	0	0	1	0	1	45	
Parameter 1	W	SLN[15:8](8'b0)									
Parameter 2	W	SLN[7:0](8'b0)									
Description	<p>The display module returns the current scanline, N, used to update the display device.</p> <p>The total number of scanlines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0.</p> <p>When in Sleep Mode, the value returned by get scanline is undefined.</p>										
Restriction	-										
Flow Chart	<pre> graph TD     A[GETSCAN(45h)] --&gt; B[Scanline MSB]     B --&gt; C[Scanline LSB]   </pre>										

### 10.2.33. WRDISBV: Write Display Brightness (51h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	W	0	1	0	1	0	0	0	1	51	
Parameter 1	W	DBV[7:0]									
Description	<p>This command is used to adjust the brightness value of the display.</p> <p>It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification.</p> <p>In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p> <p>See chapter "Brightness Control Block".</p>										
Restriction	-										
Flow Chart	<pre> graph TD     A[WRDISBV] --&gt; B[/DBV[7..0]/]     B --&gt; C{New Display Luminance Value Loaded}   </pre>										

### 10.2.34. RDDISBV: Read Display Brightness Value (52h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	W	0	1	0	1	0	0	1	0	52	
Parameter 1	R	DBV[7:0]									
Description	<p>This command returns the brightness value of the display.</p> <p>It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is.</p> <p>In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p> <p>See chapters: “10.7 Content Adaptive Brightness Control (CABC)” and “11.2.43 WRDISBV: Write Display Brightness (51h)”.</p> <p>DBV[7:0] is reset when display is in sleep-in mode.</p> <p>DBV[7:0] is ‘0’ when bit BCTRL of “11.2.45 WRCTRLD: Write CTRL Display (53h)” command is ‘0’.</p> <p>DBV[7:0] is manual set brightness specified with “11.2.45 WRCTRLD: Write CTRL Display (53h)” command when bit BCTRL is ‘1’.</p> <p>When bit BCTRL of “11.2.45 WRCTRLD: Write CTRL Display (53h)” command is ‘1’ and bit C1/C0 of “WRCABC: Write Content Adaptive Brightness Control (55h)” are ‘0’, DBV[7:0] output is the brightness value specified with “11.2.43 WRDISBV: Write Display Brightness (51h)” command.</p>										
Restriction	-										
Flow Chart	<pre> graph TD     A[Read RDDISBV] --&gt; B[/Send 1 Parameter/]   </pre>										

### 10.2.35. WRCTRLD: Write CTRL Display (53h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	1	0	1	0	0	1	1	53
Parameter 1	W	x	x	BCTRL	x	DD	BL	x	x	
This command is used to control display brightness.										
<p>BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.</p> <p>0 = Off (Brightness registers are 00h, DBV[7..0])</p> <p>1 = On (Brightness registers are active, according to the other parameters.)</p>										
<p>Display Dimming (DD): (Only for manual brightness setting)</p> <p>DD = 0: Display Dimming is off</p> <p>DD = 1: Display Dimming is on</p>										
<p>BL: Backlight Control On/Off</p> <p>0 = Off (Completely turn off backlight circuit. Control lines must be low. )</p> <p>1 = On</p> <p>Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -&gt; 1 or 1-&gt; 0.</p>										
<p>When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.</p> <p>X = Don't care.</p>										
Restriction	-									
Flow Chart	<pre> graph TD     WRCTRLD[WRCTRLD] --&gt; BCTRL[BCTRL, DD, BL]     BCTRL --&gt; NewValue{New Control Value Loaded}   </pre>									

## 10.2.36. RDCTRLD: Read CTRL Value Display (54h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	0	1	0	1	0	1	0	0	54
Parameter 1	R	0	0	BCTRL	0	DD	BL	0	0	
Description										This command returns ambient light and brightness control values, see chapter: “11.2.45 WRCTRLD: Write CTRL Display (53h)”.  BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off 1 = On  Display Dimming (DD): DD = 0: Display Dimming is off DD = 1: Display Dimming is on  BL: Backlight Control On/Off 0 = Off (completely turn off backlight circuit) 1 = On
Restriction	-									
Flow Chart	<pre> graph TD     A[Read RDCTRLD] --- B[ ]     B --- C{Send 1 Parameter}   </pre>									

### 10.2.37. WRCABC: Write Content Adaptive Brightness Control (55h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX																
Command	W	0	1	0	1	0	1	0	1	55																
Parameter 1	W	X	X	X	X	X	X	CABC[1:0]																		
Description		<p>This command is used to set parameters for image content based adaptive brightness control functionality.</p> <p>There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter “10.7 Content Adaptive Brightness Control (CABC)”.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th colspan="2">C[1:0]</th> <th>Function</th> </tr> <tr> <td>0</td> <td>0</td> <td>Off</td> </tr> <tr> <td>0</td> <td>1</td> <td>User Interface Image</td> </tr> <tr> <td>1</td> <td>0</td> <td>Still Picture</td> </tr> <tr> <td>1</td> <td>1</td> <td>Moving Image</td> </tr> </table> <p>X = Don't care.</p>										C[1:0]		Function	0	0	Off	0	1	User Interface Image	1	0	Still Picture	1	1	Moving Image
C[1:0]		Function																								
0	0	Off																								
0	1	User Interface Image																								
1	0	Still Picture																								
1	1	Moving Image																								
Restriction	-																									
Flow Chart	<pre> graph TD     A[WRCABC] --&gt; B{1st parameter: C[1:0]}     B --&gt; C{New Adaptive Image Mode}   </pre>																									

### 10.2.38. RDCABC: Read Content Adaptive Brightness Control (56h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	<b>W</b>	0	1	0	1	0	1	1	0	56															
Parameter 1	<b>R</b>	X	X	X	X	X	X	CABC[1:0]																	
Description	<p>This command is used to set parameters for image content based adaptive brightness control functionality.</p> <p>There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter “10.7 Content Adaptive Brightness Control (CABC)”.</p> <table border="1"> <thead> <tr> <th>C1</th><th>C0</th><th>Function</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>Off</td></tr> <tr> <td>0</td><td>1</td><td>User Interface Image</td></tr> <tr> <td>1</td><td>0</td><td>Still Picture</td></tr> <tr> <td>1</td><td>1</td><td>Moving Image</td></tr> </tbody> </table>										C1	C0	Function	0	0	Off	0	1	User Interface Image	1	0	Still Picture	1	1	Moving Image
C1	C0	Function																							
0	0	Off																							
0	1	User Interface Image																							
1	0	Still Picture																							
1	1	Moving Image																							
Restriction																									
-																									
<pre> graph TD     A[Read RDCABC] --- B[/Send 1 Parameter/]     </pre>																									

### 10.2.39. WRCABCMB: Write CABC Minimum Brightness (5Eh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	W	0	1	0	1	1	1	1	0	5E	
Parameter 1	W	CMB[7:0]									
Description	<p>This command is used to set the minimum brightness value of the display for CABC function.</p> <p>In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.</p> <p>See chapter “ 10.7.3 Minimum brightness setting of CABC function”.</p>										
Restriction	-										
Flow Chart	<pre> graph TD     A[WRCABCMB] --&gt; B[CMB[7..0]]     B --&gt; C{New Display Luminance Value Loaded}   </pre>										

#### 10.2.40. RDCABCMB: Read CABC Minimum Brightness (5Fh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	W	0	1	0	1	0	1	1	1	5F	
Parameter 1	R	CMB[7:0]									
Description	<p>This command returns the minimum brightness value of CABC function.</p> <p>In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p> <p>See chapter "10.7.3 Minimum brightness setting of CABC function"</p>										
Restriction	-										
Flow Chart	<pre> graph TD     A[Read RDCABCMB] --&gt; B[/Send 1 Parameter/]     </pre>										

#### 10.2.41. RDABCSDR: Read Automatic Brightness Control Self-Diagnostic Result (68h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	W	0	1	1	0	1	0	0	0	68		
Parameter 1	R	D[7:6]		X	X	X	X	X	X			
Description	<p>This command indicates the status of the display self-diagnostic results for automatic brightness control after Sleep Out -command as described in the table below:</p> <p>D7 – Register Loading Detection D6 – Functionality Detection D5, D4, D3, D2, D1 and D0 are for future use and are set to '0'.</p>											
Restriction	-											
Flow Chart	<pre> graph TD     A[Read RDABCSDR] --&gt; B[/Send 1 Parameter/]     </pre>											

## 10.2.42. RDDDB: Read DDB Start (A1h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	0	1	0	0	0	0	1	A1
Parameter 1	R	X	X	X	X	X	X	X	X	
:	R	X	X	X	X	X	X	X	X	
Parameter n	R	X	X	X	X	X	X	X	X	
Description	<p>This command reads identifying and descriptive information from the peripheral. This information is organized in the Device Descriptor Block (DDB) stored on the peripheral. The response to this command returns a sequence of bytes that may be any length up to 64K bytes. Note that the returned sequence of bytes does not necessarily correspond to the entire DDB; it may be a portion of a larger block of data.</p> <p>The format of returned data is as follows:</p> <p>Parameter 1: LS (least significant) byte of Supplier ID. Supplier ID is a unique value assigned to each peripheral supplier by the MIPI organization.</p> <p>Parameter 2: MS (most significant) byte of Supplier ID.</p> <p>Parameter 3: LS (least significant) byte of Supplier Elective Data. This is a byte of information that is determined by the supplier. It could include model number or revision information, for example.</p> <p>Parameter 4: MS (most significant) byte of Supplier Elective Data</p> <p>Parameter 5: single-byte <i>Escape or Exit Code</i> (EEC). The code is interpreted as follows:</p> <ul style="list-style-type: none"> <li>- FFh - Exit code – there is no more data in the Descriptor Block</li> <li>- 00h - Escape code – there is supplier-proprietary data in the Descriptor Block (does not conform to any MIPI standard)</li> <li>- Any other value – there is DDB data in the Descriptor Block. The format and interpretation of this data is documented in <i>MIPI Alliance Standard for Device Descriptor Block (DDB)</i>.</li> </ul> <p>DDBs may contain many more data fields providing information about the peripheral. In a DSI system, read activity takes the form of two separate transactions across the bus: first the read command</p> <p>RDDDB: Read DDB Start (A1h) from host processor to peripheral, which includes the bus turn-around token.</p> <p>The peripheral then takes control of the bus and returns the requested data. The peripheral response to</p> <p>RDDDB: Read DDB Start (A1h) is a Long Packet type, so its length may be up to 64K bytes unless limited by a previous set_max_return_size command.</p>									

	<p>The response to a RDDDB: Read DDB Start (A1h) command always starts at the beginning of the Device Descriptor Block. After receiving the first packet and processing the returned DDB data, the host processor may initiate a RDDDBCON: Read DDB Continue (A8h) command to access the next portion of the DDB. A RDDDBCON: Read DDB Continue (A8h) command begins the next read at the location following the last byte of the previous data read from the DDB.</p> <p>Subsequent RDDDBCON: Read DDB Continue (A8h) commands can be used to read a DDB or supplier-proprietary block of arbitrary size. There is, however, no obligation to read the entire block. The host processor may choose to stop reading after completion of any <b>Read DDB xxx</b> command.</p>
Restriction	-
Flow Chart	<pre> graph TD     A[Read_DDB_start] --&gt; B((DDB D1[7:0], D2[7:0], ..., Dn[7:0]))     B --&gt; C[Any Command]   </pre>

### 10.2.43. RDDDBCON: Read DDB Continue (A8h)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	0	1	0	1	0	0	0	A8
Parameter 1	R	X	X	X	X	X	X	X	X	
:	R	X	X	X	X	X	X	X	X	
Parameter n	R	X	X	X	X	X	X	X	X	
Description	<p>A</p> <p>RDDDB: Read DDB Start (A1h) command should be executed at least once before a RDDDBCON: Read DDB Continue (A8h) command to define the read location.</p> <p>Otherwise, data read with a RDDDBCON: Read DDB Continue (A8h) command is undefined.</p>									
Restriction	-									
Flow Chart	<pre> graph TD     A[Read_DDB_continue] --&gt; B((DDB D1[7:0], D2[7:0], ..., Dn[7:0]))     B --&gt; C[Any Command]   </pre>									

**10.2.44. RDID1: Read ID1 (DAh)**

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	W	1	1	0	1	1	0	1	0	DA	
Parameter 1	R	module's manufacturer[7:0]									
Description	This read byte identifies the LCD module's manufacturer. It is specified by display supplier and for xx is defined as xxHEX.										
Restriction	-										
Flow Chart	<pre>graph TD; A[Read ID1] --&gt; B[/Send 1 parameter/]</pre>										

### 10.2.45. RDID2: Read ID2 (DBh)

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX																					
Command	W	1	1	0	1	1	0	1	1	DB																					
Parameter 1	R	LCD module/driver version [7:0]																													
Description	<p>This read byte is used to track the LCD module/driver version. It is defined by display supplier and changes each time a revision is made to the display, material or construction specifications. See Table:</p> <table border="1"> <thead> <tr> <th>ID Byte Value V[7:0]</th> <th>Version</th> <th>Changes</th> </tr> </thead> <tbody> <tr> <td>80h</td><td></td><td></td></tr> <tr> <td>81h</td><td></td><td></td></tr> <tr> <td>82h</td><td></td><td></td></tr> <tr> <td>83h</td><td></td><td></td></tr> <tr> <td>84h</td><td></td><td></td></tr> <tr> <td>85h</td><td></td><td></td></tr> </tbody> </table> <p>X= Don't care</p>										ID Byte Value V[7:0]	Version	Changes	80h			81h			82h			83h			84h			85h		
ID Byte Value V[7:0]	Version	Changes																													
80h																															
81h																															
82h																															
83h																															
84h																															
85h																															
Restriction	-																														
Flow Chart	<pre> graph TD     A[Read ID2] --&gt; B[Send 1 parameter]     </pre>																														

**10.2.46. RDID3: Read ID3 (DCh)**

CMD/PAs	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	<b>W</b>	1	1	0	1	1	1	0	0	DC	
Parameter 1	<b>R</b>	LCD module/driver ID[7:0]									
Description	This read byte identifies the LCD module/driver. It is specified by display supplier and for this LCD project module is defined as xxHEX.										
Restriction	-										
Flow Chart	<pre>graph TD; A[Read ID13] --&gt; B[/Send 1 parameter/]</pre>										

## 11. Electrical Specifications

### 11.1. Absolute maximum ratings

Symbol	Parameter	Unit	Value	Note
IOVCC	Interface Supply Voltage	V	-0.3 to +3.3	Note <sup>(3),(4)</sup>
VCI	Logic Supply Voltage	V	-0.3 to +3.3	Note <sup>(3),(5)</sup>
VCIP	Analog Supply Voltage	V	-0.3 to +3.3	Note <sup>(3),(6)</sup>
VCCH	High speed interface Supply Voltage	V	-0.3 to +3.3	Note <sup>(3),(7)</sup>
AVDD	Positive Voltage input	V	-0.3 to +6.6	Note <sup>(8)</sup>
AVEE	Negative Voltage input	V	0 to -6.0	Note <sup>(9)</sup>
VGH	Power Supply Voltage	V	-0.3 to +18	Note <sup>(10)</sup>
VGL	Power Supply Voltage	V	0 to -16	Note <sup>(11)</sup>
Top	Operating Temperature	°C	-40 to +85	Note <sup>(12)</sup>
Tstg	Storage Temperature	°C	-55 to +110	Note <sup>(13)</sup>

**Note:** (1) Permanent device damage may occur if absolute maximum conditions are exceeded.

(2) Functional operation should be restricted to the conditions described under DC Characteristics.

(3) IOVCC, VSSD must be maintained.

(4) To make sure IOVCC  $\geq$  VSSD.

(5) To make sure VCIP  $\geq$  AVSS.

(6) To make sure VCI  $\geq$  AVSS.

(7) To make sure VCCH  $\geq$  VSSH.

(8) To make sure AVDD  $\geq$  AVSS.

(9) To make sure AVSS  $\geq$  VSN

(10) To make sure VGH  $\geq$  AVSS.

(11) To make sure AVSS  $\geq$  VGL

$VGH + |VGL| < 30V$

(12) For die and wafer products, specified up to +85°C.

(13) This temperature specifications apply to the TCP package.

**Table 11.1: Absolute maximum ratings**

## 11.2. DC characteristics

( $T_A = -40 \sim 85^\circ C$ ,  $V_{CIP} = 2.5 \sim 3.3V$ ,  $V_{CI} = 2.5 \sim 3.3V$ ,  $IOVCC = 1.65 \sim 3.3V$ )

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
IOVCC	$V_{IN}$	Interface Supply Voltage	1.65	-	3.3	
VCIP/VCIP2/VCIP3	$V_{IN}$	Logic Supply Voltage	2.5	-	3.3	
VCI	$V_{IN}$	Analog Supply Voltage	2.5	-	3.3	
VCCH	$V_{IN}$	High speed interface Supply Voltage	1.65	-	3.3	
Input high voltage	$V_{IH}$	$IOVCC = 1.65 \sim 3.3V$ $VCIP = 2.5 \sim 3.3V$ $VCI = 2.5 \sim 3.3V$	0.7 $IOVCC$	-	$IOVCC$	V
Input low voltage	$V_{IL}$		0	-	0.3 $IOVCC$	V
VPP	$V_{IH}$	VPP	8.2V	8.3V	8.4V	V
	$V_{IL}$					
Output high voltage (LEDON, LEDPWM)	$V_{OH1}$	$I_{OH} = -1.0 \text{ mA}$	0.8 $IOVCC$	-	$IOVCC$	V
Output low voltage (LEDON, LEDPWM)	$V_{OL1}$	$IOVCC = 1.65 \sim 2.4V$ $I_{OL} = 1.0 \text{ mA}$	0	-	0.2 $IOVCC$	V
Current consumption Sleep IN mode(LP-11)	$I_{VCI}$	$VCI/VCCH = 2.8V$ , $IOVCC = 1.8V$ $T_A = 25^\circ C$	-	TBD	-	$\mu A$
	$I_{VCCH}$		-	TBD	-	$\mu A$
	$I_{IOVCC}$		-	TBD	-	$\mu A$
Current consumption during Deep-standby mode(ULPS)	$I_{VCI+VCCH}$	$VCI/VCCH = 2.8V$ , $IOVCC = 1.8V$ $T_A = 25^\circ C$	-	TBD	-	$\mu A$
	$I_{IOVCC}$		-	TBD	-	$\mu A$

Note: 1. The VOTP pin is open on normal mode and in used while OTP programming condition.  
 2. The GRAM data is eliminated under the Deep-standby mode.

Table 11.2: DC characteristic

### 11.3.AC characteristics

#### 11.3.1.Reset input timings

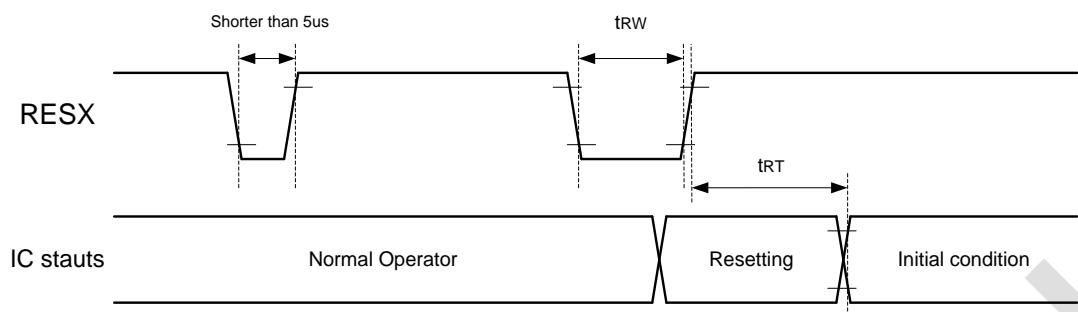


Figure 11.1: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
$t_{RW}$	Reset pulse width <sup>(2)</sup>	RESX	10	-	μs
$t_{RT}$	Reset complete time <sup>(3)</sup>	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7, 8)	ms

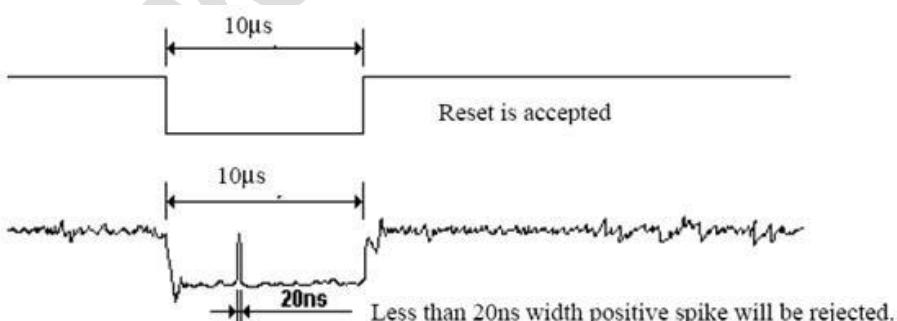
**Note:** (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time ( $t_{RT}$ ) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) It is need 120mS to read ID after Reset.

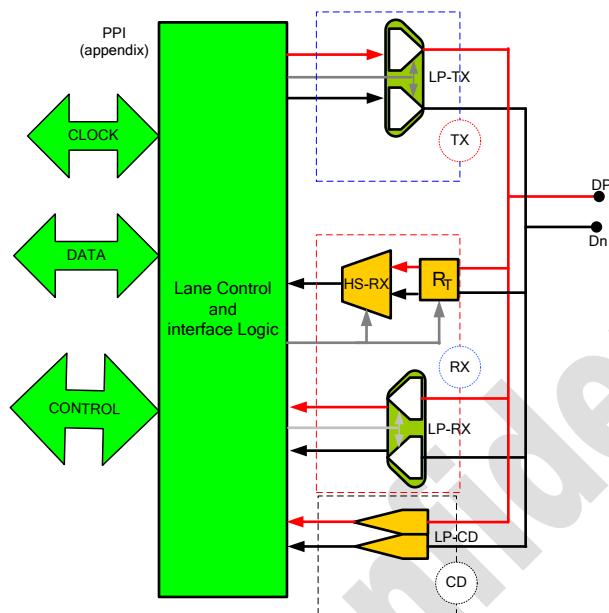
(9) After Sleep Out command, it is necessary to wait 120msec then send RESX.

Table 11.3: Reset timings

### 11.3.2.DSI D-PHY electronic characteristics

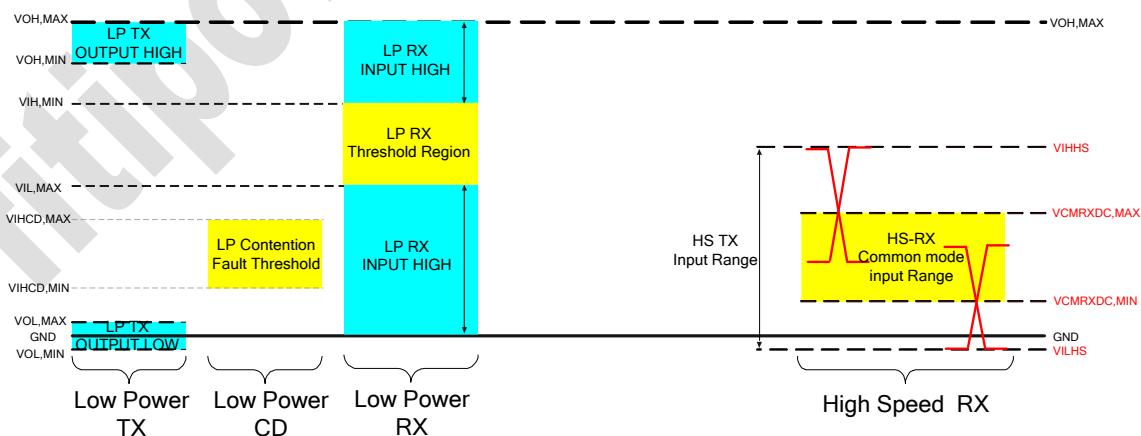
#### The Description of D-PHY Layer

In general, the DSI - PHY may contain the following electrical functions: Low-Power Receiver (LP-RX), High-Speed Receiver (HS-RX), the Low-Power Contention Detector (LP-CD), and Low Power Transmitter (LP-TX). Figure 11.6 shows the complete set of electronic functions required for a fully featured PHY transceiver.



**Figure 11.2: Electronic functions of a D-PHY transceiver**

Figure 11.7 shows both the HS and LP signal levels of electronic characteristics, respectively. Where, the HS receiver utilizes low-voltage swing differential signaling. The LP transmitter and LP receiver utilize low-voltage swing single signaling. Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.



**Figure 11.3: HS and LP signal levels**

## The Electronic Characteristics of Low-Power Transmitter (TX)

The Low-Power TX shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power modes. Hence, it is important to keep static power consumption of a LP TX be as low as possible. Under tables list DC and AC characteristic for Low power transmitter.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$V_{OH}$	Thevenin output high level	1.1	1.2	1.3	V	-
$V_{OL}$	Thevenin output low level	-50	-	50	mV	
$Z_{OLP}$	Output impedance of LP-TX	110	-	-	$\Omega$	(1)

**Note:** (1)Though no maximum value for  $Z_{OLP}$  is specified, the LP transmitter output impedance shall ensure the  $t_{RLP}/t_{FLP}$  specification is met.

Table 11.4: LP-TX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$t_{RLP}/t_{FLP}$	15%-85% rise time and fall time	-	-	25	ns	(1)
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock	90			ns	
$\delta V/\delta t_{SR}$	Slew rate @ CLOAD = 0pF	30	-	500	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 5pF	-	-	300	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 20pF	-	-	250	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 70pF	-	-	150	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	(1),(3),(7)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30 – 0.075 * (VO,INST- 700)	-	-	mV/ns	(1),(8),(9)
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	(1),(2),(3)
	$C_{LOAD}$	Load capacitance	-	-	70	pF

**Note:** (1) CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

- (2) When the output voltage is between 400 mV and 930 mV.
- (3) Measured as average across any 50 mV segment of the output signal transition.
- (4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.
- (5) This value represents a corner point in a piecewise linear curve.
- (6) When the output voltage is in the range specified by VPIN(absmax).
- (7) When the output voltage is between 400 mV and 700 mV.
- (8) Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.
- (9) When the output voltage is between 700 mV and 930 mV.

Table 11.5: LP-TX AC Specifications

## The Electronic Characteristics of Receiver (RX)

This part includes two parts which Low-Power RX and High-Speed RX. Because they have differential DC and AC characteristic, first to describe LP-RX then describe HS-RX.

### Low-Power Receiver (RX)

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSPIKE. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The Figure 11.8 shows Input Glitch Rejection of Low-Power RX. In addition, under tables list DC and AC characteristic for LP-RX.

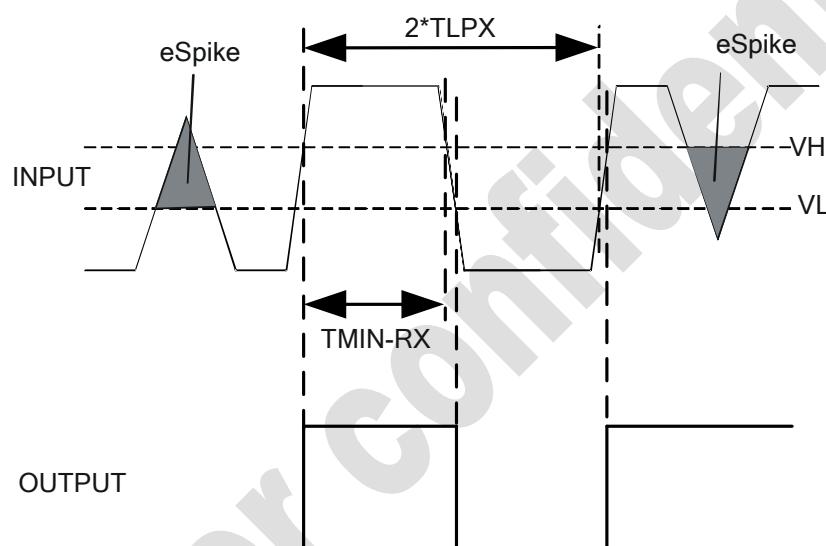


Figure 11.4: Input Glitch Rejections of Low-Power Receivers

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$V_{IH}$	Logic 1 input threshold	880	-	-	mV	-
$V_{IL}$	Logic 0 input threshold, not in ULP state	-	-	550	mV	-

Table 11.6: LP-RX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$e_{SPIKE}$	Input pulse rejection	-	-	300	V.ps	1, 2, 3
$T_{MIN}$	Minimum pulse width response	20	-	-	ns	4
$V_{INT}$	Peak-to-peak interference voltage	-	-	200	mV	-
$f_{INT}$	Interference frequency	450	-	-	MHz	-

**Note:** (1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state

(2) An impulse less than this will not change the receiver state.

(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.

(4) An input pulse greater than this shall toggle the output.

Table 11.7: LP-RX AC Specifications

## Line Contention Detection

Contention can be inferred by following conditions:

1. Detect an LP high fault when the LP transmitter is driving high and the pin voltage is less than VIL.
2. Detect an LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than VIHCD.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$V_{IHCD}$	Logic 1 contention threshold	450	-	-	mV	-
$V_{ILCD}$	Logic 0 contention threshold	-	-	200	mV	-

Table 11.8: Contention Detector DC Specifications

## High-Speed Receiver (RX)

The HS receiver is a differential line receiver. It contains a switchable parallel input termination, ZID, between the positive input pin Dp and the negative input pin Dn. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$V_{CMRXDC}$	Common-mode voltage HS receive mode	70	-	330	mV	(1),(2)
$V_{IDTH}$	Differential input high threshold	-	-	70	mV	-
$V_{IDTL}$	Differential input low threshold	-70	-	-	mV	-
$V_{IHHS}$	Single-ended input high voltage	-	-	460	mV	(1)
$V_{ILHS}$	Single-ended input low voltage	-40	-	-	mV	(1)
$Z_{ID}$	Differential input impedance	80	100	125	$\Omega$	-

**Note:** (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 11.9: HS Receiver DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	-	-	100	$mV_{PP}$	(1)
$C_{CM}$	Common mode termination	-	-	60	pF	(2)

**Note:** (1)  $\Delta V_{CMRX(HF)}$  is the peak amplitude of a sine wave superimposed on the receiver inputs.

(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

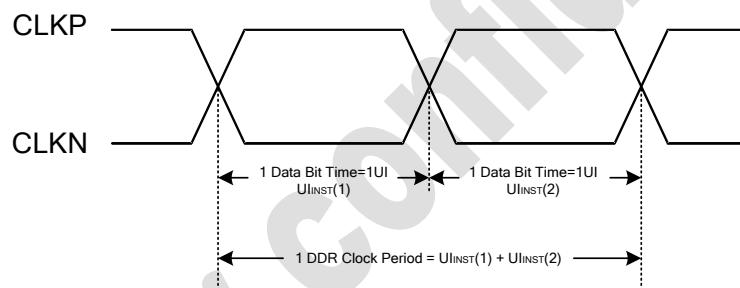
Table 11.10: HS Receiver AC Specifications

## High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CLK<sub>P</sub> – CLK<sub>N</sub>, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 11.9.



**Figure 11.5: DDR Clock Definition**

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in following Table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI <sub>INST</sub>	1.82	-	-	ns	(1), (2)

**Note:** (1) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.  
(2) Maximum total bit rate is 550Mbps/per lane @ 2 data lane 24-bit data format.

Table 11.11: Reverse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 11.10. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

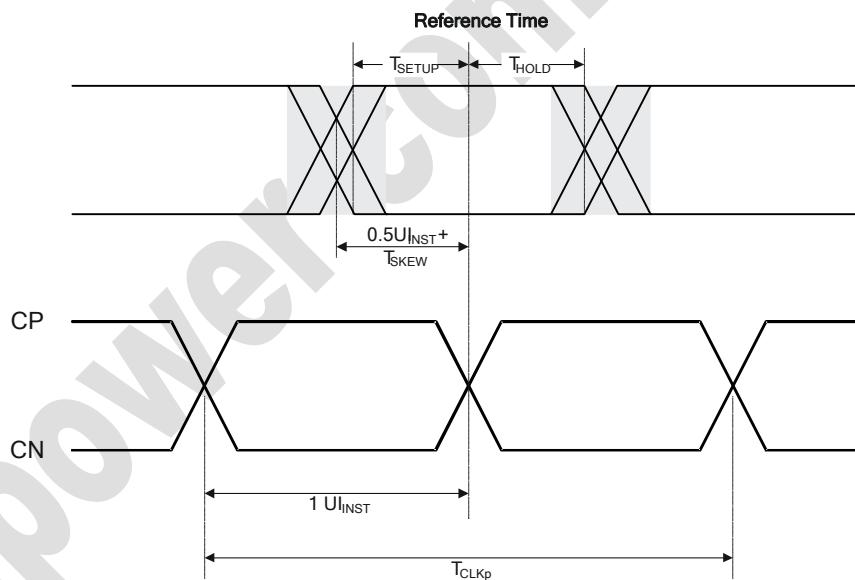


Figure 11.6: Data to Clock Timing Definitions

## Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 11.16. Implementers shall specify a value  $UI_{INST,MIN}$  that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 11.12 are specified as a part of this value.. The setup and hold times,  $T_{SETUP[RX]}$  and  $T_{HOLD[RX]}$ , respectively, describe the timing relationships between the data and clock signals.  $T_{SETUP[RX]}$  is the minimum time that data shall be present before a rising or falling clock edge and  $T_{HOLD[RX]}$  is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave  $0.4*UI_{INST}$ , i.e.  $\pm 0.2*UI_{INST}$  for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [RX]	$T_{SETUP[RX]}$	0.15	-	-	UIINST	1
Clock to Data Hold Time [RX]	$T_{HOLD[RX]}$	0.15	-	-	UIINST	1

**Note:** (1) Total setup and hold window for receiver of  $0.3*UIINST$ .

**Table 11.12: Data to Clock Timing Specifications**

### 11.3.3.Timings for DSI Video mode

#### Vertical Timings

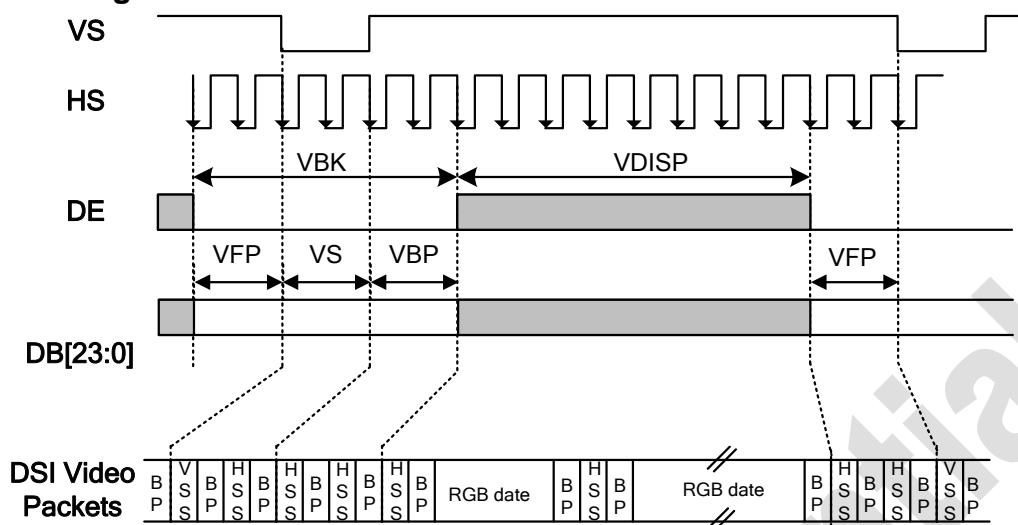


Figure 11.7: Vertical Timings for DSI Video mode I/F

Resolution=480x854(TA=25°C, IOVCC=1.8V, VCIP=2.8V, VCI=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical low pulse width	VS	-	2	-	Note(1)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(1)	Line
Vertical blanking period	VBK	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	854	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

**Note:** (1) The VS and VBP pulse width are related to GIP start pulse and GIP clock pulse timing. The GIP start pulse and GIP clock pulse must be set at corresponding position for LCD normal display.

Resolution=480x800 (TA=25°C, IOVCC=1.8V, VCIP=2.8V, VCI=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical low pulse width	VS	-	2	-	Note(1)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(1)	Line
Vertical blanking period	VBK	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	800	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

**Note:** (1) The VS and VBP pulse width are related to GIP start pulse and GIP clock pulse timing. The GIP start pulse and GIP clock pulse must be set at corresponding position for LCD normal display.

Table 11.13: Vertical Timings for DSI Video mode I/F

## Horizontal Timings

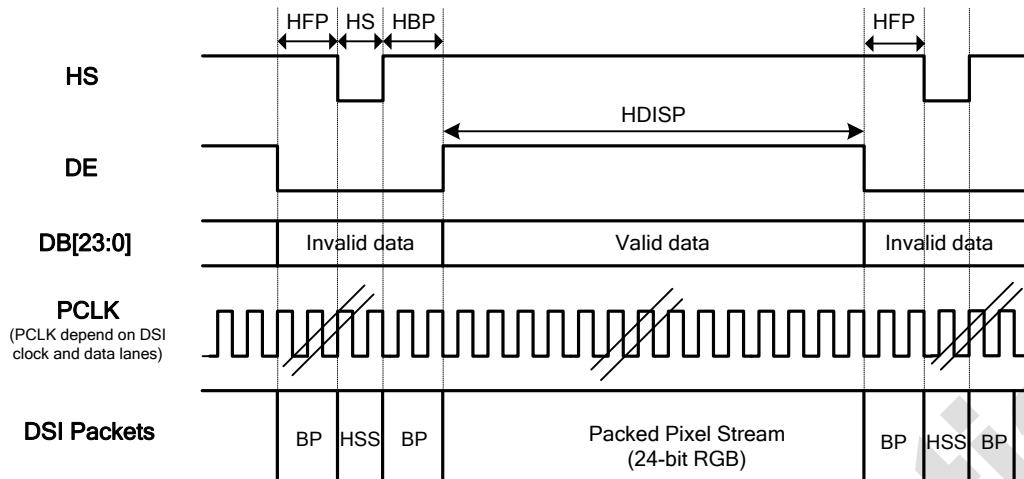


Figure 11.8: Horizontal Timing for DSI Video mode I/F

Resolution=480x854 (TA=25°C, IOVCC=1.8V, VCIP=2.8V, VCI=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	6	-	78	DCK
Horizontal back porch	HBP	-	5	-	78	DCK
Horizontal front porch	HFP	-	5	-	78	DCK
Horizontal blanking period	HBLK	HS+HBP+HFP	16	-	88	DCK
Horizontal active area	HDISP	-	-	480	-	DCK

Resolution=480x800 (TA=25°C, IOVCC=1.8V, VCIP=2.8V, VCI=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	6	-	78	DCK
Horizontal back porch	HBP	-	5	-	78	DCK
Horizontal front porch	HFP	-	5	-	78	DCK
Horizontal blanking period	HBLK	HS+HBP+HFP	16	-	88	DCK
Horizontal active area	HDISP	-	-	480	-	DCK

Note: (1) HS+HBP>0.5uS.

(2) HFP>0.5uS.

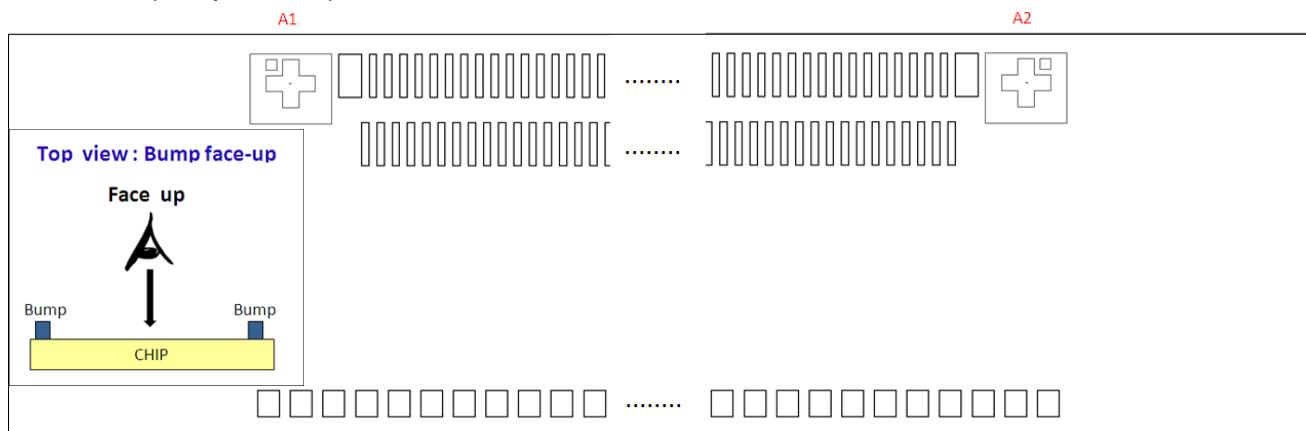
Table 11.14: Horizontal Timings for DSI Video mode I/F

## 12. Chip information

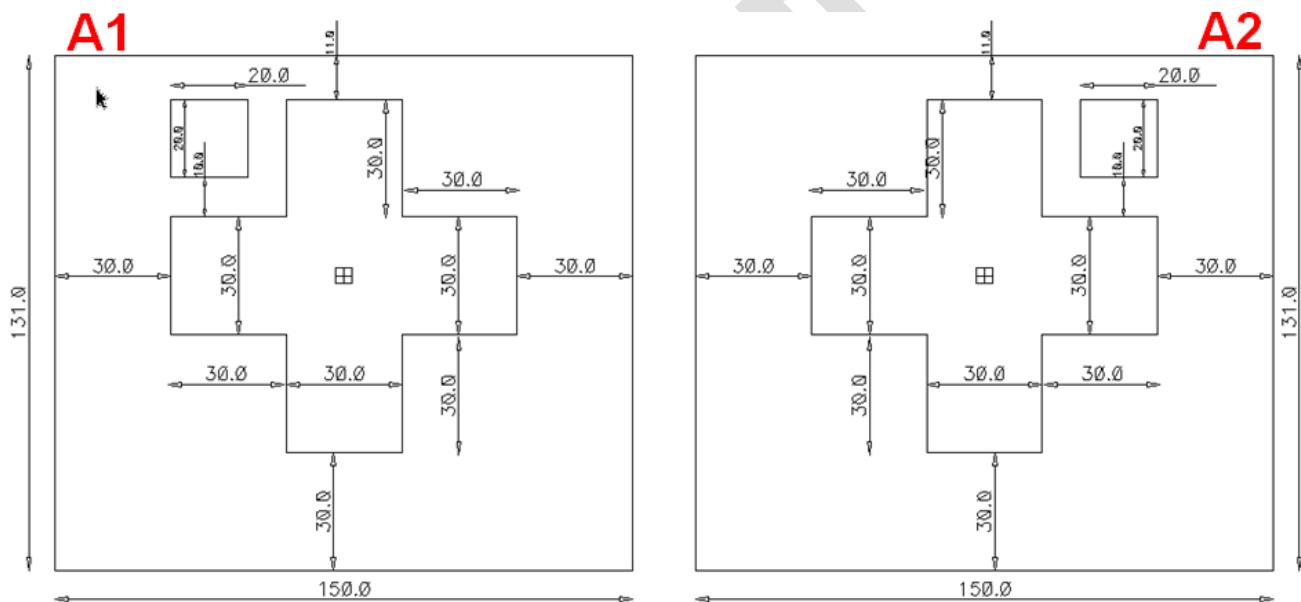
### 12.1. PAD assignment

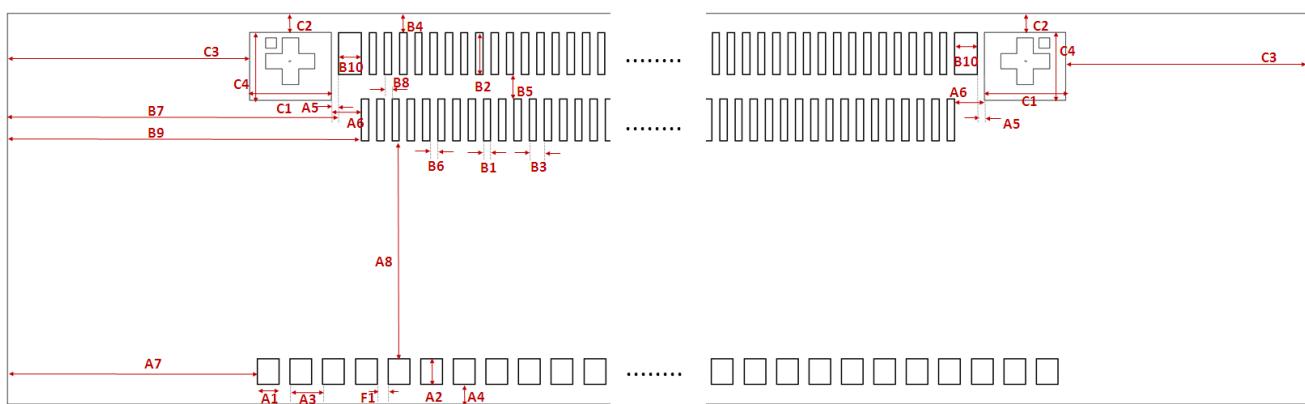
IC chip size: 24780um X754um (Include Scribe-Line)

Overview (Simple view)



Alignment Mark:





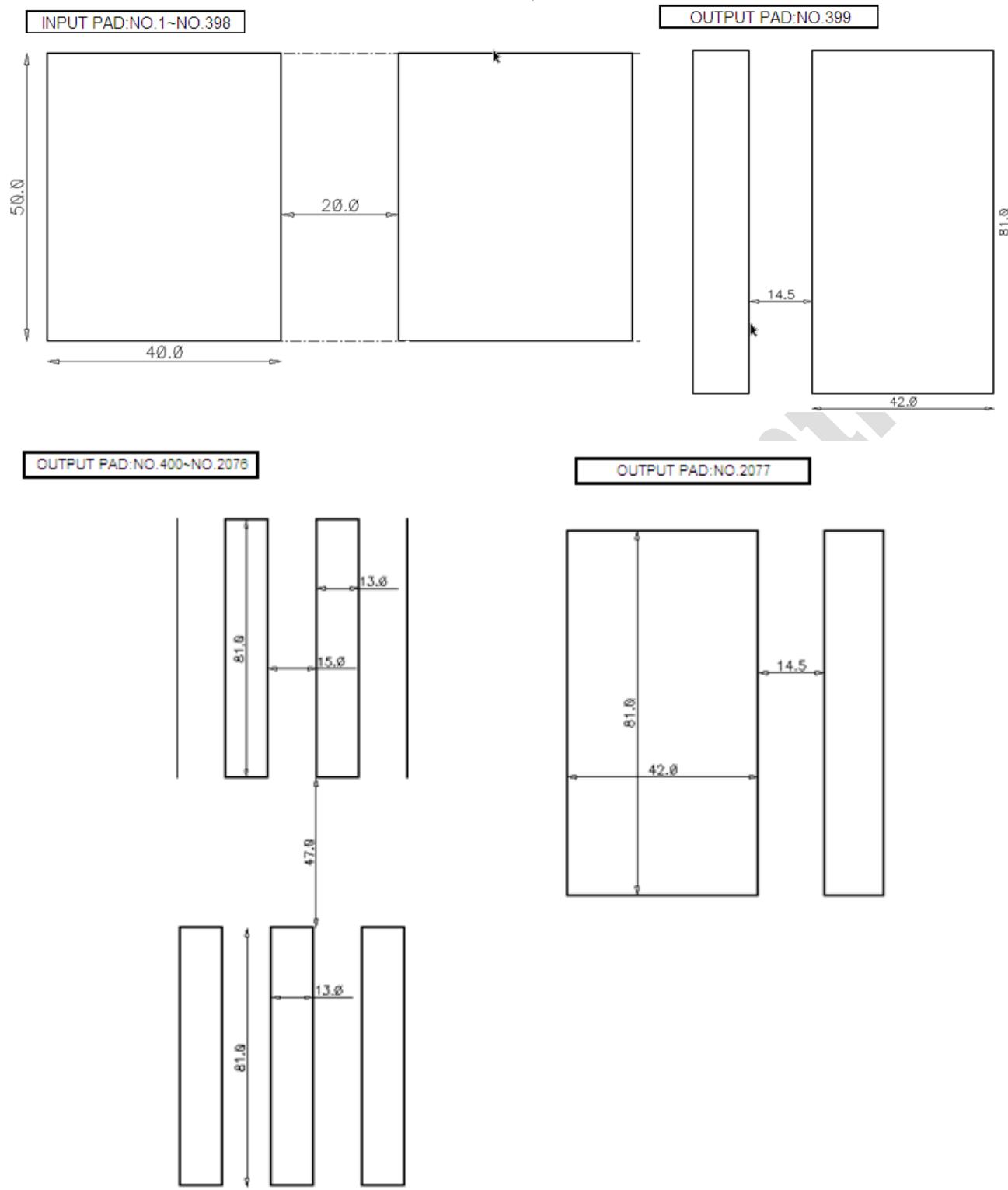
Condition-1 (+/- 3um temp. compensation) Unit=um

#### Input Pad (From NO.1 ~ NO.398)

INPUT PAD			INPUT PAD Special		
Symbol	Size	Number	Symbol	Size	Number
A1	40	No.1~398	F1	20	No.1~398
A2	50				
A3	60				
A4	37				
A5	14				
A6	56.5				
A7	460				
A8	421				

#### Output Pad (From NO.400 ~ NO.2076)

OUTPUT PAD			AMARK	
Symbol	Size	Number	Symbol	Size
B1	13	No.400~2076	C1	150
B2	81		C2	36
B3	28		C3	445
B4	37		C4	131
B5	47			
B6	15			
B7	609			
B8	14			
B9	651			
B10	42			



## 12.2. PAD location

No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axi	Y-axi
1	AVSS	-11910	-315	61	VSSP2	-8310	-315	121	DUMMY	-4710	-315	181	VDDD	-1110	-315
2	AVSS	-11850	-315	62	VSSP2	-8250	-315	122	DUMMY	-4650	-315	182	VSSH	-1050	-315
3	AVSS	-11790	-315	63	VSSD	-8190	-315	123	DUMMY	-4590	-315	183	VSSH	-990	-315
4	COGTESTA[1]	-11730	-315	64	VSSD	-8130	-315	124	DUMMY	-4530	-315	184	VSSH	-930	-315
5	COGTESTA[2]	-11670	-315	65	VSSD	-8070	-315	125	DUMMY	-4470	-315	185	VSSH	-870	-315
6	VCOM	-11610	-315	66	VDDD	-8010	-315	126	DUMMY	-4410	-315	186	VSSH	-810	-315
7	VCOM	-11550	-315	67	VDDD	-7950	-315	127	DUMMY	-4350	-315	187	HS_D1P	-750	-315
8	VCOM	-11490	-315	68	VDDD	-7890	-315	128	DUMMY	-4290	-315	188	HS_D1P	-690	-315
9	VCOM	-11430	-315	69	VCIP	-7830	-315	129	DUMMY	-4230	-315	189	HS_D1P	-630	-315
10	VCOM	-11370	-315	70	VCIP	-7770	-315	130	DUMMY	-4170	-315	190	HS_D1P	-570	-315
11	COGTESTB[1]	-11310	-315	71	VCIP	-7710	-315	131	DUMMY	-4110	-315	191	HS_D1N	-510	-315
12	COGTESTB[2]	-11250	-315	72	VSSP2	-7650	-315	132	DUMMY	-4050	-315	192	HS_D1N	-450	-315
13	VPP	-11190	-315	73	VSSP2	-7590	-315	133	NC	-3990	-315	193	HS_D1N	-390	-315
14	VPP	-11130	-315	74	VSSP2	-7530	-315	134	NC	-3930	-315	194	HS_D1N	-330	-315
15	VPP	-11070	-315	75	VSSP2	-7470	-315	135	NC	-3870	-315	195	VSSH	-270	-315
16	VPP	-11010	-315	76	VSSP2	-7410	-315	136	NC	-3810	-315	196	VSSH	-210	-315
17	VPP	-10950	-315	77	VSSP2	-7350	-315	137	NC	-3750	-315	197	HS_CKP	-150	-315
18	VGL	-10890	-315	78	VSSP	-7290	-315	138	NC	-3690	-315	198	HS_CKP	-90	-315
19	VGL	-10830	-315	79	VSSP	-7230	-315	139	NC	-3630	-315	199	HS_CKP	-30	-315
20	VGL	-10770	-315	80	VSSP	-7170	-315	140	NC	-3570	-315	200	HS_CKP	30	-315
21	VGL	-10710	-315	81	IOVCC	-7110	-315	141	NC	-3510	-315	201	HS_CKN	90	-315
22	VGL	-10650	-315	82	LANSEL	-7050	-315	142	NC	-3450	-315	202	HS_CKN	150	-315
23	VGL	-10590	-315	83	DSWAP	-6990	-315	143	DUMMY	-3390	-315	203	HS_CKN	210	-315
24	VGH2_L	-10530	-315	84	PSWAP	-6930	-315	144	DUMMY	-3330	-315	204	HS_CKN	270	-315
25	VGH1_L	-10470	-315	85	VSSD	-6870	-315	145	DUMMY	-3270	-315	205	VSSH	330	-315
26	VSSP2	-10410	-315	86	TESTS[0]	-6810	-315	146	DUMMY	-3210	-315	206	VSSH	390	-315
27	VSSP2	-10350	-315	87	NBWSEL	-6750	-315	147	LEDPWM	-3150	-315	207	HS_D0P	450	-315
28	VSSP2	-10290	-315	88	VSSP2	-6690	-315	148	LEDON	-3090	-315	208	HS_D0P	510	-315
29	VSSP2	-10230	-315	89	VSSP2	-6630	-315	149	TEST_OSC	-3030	-315	209	HS_D0P	570	-315
30	VSSP2	-10170	-315	90	VSSP2	-6570	-315	150	DUMMY	-2970	-315	210	HS_D0P	630	-315
31	VSSP2	-10110	-315	91	VSSP2	-6510	-315	151	IOVCC	-2910	-315	211	HS_D0N	690	-315
32	VSSP2	-10050	-315	92	IOVCC	-6450	-315	152	IOVCC	-2850	-315	212	HS_D0N	750	-315
33	VSSP2	-9990	-315	93	DUMMY	-6390	-315	153	IOVCC	-2790	-315	213	HS_D0N	810	-315
34	VSSP	-9930	-315	94	DUMMY	-6330	-315	154	VSSD	-2730	-315	214	HS_D0N	870	-315
35	VSSP	-9870	-315	95	DUMMY	-6270	-315	155	VSSD	-2670	-315	215	VSSH	930	-315
36	VSSP	-9810	-315	96	DUMMY	-6210	-315	156	VSSD	-2610	-315	216	VSSH	990	-315
37	VSSP	-9750	-315	97	IM[1]	-6150	-315	157	VCIP2	-2550	-315	217	VDDH	1050	-315
38	VCIP	-9690	-315	98	IM[0]	-6090	-315	158	VCIP2	-2490	-315	218	VDDH	1110	-315
39	VCIP	-9630	-315	99	VSSP3	-6030	-315	159	VCIP2	-2430	-315	219	VDDH	1170	-315
40	VCIP	-9570	-315	100	VSSP3	-5970	-315	160	VCIP2	-2370	-315	220	DUMMY	1230	-315
41	VCIP	-9510	-315	101	VSSP3	-5910	-315	161	AVSS	-2310	-315	221	DUMMY	1290	-315
42	VCIP	-9450	-315	102	VSSP3	-5850	-315	162	AVSS	-2250	-315	222	DUMMY	1350	-315
43	VCIP	-9390	-315	103	DUMMY	-5790	-315	163	AVSS	-2190	-315	223	VCCH	1410	-315
44	VCIP	-9330	-315	104	TE_L	-5730	-315	164	AVSS	-2130	-315	224	VCCH	1470	-315
45	VCIP	-9270	-315	105	TESTS[1]	-5670	-315	165	VSSP2	-2070	-315	225	VCCH	1530	-315
46	AVSS	-9210	-315	106	NC	-5610	-315	166	VSSP2	-2010	-315	226	VCCH	1590	-315
47	AVSS	-9150	-315	107	NC	-5550	-315	167	VSSP2	-1950	-315	227	VCCH	1650	-315
48	AVSS	-9090	-315	108	NC	-5490	-315	168	VSSP2	-1890	-315	228	VCIR	1710	-315
49	AVSS	-9030	-315	109	NC	-5430	-315	169	VSSP2	-1830	-315	229	VCIR	1770	-315
50	TESTI[0]	-8970	-315	110	NC	-5370	-315	170	VCIP	-1770	-315	230	VCIR	1830	-315
51	TESTI[1]	-8910	-315	111	NC	-5310	-315	171	VCIP	-1710	-315	231	DUMMY	1890	-315
52	TESTI[2]	-8850	-315	112	RESX	-5250	-315	172	VCIP	-1650	-315	232	TE_R	1950	-315
53	TESTI[3]	-8790	-315	113	VSSD	-5190	-315	173	VCIP	-1590	-315	233	AVSS	2010	-315
54	VCIP	-8730	-315	114	VSSD	-5130	-315	174	VSSD	-1530	-315	234	AVSS	2070	-315
55	NC	-8670	-315	115	VSSD	-5070	-315	175	VSSD	-1470	-315	235	AVSS	2130	-315
56	NC	-8610	-315	116	IOVCC	-5010	-315	176	VSSD	-1410	-315	236	AVSS	2190	-315
57	D_TEST_N	-8550	-315	117	IOVCC	-4950	-315	177	VSSD	-1350	-315	237	TEST_P	2250	-315
58	D_TEST_N	-8490	-315	118	IOVCC	-4890	-315	178	VDDD	-1290	-315	238	TEST_N	2310	-315
59	VSSP2	-8430	-315	119	DUMMY	-4830	-315	179	VDDD	-1230	-315	239	DUMMY	2370	-315
60	VSSP2	-8370	-315	120	DUMMY	-4770	-315	180	VDDD	-1170	-315	240	DUMMY	2430	-315

No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi
241	DUMMY	2490	-315	301	VSSP2	6090	-315	361	VSSP2	9690	-315	421	VGL	11438	299.5
242	DUMMY	2550	-315	302	VSSP2	6150	-315	362	VSSP2	9750	-315	422	VGL	11424	171.5
243	DUMMY	2610	-315	303	VSSP2	6210	-315	363	VSSP2	9810	-315	423	GCK[3]_R	11410	299.5
244	DUMMY	2670	-315	304	VSSP2	6270	-315	364	VSSP2	9870	-315	424	GCK[3]_R	11396	171.5
245	TEST_P1	2730	-315	305	VSSP2	6330	-315	365	VGH	9930	-315	425	GCK[4]_R	11382	299.5
246	TEST_P1	2790	-315	306	VSSP2	6390	-315	366	VGH	9990	-315	426	GCK[4]_R	11368	171.5
247	TEST_P2	2850	-315	307	VSSP2	6450	-315	367	VGH1_R	10050	-315	427	GCK[5]_R	11354	299.5
248	TEST_P2	2910	-315	308	VSSP2	6510	-315	368	VGH1_R	10110	-315	428	GCK[5]_R	11340	171.5
249	VCIP	2970	-315	309	VSSP2	6570	-315	369	VGH2_R	10170	-315	429	GCK[6]_R	11326	299.5
250	VCIP	3030	-315	310	VSSP2	6630	-315	370	VGH2_R	10230	-315	430	GCK[6]_R	11312	171.5
251	VCIP	3090	-315	311	VSSP2	6690	-315	371	VCIP2	10290	-315	431	GCK[7]_R	11298	299.5
252	VCIP	3150	-315	312	VSSP2	6750	-315	372	VCIP2	10350	-315	432	GCK[7]_R	11284	171.5
253	VCIP	3210	-315	313	VSSP2	6810	-315	373	VCIP2	10410	-315	433	GCK[8]_R	11270	299.5
254	VCIP	3270	-315	314	VSSP2	6870	-315	374	VCIP2	10470	-315	434	GCK[8]_R	11256	171.5
255	VSSP	3330	-315	315	VCIP2	6930	-315	375	VGL	10530	-315	435	GCK[9]_R	11242	299.5
256	VSSP	3390	-315	316	VCIP2	6990	-315	376	VGL	10590	-315	436	GCK[9]_R	11228	171.5
257	VSSP	3450	-315	317	VCIP2	7050	-315	377	VGL	10650	-315	437	GCK[10]_R	11214	299.5
258	VSSP	3510	-315	318	VCIP2	7110	-315	378	VGL	10710	-315	438	GCK[10]_R	11200	171.5
259	VSSP	3570	-315	319	VCIP2	7170	-315	379	VGL	10770	-315	439	GCK[11]_R	11186	299.5
260	VSSP	3630	-315	320	VCIP2	7230	-315	380	VGL	10830	-315	440	GCK[11]_R	11172	171.5
261	VSSP3	3690	-315	321	VCIP2	7290	-315	381	VGL	10890	-315	441	GCK[12]_R	11158	299.5
262	VSSP3	3750	-315	322	VCIP2	7350	-315	382	VGL	10950	-315	442	GCK[12]_R	11144	171.5
263	VSSP3	3810	-315	323	VCIP2	7410	-315	383	NC	11010	-315	443	GCK[13]_R	11130	299.5
264	VSSP3	3870	-315	324	VCIP	7470	-315	384	NC	11070	-315	444	GCK[13]_R	11116	171.5
265	VSSP3	3930	-315	325	VCIP	7530	-315	385	HVTEST1	11130	-315	445	GCK[14]_R	11102	299.5
266	VSSP3	3990	-315	326	VCIP	7590	-315	386	HVTEST1	11190	-315	446	GCK[14]_R	11088	171.5
267	AVEE	4050	-315	327	VCIP	7650	-315	387	COGTESTC[1]	11250	-315	447	GCK[15]_R	11074	299.5
268	AVEE	4110	-315	328	VCIP	7710	-315	388	COGTESTC[2]	11310	-315	448	GCK[15]_R	11060	171.5
269	AVEE	4170	-315	329	VSSP2	7770	-315	389	VCOM	11370	-315	449	GCK[16]_R	11046	299.5
270	AVDD	4230	-315	330	VSSP2	7830	-315	390	VCOM	11430	-315	450	GCK[16]_R	11032	171.5
271	AVDD	4290	-315	331	VSSP2	7890	-315	391	VCOM	11490	-315	451	VGH	11018	299.5
272	AVDD	4350	-315	332	VSSP2	7950	-315	392	VCOM	11550	-315	452	VGH	11004	171.5
273	VCIP3	4410	-315	333	VSSP2	8010	-315	393	VCOM	11610	-315	453	VGH	10990	299.5
274	VCIP3	4470	-315	334	VSSP2	8070	-315	394	COGTESTD[1]	11670	-315	454	VGH	10976	171.5
275	VCIP3	4530	-315	335	VSSP2	8130	-315	395	COGTESTD[2]	11730	-315	455	VGH	10962	299.5
276	VCIP3	4590	-315	336	AVSS	8190	-315	396	AVSS	11790	-315	456	VGH	10948	171.5
277	VCIP3	4650	-315	337	AVSS	8250	-315	397	AVSS	11850	-315	457	VGH	10934	299.5
278	VCIP3	4710	-315	338	AVSS	8310	-315	398	AVSS	11910	-315	458	VGH	10920	171.5
279	VCIP2	4770	-315	339	VSSP	8370	-315	399	AVSS	11760	299.5	459	VGL	10906	299.5
280	VCIP2	4830	-315	340	VSSP	8430	-315	400	AVSS	11732	171.5	460	VGL	10892	171.5
281	VCIP2	4890	-315	341	VSSP	8490	-315	401	AVSS	11718	299.5	461	VGL	10878	299.5
282	VCIP2	4950	-315	342	VSSP	8550	-315	402	COGTESTE[1]	11704	171.5	462	VGL	10864	171.5
283	VCIP2	5010	-315	343	VCIP2	8610	-315	403	COGTESTE[2]	11690	299.5	463	VGL	10850	299.5
284	VCIP2	5070	-315	344	VCIP2	8670	-315	404	VGH	11676	171.5	464	VGL	10836	171.5
285	VCIP2	5130	-315	345	VCIP2	8730	-315	405	VGH	11662	299.5	465	VGL	10822	299.5
286	VCIP2	5190	-315	346	VCIP2	8790	-315	406	VGH	11648	171.5	466	VGL	10808	171.5
287	VCIP2	5250	-315	347	VCIP2	8850	-315	407	VGL	11634	299.5	467	VGL	10794	299.5
288	VCIP2	5310	-315	348	VCIP2	8910	-315	408	VGL	11620	171.5	468	AVSS	10780	171.5
289	VSSP	5370	-315	349	VCIP2	8970	-315	409	VGL	11606	299.5	469	AVSS	10766	299.5
290	VSSP	5430	-315	350	VCIP2	9030	-315	410	GCK[1]_R	11592	171.5	470	NC	10752	171.5
291	VSSP	5490	-315	351	VCIP2	9090	-315	411	GCK[1]_R	11578	299.5	471	NC	10738	299.5
292	VSSP	5550	-315	352	VCIP3	9150	-315	412	GCK[2]_R	11564	171.5	472	S[1]	10724	171.5
293	VSSP	5610	-315	353	VCIP3	9210	-315	413	GCK[2]_R	11550	299.5	473	S[2]	10710	299.5
294	VSSP2	5670	-315	354	VCIP3	9270	-315	414	VGL	11536	171.5	474	S[3]	10696	171.5
295	VSSP2	5730	-315	355	VDDD	9330	-315	415	VGL	11522	299.5	475	S[4]	10682	299.5
296	VSSP2	5790	-315	356	VDDD	9390	-315	416	VGL	11508	171.5	476	S[5]	10668	171.5
297	VSSP2	5850	-315	357	VDDD	9450	-315	417	DUMMY	11494	299.5	477	S[6]	10654	299.5
298	VSSP2	5910	-315	358	VSSA	9510	-315	418	DUMMY	11480	171.5	478	S[7]	10640	171.5
299	VSSP2	5970	-315	359	VSSA	9570	-315	419	DUMMY	11466	299.5	479	S[8]	10626	299.5
300	VSSP2	6030	-315	360	VSSA	9630	-315	420	VGL	11452	171.5	480	S[9]	10612	171.5

No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi
481	S[10]	10598	299.5	541	S[70]	9758	299.5	601	S[130]	8918	299.5	661	S[190]	8078	299.5
482	S[11]	10584	171.5	542	S[71]	9744	171.5	602	S[131]	8904	171.5	662	S[191]	8064	171.5
483	S[12]	10570	299.5	543	S[72]	9730	299.5	603	S[132]	8890	299.5	663	S[192]	8050	299.5
484	S[13]	10556	171.5	544	S[73]	9716	171.5	604	S[133]	8876	171.5	664	S[193]	8036	171.5
485	S[14]	10542	299.5	545	S[74]	9702	299.5	605	S[134]	8862	299.5	665	S[194]	8022	299.5
486	S[15]	10528	171.5	546	S[75]	9688	171.5	606	S[135]	8848	171.5	666	S[195]	8008	171.5
487	S[16]	10514	299.5	547	S[76]	9674	299.5	607	S[136]	8834	299.5	667	S[196]	7994	299.5
488	S[17]	10500	171.5	548	S[77]	9660	171.5	608	S[137]	8820	171.5	668	S[197]	7980	171.5
489	S[18]	10486	299.5	549	S[78]	9646	299.5	609	S[138]	8806	299.5	669	S[198]	7966	299.5
490	S[19]	10472	171.5	550	S[79]	9632	171.5	610	S[139]	8792	171.5	670	S[199]	7952	171.5
491	S[20]	10458	299.5	551	S[80]	9618	299.5	611	S[140]	8778	299.5	671	S[200]	7938	299.5
492	S[21]	10444	171.5	552	S[81]	9604	171.5	612	S[141]	8764	171.5	672	S[201]	7924	171.5
493	S[22]	10430	299.5	553	S[82]	9590	299.5	613	S[142]	8750	299.5	673	S[202]	7910	299.5
494	S[23]	10416	171.5	554	S[83]	9576	171.5	614	S[143]	8736	171.5	674	S[203]	7896	171.5
495	S[24]	10402	299.5	555	S[84]	9562	299.5	615	S[144]	8722	299.5	675	S[204]	7882	299.5
496	S[25]	10388	171.5	556	S[85]	9548	171.5	616	S[145]	8708	171.5	676	S[205]	7868	171.5
497	S[26]	10374	299.5	557	S[86]	9534	299.5	617	S[146]	8694	299.5	677	S[206]	7854	299.5
498	S[27]	10360	171.5	558	S[87]	9520	171.5	618	S[147]	8680	171.5	678	S[207]	7840	171.5
499	S[28]	10346	299.5	559	S[88]	9506	299.5	619	S[148]	8666	299.5	679	S[208]	7826	299.5
500	S[29]	10332	171.5	560	S[89]	9492	171.5	620	S[149]	8652	171.5	680	S[209]	7812	171.5
501	S[30]	10318	299.5	561	S[90]	9478	299.5	621	S[150]	8638	299.5	681	S[210]	7798	299.5
502	S[31]	10304	171.5	562	S[91]	9464	171.5	622	S[151]	8624	171.5	682	S[211]	7784	171.5
503	S[32]	10290	299.5	563	S[92]	9450	299.5	623	S[152]	8610	299.5	683	S[212]	7770	299.5
504	S[33]	10276	171.5	564	S[93]	9436	171.5	624	S[153]	8596	171.5	684	S[213]	7756	171.5
505	S[34]	10262	299.5	565	S[94]	9422	299.5	625	S[154]	8582	299.5	685	S[214]	7742	299.5
506	S[35]	10248	171.5	566	S[95]	9408	171.5	626	S[155]	8568	171.5	686	S[215]	7728	171.5
507	S[36]	10234	299.5	567	S[96]	9394	299.5	627	S[156]	8554	299.5	687	S[216]	7714	299.5
508	S[37]	10220	171.5	568	S[97]	9380	171.5	628	S[157]	8540	171.5	688	S[217]	7700	171.5
509	S[38]	10206	299.5	569	S[98]	9366	299.5	629	S[158]	8526	299.5	689	S[218]	7686	299.5
510	S[39]	10192	171.5	570	S[99]	9352	171.5	630	S[159]	8512	171.5	690	S[219]	7672	171.5
511	S[40]	10178	299.5	571	S[100]	9338	299.5	631	S[160]	8498	299.5	691	S[220]	7658	299.5
512	S[41]	10164	171.5	572	S[101]	9324	171.5	632	S[161]	8484	171.5	692	S[221]	7644	171.5
513	S[42]	10150	299.5	573	S[102]	9310	299.5	633	S[162]	8470	299.5	693	S[222]	7630	299.5
514	S[43]	10136	171.5	574	S[103]	9296	171.5	634	S[163]	8456	171.5	694	S[223]	7616	171.5
515	S[44]	10122	299.5	575	S[104]	9282	299.5	635	S[164]	8442	299.5	695	S[224]	7602	299.5
516	S[45]	10108	171.5	576	S[105]	9268	171.5	636	S[165]	8428	171.5	696	S[225]	7588	171.5
517	S[46]	10094	299.5	577	S[106]	9254	299.5	637	S[166]	8414	299.5	697	S[226]	7574	299.5
518	S[47]	10080	171.5	578	S[107]	9240	171.5	638	S[167]	8400	171.5	698	S[227]	7560	171.5
519	S[48]	10066	299.5	579	S[108]	9226	299.5	639	S[168]	8386	299.5	699	S[228]	7546	299.5
520	S[49]	10052	171.5	580	S[109]	9212	171.5	640	S[169]	8372	171.5	700	S[229]	7532	171.5
521	S[50]	10038	299.5	581	S[110]	9198	299.5	641	S[170]	8358	299.5	701	S[230]	7518	299.5
522	S[51]	10024	171.5	582	S[111]	9184	171.5	642	S[171]	8344	171.5	702	S[231]	7504	171.5
523	S[52]	10010	299.5	583	S[112]	9170	299.5	643	S[172]	8330	299.5	703	S[232]	7490	299.5
524	S[53]	9996	171.5	584	S[113]	9156	171.5	644	S[173]	8316	171.5	704	S[233]	7476	171.5
525	S[54]	9982	299.5	585	S[114]	9142	299.5	645	S[174]	8302	299.5	705	S[234]	7462	299.5
526	S[55]	9968	171.5	586	S[115]	9128	171.5	646	S[175]	8288	171.5	706	S[235]	7448	171.5
527	S[56]	9954	299.5	587	S[116]	9114	299.5	647	S[176]	8274	299.5	707	S[236]	7434	299.5
528	S[57]	9940	171.5	588	S[117]	9100	171.5	648	S[177]	8260	171.5	708	S[237]	7420	171.5
529	S[58]	9926	299.5	589	S[118]	9086	299.5	649	S[178]	8246	299.5	709	S[238]	7406	299.5
530	S[59]	9912	171.5	590	S[119]	9072	171.5	650	S[179]	8232	171.5	710	S[239]	7392	171.5
531	S[60]	9898	299.5	591	S[120]	9058	299.5	651	S[180]	8218	299.5	711	S[240]	7378	299.5
532	S[61]	9884	171.5	592	S[121]	9044	171.5	652	S[181]	8204	171.5	712	S[241]	7364	171.5
533	S[62]	9870	299.5	593	S[122]	9030	299.5	653	S[182]	8190	299.5	713	S[242]	7350	299.5
534	S[63]	9856	171.5	594	S[123]	9016	171.5	654	S[183]	8176	171.5	714	S[243]	7336	171.5
535	S[64]	9842	299.5	595	S[124]	9002	299.5	655	S[184]	8162	299.5	715	S[244]	7322	299.5
536	S[65]	9828	171.5	596	S[125]	8988	171.5	656	S[185]	8148	171.5	716	S[245]	7308	171.5
537	S[66]	9814	299.5	597	S[126]	8974	299.5	657	S[186]	8134	299.5	717	S[246]	7294	299.5
538	S[67]	9800	171.5	598	S[127]	8960	171.5	658	S[187]	8120	171.5	718	S[247]	7280	171.5
539	S[68]	9786	299.5	599	S[128]	8946	299.5	659	S[188]	8106	299.5	719	S[248]	7266	299.5
540	S[69]	9772	171.5	600	S[129]	8932	171.5	660	S[189]	8092	171.5	720	S[249]	7252	171.5

No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi
721	S[250]	7238	299.5	781	S[310]	6398	299.5	841	S[370]	5558	299.5	901	S[430]	4718	299.5
722	S[251]	7224	171.5	782	S[311]	6384	171.5	842	S[371]	5544	171.5	902	S[431]	4704	171.5
723	S[252]	7210	299.5	783	S[312]	6370	299.5	843	S[372]	5530	299.5	903	S[432]	4690	299.5
724	S[253]	7196	171.5	784	S[313]	6356	171.5	844	S[373]	5516	171.5	904	S[433]	4676	171.5
725	S[254]	7182	299.5	785	S[314]	6342	299.5	845	S[374]	5502	299.5	905	S[434]	4662	299.5
726	S[255]	7168	171.5	786	S[315]	6328	171.5	846	S[375]	5488	171.5	906	S[435]	4648	171.5
727	S[256]	7154	299.5	787	S[316]	6314	299.5	847	S[376]	5474	299.5	907	S[436]	4634	299.5
728	S[257]	7140	171.5	788	S[317]	6300	171.5	848	S[377]	5460	171.5	908	S[437]	4620	171.5
729	S[258]	7126	299.5	789	S[318]	6286	299.5	849	S[378]	5446	299.5	909	S[438]	4606	299.5
730	S[259]	7112	171.5	790	S[319]	6272	171.5	850	S[379]	5432	171.5	910	S[439]	4592	171.5
731	S[260]	7098	299.5	791	S[320]	6258	299.5	851	S[380]	5418	299.5	911	S[440]	4578	299.5
732	S[261]	7084	171.5	792	S[321]	6244	171.5	852	S[381]	5404	171.5	912	S[441]	4564	171.5
733	S[262]	7070	299.5	793	S[322]	6230	299.5	853	S[382]	5390	299.5	913	S[442]	4550	299.5
734	S[263]	7056	171.5	794	S[323]	6216	171.5	854	S[383]	5376	171.5	914	S[443]	4536	171.5
735	S[264]	7042	299.5	795	S[324]	6202	299.5	855	S[384]	5362	299.5	915	S[444]	4522	299.5
736	S[265]	7028	171.5	796	S[325]	6188	171.5	856	S[385]	5348	171.5	916	S[445]	4508	171.5
737	S[266]	7014	299.5	797	S[326]	6174	299.5	857	S[386]	5334	299.5	917	S[446]	4494	299.5
738	S[267]	7000	171.5	798	S[327]	6160	171.5	858	S[387]	5320	171.5	918	S[447]	4480	171.5
739	S[268]	6986	299.5	799	S[328]	6146	299.5	859	S[388]	5306	299.5	919	S[448]	4466	299.5
740	S[269]	6972	171.5	800	S[329]	6132	171.5	860	S[389]	5292	171.5	920	S[449]	4452	171.5
741	S[270]	6958	299.5	801	S[330]	6118	299.5	861	S[390]	5278	299.5	921	S[450]	4438	299.5
742	S[271]	6944	171.5	802	S[331]	6104	171.5	862	S[391]	5264	171.5	922	S[451]	4424	171.5
743	S[272]	6930	299.5	803	S[332]	6090	299.5	863	S[392]	5250	299.5	923	S[452]	4410	299.5
744	S[273]	6916	171.5	804	S[333]	6076	171.5	864	S[393]	5236	171.5	924	S[453]	4396	171.5
745	S[274]	6902	299.5	805	S[334]	6062	299.5	865	S[394]	5222	299.5	925	S[454]	4382	299.5
746	S[275]	6888	171.5	806	S[335]	6048	171.5	866	S[395]	5208	171.5	926	S[455]	4368	171.5
747	S[276]	6874	299.5	807	S[336]	6034	299.5	867	S[396]	5194	299.5	927	S[456]	4354	299.5
748	S[277]	6860	171.5	808	S[337]	6020	171.5	868	S[397]	5180	171.5	928	S[457]	4340	171.5
749	S[278]	6846	299.5	809	S[338]	6006	299.5	869	S[398]	5166	299.5	929	S[458]	4326	299.5
750	S[279]	6832	171.5	810	S[339]	5992	171.5	870	S[399]	5152	171.5	930	S[459]	4312	171.5
751	S[280]	6818	299.5	811	S[340]	5978	299.5	871	S[400]	5138	299.5	931	S[460]	4298	299.5
752	S[281]	6804	171.5	812	S[341]	5964	171.5	872	S[401]	5124	171.5	932	S[461]	4284	171.5
753	S[282]	6790	299.5	813	S[342]	5950	299.5	873	S[402]	5110	299.5	933	S[462]	4270	299.5
754	S[283]	6776	171.5	814	S[343]	5936	171.5	874	S[403]	5096	171.5	934	S[463]	4256	171.5
755	S[284]	6762	299.5	815	S[344]	5922	299.5	875	S[404]	5082	299.5	935	S[464]	4242	299.5
756	S[285]	6748	171.5	816	S[345]	5908	171.5	876	S[405]	5068	171.5	936	S[465]	4228	171.5
757	S[286]	6734	299.5	817	S[346]	5894	299.5	877	S[406]	5054	299.5	937	S[466]	4214	299.5
758	S[287]	6720	171.5	818	S[347]	5880	171.5	878	S[407]	5040	171.5	938	S[467]	4200	171.5
759	S[288]	6706	299.5	819	S[348]	5866	299.5	879	S[408]	5026	299.5	939	S[468]	4186	299.5
760	S[289]	6692	171.5	820	S[349]	5852	171.5	880	S[409]	5012	171.5	940	S[469]	4172	171.5
761	S[290]	6678	299.5	821	S[350]	5838	299.5	881	S[410]	4998	299.5	941	S[470]	4158	299.5
762	S[291]	6664	171.5	822	S[351]	5824	171.5	882	S[411]	4984	171.5	942	S[471]	4144	171.5
763	S[292]	6650	299.5	823	S[352]	5810	299.5	883	S[412]	4970	299.5	943	S[472]	4130	299.5
764	S[293]	6636	171.5	824	S[353]	5796	171.5	884	S[413]	4956	171.5	944	S[473]	4116	171.5
765	S[294]	6622	299.5	825	S[354]	5782	299.5	885	S[414]	4942	299.5	945	S[474]	4102	299.5
766	S[295]	6608	171.5	826	S[355]	5768	171.5	886	S[415]	4928	171.5	946	S[475]	4088	171.5
767	S[296]	6594	299.5	827	S[356]	5754	299.5	887	S[416]	4914	299.5	947	S[476]	4074	299.5
768	S[297]	6580	171.5	828	S[357]	5740	171.5	888	S[417]	4900	171.5	948	S[477]	4060	171.5
769	S[298]	6566	299.5	829	S[358]	5726	299.5	889	S[418]	4886	299.5	949	S[478]	4046	299.5
770	S[299]	6552	171.5	830	S[359]	5712	171.5	890	S[419]	4872	171.5	950	S[479]	4032	171.5
771	S[300]	6538	299.5	831	S[360]	5698	299.5	891	S[420]	4858	299.5	951	S[480]	4018	299.5
772	S[301]	6524	171.5	832	S[361]	5684	171.5	892	S[421]	4844	171.5	952	S[481]	4004	171.5
773	S[302]	6510	299.5	833	S[362]	5670	299.5	893	S[422]	4830	299.5	953	S[482]	3990	299.5
774	S[303]	6496	171.5	834	S[363]	5656	171.5	894	S[423]	4816	171.5	954	S[483]	3976	171.5
775	S[304]	6482	299.5	835	S[364]	5642	299.5	895	S[424]	4802	299.5	955	S[484]	3962	299.5
776	S[305]	6468	171.5	836	S[365]	5628	171.5	896	S[425]	4788	171.5	956	S[485]	3948	171.5
777	S[306]	6454	299.5	837	S[366]	5614	299.5	897	S[426]	4774	299.5	957	S[486]	3934	299.5
778	S[307]	6440	171.5	838	S[367]	5600	171.5	898	S[427]	4760	171.5	958	S[487]	3920	171.5
779	S[308]	6426	299.5	839	S[368]	5586	299.5	899	S[428]	4746	299.5	959	S[488]	3906	299.5
780	S[309]	6412	171.5	840	S[369]	5572	171.5	900	S[429]	4732	171.5	960	S[489]	3892	171.5

No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi
961	S[490]	3878	299.5	1021	S[550]	3038	299.5	1081	S[610]	2198	299.5	1141	S[670]	1358	299.5
962	S[491]	3864	171.5	1022	S[551]	3024	171.5	1082	S[611]	2184	171.5	1142	S[671]	1344	171.5
963	S[492]	3850	299.5	1023	S[552]	3010	299.5	1083	S[612]	2170	299.5	1143	S[672]	1330	299.5
964	S[493]	3836	171.5	1024	S[553]	2996	171.5	1084	S[613]	2156	171.5	1144	S[673]	1316	171.5
965	S[494]	3822	299.5	1025	S[554]	2982	299.5	1085	S[614]	2142	299.5	1145	S[674]	1302	299.5
966	S[495]	3808	171.5	1026	S[555]	2968	171.5	1086	S[615]	2128	171.5	1146	S[675]	1288	171.5
967	S[496]	3794	299.5	1027	S[556]	2954	299.5	1087	S[616]	2114	299.5	1147	S[676]	1274	299.5
968	S[497]	3780	171.5	1028	S[557]	2940	171.5	1088	S[617]	2100	171.5	1148	S[677]	1260	171.5
969	S[498]	3766	299.5	1029	S[558]	2926	299.5	1089	S[618]	2086	299.5	1149	S[678]	1246	299.5
970	S[499]	3752	171.5	1030	S[559]	2912	171.5	1090	S[619]	2072	171.5	1150	S[679]	1232	171.5
971	S[500]	3738	299.5	1031	S[560]	2898	299.5	1091	S[620]	2058	299.5	1151	S[680]	1218	299.5
972	S[501]	3724	171.5	1032	S[561]	2884	171.5	1092	S[621]	2044	171.5	1152	S[681]	1204	171.5
973	S[502]	3710	299.5	1033	S[562]	2870	299.5	1093	S[622]	2030	299.5	1153	S[682]	1190	299.5
974	S[503]	3696	171.5	1034	S[563]	2856	171.5	1094	S[623]	2016	171.5	1154	S[683]	1176	171.5
975	S[504]	3682	299.5	1035	S[564]	2842	299.5	1095	S[624]	2002	299.5	1155	S[684]	1162	299.5
976	S[505]	3668	171.5	1036	S[565]	2828	171.5	1096	S[625]	1988	171.5	1156	S[685]	1148	171.5
977	S[506]	3654	299.5	1037	S[566]	2814	299.5	1097	S[626]	1974	299.5	1157	S[686]	1134	299.5
978	S[507]	3640	171.5	1038	S[567]	2800	171.5	1098	S[627]	1960	171.5	1158	S[687]	1120	171.5
979	S[508]	3626	299.5	1039	S[568]	2786	299.5	1099	S[628]	1946	299.5	1159	S[688]	1106	299.5
980	S[509]	3612	171.5	1040	S[569]	2772	171.5	1100	S[629]	1932	171.5	1160	S[689]	1092	171.5
981	S[510]	3598	299.5	1041	S[570]	2758	299.5	1101	S[630]	1918	299.5	1161	S[690]	1078	299.5
982	S[511]	3584	171.5	1042	S[571]	2744	171.5	1102	S[631]	1904	171.5	1162	S[691]	1064	171.5
983	S[512]	3570	299.5	1043	S[572]	2730	299.5	1103	S[632]	1890	299.5	1163	S[692]	1050	299.5
984	S[513]	3556	171.5	1044	S[573]	2716	171.5	1104	S[633]	1876	171.5	1164	S[693]	1036	171.5
985	S[514]	3542	299.5	1045	S[574]	2702	299.5	1105	S[634]	1862	299.5	1165	S[694]	1022	299.5
986	S[515]	3528	171.5	1046	S[575]	2688	171.5	1106	S[635]	1848	171.5	1166	S[695]	1008	171.5
987	S[516]	3514	299.5	1047	S[576]	2674	299.5	1107	S[636]	1834	299.5	1167	S[696]	994	299.5
988	S[517]	3500	171.5	1048	S[577]	2660	171.5	1108	S[637]	1820	171.5	1168	S[697]	980	171.5
989	S[518]	3486	299.5	1049	S[578]	2646	299.5	1109	S[638]	1806	299.5	1169	S[698]	966	299.5
990	S[519]	3472	171.5	1050	S[579]	2632	171.5	1110	S[639]	1792	171.5	1170	S[699]	952	171.5
991	S[520]	3458	299.5	1051	S[580]	2618	299.5	1111	S[640]	1778	299.5	1171	S[700]	938	299.5
992	S[521]	3444	171.5	1052	S[581]	2604	171.5	1112	S[641]	1764	171.5	1172	S[701]	924	171.5
993	S[522]	3430	299.5	1053	S[582]	2590	299.5	1113	S[642]	1750	299.5	1173	S[702]	910	299.5
994	S[523]	3416	171.5	1054	S[583]	2576	171.5	1114	S[643]	1736	171.5	1174	S[703]	896	171.5
995	S[524]	3402	299.5	1055	S[584]	2562	299.5	1115	S[644]	1722	299.5	1175	S[704]	882	299.5
996	S[525]	3388	171.5	1056	S[585]	2548	171.5	1116	S[645]	1708	171.5	1176	S[705]	868	171.5
997	S[526]	3374	299.5	1057	S[586]	2534	299.5	1117	S[646]	1694	299.5	1177	S[706]	854	299.5
998	S[527]	3360	171.5	1058	S[587]	2520	171.5	1118	S[647]	1680	171.5	1178	S[707]	840	171.5
999	S[528]	3346	299.5	1059	S[588]	2506	299.5	1119	S[648]	1666	299.5	1179	S[708]	826	299.5
1000	S[529]	3332	171.5	1060	S[589]	2492	171.5	1120	S[649]	1652	171.5	1180	S[709]	812	171.5
1001	S[530]	3318	299.5	1061	S[590]	2478	299.5	1121	S[650]	1638	299.5	1181	S[710]	798	299.5
1002	S[531]	3304	171.5	1062	S[591]	2464	171.5	1122	S[651]	1624	171.5	1182	S[711]	784	171.5
1003	S[532]	3290	299.5	1063	S[592]	2450	299.5	1123	S[652]	1610	299.5	1183	S[712]	770	299.5
1004	S[533]	3276	171.5	1064	S[593]	2436	171.5	1124	S[653]	1596	171.5	1184	S[713]	756	171.5
1005	S[534]	3262	299.5	1065	S[594]	2422	299.5	1125	S[654]	1582	299.5	1185	S[714]	742	299.5
1006	S[535]	3248	171.5	1066	S[595]	2408	171.5	1126	S[655]	1568	171.5	1186	S[715]	728	171.5
1007	S[536]	3234	299.5	1067	S[596]	2394	299.5	1127	S[656]	1554	299.5	1187	S[716]	714	299.5
1008	S[537]	3220	171.5	1068	S[597]	2380	171.5	1128	S[657]	1540	171.5	1188	S[717]	700	171.5
1009	S[538]	3206	299.5	1069	S[598]	2366	299.5	1129	S[658]	1526	299.5	1189	S[718]	686	299.5
1010	S[539]	3192	171.5	1070	S[599]	2352	171.5	1130	S[659]	1512	171.5	1190	S[719]	672	171.5
1011	S[540]	3178	299.5	1071	S[600]	2338	299.5	1131	S[660]	1498	299.5	1191	S[720]	658	299.5
1012	S[541]	3164	171.5	1072	S[601]	2324	171.5	1132	S[661]	1484	171.5	1192	AVSS	644	171.5
1013	S[542]	3150	299.5	1073	S[602]	2310	299.5	1133	S[662]	1470	299.5	1193	AVSS	630	299.5
1014	S[543]	3136	171.5	1074	S[603]	2296	171.5	1134	S[663]	1456	171.5	1194	AVSS	616	171.5
1015	S[544]	3122	299.5	1075	S[604]	2282	299.5	1135	S[664]	1442	299.5	1195	AVSS	602	299.5
1016	S[545]	3108	171.5	1076	S[605]	2268	171.5	1136	S[665]	1428	171.5	1196	AVSS	588	171.5
1017	S[546]	3094	299.5	1077	S[606]	2254	299.5	1137	S[666]	1414	299.5	1197	AVSS	574	299.5
1018	S[547]	3080	171.5	1078	S[607]	2240	171.5	1138	S[667]	1400	171.5	1198	AVSS	560	171.5
1019	S[548]	3066	299.5	1079	S[608]	2226	299.5	1139	S[668]	1386	299.5	1199	AVSS	546	299.5
1020	S[549]	3052	171.5	1080	S[609]	2212	171.5	1140	S[669]	1372	171.5	1200	AVSS	532	171.5

No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi
1201	AVSS	518	299.5	1261	S[741]	-322	299.5	1321	S[801]	-1162	299.5	1381	S[861]	-2002	299.5
1202	AVSS	504	171.5	1262	S[742]	-336	171.5	1322	S[802]	-1176	171.5	1382	S[862]	-2016	171.5
1203	AVSS	490	299.5	1263	S[743]	-350	299.5	1323	S[803]	-1190	299.5	1383	S[863]	-2030	299.5
1204	AVSS	476	171.5	1264	S[744]	-364	171.5	1324	S[804]	-1204	171.5	1384	S[864]	-2044	171.5
1205	AVSS	462	299.5	1265	S[745]	-378	299.5	1325	S[805]	-1218	299.5	1385	S[865]	-2058	299.5
1206	AVSS	448	171.5	1266	S[746]	-392	171.5	1326	S[806]	-1232	171.5	1386	S[866]	-2072	171.5
1207	AVSS	434	299.5	1267	S[747]	-406	299.5	1327	S[807]	-1246	299.5	1387	S[867]	-2086	299.5
1208	AVSS	420	171.5	1268	S[748]	-420	171.5	1328	S[808]	-1260	171.5	1388	S[868]	-2100	171.5
1209	AVSS	406	299.5	1269	S[749]	-434	299.5	1329	S[809]	-1274	299.5	1389	S[869]	-2114	299.5
1210	AVSS	392	171.5	1270	S[750]	-448	171.5	1330	S[810]	-1288	171.5	1390	S[870]	-2128	171.5
1211	AVSS	378	299.5	1271	S[751]	-462	299.5	1331	S[811]	-1302	299.5	1391	S[871]	-2142	299.5
1212	AVSS	364	171.5	1272	S[752]	-476	171.5	1332	S[812]	-1316	171.5	1392	S[872]	-2156	171.5
1213	AVSS	350	299.5	1273	S[753]	-490	299.5	1333	S[813]	-1330	299.5	1393	S[873]	-2170	299.5
1214	AVSS	336	171.5	1274	S[754]	-504	171.5	1334	S[814]	-1344	171.5	1394	S[874]	-2184	171.5
1215	AVSS	322	299.5	1275	S[755]	-518	299.5	1335	S[815]	-1358	299.5	1395	S[875]	-2198	299.5
1216	AVSS	308	171.5	1276	S[756]	-532	171.5	1336	S[816]	-1372	171.5	1396	S[876]	-2212	171.5
1217	AVSS	294	299.5	1277	S[757]	-546	299.5	1337	S[817]	-1386	299.5	1397	S[877]	-2226	299.5
1218	AVSS	280	171.5	1278	S[758]	-560	171.5	1338	S[818]	-1400	171.5	1398	S[878]	-2240	171.5
1219	AVSS	266	299.5	1279	S[759]	-574	299.5	1339	S[819]	-1414	299.5	1399	S[879]	-2254	299.5
1220	AVSS	252	171.5	1280	S[760]	-588	171.5	1340	S[820]	-1428	171.5	1400	S[880]	-2268	171.5
1221	AVSS	238	299.5	1281	S[761]	-602	299.5	1341	S[821]	-1442	299.5	1401	S[881]	-2282	299.5
1222	AVSS	224	171.5	1282	S[762]	-616	171.5	1342	S[822]	-1456	171.5	1402	S[882]	-2296	171.5
1223	AVSS	210	299.5	1283	S[763]	-630	299.5	1343	S[823]	-1470	299.5	1403	S[883]	-2310	299.5
1224	AVSS	196	171.5	1284	S[764]	-644	171.5	1344	S[824]	-1484	171.5	1404	S[884]	-2324	171.5
1225	AVSS	182	299.5	1285	S[765]	-658	299.5	1345	S[825]	-1498	299.5	1405	S[885]	-2338	299.5
1226	AVSS	168	171.5	1286	S[766]	-672	171.5	1346	S[826]	-1512	171.5	1406	S[886]	-2352	171.5
1227	AVSS	154	299.5	1287	S[767]	-686	299.5	1347	S[827]	-1526	299.5	1407	S[887]	-2366	299.5
1228	AVSS	140	171.5	1288	S[768]	-700	171.5	1348	S[828]	-1540	171.5	1408	S[888]	-2380	171.5
1229	AVSS	126	299.5	1289	S[769]	-714	299.5	1349	S[829]	-1554	299.5	1409	S[889]	-2394	299.5
1230	AVSS	112	171.5	1290	S[770]	-728	171.5	1350	S[830]	-1568	171.5	1410	S[890]	-2408	171.5
1231	AVSS	98	299.5	1291	S[771]	-742	299.5	1351	S[831]	-1582	299.5	1411	S[891]	-2422	299.5
1232	AVSS	84	171.5	1292	S[772]	-756	171.5	1352	S[832]	-1596	171.5	1412	S[892]	-2436	171.5
1233	AVSS	70	299.5	1293	S[773]	-770	299.5	1353	S[833]	-1610	299.5	1413	S[893]	-2450	299.5
1234	AVSS	56	171.5	1294	S[774]	-784	171.5	1354	S[834]	-1624	171.5	1414	S[894]	-2464	171.5
1235	AVSS	42	299.5	1295	S[775]	-798	299.5	1355	S[835]	-1638	299.5	1415	S[895]	-2478	299.5
1236	AVSS	28	171.5	1296	S[776]	-812	171.5	1356	S[836]	-1652	171.5	1416	S[896]	-2492	171.5
1237	AVSS	14	299.5	1297	S[777]	-826	299.5	1357	S[837]	-1666	299.5	1417	S[897]	-2506	299.5
1238	AVSS	0	171.5	1298	S[778]	-840	171.5	1358	S[838]	-1680	171.5	1418	S[898]	-2520	171.5
1239	AVSS	-14	299.5	1299	S[779]	-854	299.5	1359	S[839]	-1694	299.5	1419	S[899]	-2534	299.5
1240	AVSS	-28	171.5	1300	S[780]	-868	171.5	1360	S[840]	-1708	171.5	1420	S[900]	-2548	171.5
1241	S[721]	-42	299.5	1301	S[781]	-882	299.5	1361	S[841]	-1722	299.5	1421	S[901]	-2562	299.5
1242	S[722]	-56	171.5	1302	S[782]	-896	171.5	1362	S[842]	-1736	171.5	1422	S[902]	-2576	171.5
1243	S[723]	-70	299.5	1303	S[783]	-910	299.5	1363	S[843]	-1750	299.5	1423	S[903]	-2590	299.5
1244	S[724]	-84	171.5	1304	S[784]	-924	171.5	1364	S[844]	-1764	171.5	1424	S[904]	-2604	171.5
1245	S[725]	-98	299.5	1305	S[785]	-938	299.5	1365	S[845]	-1778	299.5	1425	S[905]	-2618	299.5
1246	S[726]	-112	171.5	1306	S[786]	-952	171.5	1366	S[846]	-1792	171.5	1426	S[906]	-2632	171.5
1247	S[727]	-126	299.5	1307	S[787]	-966	299.5	1367	S[847]	-1806	299.5	1427	S[907]	-2646	299.5
1248	S[728]	-140	171.5	1308	S[788]	-980	171.5	1368	S[848]	-1820	171.5	1428	S[908]	-2660	171.5
1249	S[729]	-154	299.5	1309	S[789]	-994	299.5	1369	S[849]	-1834	299.5	1429	S[909]	-2674	299.5
1250	S[730]	-168	171.5	1310	S[790]	-1008	171.5	1370	S[850]	-1848	171.5	1430	S[910]	-2688	171.5
1251	S[731]	-182	299.5	1311	S[791]	-1022	299.5	1371	S[851]	-1862	299.5	1431	S[911]	-2702	299.5
1252	S[732]	-196	171.5	1312	S[792]	-1036	171.5	1372	S[852]	-1876	171.5	1432	S[912]	-2716	171.5
1253	S[733]	-210	299.5	1313	S[793]	-1050	299.5	1373	S[853]	-1890	299.5	1433	S[913]	-2730	299.5
1254	S[734]	-224	171.5	1314	S[794]	-1064	171.5	1374	S[854]	-1904	171.5	1434	S[914]	-2744	171.5
1255	S[735]	-238	299.5	1315	S[795]	-1078	299.5	1375	S[855]	-1918	299.5	1435	S[915]	-2758	299.5
1256	S[736]	-252	171.5	1316	S[796]	-1092	171.5	1376	S[856]	-1932	171.5	1436	S[916]	-2772	171.5
1257	S[737]	-266	299.5	1317	S[797]	-1106	299.5	1377	S[857]	-1946	299.5	1437	S[917]	-2786	299.5
1258	S[738]	-280	171.5	1318	S[798]	-1120	171.5	1378	S[858]	-1960	171.5	1438	S[918]	-2800	171.5
1259	S[739]	-294	299.5	1319	S[799]	-1134	299.5	1379	S[859]	-1974	299.5	1439	S[919]	-2814	299.5
1260	S[740]	-308	171.5	1320	S[800]	-1148	171.5	1380	S[860]	-1988	171.5	1440	S[920]	-2828	171.5

No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi
1441	S[921]	-2842	299.5	1501	S[981]	-3682	299.5	1561	S[1041]	-4522	299.5	1621	S[1101]	-5362	299.5
1442	S[922]	-2856	171.5	1502	S[982]	-3696	171.5	1562	S[1042]	-4536	171.5	1622	S[1102]	-5376	171.5
1443	S[923]	-2870	299.5	1503	S[983]	-3710	299.5	1563	S[1043]	-4550	299.5	1623	S[1103]	-5390	299.5
1444	S[924]	-2884	171.5	1504	S[984]	-3724	171.5	1564	S[1044]	-4564	171.5	1624	S[1104]	-5404	171.5
1445	S[925]	-2898	299.5	1505	S[985]	-3738	299.5	1565	S[1045]	-4578	299.5	1625	S[1105]	-5418	299.5
1446	S[926]	-2912	171.5	1506	S[986]	-3752	171.5	1566	S[1046]	-4592	171.5	1626	S[1106]	-5432	171.5
1447	S[927]	-2926	299.5	1507	S[987]	-3766	299.5	1567	S[1047]	-4606	299.5	1627	S[1107]	-5446	299.5
1448	S[928]	-2940	171.5	1508	S[988]	-3780	171.5	1568	S[1048]	-4620	171.5	1628	S[1108]	-5460	171.5
1449	S[929]	-2954	299.5	1509	S[989]	-3794	299.5	1569	S[1049]	-4634	299.5	1629	S[1109]	-5474	299.5
1450	S[930]	-2968	171.5	1510	S[990]	-3808	171.5	1570	S[1050]	-4648	171.5	1630	S[1110]	-5488	171.5
1451	S[931]	-2982	299.5	1511	S[991]	-3822	299.5	1571	S[1051]	-4662	299.5	1631	S[1111]	-5502	299.5
1452	S[932]	-2996	171.5	1512	S[992]	-3836	171.5	1572	S[1052]	-4676	171.5	1632	S[1112]	-5516	171.5
1453	S[933]	-3010	299.5	1513	S[993]	-3850	299.5	1573	S[1053]	-4690	299.5	1633	S[1113]	-5530	299.5
1454	S[934]	-3024	171.5	1514	S[994]	-3864	171.5	1574	S[1054]	-4704	171.5	1634	S[1114]	-5544	171.5
1455	S[935]	-3038	299.5	1515	S[995]	-3878	299.5	1575	S[1055]	-4718	299.5	1635	S[1115]	-5558	299.5
1456	S[936]	-3052	171.5	1516	S[996]	-3892	171.5	1576	S[1056]	-4732	171.5	1636	S[1116]	-5572	171.5
1457	S[937]	-3066	299.5	1517	S[997]	-3906	299.5	1577	S[1057]	-4746	299.5	1637	S[1117]	-5586	299.5
1458	S[938]	-3080	171.5	1518	S[998]	-3920	171.5	1578	S[1058]	-4760	171.5	1638	S[1118]	-5600	171.5
1459	S[939]	-3094	299.5	1519	S[999]	-3934	299.5	1579	S[1059]	-4774	299.5	1639	S[1119]	-5614	299.5
1460	S[940]	-3108	171.5	1520	S[1000]	-3948	171.5	1580	S[1060]	-4788	171.5	1640	S[1120]	-5628	171.5
1461	S[941]	-3122	299.5	1521	S[1001]	-3962	299.5	1581	S[1061]	-4802	299.5	1641	S[1121]	-5642	299.5
1462	S[942]	-3136	171.5	1522	S[1002]	-3976	171.5	1582	S[1062]	-4816	171.5	1642	S[1122]	-5656	171.5
1463	S[943]	-3150	299.5	1523	S[1003]	-3990	299.5	1583	S[1063]	-4830	299.5	1643	S[1123]	-5670	299.5
1464	S[944]	-3164	171.5	1524	S[1004]	-4004	171.5	1584	S[1064]	-4844	171.5	1644	S[1124]	-5684	171.5
1465	S[945]	-3178	299.5	1525	S[1005]	-4018	299.5	1585	S[1065]	-4858	299.5	1645	S[1125]	-5698	299.5
1466	S[946]	-3192	171.5	1526	S[1006]	-4032	171.5	1586	S[1066]	-4872	171.5	1646	S[1126]	-5712	171.5
1467	S[947]	-3206	299.5	1527	S[1007]	-4046	299.5	1587	S[1067]	-4886	299.5	1647	S[1127]	-5726	299.5
1468	S[948]	-3220	171.5	1528	S[1008]	-4060	171.5	1588	S[1068]	-4900	171.5	1648	S[1128]	-5740	171.5
1469	S[949]	-3234	299.5	1529	S[1009]	-4074	299.5	1589	S[1069]	-4914	299.5	1649	S[1129]	-5754	299.5
1470	S[950]	-3248	171.5	1530	S[1010]	-4088	171.5	1590	S[1070]	-4928	171.5	1650	S[1130]	-5768	171.5
1471	S[951]	-3262	299.5	1531	S[1011]	-4102	299.5	1591	S[1071]	-4942	299.5	1651	S[1131]	-5782	299.5
1472	S[952]	-3276	171.5	1532	S[1012]	-4116	171.5	1592	S[1072]	-4956	171.5	1652	S[1132]	-5796	171.5
1473	S[953]	-3290	299.5	1533	S[1013]	-4130	299.5	1593	S[1073]	-4970	299.5	1653	S[1133]	-5810	299.5
1474	S[954]	-3304	171.5	1534	S[1014]	-4144	171.5	1594	S[1074]	-4984	171.5	1654	S[1134]	-5824	171.5
1475	S[955]	-3318	299.5	1535	S[1015]	-4158	299.5	1595	S[1075]	-4998	299.5	1655	S[1135]	-5838	299.5
1476	S[956]	-3332	171.5	1536	S[1016]	-4172	171.5	1596	S[1076]	-5012	171.5	1656	S[1136]	-5852	171.5
1477	S[957]	-3346	299.5	1537	S[1017]	-4186	299.5	1597	S[1077]	-5026	299.5	1657	S[1137]	-5866	299.5
1478	S[958]	-3360	171.5	1538	S[1018]	-4200	171.5	1598	S[1078]	-5040	171.5	1658	S[1138]	-5880	171.5
1479	S[959]	-3374	299.5	1539	S[1019]	-4214	299.5	1599	S[1079]	-5054	299.5	1659	S[1139]	-5894	299.5
1480	S[960]	-3388	171.5	1540	S[1020]	-4228	171.5	1600	S[1080]	-5068	171.5	1660	S[1140]	-5908	171.5
1481	S[961]	-3402	299.5	1541	S[1021]	-4242	299.5	1601	S[1081]	-5082	299.5	1661	S[1141]	-5922	299.5
1482	S[962]	-3416	171.5	1542	S[1022]	-4256	171.5	1602	S[1082]	-5096	171.5	1662	S[1142]	-5936	171.5
1483	S[963]	-3430	299.5	1543	S[1023]	-4270	299.5	1603	S[1083]	-5110	299.5	1663	S[1143]	-5950	299.5
1484	S[964]	-3444	171.5	1544	S[1024]	-4284	171.5	1604	S[1084]	-5124	171.5	1664	S[1144]	-5964	171.5
1485	S[965]	-3458	299.5	1545	S[1025]	-4298	299.5	1605	S[1085]	-5138	299.5	1665	S[1145]	-5978	299.5
1486	S[966]	-3472	171.5	1546	S[1026]	-4312	171.5	1606	S[1086]	-5152	171.5	1666	S[1146]	-5992	171.5
1487	S[967]	-3486	299.5	1547	S[1027]	-4326	299.5	1607	S[1087]	-5166	299.5	1667	S[1147]	-6006	299.5
1488	S[968]	-3500	171.5	1548	S[1028]	-4340	171.5	1608	S[1088]	-5180	171.5	1668	S[1148]	-6020	171.5
1489	S[969]	-3514	299.5	1549	S[1029]	-4354	299.5	1609	S[1089]	-5194	299.5	1669	S[1149]	-6034	299.5
1490	S[970]	-3528	171.5	1550	S[1030]	-4368	171.5	1610	S[1090]	-5208	171.5	1670	S[1150]	-6048	171.5
1491	S[971]	-3542	299.5	1551	S[1031]	-4382	299.5	1611	S[1091]	-5222	299.5	1671	S[1151]	-6062	299.5
1492	S[972]	-3556	171.5	1552	S[1032]	-4396	171.5	1612	S[1092]	-5236	171.5	1672	S[1152]	-6076	171.5
1493	S[973]	-3570	299.5	1553	S[1033]	-4410	299.5	1613	S[1093]	-5250	299.5	1673	S[1153]	-6090	299.5
1494	S[974]	-3584	171.5	1554	S[1034]	-4424	171.5	1614	S[1094]	-5264	171.5	1674	S[1154]	-6104	171.5
1495	S[975]	-3598	299.5	1555	S[1035]	-4438	299.5	1615	S[1095]	-5278	299.5	1675	S[1155]	-6118	299.5
1496	S[976]	-3612	171.5	1556	S[1036]	-4452	171.5	1616	S[1096]	-5292	171.5	1676	S[1156]	-6132	171.5
1497	S[977]	-3626	299.5	1557	S[1037]	-4466	299.5	1617	S[1097]	-5306	299.5	1677	S[1157]	-6146	299.5
1498	S[978]	-3640	171.5	1558	S[1038]	-4480	171.5	1618	S[1098]	-5320	171.5	1678	S[1158]	-6160	171.5
1499	S[979]	-3654	299.5	1559	S[1039]	-4494	299.5	1619	S[1099]	-5334	299.5	1679	S[1159]	-6174	299.5
1500	S[980]	-3668	171.5	1560	S[1040]	-4508	171.5	1620	S[1100]	-5348	171.5	1680	S[1160]	-6188	171.5

No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi
1681	S[1161]	-6202	299.5	1741	S[1221]	-7042	299.5	1801	S[1281]	-7882	299.5	1861	S[1341]	-8722	299.5
1682	S[1162]	-6216	171.5	1742	S[1222]	-7056	171.5	1802	S[1282]	-7896	171.5	1862	S[1342]	-8736	171.5
1683	S[1163]	-6230	299.5	1743	S[1223]	-7070	299.5	1803	S[1283]	-7910	299.5	1863	S[1343]	-8750	299.5
1684	S[1164]	-6244	171.5	1744	S[1224]	-7084	171.5	1804	S[1284]	-7924	171.5	1864	S[1344]	-8764	171.5
1685	S[1165]	-6258	299.5	1745	S[1225]	-7098	299.5	1805	S[1285]	-7938	299.5	1865	S[1345]	-8778	299.5
1686	S[1166]	-6272	171.5	1746	S[1226]	-7112	171.5	1806	S[1286]	-7952	171.5	1866	S[1346]	-8792	171.5
1687	S[1167]	-6286	299.5	1747	S[1227]	-7126	299.5	1807	S[1287]	-7966	299.5	1867	S[1347]	-8806	299.5
1688	S[1168]	-6300	171.5	1748	S[1228]	-7140	171.5	1808	S[1288]	-7980	171.5	1868	S[1348]	-8820	171.5
1689	S[1169]	-6314	299.5	1749	S[1229]	-7154	299.5	1809	S[1289]	-7994	299.5	1869	S[1349]	-8834	299.5
1690	S[1170]	-6328	171.5	1750	S[1230]	-7168	171.5	1810	S[1290]	-8008	171.5	1870	S[1350]	-8848	171.5
1691	S[1171]	-6342	299.5	1751	S[1231]	-7182	299.5	1811	S[1291]	-8022	299.5	1871	S[1351]	-8862	299.5
1692	S[1172]	-6356	171.5	1752	S[1232]	-7196	171.5	1812	S[1292]	-8036	171.5	1872	S[1352]	-8876	171.5
1693	S[1173]	-6370	299.5	1753	S[1233]	-7210	299.5	1813	S[1293]	-8050	299.5	1873	S[1353]	-8890	299.5
1694	S[1174]	-6384	171.5	1754	S[1234]	-7224	171.5	1814	S[1294]	-8064	171.5	1874	S[1354]	-8904	171.5
1695	S[1175]	-6398	299.5	1755	S[1235]	-7238	299.5	1815	S[1295]	-8078	299.5	1875	S[1355]	-8918	299.5
1696	S[1176]	-6412	171.5	1756	S[1236]	-7252	171.5	1816	S[1296]	-8092	171.5	1876	S[1356]	-8932	171.5
1697	S[1177]	-6426	299.5	1757	S[1237]	-7266	299.5	1817	S[1297]	-8106	299.5	1877	S[1357]	-8946	299.5
1698	S[1178]	-6440	171.5	1758	S[1238]	-7280	171.5	1818	S[1298]	-8120	171.5	1878	S[1358]	-8960	171.5
1699	S[1179]	-6454	299.5	1759	S[1239]	-7294	299.5	1819	S[1299]	-8134	299.5	1879	S[1359]	-8974	299.5
1700	S[1180]	-6468	171.5	1760	S[1240]	-7308	171.5	1820	S[1300]	-8148	171.5	1880	S[1360]	-8988	171.5
1701	S[1181]	-6482	299.5	1761	S[1241]	-7322	299.5	1821	S[1301]	-8162	299.5	1881	S[1361]	-9002	299.5
1702	S[1182]	-6496	171.5	1762	S[1242]	-7336	171.5	1822	S[1302]	-8176	171.5	1882	S[1362]	-9016	171.5
1703	S[1183]	-6510	299.5	1763	S[1243]	-7350	299.5	1823	S[1303]	-8190	299.5	1883	S[1363]	-9030	299.5
1704	S[1184]	-6524	171.5	1764	S[1244]	-7364	171.5	1824	S[1304]	-8204	171.5	1884	S[1364]	-9044	171.5
1705	S[1185]	-6538	299.5	1765	S[1245]	-7378	299.5	1825	S[1305]	-8218	299.5	1885	S[1365]	-9058	299.5
1706	S[1186]	-6552	171.5	1766	S[1246]	-7392	171.5	1826	S[1306]	-8232	171.5	1886	S[1366]	-9072	171.5
1707	S[1187]	-6566	299.5	1767	S[1247]	-7406	299.5	1827	S[1307]	-8246	299.5	1887	S[1367]	-9086	299.5
1708	S[1188]	-6580	171.5	1768	S[1248]	-7420	171.5	1828	S[1308]	-8260	171.5	1888	S[1368]	-9100	171.5
1709	S[1189]	-6594	299.5	1769	S[1249]	-7434	299.5	1829	S[1309]	-8274	299.5	1889	S[1369]	-9114	299.5
1710	S[1190]	-6608	171.5	1770	S[1250]	-7448	171.5	1830	S[1310]	-8288	171.5	1890	S[1370]	-9128	171.5
1711	S[1191]	-6622	299.5	1771	S[1251]	-7462	299.5	1831	S[1311]	-8302	299.5	1891	S[1371]	-9142	299.5
1712	S[1192]	-6636	171.5	1772	S[1252]	-7476	171.5	1832	S[1312]	-8316	171.5	1892	S[1372]	-9156	171.5
1713	S[1193]	-6650	299.5	1773	S[1253]	-7490	299.5	1833	S[1313]	-8330	299.5	1893	S[1373]	-9170	299.5
1714	S[1194]	-6664	171.5	1774	S[1254]	-7504	171.5	1834	S[1314]	-8344	171.5	1894	S[1374]	-9184	171.5
1715	S[1195]	-6678	299.5	1775	S[1255]	-7518	299.5	1835	S[1315]	-8358	299.5	1895	S[1375]	-9198	299.5
1716	S[1196]	-6692	171.5	1776	S[1256]	-7532	171.5	1836	S[1316]	-8372	171.5	1896	S[1376]	-9212	171.5
1717	S[1197]	-6706	299.5	1777	S[1257]	-7546	299.5	1837	S[1317]	-8386	299.5	1897	S[1377]	-9226	299.5
1718	S[1198]	-6720	171.5	1778	S[1258]	-7560	171.5	1838	S[1318]	-8400	171.5	1898	S[1378]	-9240	171.5
1719	S[1199]	-6734	299.5	1779	S[1259]	-7574	299.5	1839	S[1319]	-8414	299.5	1899	S[1379]	-9254	299.5
1720	S[1200]	-6748	171.5	1780	S[1260]	-7588	171.5	1840	S[1320]	-8428	171.5	1900	S[1380]	-9268	171.5
1721	S[1201]	-6762	299.5	1781	S[1261]	-7602	299.5	1841	S[1321]	-8442	299.5	1901	S[1381]	-9282	299.5
1722	S[1202]	-6776	171.5	1782	S[1262]	-7616	171.5	1842	S[1322]	-8456	171.5	1902	S[1382]	-9296	171.5
1723	S[1203]	-6790	299.5	1783	S[1263]	-7630	299.5	1843	S[1323]	-8470	299.5	1903	S[1383]	-9310	299.5
1724	S[1204]	-6804	171.5	1784	S[1264]	-7644	171.5	1844	S[1324]	-8484	171.5	1904	S[1384]	-9324	171.5
1725	S[1205]	-6818	299.5	1785	S[1265]	-7658	299.5	1845	S[1325]	-8498	299.5	1905	S[1385]	-9338	299.5
1726	S[1206]	-6832	171.5	1786	S[1266]	-7672	171.5	1846	S[1326]	-8512	171.5	1906	S[1386]	-9352	171.5
1727	S[1207]	-6846	299.5	1787	S[1267]	-7686	299.5	1847	S[1327]	-8526	299.5	1907	S[1387]	-9366	299.5
1728	S[1208]	-6860	171.5	1788	S[1268]	-7700	171.5	1848	S[1328]	-8540	171.5	1908	S[1388]	-9380	171.5
1729	S[1209]	-6874	299.5	1789	S[1269]	-7714	299.5	1849	S[1329]	-8554	299.5	1909	S[1389]	-9394	299.5
1730	S[1210]	-6888	171.5	1790	S[1270]	-7728	171.5	1850	S[1330]	-8568	171.5	1910	S[1390]	-9408	171.5
1731	S[1211]	-6902	299.5	1791	S[1271]	-7742	299.5	1851	S[1331]	-8582	299.5	1911	S[1391]	-9422	299.5
1732	S[1212]	-6916	171.5	1792	S[1272]	-7756	171.5	1852	S[1332]	-8596	171.5	1912	S[1392]	-9436	171.5
1733	S[1213]	-6930	299.5	1793	S[1273]	-7770	299.5	1853	S[1333]	-8610	299.5	1913	S[1393]	-9450	299.5
1734	S[1214]	-6944	171.5	1794	S[1274]	-7784	171.5	1854	S[1334]	-8624	171.5	1914	S[1394]	-9464	171.5
1735	S[1215]	-6958	299.5	1795	S[1275]	-7798	299.5	1855	S[1335]	-8638	299.5	1915	S[1395]	-9478	299.5
1736	S[1216]	-6972	171.5	1796	S[1276]	-7812	171.5	1856	S[1336]	-8652	171.5	1916	S[1396]	-9492	171.5
1737	S[1217]	-6986	299.5	1797	S[1277]	-7826	299.5	1857	S[1337]	-8666	299.5	1917	S[1397]	-9506	299.5
1738	S[1218]	-7000	171.5	1798	S[1278]	-7840	171.5	1858	S[1338]	-8680	171.5	1918	S[1398]	-9520	171.5
1739	S[1219]	-7014	299.5	1799	S[1279]	-7854	299.5	1859	S[1339]	-8694	299.5	1919	S[1399]	-9534	299.5
1740	S[1220]	-7028	171.5	1800	S[1280]	-7868	171.5	1860	S[1340]	-8708	171.5	1920	S[1400]	-9548	171.5

No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi	No.	Pad Name	X-axis	Y-axi
1921	S[1401]	-9562	299.5	1981	VGH	-10402	299.5	2041	GCK[9]_L	-11242	299.5
1922	S[1402]	-9576	171.5	1982	AVSS	-10416	171.5	2042	GCK[8]_L	-11256	171.5
1923	S[1403]	-9590	299.5	1983	AVSS	-10430	299.5	2043	GCK[8]_L	-11270	299.5
1924	S[1404]	-9604	171.5	1984	AVSS	-10444	171.5	2044	GCK[7]_L	-11284	171.5
1925	S[1405]	-9618	299.5	1985	AVSS	-10458	299.5	2045	GCK[7]_L	-11298	299.5
1926	S[1406]	-9632	171.5	1986	AVSS	-10472	171.5	2046	GCK[6]_L	-11312	171.5
1927	S[1407]	-9646	299.5	1987	AVSS	-10486	299.5	2047	GCK[6]_L	-11326	299.5
1928	S[1408]	-9660	171.5	1988	AVSS	-10500	171.5	2048	GCK[5]_L	-11340	171.5
1929	S[1409]	-9674	299.5	1989	AVSS	-10514	299.5	2049	GCK[5]_L	-11354	299.5
1930	S[1410]	-9688	171.5	1990	AVSS	-10528	171.5	2050	GCK[4]_L	-11368	171.5
1931	S[1411]	-9702	299.5	1991	AVSS	-10542	299.5	2051	GCK[4]_L	-11382	299.5
1932	S[1412]	-9716	171.5	1992	AVSS	-10556	171.5	2052	GCK[3]_L	-11396	171.5
1933	S[1413]	-9730	299.5	1993	AVSS	-10570	299.5	2053	GCK[3]_L	-11410	299.5
1934	S[1414]	-9744	171.5	1994	AVSS	-10584	171.5	2054	VGL	-11424	171.5
1935	S[1415]	-9758	299.5	1995	AVSS	-10598	299.5	2055	VGL	-11438	299.5
1936	S[1416]	-9772	171.5	1996	AVSS	-10612	171.5	2056	VGL	-11452	171.5
1937	S[1417]	-9786	299.5	1997	AVSS	-10626	299.5	2057	DUMMY	-11466	299.5
1938	S[1418]	-9800	171.5	1998	AVSS	-10640	171.5	2058	DUMMY	-11480	171.5
1939	S[1419]	-9814	299.5	1999	AVSS	-10654	299.5	2059	DUMMY	-11494	299.5
1940	S[1420]	-9828	171.5	2000	AVSS	-10668	171.5	2060	VGL	-11508	171.5
1941	S[1421]	-9842	299.5	2001	AVSS	-10682	299.5	2061	VGL	-11522	299.5
1942	S[1422]	-9856	171.5	2002	AVSS	-10696	171.5	2062	VGL	-11536	171.5
1943	S[1423]	-9870	299.5	2003	AVSS	-10710	299.5	2063	GCK[2]_L	-11550	299.5
1944	S[1424]	-9884	171.5	2004	AVSS	-10724	171.5	2064	GCK[2]_L	-11564	171.5
1945	S[1425]	-9898	299.5	2005	AVSS	-10738	299.5	2065	GCK[1]_L	-11578	299.5
1946	S[1426]	-9912	171.5	2006	AVSS	-10752	171.5	2066	GCK[1]_L	-11592	171.5
1947	S[1427]	-9926	299.5	2007	AVSS	-10766	299.5	2067	VGL	-11606	299.5
1948	S[1428]	-9940	171.5	2008	AVSS	-10780	171.5	2068	VGL	-11620	171.5
1949	S[1429]	-9954	299.5	2009	AVSS	-10794	299.5	2069	VGL	-11634	299.5
1950	S[1430]	-9968	171.5	2010	AVSS	-10808	171.5	2070	VGH	-11648	171.5
1951	S[1431]	-9982	299.5	2011	AVSS	-10822	299.5	2071	VGH	-11662	299.5
1952	S[1432]	-9996	171.5	2012	AVSS	-10836	171.5	2072	VGH	-11676	171.5
1953	S[1433]	-10010	299.5	2013	AVSS	-10850	299.5	2073	COGTESTF[1]	-11690	299.5
1954	S[1434]	-10024	171.5	2014	AVSS	-10864	171.5	2074	COGTESTF[2]	-11704	171.5
1955	S[1435]	-10038	299.5	2015	AVSS	-10878	299.5	2075	AVSS	-11718	299.5
1956	S[1436]	-10052	171.5	2016	AVSS	-10892	171.5	2076	AVSS	-11732	171.5
1957	S[1437]	-10066	299.5	2017	AVSS	-10906	299.5	2077	AVSS	-11760	299.5
1958	S[1438]	-10080	171.5	2018	AVSS	-10920	171.5				
1959	S[1439]	-10094	299.5	2019	AVSS	-10934	299.5				
1960	S[1440]	-10108	171.5	2020	AVSS	-10948	171.5				
1961	NC	-10122	299.5	2021	AVSS	-10962	299.5				
1962	NC	-10136	171.5	2022	AVSS	-10976	171.5				
1963	AVSS	-10150	299.5	2023	AVSS	-10990	299.5				
1964	AVSS	-10164	171.5	2024	AVSS	-11004	171.5				
1965	VGL	-10178	299.5	2025	AVSS	-11018	299.5				
1966	VGL	-10192	171.5	2026	GCK[16]_L	-11032	171.5				
1967	VGL	-10206	299.5	2027	GCK[16]_L	-11046	299.5				
1968	VGL	-10220	171.5	2028	GCK[15]_L	-11060	171.5				
1969	VGL	-10234	299.5	2029	GCK[15]_L	-11074	299.5				
1970	VGL	-10248	171.5	2030	GCK[14]_L	-11088	171.5				
1971	VGL	-10262	299.5	2031	GCK[14]_L	-11102	299.5				
1972	VGL	-10276	171.5	2032	GCK[13]_L	-11116	171.5				
1973	VGL	-10290	299.5	2033	GCK[13]_L	-11130	299.5				
1974	VGH	-10304	171.5	2034	GCK[12]_L	-11144	171.5				
1975	VGH	-10318	299.5	2035	GCK[12]_L	-11158	299.5				
1976	VGH	-10332	171.5	2036	GCK[11]_L	-11172	171.5				
1977	VGH	-10346	299.5	2037	GCK[11]_L	-11186	299.5				
1978	VGH	-10360	171.5	2038	GCK[10]_L	-11200	171.5				
1979	VGH	-10374	299.5	2039	GCK[10]_L	-11214	299.5				
1980	VGH	-10388	171.5	2040	GCK[9]_L	-11228	171.5				

## 13. Ordering Information

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