SC7705 Data Sheet

TFT Mobile Single Chip Driver
For 800 x RGB x 1280 Dot, A-Si TFT LCD, 16.7M Color
With MIPI Interface

Version 01 Preliminary
September 2018

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Revision History

Version	Date	Description of Change
01	2018/01/16	1. New setup

1. General Description

The SC7705 is a single-chip solution for A-Si TFT AMLCD that combines a source driver, power supply circuit to drive A-Si TFT dot matrix AMLCD with 800xRGBx1280 dots at maximum. The SC7705 supports MIPI Interface.

The SC7705 incorporates step-up and voltage follower circuits to generate drive voltage required for a-Si TFT and gate in panel (GIP) which including a dynamic backlight control function to control backlight brightness depending on image data, reducing power consumption at the backlight with the slightest influence on image quality.

The SC7705 is suitable for small or medium-sized portable mobile solutions requiring long-term driving capabilities, such as digital mobile phones, PDAs and Smartphones.

2. Features

- Single chip solution for a HD800 GIP (Gate In Panel) type TFT LCD display

- Resolution:
  - 800RGB x (RES_V_MSB, NL [7:0], RES_V_LSB [1:0])
  - 768RGB x (RES_V_MSB, NL [7:0], RES_V_LSB [1:0])
  - 640RGB x (RES_V_MSB, NL [7:0], RES_V_LSB [1:0])
  - 600RGB x (RES_V_MSB, NL [7:0], RES_V_LSB [1:0])
  - 540RGB x (RES_V_MSB, NL [7:0], RES_V_LSB [1:0])
  - 750RGB x (RES_V_MSB, NL [7:0], RES_V_LSB [1:0])

- Display color modes
  - Full color mode: 16.7M colors
  - Reduce color mode: 262k colors
  - Reduce color mode: 65k colors
  - Idle mode: 8 colors

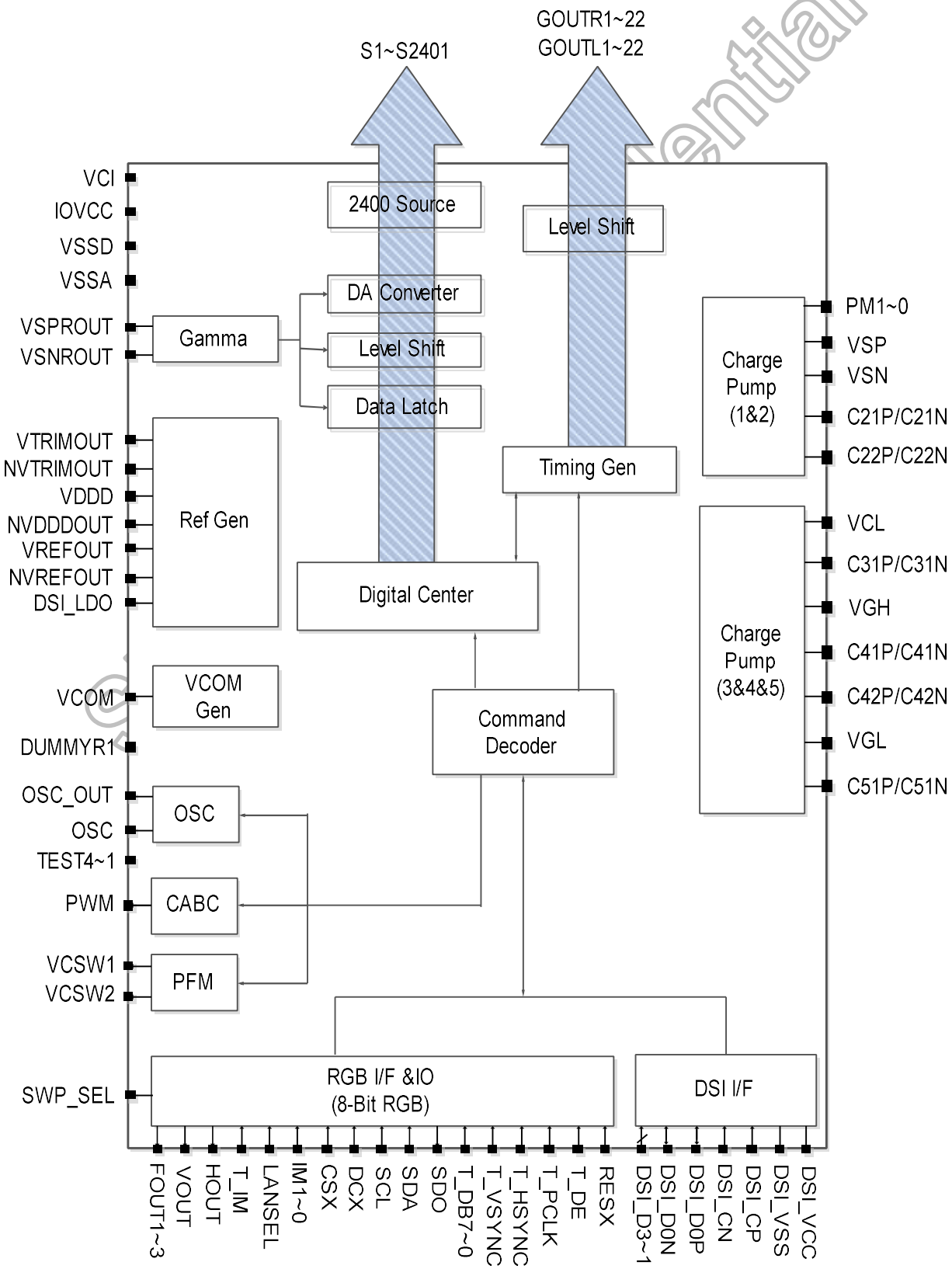
- Display interface types supported
  - MIPI Display Serial Interface (DSI V1.01)

- Input power：
  - External power IC and PFM：
    - I/O and interface power supply (IOVCC)：1.65V to 3.3V
    - Analog power supply (VCI)：2.5V to 3.3V
  - Three-Power Mode：
    - I/O and interface power supply (IOVCC)：1.65V to 3.3V
    - Analog power supply (VSP)：4.5V to 6.0V
    - Analog power supply (VSN)：-4.5V to -6.0V

- Output Voltage
  - Positive source output voltage level: VSPR=3.3V to 5.6V
  - Negative source output voltage level: VSNR=-5.6V to -3.3V
  - Positive gate driver output voltage level: VGH=+10V to +20V
  - Negative gate driver output voltage level: VGL=-7.5V to -15V
  - Most negative reference voltage: LVGL=VGL
  - VCOM=-3.5V to 0V

- On Chip
  - VGH/VGL for GIP gate control
  - 1-Dot / 2-Dot / 3-Dot / 4-Dot / 8-Dot / Column / Zig-Zag/ Zig-Zag2 Inversion
  - Gamma correction function
  - Oscillator for display clock generation
  - Internal OTP programming voltage generator
  - 4 times MTP for VCOM setting ,ID setting
  - CABC (Content Adaptive Brightness Control) function
  - DGC (Digital Gamma Correction) function

3. Block Diagram



4. IC Pin Description

4.1 IC Pin Description

Power Supply Pin

Symbol	I/O	Description	Connection when Not Used
VCI	P	Power supply for analog circuit.	-
IOVCC	P	Power supply for logic circuit.	-
DSI_VCC	P	Power supply for MIPI-DSI circuit.	-
VSSA	P	System ground for analog circuit.	-
VSSD	P	System ground for logic circuit.	-
DSI_VSS	P	Ground for MIPI-DSI circuit	-

Interface Logic Pin

Symbol	I/O	Description	Connection when not used
IM1~0 LANSEL	I	Interface mode select pins. IM1~IM0 and LANSEL are used for the combination of polarity swap and data lane swap of DSI.	GND
RESX	I	Reset pin. This signal will reset the device and must be applied to properly initialize the chip.	-
VOUT	O	Frame synchronization output signal pin.	OPEN
HOUT	O	Scan line synchronization output signal pin.	OPEN
FOUT1-3	O	Frame synchronization or Scan line synchronization or PWM output	OPEN

IM1	IM0	LANSEL	D0P/N	D1P/N	CP/N	D2P/N	D3/PN
0	0	0	D3P/N	D2P/N	CP/N	D1P/N	D0P/N
0	1	0	D3N/P	D2N/P	CN/P	D1N/P	D0N/P
1	0	0	D0P/N	D1P/N	CP/N	D2P/N	D3P/N
1	1	0	D0N/P	D1N/P	CN/P	D2N/P	D3N/P
0	0	1	D2P/N	D1P/N	CP/N	D0P/N	D3P/N
0	1	1	D2N/P	D1N/P	CN/P	D0N/P	D3N/P
1	0	1	D3P/N	D0P/N	CP/N	D1P/N	D2P/N
1	1	1	D3N/P	D0N/P	CN/P	D1N/P	D2N/P

Interface Pin

Symbol	I/O	Description	Connection when not used
DSI_D0P, DSI_D0P	I/O	High speed interface data differential signal input/output pins.	OPEN/GND
DSI_CP, DSI_CN	I	High speed interface CLOCK differential signal input pins.	OPEN/GND
DSI_D3P~1P, DSI_D3N~1N	I	High speed interface data differential signal input/output pins.	OPEN/GND

DC/DC Converter Pin

Symbol	I/O	Description	Connection when not used
VSP	I	Input voltage from the set-up circuit.	-
VSN	I	Input voltage from the set-up circuit.	-
C21P,C21N C22P,C22N	I/O	Capacitor connection pins for step-up circuit which generate the VSN voltage.	Open
C31P,C31N	I/O	Capacitor connection pins for step-up circuit which generate the VCL voltage.	Open
C41P,C41N C42P,C42N	I/O	Capacitor connection pins for step-up circuit which generate the VGH voltage.	Open
C51P,C51N	I/O	Capacitor connection pins for step-up circuit which generate the VGL voltage.	Open
VGL_REG	O	Output voltage generated from VGL.	Open
VDDD	O	Reference voltage for internal logic.	-
NVDDDOUT	O	Negative reference voltage for internal logic.	-
VGH	O	Output voltage from the step-up circuit.	-
LVGL	O	Negative voltage for special GIP circuits.	
VGL	O	Output voltage from the step-up circuit.	-
DSI_LDO	O	High speed interface regulator output pin.	Open
VSPROUT	O	Output voltage generated from VSP. Output for positive gamma voltage generator.	
VSNROUT	O	Output voltage generated from VSN. Output for negative gamma voltage generator.	
VTRIMOUT	O	Reference voltage for internal voltage generating circuit.	
NVTRIMOUT	O	Reference voltage for internal voltage generating circuit.	
VCL	O	An output from the step-up circuit3.	
VCSW1	O	PFM and Power IC control output for DC/DC converter to generate VSP.	-
VCSW2	O	PFM and Power IC control output for DC/DC converter to generate VSN.	-
EXT_VSP	I	When EXBT =0, PSSC [2:0] =101 then connect VSP others let it open.	Open
EXT_VSN	I	When EXBT =0, PSSC [2:0] =101 then connect VSN others let it open.	Open
IOVCC_MIPI	O	Reference voltage for internal logic.	-

Driver Output pins

Symbol	I/O	Description	Connection when not used
S1 to S2401	O	Pixel electrode driving output Display Resolution / Used Source Pins 800RGB: S1~S2400 768RGB: S1~S1152 and S1249~S2400 720RGB: S1~S1080 and S1321~S2400 640RGB: S1~S960 and S1441~S2400 600RGB: S1~S900 and S1501~S2400 540RGB: S1~S810 and S1501~S2400	Open
CGOUTL_1~22 CGOUTR_1~22	O	Gate control signals for panel.	Open
VCOM	O	Regulator output for common voltage of panel	

CABC Control Pin

Symbol	I/O	Description	Connection when not used
PWM	O	This pin is connecting with the external LED driver.	Open

Test Pin

Symbol	I/O	Description	Connection when not used
OSC	I	Oscillator test pin	Open
CSX	I	Chip select input pin (“Low” enable) in RGB I/F test mode.	OPEN
DCX	I	Command/parameter selection in RGB I/F test mode. Low: Select command. High: Select data.	IOVCC/GND/OPEN
SCL	I	A synchronous clock signals in RGB I/F test mode.	IOVCC/GND/OPEN
SDA	I/O	Serial data input/output pin in RGB I/F test mode.	IOVCC/GND/OPEN
SDO	O	A serial data output pin in RGB I/F test mode.	OPEN
T_DB7~0	I	8-bit input data bus in RGB I/F test mode.	IOVCC/GND/OPEN
T_HSYNC	I	Line synchronizing signal in RGB I/F test mode.	IOVCC/GND/OPEN
T_DE	I	Data enable signal in RGB I/F test mode.	IOVCC/GND/OPEN
T_VSYNC	I	Vertical synchronizing signal in RGB I/F test mode.	IOVCC/GND/OPEN
T_PCLK	I	Pixel clock signal in RGB I/F test mode.	IOVCC/GND/OPEN
T_IM	I	Let driver IC into RGB I/F test mode if set T_IM= high.	Open
TEST4~1	I	Test pins	Open/GND
OSC_OUT	O	Test pin.	Open
VTESTOUTP	O	Test pin.	Open
VTESTOUTN	O	Test pin.	Open
NVREFOUT	O	Test pin.	Open
VREFOUT	O	Test pin.	Open
PM1~0	I	Test pin.	Open
DUMMYR1	-	Test pin for bonding quality test. They are short-circuited within the chip.	Open
DUMMY78~1	-	Not used. Let it open.	Open
DUMMY_C32P DUMMY_C32N	-	Not used. Let it open.	Open
VCC1_DUMMY	-	Not used.Let it open.	Open
VCC2_DUMMY	-	Not used. Let it open.	Open
DUMMY_HVN	-	Not used. Let it open.	Open
DUMMY_VPP DUMMY_RS0 DUMMY_RS1	-	No use. Let them open.	Open

4.2 BOM

NO	IC Pin Name	Capacitance (uF)	Permissible Voltage (V)	Note
1	VCI	2.2	6.3	
2	IOVCC	2.2	6.3	
3	C31P / C31N	1	10	Flying Capacitor
4	C41P / C41N	1	16	Flying Capacitor
5	C51P / C51N	1	16	Flying Capacitor
6	VSP	2.2	10	
7	VSN	2.2	10	
8	VGH	1	25	
9	VGL	1	16	
10	VTRIMOUT	1	6.3	
11	VREFOUT	1	6.3	Optional
12	NVREFOUT	1	6.3	Optional
13	VSPROUT	1	6.3	
14	VSNROUT	1	6.3	
15	VCOM	1	6.3	
16	VCL	1	6.3	Not necessary if VCL is not used.
17	VDDD	1	6.3	
18	NVDDOUT	1	6.3	
19	DSI_LDO	1	6.3	Not necessary if using DBI + DPI

5. Function Description

5.1 MIPI Interface

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The SC7705 only support Video mode.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the driver IC relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode.

Lane Pair	HOST(Master)/ Driver IC(Slave)
Clock Lane	-Unidirectional Lane -Clock Only -Escape mode (ULPS only)
Data Lane 0	-Bi-directional Lane -Forward High Speed -Bi-directional Escape Mode -Bi-directional LPDT
Data Lane 1	-Unidirectional Lane -Forward High Speed - Escape mode (ULPS only) -NO LPDT

Table 5.1: MIPI interface configuration

5.1.1 DSI General Interface communication

The driver IC uses data and clock lane differential pairs for DSI. Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode. Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode. There are used different modes and protocol in each mode when there is wanted to transfer information from the HOST to the driver IC and vice versa.

State code	Line voltage Levels		High speed	Low power	
	DP	DN		Control mode	Escape mode
HS-0	HS Low	HS High	Differential-0	Note 1	Note 1
HS-1	HS High	HS Low	Differential-1	Note 1	Note 1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	Note 2

Note 1 : During high-speed transmission, the low power receivers observe LP-00 on the lines.
Note 2 :If LP-11 occurs during Escape mode, the lane returns to Stop state (Control mode LP-11)

Table 5.2: Lane State Description

5.1.1.1 DSI Clock Lane

The principle flow chart of the different clock lanes power modes is illustrated below.

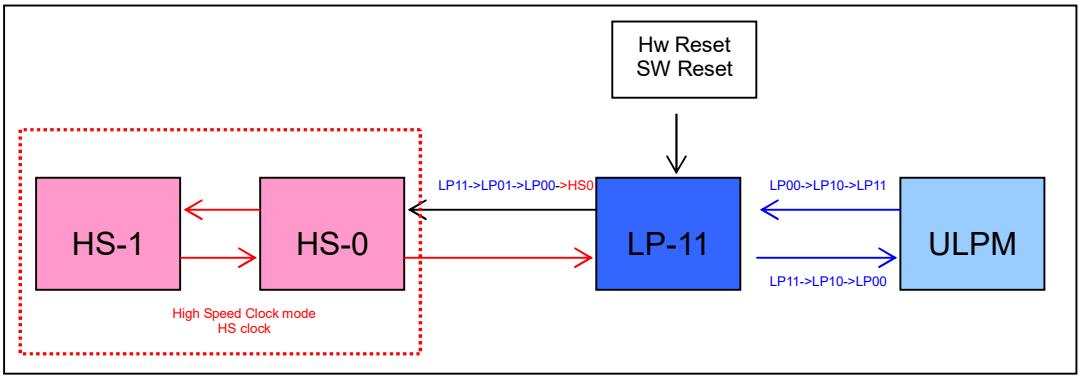


Figure 5.1: DSI Clock Lane State Diagram

Low Power Mode (LP-11: Stop)

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11:

1. After SW Reset, HW Reset or Power On Sequence =>LP-11
2. After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.

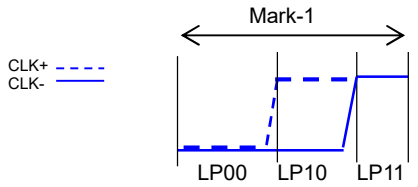


Figure 5.2: From ULPM to LPM

3. After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence and all three mode changes are illustrated below.

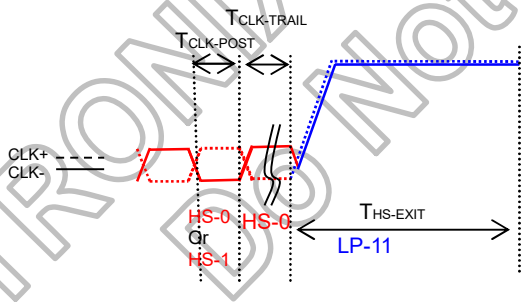


Figure 5.3: From High Speed Clock mode to LPM

Ultra Low Power Mode (LP-00: ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State. The entering way is from the Low Power Mode (LPM, LP-11 State) =>LP-10 =>LP-00 (ULPM). This sequence is illustrated below.

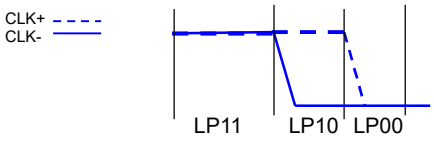


Figure 5.4: From LPM mode to ULPM

High Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State. The entering way is from the Low Power Mode (LPM, LP-11 State) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

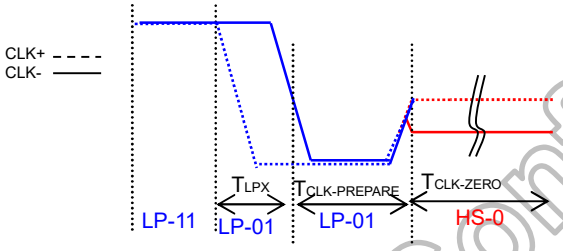


Figure 5.5: From LPM mode to HSCM

High Speed Clock Burst

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

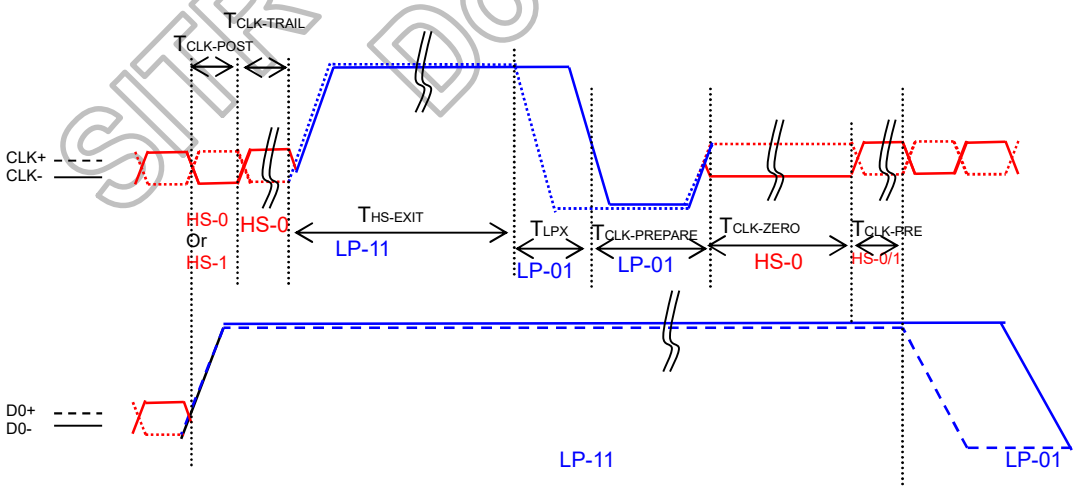


Figure 5.6: Switching the Clock Lane between HSCM and LPM

5.1.1.2 DSI-D0 Data Lane

DSI-D0+/- Data Lanes can be driven in different modes which are: Escape Mode, High-Speed Data Transmission and Bus Turnaround Request. The flow chart of the D0 data lanes is illustrated below.

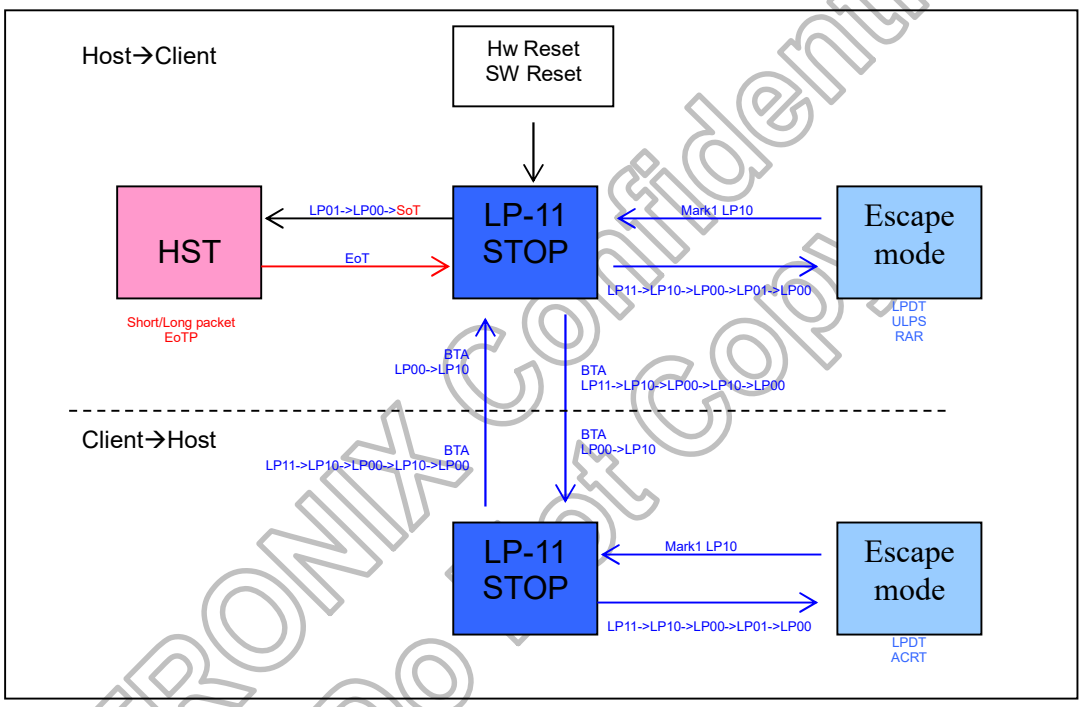


Figure 5.7: DSI Data Lane D0 State Diagram

Description	Operation code
High Speed Data Transmission Burst	LP11->LP01->LP00
Escape mode entry	LP11->LP10->LP00->LP01->LP00
Bus turn around	LP11->LP10->LP00->LP10->LP00
Exit Escape mode (Mark-1)	LP00->LP10->LP11

Table 5.3: Data Lane D0 Operation Modes

ESCAPE MODE

Data lanes (DSI-D0+/-) can be used in different Escape Modes when data lanes are in Low Power (LP) mode.

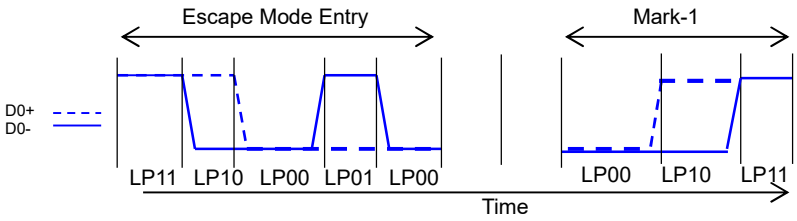


Figure 5.8: DSI Data Lane D0 general escape mode sequence

SC7705 can support three different Escape Commands. The commands (EC) can be divided 2 different groups: Mode or Trigger. The HOST is informing to the driver IC that it is controlling data lanes (DSI-D0+/-) with the mode. Escape commands are defined as below table.

Escape Command	Command Type	Entry Command Pattern (First Bit→Last Bit Transmitted)
Low Power Data Transmission	Mode	1110 0001
Ultra-Low Power mode	Mode	0001 1110
Remote Application Reset	Trigger	0110 0010
Tearing Effect	Trigger	0101 1101
Acknowledge	Trigger	0010 0001

Table 5.4: Escape mode commands

Low-Power Data Transmission (LPDT)

The HOST can send data to the driver IC in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command will been sent to this driver IC. The driver IC is also using the same sequence when it is sending data to the HOST. The Low Power Data Transmission (LPDT) is using a following sequence:

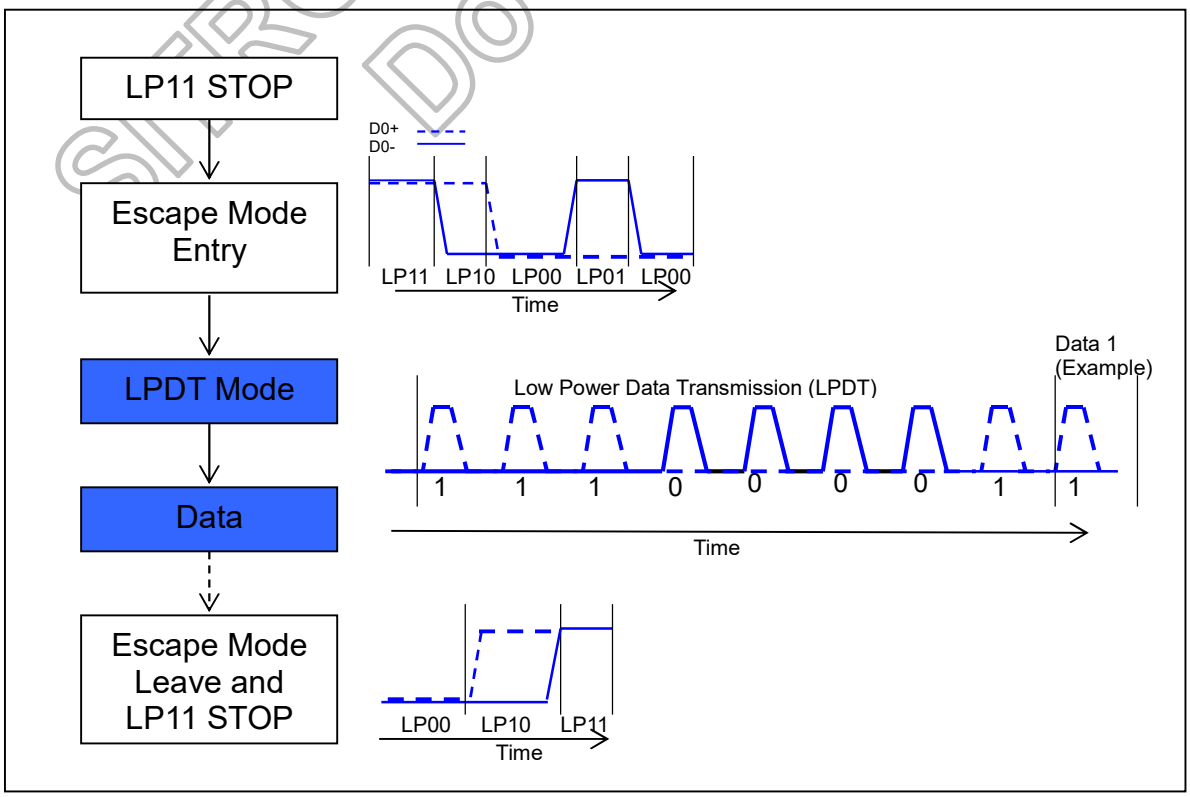


Figure 5.9: DSI Data Lane D0 LPDT sequence

Ultra Low Power State (ULPS)

The driver IC can enter this Ultra Low Power Sate to save power consumption when HOST send this ULPS command. Ultra Low Power State is using below sequence:

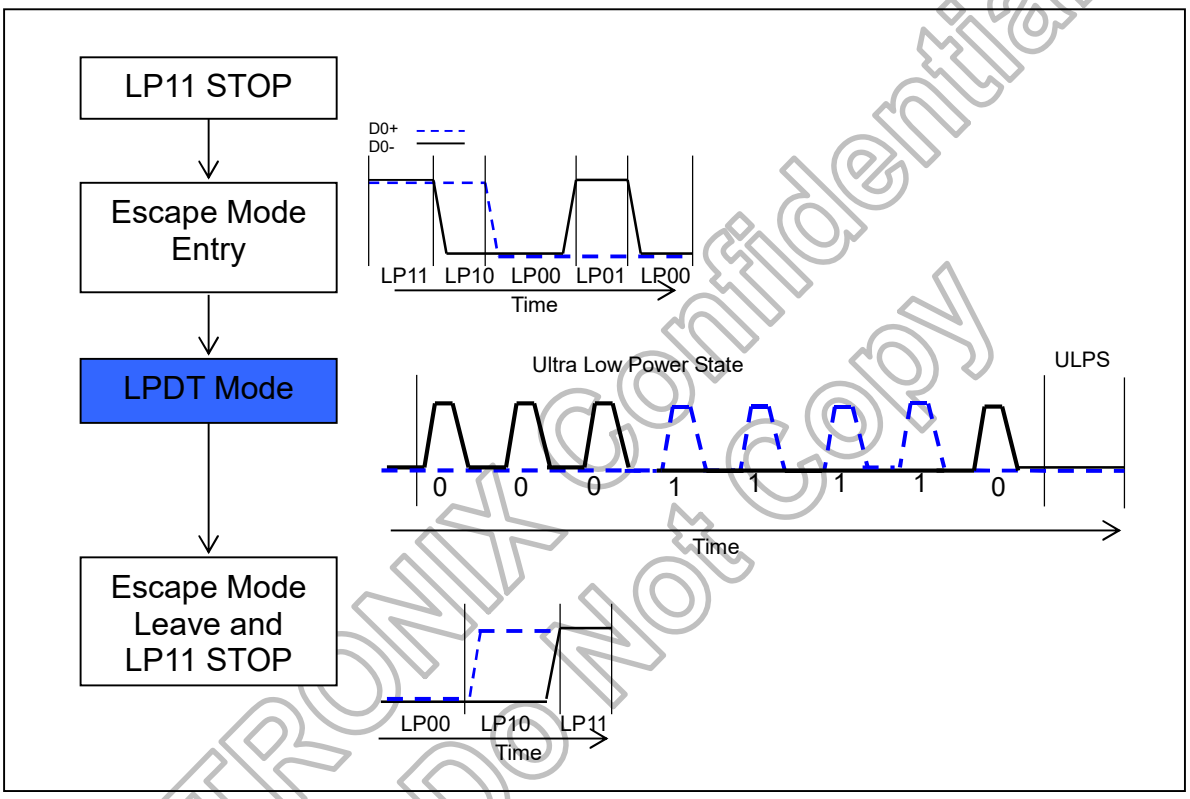


Figure 5.10: DSI Data Lane D0 ULPS sequence

Remote Application Reset (RAR)

The HOST can inform to the driver IC that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode. The Remote Application Reset (RAR) is using a following sequence:

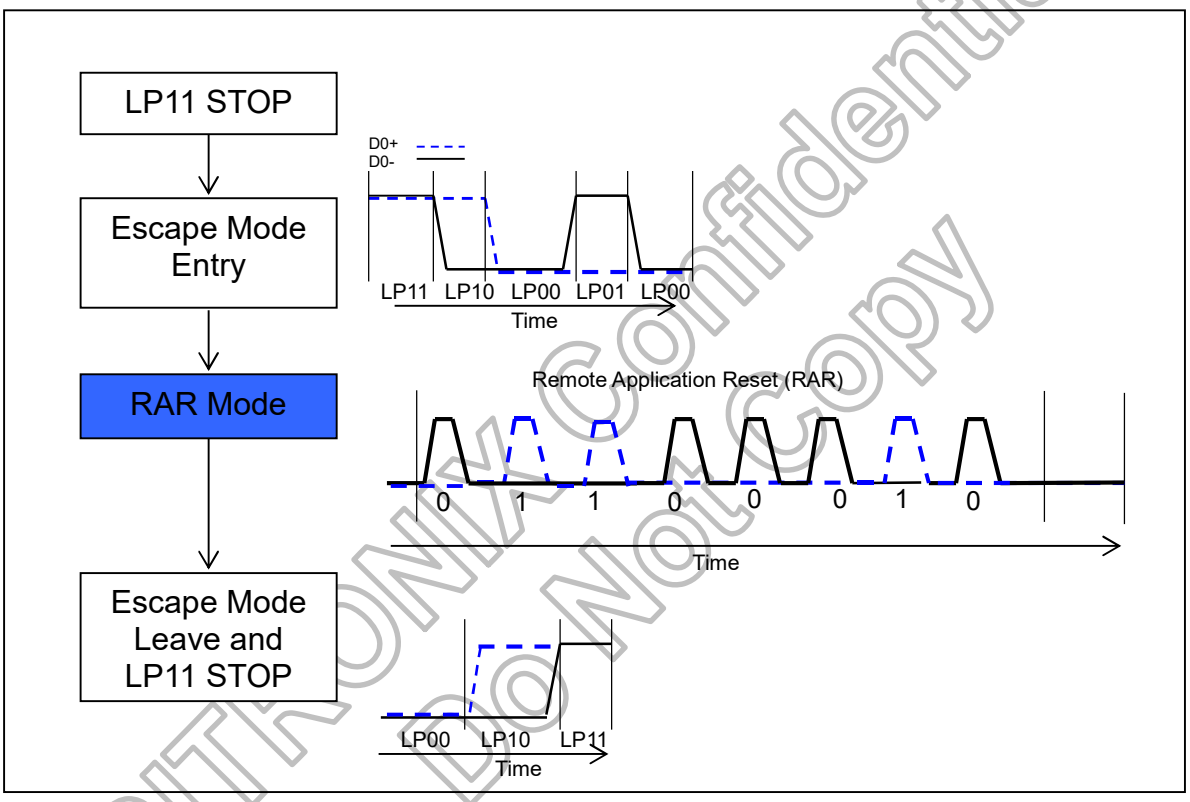


Figure 5.11: DSI Data Lane D0 RAR sequence

Tearing Effect (TEE)

The driver IC can inform to the HOST when a tearing effect event (New V-synch) has been happen on the driver IC by Tearing Effect (TEE). The Tearing Effect (TEE) is using a following sequence:

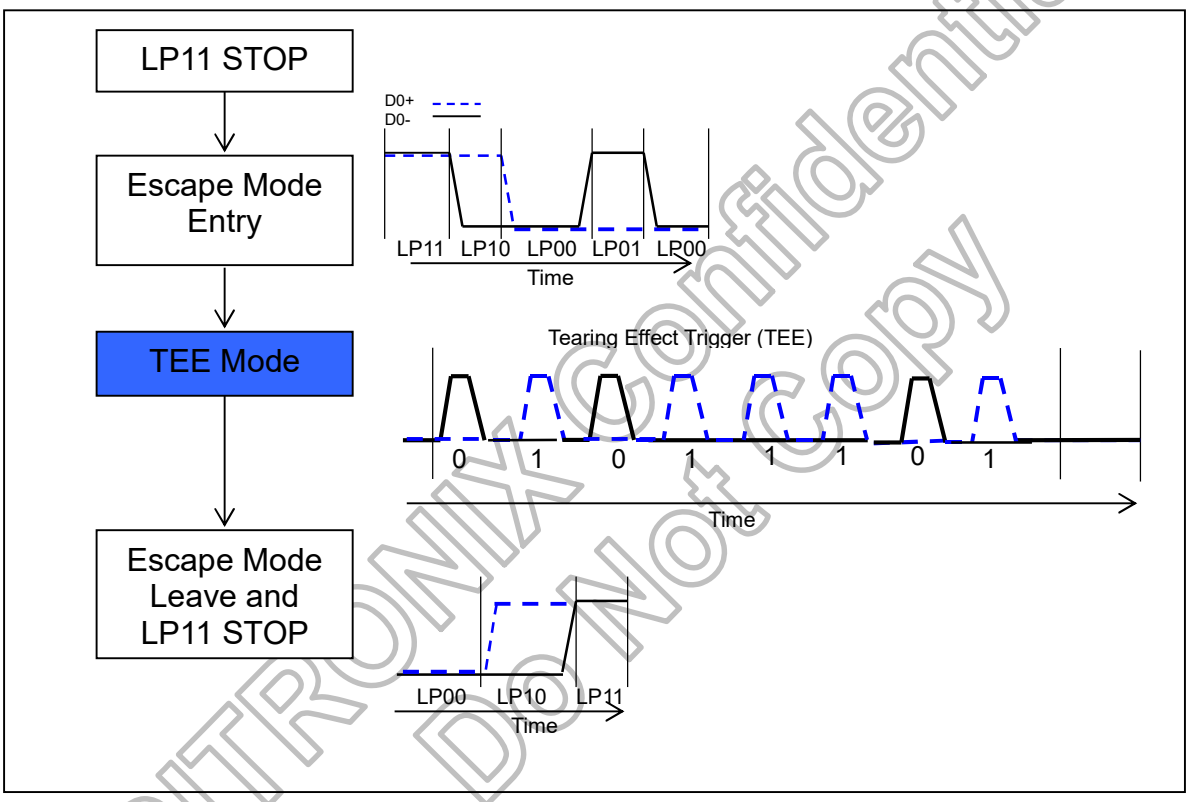


Figure 5.12: DSI Data Lane D0 TEE sequence

Acknowledge (ACK)

The driver IC can inform to the HOST when an error has not recognized on it by Acknowledge (ACK). The Acknowledge (ACK) is using a following sequence:

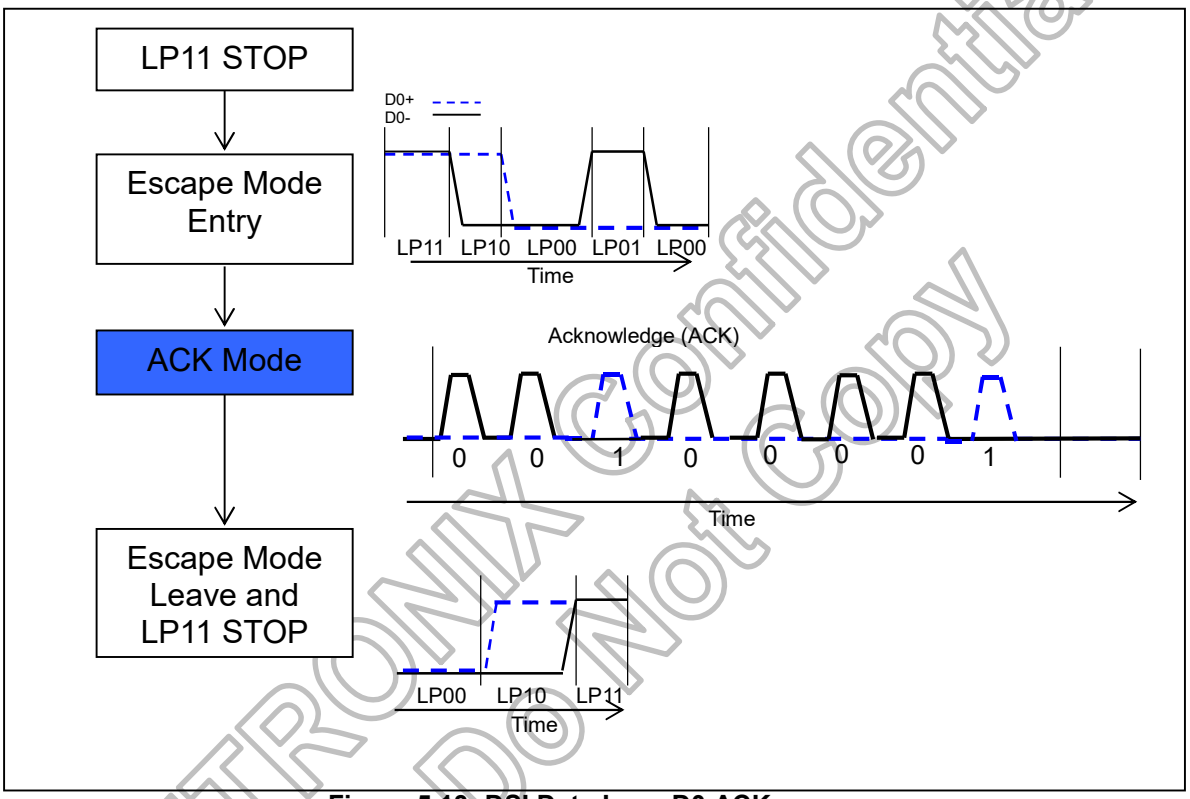


Figure 5.13: DSI Data Lane D0 ACK sequence

High Speed Data Transmission

The driver IC is entering High-Speed Data Transmission when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode by the HOST. Data lanes of the driver IC are entering (TSOT) in the High-Speed Data Transmission (HSDT) as below figure.

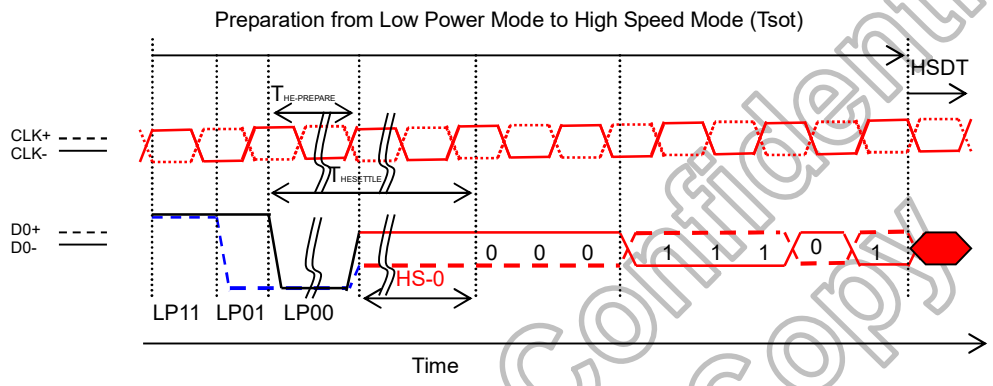
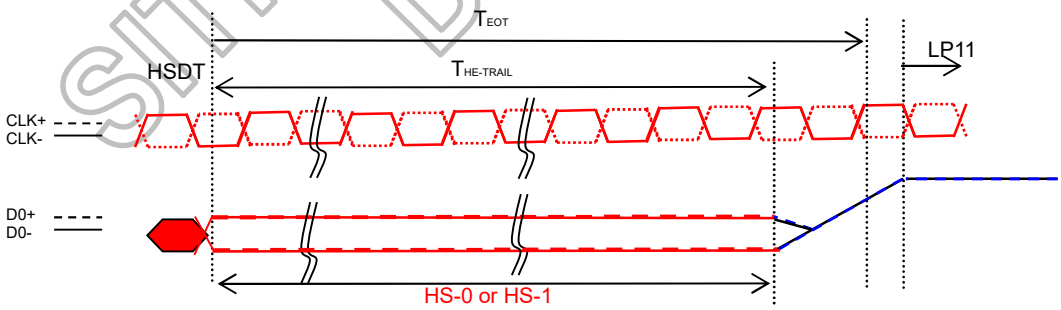


Figure 5.14: DSI Data Lane Entering High Speed Data Transmission

Leaving High Speed Data Transmission

The driver IC is leaving the High-Speed Data Transmission (TEOT of HSDT) when Clock lanes DSI-CLK+/- are in the High-Speed Clock Mode by the HOST and it is kept until data lanes are in LP-11 mode.Data lanes of the driver IC are leaving from the High-Speed Data Transmission (TEOT of HSDT) as follows



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Figure 5.15: DSI Data Lane Entering High Speed Data Transmission

Bus Turnaround (BTA)

The HOST or driver IC, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the HOST or driver IC. The HOST or driver IC is using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the HOST wants to do the bus turnaround procedure to the driver IC, as below.

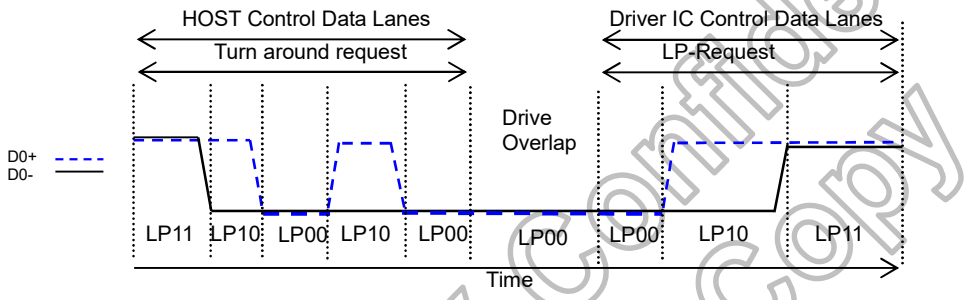
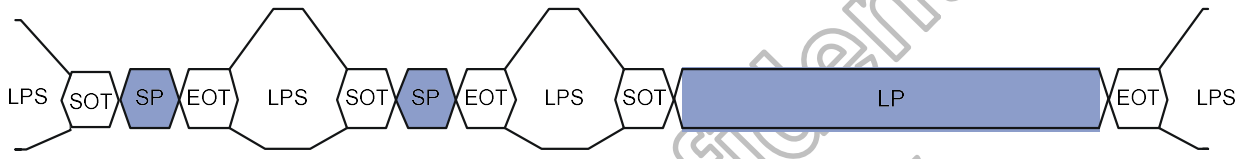


Figure 5.16: DSI Bus Turn Around Procedure

5.1.2 DSI Packet Level Communication

The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded separate write commands at system startup. Below figure illustrates multiple HS Transmission packets.



LPS：Low power state
SOT：Start of Transmission
SP：Short Packet
LP：Long Packet
EOT：End of Transmission

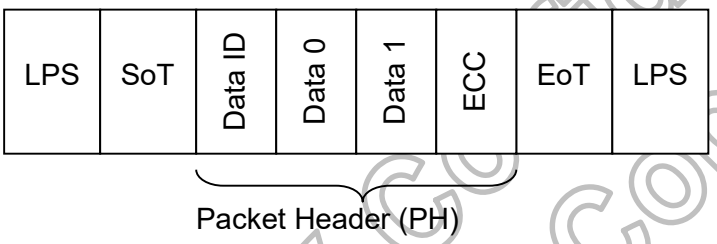
Figure 5.17: DSI multiple HS transmission packets

The packet includes two types which are Long packet and short packet. The first byte of the packet, the Data Identifier (DI), includes information specifying the length of the packet. Command Mode systems send commands and an associated set of parameters, with the number of parameters depending on the command type.

5.1.2.1 General Packet Structure

Short packets

Specify the payload length using the Data Type field and are from two to nine bytes in length. Short packet is used for most Command Mode commands and associated parameters. Where short packets format include an 8-bit Data ID followed by zero to seven bytes and an 8-bit ECC. Below figure shows the structure of the Short packet.

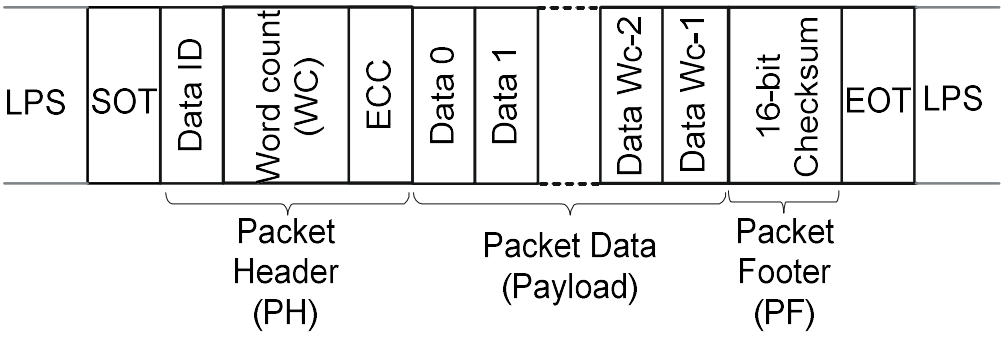


SOT: Start of Transmission
DI(Data ID): 8-bit Contain Virtual Channel Identifier and Data Type.
Data 0 and Data 1: Packet Data (8+8bit)
ECC(Error Correction Code): The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.

Figure 5.18: Structure of the short packet

Long packets

Specify the payload length using a two-byte Word Count field and then the payload maybe from 0 to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data. Below figure shows the structure of the Long packet. Long Packet Header composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length. Where 65,541 bytes = (216-1) + 4 bytes PH + 2 bytes PF



DI (Data ID)：Contain Virtual Channel Identifier and Data Type.
WC (Word Count)：8+8 bits The receiver use WC to define packet end.
ECC (Error Correction Code)：The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.
PF(Packet Footer)：Mean 16-bit Checksum.

Figure 5.19: Structure of the long packet

According to packet form, basic elements include DI and ECC. Figure 4.44 the shows format of Data ID.

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
VC (Virtual Channel)		DT (Data Type)					

DI[7:6] ➔ These two bits identify the data as directed to one of four virtual channels.
DI[5:0]: These six bits specify the Data Type, which specifies the size, format and, in some cases, the interpretation of the packet contents.

Figure 5.20: Format of data ID

Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the HOST. The FL11280 supports Virtual Channel only when VC = 00.

Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Data type, hex	Data type, binary	Description packet	Size
05h	00 0101	DCS Write, no parameters	Short
15h	01 0101	DCS Write, 1 parameter	Short
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	Shut Down Peripheral Command	Short
32h	11 0010	Turn On Peripheral Command	Short
13h	01 0011	Generic Short Write, 1 parameter	Short
23h	10 0011	Generic Short Write, 2 parameter	Short
14h	01 0100	Generic Read, 1 parameter	Short
29h	10 1001	Generic Long Write	Long
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
X0h and XFh, unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	-

Table 5.5: Data types from Host to the driver IC

Data type, hex	Data type, binary	Description packet	Size
02h	00 0010	Acknowledge with Error Report	Short
21h	01 0001	Generic short READ Response, 1 byte returned	Short
22h	01 0010	Generic short READ Response, 2 byte returned	Short
1Ah	01 1010	Generic Read Long Response	Long
1Ch	01 1100	DCS Long READ Response	Long

Table 5.6: Data types from the driver IC to Host

Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors on the Packet Header (PH).

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function, as follows.

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

PACKET DATA (PD) ON THE LONG PACKET

Packet Data (PD) of the Long Packet is defined after Packet Header (PH) of the Long Packet. The number of the data bytes is defined on chapter "Word Count (WC) on the Long Packet".

PACKET FOOTER (PF) ON THE LONG PACKET

Packet Footer (PF) of the Long Packet is defined after the Packet Data (PD) of the Long Packet. The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet .The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial $X^{16}+X^{12}+X^{5}+X^{0}$.

5.1.2.2 Detail Format Description

Generic Write, 1 Parameter, Data Type = 01 0011 (13h)
Generic Write, 1 Parameter is always using a Short Packet from the HOST to the driver IC. The content of 2 payload bytes is “command” and “00h”.

Generic Write, 2 Parameter, Data Type = 10 0011 (23h)
Generic Write, 2 Parameter is always using a Short Packet from the HOST to the driver IC. The content of 2 payload bytes is “command” and “parameter”.

Generic Long Write, Data Type = 10 1001 (29h)
Generic Long Write is always using a Long Packet from the HOST to the driver IC. The content can include Command (No Parameters) or Command with 1 or more parameters.

Generic Read, 1 Parameter, Data Type = 01 0100 (14h)
Generic Read, 1 Parameter is always using a Short Packet from the HOST to the driver IC. The HOST has to define to the driver IC, what is the maximum size of the return packet. A command, what is used for this purpose, is “Set Maximum Return Packet Size”, which Data Type is 11 0111 and which is using Short Packet before the HOST can send “Generic Read, 1 Parameter” to the driver IC.

Display Command Set Write, No Parameter, Data Type = 00 0101 (05h)
Display Command Set (DCS) Write, No Parameter is always using a Short Packet from the HOST to the driver IC. The content of 2 payload bytes is “command” and “00h”.

Display Command Set Write, 1 Parameter, Data Type = 01 0101 (15h)
Display Command Set (DCS) Write, 1 Parameter is always using a Short Packet from the HOST to the driver IC. The content of 2 payload bytes is “command” and “parameter”.

Display Command Set Long Write, Data Type = 11 1001 (39h)
Display Command Set (DCS) Long Write is always using a Long Packet from the HOST to the driver IC. The content can include Command (No Parameters) or Command with 1 or more parameters.

Display Command Set (DCS) Read, No Parameter, Data Type = 00 0110 (06h)
Display Command Set (DCS) Read, No Parameter is always using a Short Packet, from the HOST to the driver IC. The HOST has to define to the driver IC, what is the maximum size of the return packet. A command, what is used for this purpose, is “Set Maximum Return Packet Size”, which Data Type is 11 0111 and which is using Short Packet before the HOST can send “Display Command Set (DCS) Read, No Parameter” to the driver IC.

Null Packet, No Data , Data Type = 00 1001 (09h)

Null Packet, No Data is always using a Long Packet, what is defined on Data Type from the HOST to the driver IC. The purpose of this command is keeping data lanes in the high speed mode, if it is needed. The driver IC is ignored Packet Data what the HOST is sending.

Set Maximum Return Packet Size, Data Type = 11 0011 (37h)

Set Maximum Return Packet Size is always using a Long Packet, what is defined on Data Type from the HOST to the driver IC. The purpose of this command is specifies the maximum size of the payload in a Long packet transmitted from peripheral back to the host processor.

Sync Event (H Start, H End, V Start, V End), Data Type = XX 0001 (0xX1)

Sync Events are Short packets and, therefore, can time-accurately represent events like the start and end of sync pulses. As “start” and “end” are separate and distinct events, the length of sync pulses, as well as position relative to active pixel data, The Sync Events are defined as follows:

- Data Type = 00 0001 (01h) V Sync Start
- Data Type = 01 0001 (11h) V Sync End
- Data Type = 10 0001 (21h) H Sync Start
- Data Type = 11 0001 (31h) H Sync End

Color Mode On Command, and, Data Type = 01 0010 (12h)

Color Mode On is a Short packet command that switches a Video Mode driver IC to 8-colors mode for power saving.

Color Mode Off Command, Data Type = 00 0010 (02h)

Color Mode Off is a Short packet command that returns a Video Mode driver IC from 8-colors mode to normal display operation.

Shutdown Peripheral Command, Data Type = 10 0010 (22h)

Shutdown Peripheral command is a Short packet command that turns off the display in a Video Mode driver IC for power saving. Note the interface shall remain powered in order to receive the turn-on, or wake-up command.

Turn On Peripheral Command, Data Type = 11 0010 (32h)

Turn On Peripheral command is Short packet command that turns on the display in a Video Mode driver IC for normal display operation.

Blanking Packet (Long), Data Type = 01 1001 (19h)

A Blanking packet is used to convey blanking timing information in a Long packet. Normally, the packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the driver IC.

Packed Pixel Stream, 16-bit Format, Long packet, Data Type = 00 1110 (0Eh)

Packed Pixel Stream 16-Bit Format is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode driver IC. Pixel format is five bits red, six bits green, five bits blue, in that order. Note that the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

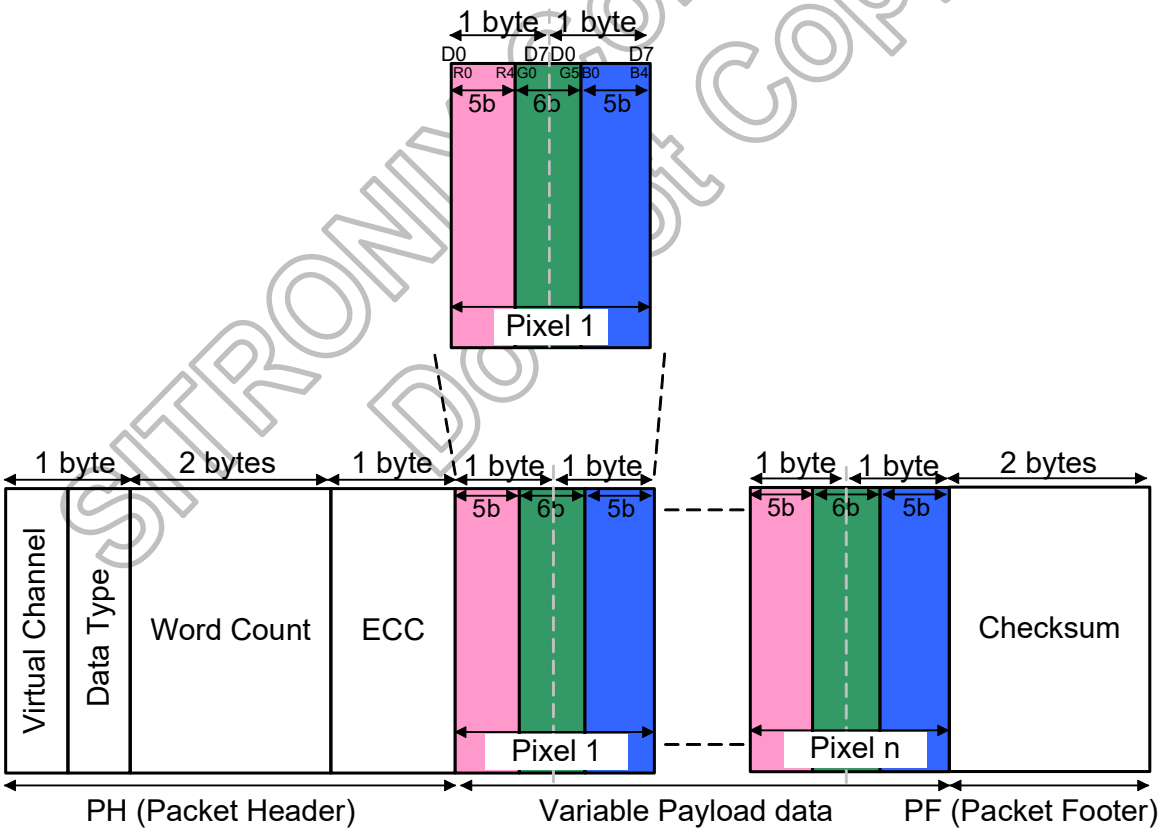
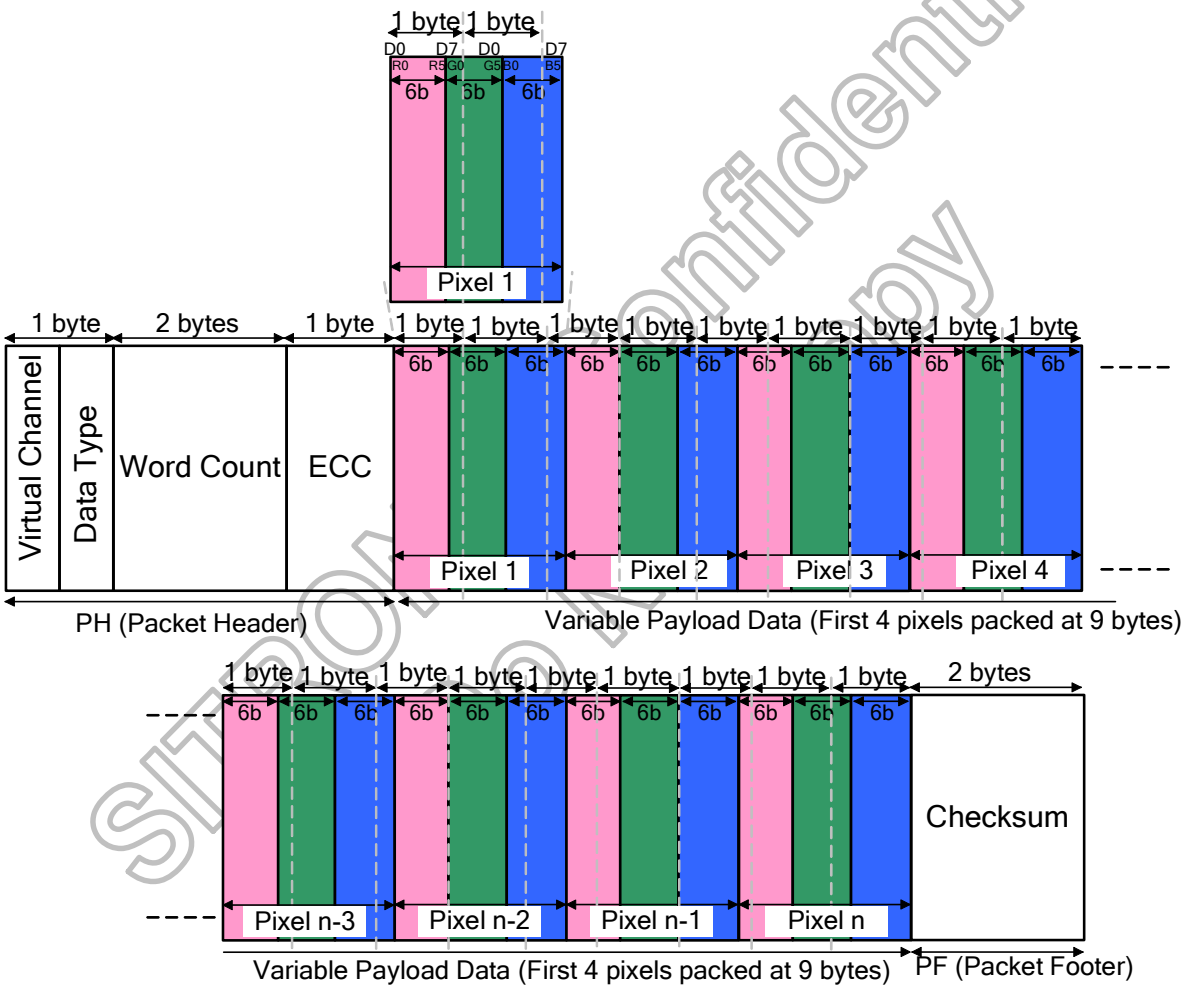


Figure 5.21: 16-bit RGB Color Format, Long packet

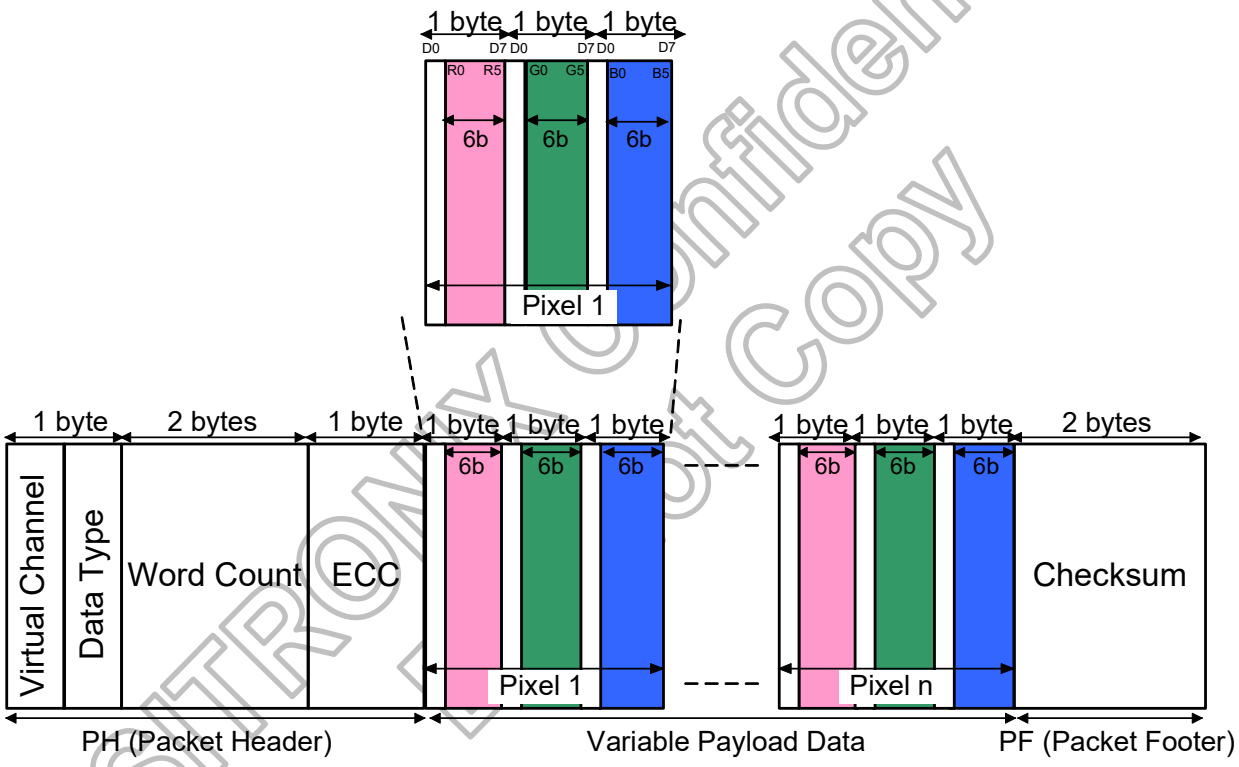
Packed Pixel Stream, 18-bit Format, Long packet, Data type = 01 1110 (1Eh)

Packed Pixel Stream 18-Bit Format is a Long packet used to transmit image data formatted as 18-bit pixels to a Video Mode driver IC. Pixel format is six bits red, six bits green, six bits blue, in that order.



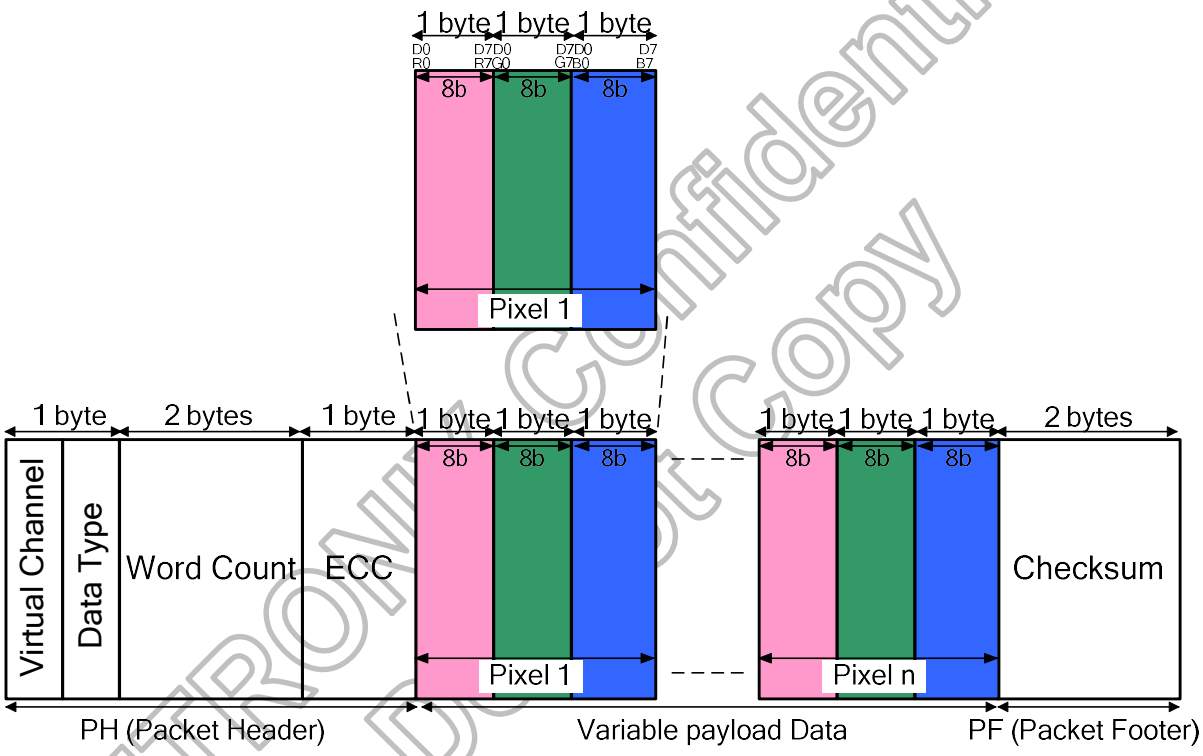
Pixel Stream, 18-bit Format in Three Bytes, Long packet, Data Type = 101110 (2Eh)

Packed Pixel Stream 18-Bit Format is a Long packet used to transmit image data formatted as 18-bit pixels to a Video Mode driver IC. Each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored.



Packed Pixel Stream, 24-bit Format, Long packet, Data Type = 11 1110 (3Eh)

Packed Pixel Stream 24-Bit Format is a Long packet used to transmit image data formatted as 18-bit pixels to a Video Mode driver IC. Pixel format is eight bits red, eight bits green, eight bits blue, in that order.



Acknowledge with Error Report, Data Type = 00 0010(02h)

"Acknowledge with Error Report" is always using a Short Packet, from the driver IC to the HOST. The Packet Data can include bits, which are defining the current error, when a corresponding bit is set to '1', as they are defined on the following table.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	HS Receive Timeout Error
6	reserved
7	reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	reserved
14	reserved
15	reserved

These errors of the previous packets can check "Read Display Signal Mode (0Eh)" and "Read Number of the Errors on DSI (05h)" commands. The bit D0 of the "Read Display Signal Mode (0Eh)" command has been set to '1' if a received packet includes an error.
The number of the packets, which are including an ECC or CRC error, are calculated on the RDNUMED register, which can read "Read Number of the Errors on DSI (05h)" command.

DCS Read Long Response, Data Type = 01 1100(1Ch)

DCS Read Long Response is always using a Long Packet, from the driver IC to the Host. "DCS Read Long Response" is used when the driver IC wants to response a DCS Read command, which the Host has sent to the driver IC.

DCS Read Short Response, 1 Byte Returned, Data Type = 10 0001(21h)

DCS Read Short Response, 1 Byte Returned is always using a Short Packet from the driver IC to the Host. "DCS Read Short Response, 1 Byte Returned" is used when the driver IC wants to response a DCS Read command, which the Host has sent to the driver IC.

DCS Read Short Response, 2 Bytes Returned, Data Type = 10 0010(22h)

DCS Read Short Response, 2 Bytes Returned is always using a Short Packet from the driver IC to the Host. "DCS Read Short Response, 2 Bytes Returned" is used when the driver IC wants to response a DCS Read command, which the Host has sent to the driver IC.

Generic Read Long Response, Data Type = 01 1010(1Ah)

Generic Read Long Response is always using a Long Packet from the driver IC to the HOST. “Generic Read Long Response” is used when the driver IC wants to response a Generic Read command.

Generic Read Short Response, 1 Byte Returned, Data Type = 01 0001(11h)

Generic Read Short Response, 1 Byte Returned is always using a Short Packet from the driver IC to the HOST. “Generic Read Short Response, 1 Byte Returned” is used when the driver IC wants to response a Generic Read command, which the HOST has sent to the driver IC.

Generic Read Short Response, 2 Bytes Returned, Data Type = 01 0010(12h)

Generic Read Short Response, 2 Bytes Returned is always using a Short Packet from the driver IC to the HOST. “Generic Read Short Response, 2 Bytes Returned” is used when the driver IC wants to response a Generic Read command, which the HOST has sent to the driver IC.

5.2 Inversion

The SC7705 can support the column, 1–dot, 3-dot, 2-dot, 4-dot and 8-dot inversion of liquid crystal. These inversions can provide a solution for improving display quality. In determining the inversion drive for the inversion cycle, check the quality of display on the liquid crystal panel.

The SC7705 also can support the ZigZag inversion. Two kinds of ZigZag inversion can be selected by software setting. These two kinds are as below figure:

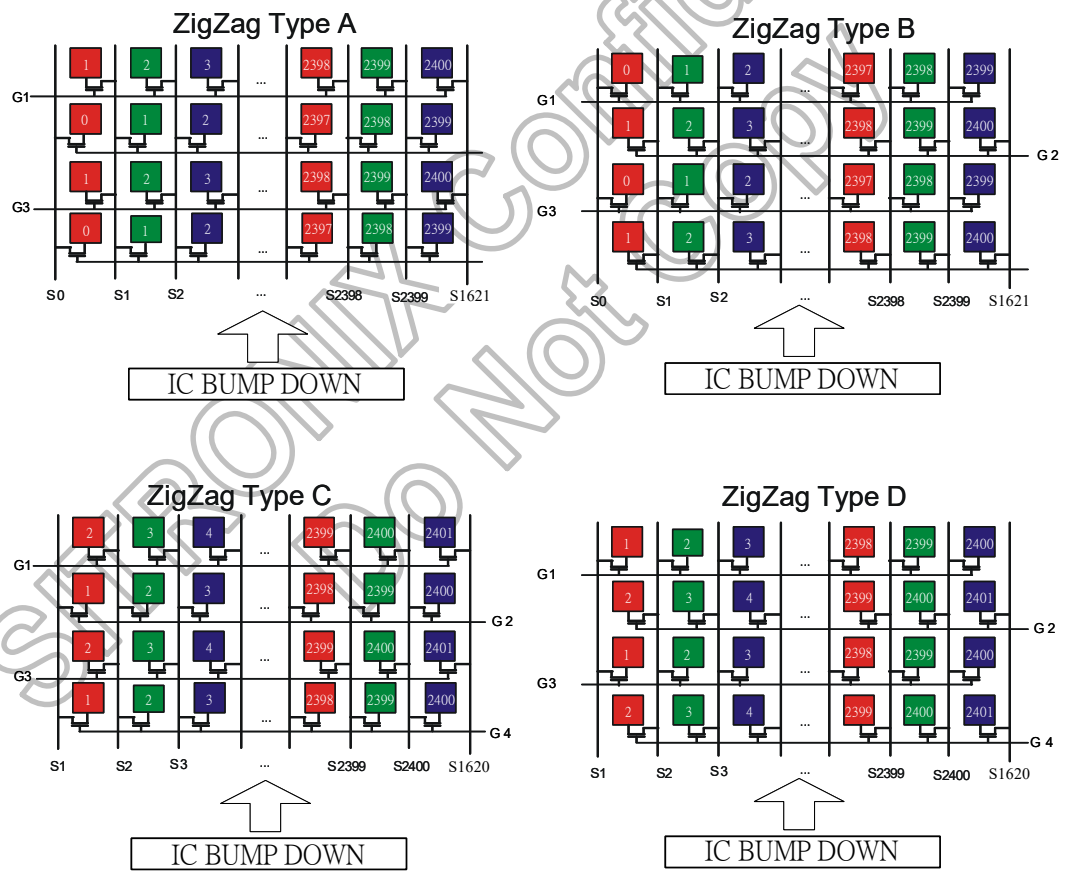


Figure 5.22: Source channels of ZigZag inversion mode

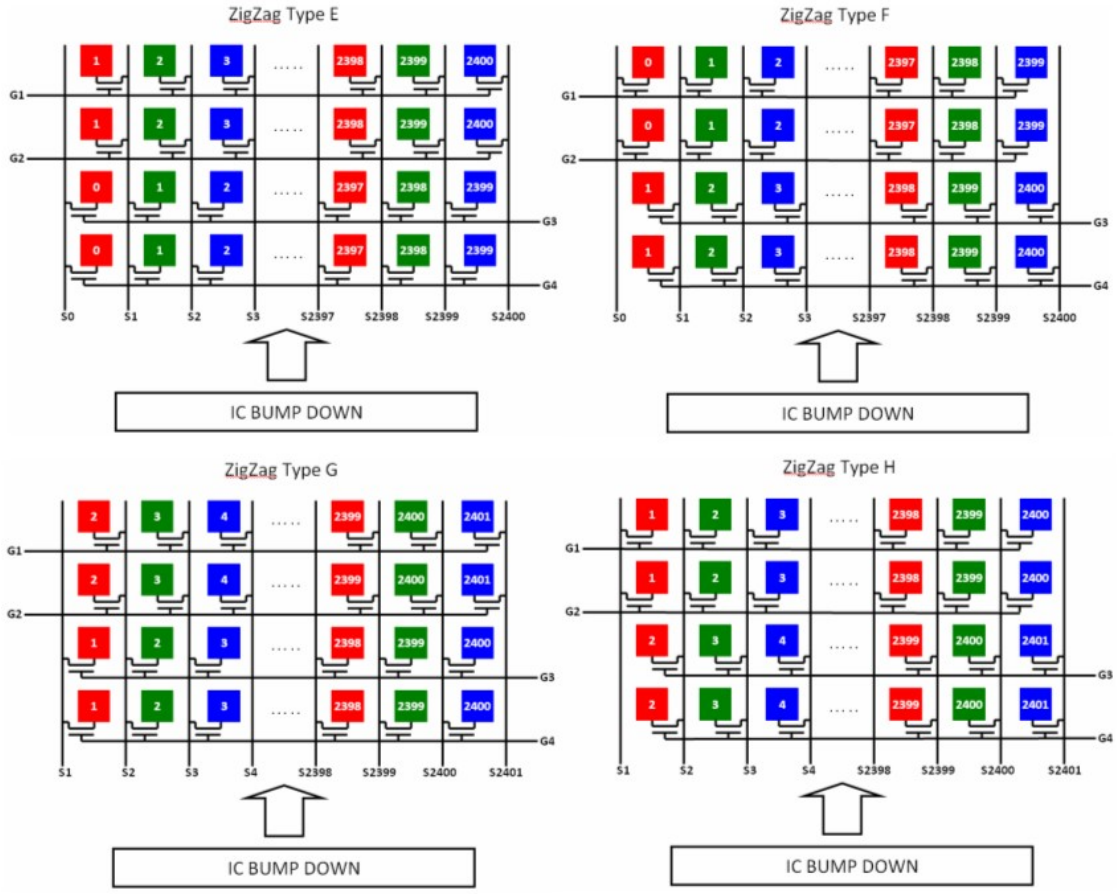


Figure 5.23: Source channels of ZigZag inversion mode

5.3 Gamma function

The SC7705 offers two kinds of Gamma adjustment ways to come to accord with LC characteristic, one kind is through Source Driver directly, another one is adjusted by the digital gamma correction. The adjustment of digital gamma is selected by internal register DGC_EN bit.

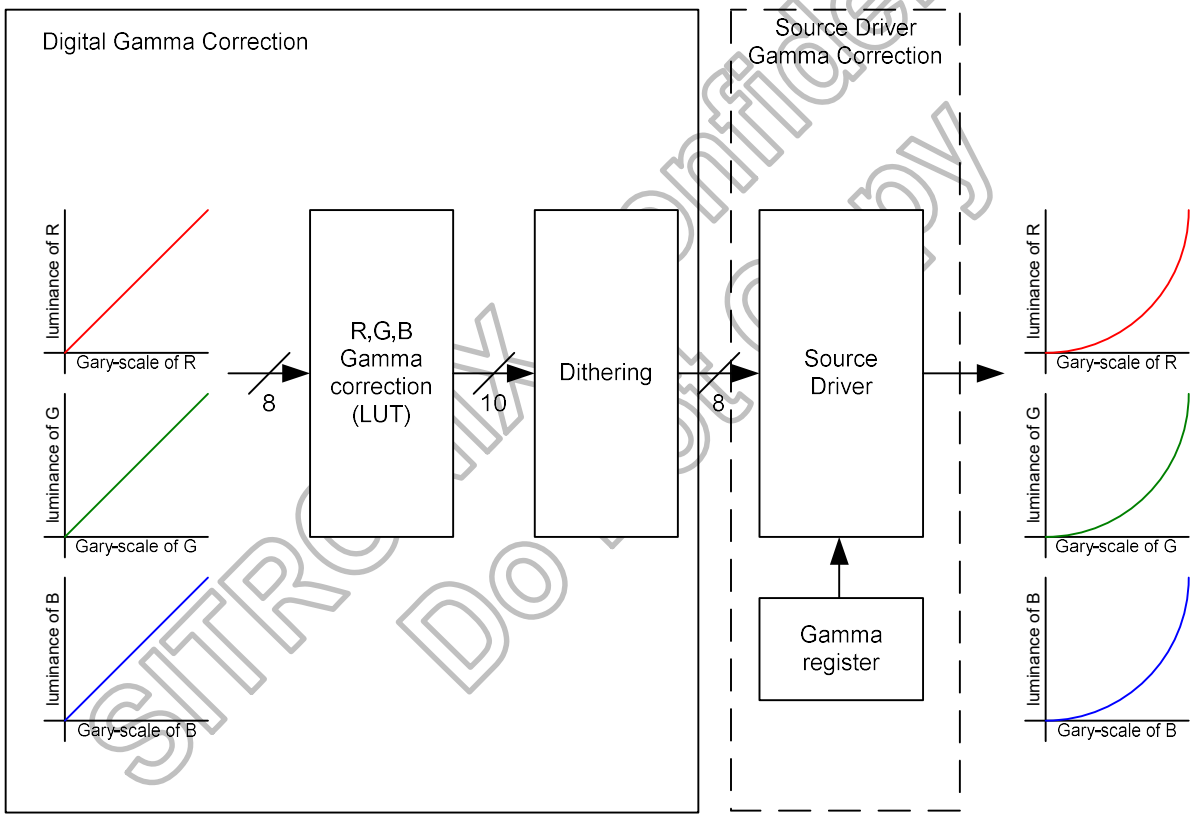
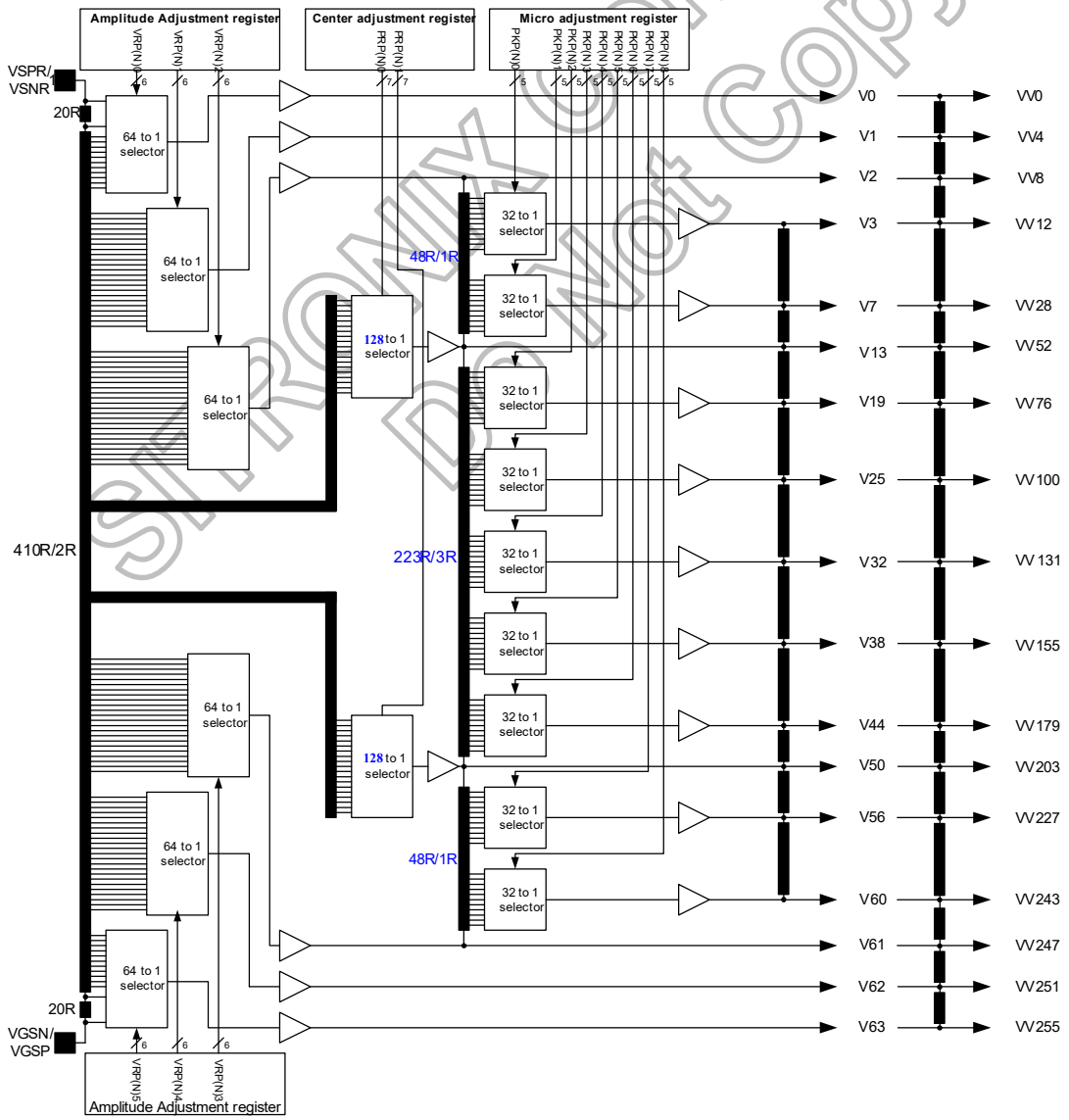


Figure 5.24: Gamma adjustments different of source driver with digital gamma correction

5.3.1 Gamma characteristic correction function

The SC7705 incorporates gamma adjustment function for the 16.7m-color display. Gamma adjustment operation is implemented by deciding the 17 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available both for positive polarities and negative polarities.

The block consists of two gamma resister streams one is for positive polarity and the other is for negative polarity, each one including 17 gamma reference voltages. VgP/N (0, 4, 8, 12, 28, 52, 76, 100, 131, 155, 179, 203, 227, 273, 247, 251, 255).



5.3.2 Gray voltage generator for digital gamma correction

The SC7705 digital gamma correction can reach the independent GAMMA curve of RGB. The SC7705 utilizes DGC_LUT (Digital Gamma Correction Look Up Table) to change input data from 8-bit into 10-bit and sends 10-bit data to Dithering circuit, and then drive Source Driver via Dithering circuit. The following of the block diagram of the function.

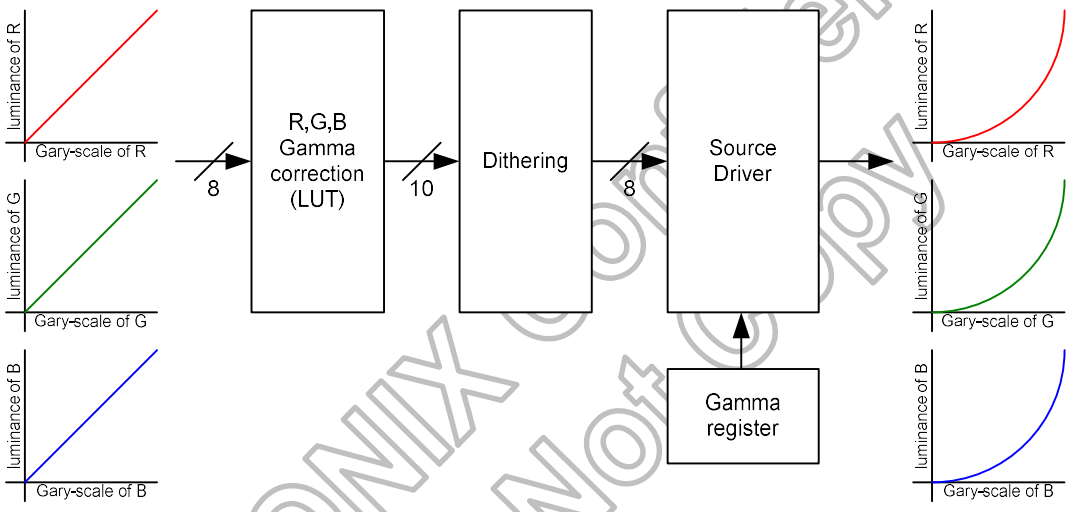


Figure 5.25: Block diagram of digital gamma correction

There are 99 bytes DGC LUT to set R, G, B gamma independently. When DGC_EN=1, R, G, B gamma will mapping V0, V8, V16, ..., V240, V248, V255 voltage to the LUT register setting gray level voltage.

CDh	DGC_R								
Parameter	D7	D6	D5	D4	D3	D2	D1	D0	Default
1st	x	x	x	x	x	DITH_EN	DITH_OPT	DGC_EN	04
2nd	DGC_LUT_R00	DGC_LUT_R00	DGC_LUT_R00	DGC_LUT_R00	DGC_LUT_R00	DGC_LUT_R00	DGC_LUT_R00	DGC_LUT_R00	80
3rd	DGC_LUT_R01	DGC_LUT_R01	DGC_LUT_R01	DGC_LUT_R01	DGC_LUT_R01	DGC_LUT_R01	DGC_LUT_R01	DGC_LUT_R01	80
:	:	:	:	:	:	:	:	:	:
33rd	DGC_LUT_R31	DGC_LUT_R31	DGC_LUT_R31	DGC_LUT_R31	DGC_LUT_R31	DGC_LUT_R31	DGC_LUT_R31	DGC_LUT_R31	80
34th	DGC_LUT_R32	DGC_LUT_R32	DGC_LUT_R32	DGC_LUT_R32	DGC_LUT_R32	DGC_LUT_R32	DGC_LUT_R32	DGC_LUT_R32	80

CEh	DGC_G								
Parameter	D7	D6	D5	D4	D3	D2	D1	D0	Default
1st	DGC_LUT_G00	DGC_LUT_G00	DGC_LUT_G00	DGC_LUT_G00	DGC_LUT_G00	DGC_LUT_G00	DGC_LUT_G00	DGC_LUT_G00	80
2nd	DGC_LUT_G01	DGC_LUT_G01	DGC_LUT_G01	DGC_LUT_G01	DGC_LUT_G01	DGC_LUT_G01	DGC_LUT_G01	DGC_LUT_G01	80
:	:	:	:	:	:	:	:	:	:
32rd	DGC_LUT_G31	DGC_LUT_G31	DGC_LUT_G31	DGC_LUT_G31	DGC_LUT_G31	DGC_LUT_G31	DGC_LUT_G31	DGC_LUT_G31	80
33th	DGC_LUT_G32	DGC_LUT_G32	DGC_LUT_G32	DGC_LUT_G32	DGC_LUT_G32	DGC_LUT_G32	DGC_LUT_G32	DGC_LUT_G32	80

CFh	DGC_B								
Parameter	D7	D6	D5	D4	D3	D2	D1	D0	Default
1st	DGC_LUT_B00	DGC_LUT_B00	DGC_LUT_B00	DGC_LUT_B00	DGC_LUT_B00	DGC_LUT_B00	DGC_LUT_B00	DGC_LUT_B00	80
2nd	DGC_LUT_B01	DGC_LUT_B01	DGC_LUT_B01	DGC_LUT_B01	DGC_LUT_B01	DGC_LUT_B01	DGC_LUT_B01	DGC_LUT_B01	80
:	:	:	:	:	:	:	:	:	:
32rd	DGC_LUT_B31	DGC_LUT_B31	DGC_LUT_B31	DGC_LUT_B31	DGC_LUT_B31	DGC_LUT_B31	DGC_LUT_B31	DGC_LUT_B31	80
33th	DGC_LUT_B32	DGC_LUT_B32	DGC_LUT_B32	DGC_LUT_B32	DGC_LUT_B32	DGC_LUT_B32	DGC_LUT_B32	DGC_LUT_B32	80

5.4 Sleep Out –command and self-diagnostic functions of the display module

5.4.1 Register loading detection

Sleep Out-command (11h) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (or similar device) to registers of the display controller is working properly. There are compared factory values of the OTP and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (=increased by 1).

The flow chart for this internal function is following:

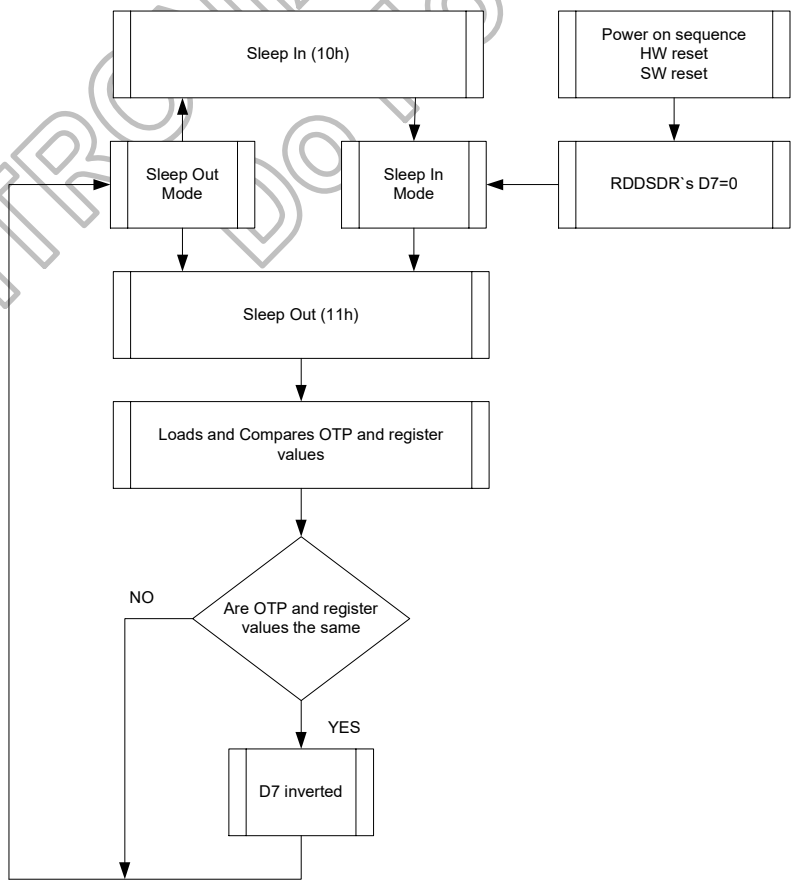


Figure 5.26: Sleep out flow chart–command and self-diagnostic functions

5.4.2 Functionality detection

Sleep Out-command (11h) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function is comparing, if the display module still meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, 1 bit will be inverted (=increased by 1), which is defined in command "Read Display Self- Diagnostic Result (0Fh)" (=RDDSDR) (The used bit of this command is D6). If functionality requirement is not the same, this bit (D6) is not inverted (=increased by 1). The flow chart for this internal function is shown as below.

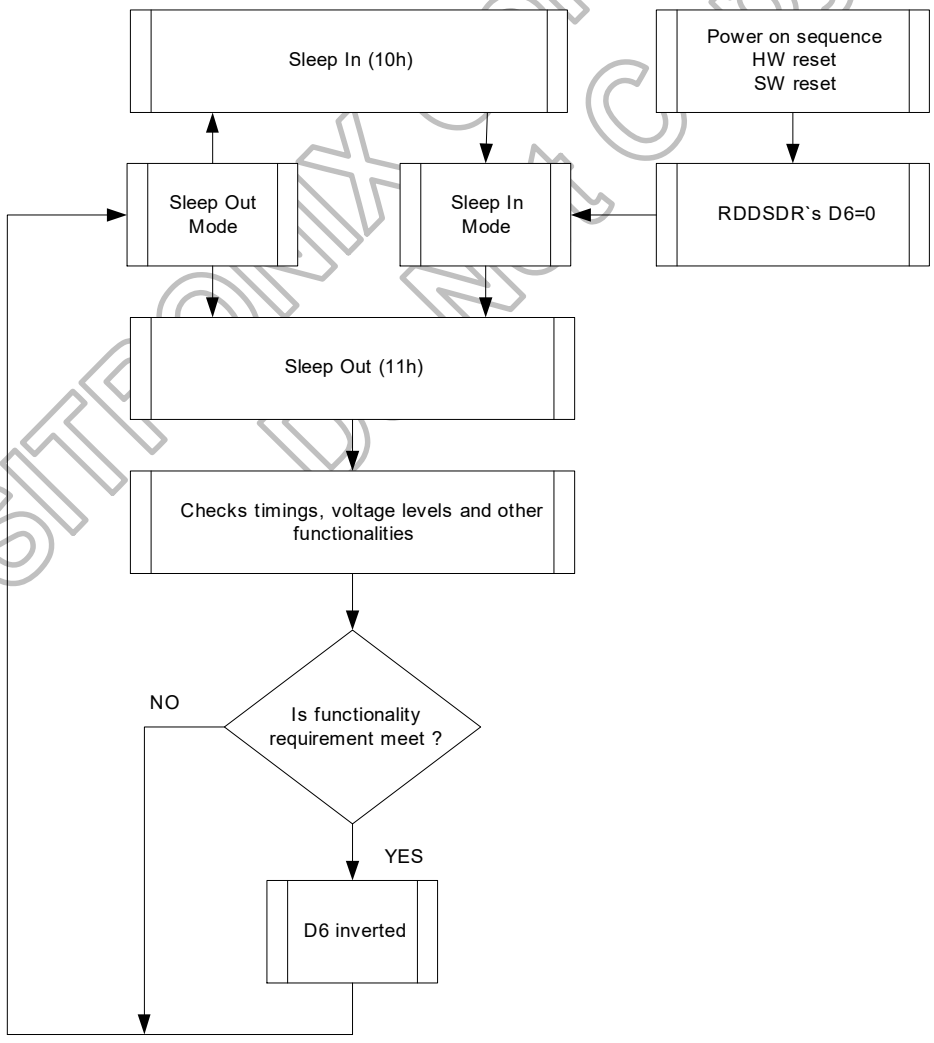


Figure 5.27: Sleep out flow chart internal function detection

5.5 Power on/off sequence

Power source IOVCC, VCI can be applied and powered down in any order. IOVCC, VCI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, IOVCC, VCI must be powered down minimum 120msec after NRESET has been released.

During power off, if LCD is in the Sleep In mode, IOVCC, VCI can be powered down minimum 0msec after NRESET has been released.

NCS can be applied at any timing or can be permanently grounded. NRESET has priority over NCS.

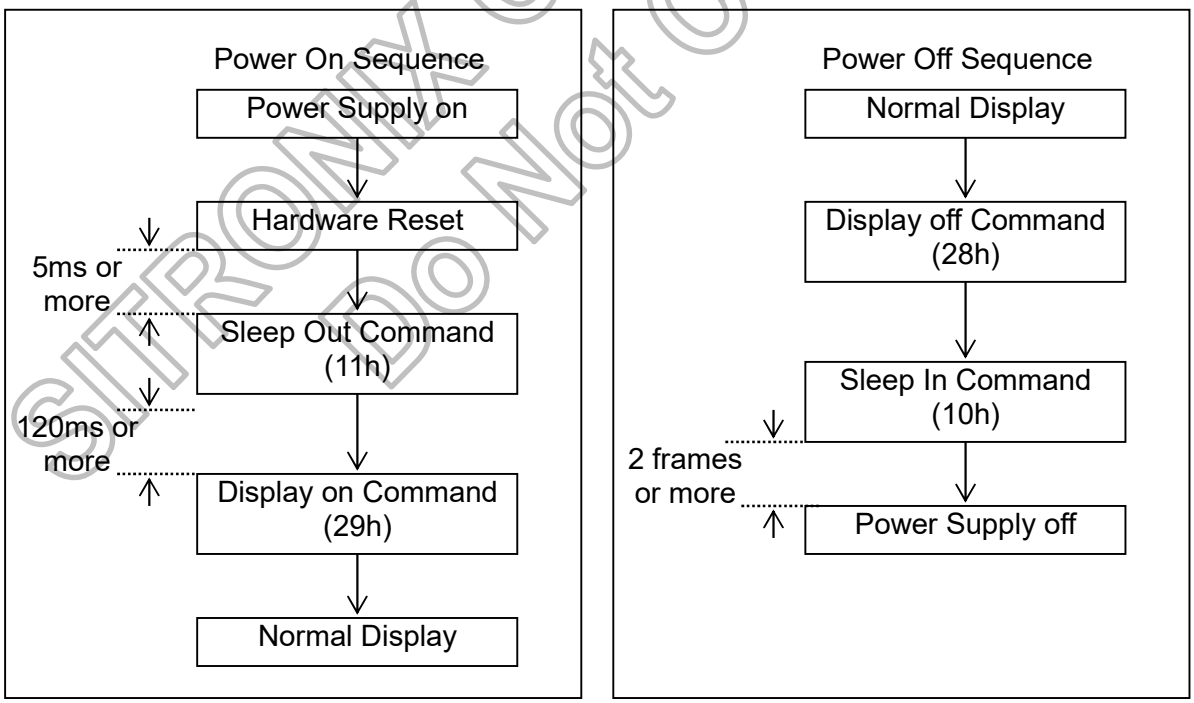


Figure 5.28: The power supply ON/OFF setting for Display ON/OFF and Sleep In/out

5.5.1 Case 1: RESX line is held high or unstable by host at power on

If RESX line is held high or unstable by the host during power on, then a Hardware Reset must be applied after both VDD1, VDD2 and VDD3 have been applied- otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

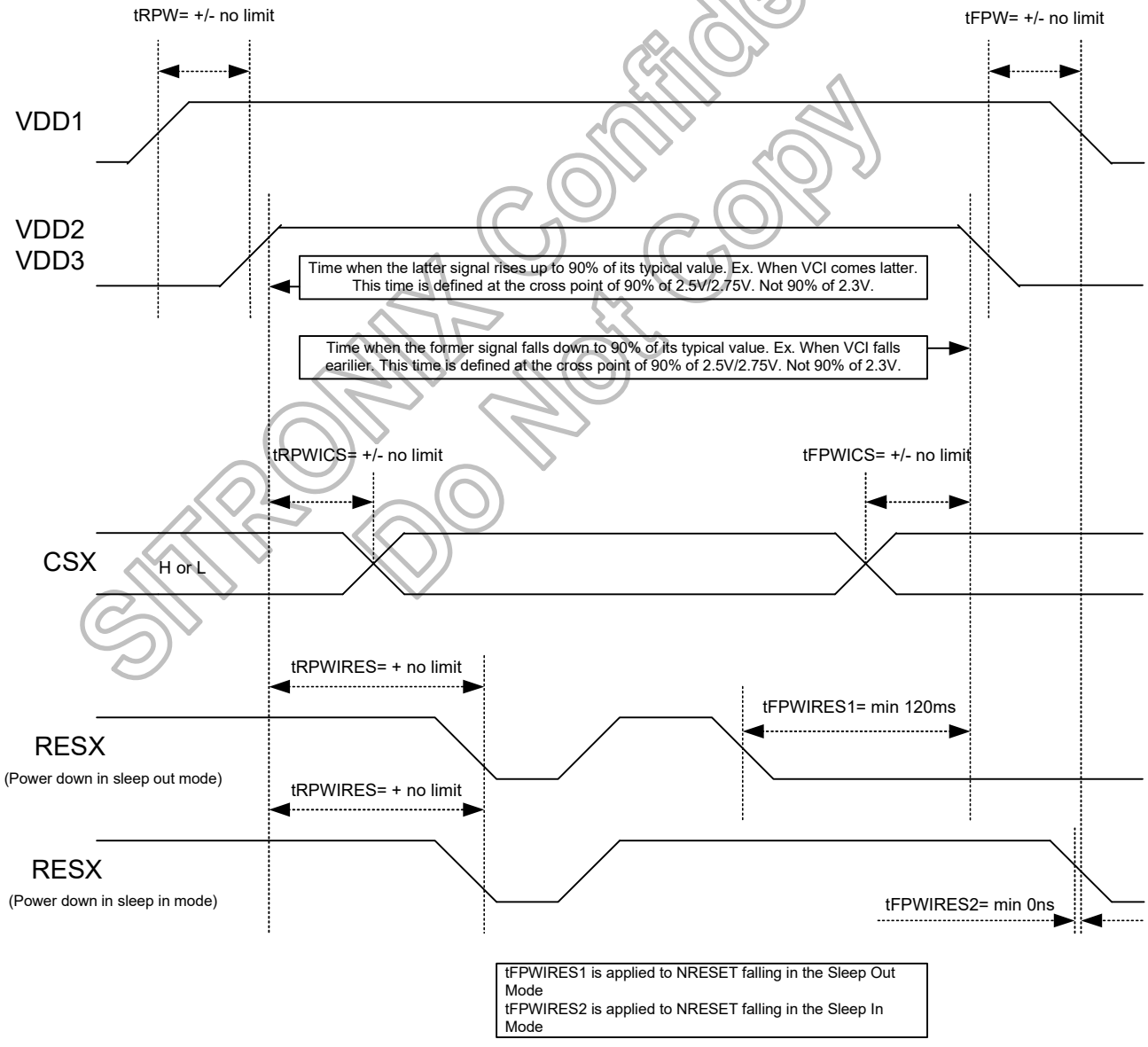
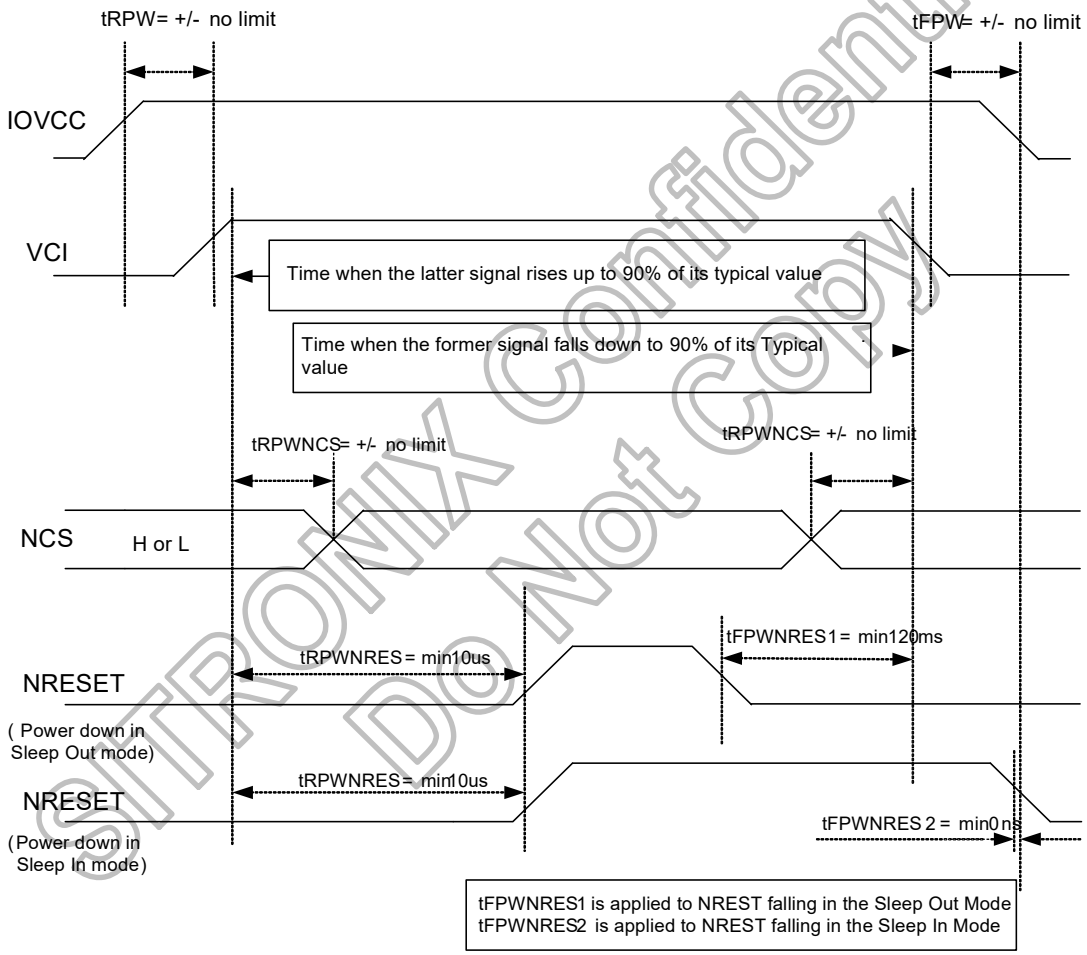


Figure 5.29: Case 1: RESX line is held high or unstable by host at power on

5.5.2 Case 2: RESX line is held low by host at power on

If RESX line is held low (and stable) by the host during power on, then the RESX must be held low for minimum 10µsec after both VDD1, VDD2 and VDD3 have been applied.



Note: Unless otherwise specified timings herein show cross point at 50% of signal/power level

Figure 5.30: Case 2: RESX line is held low by host at power on

5.6 Power levels definition

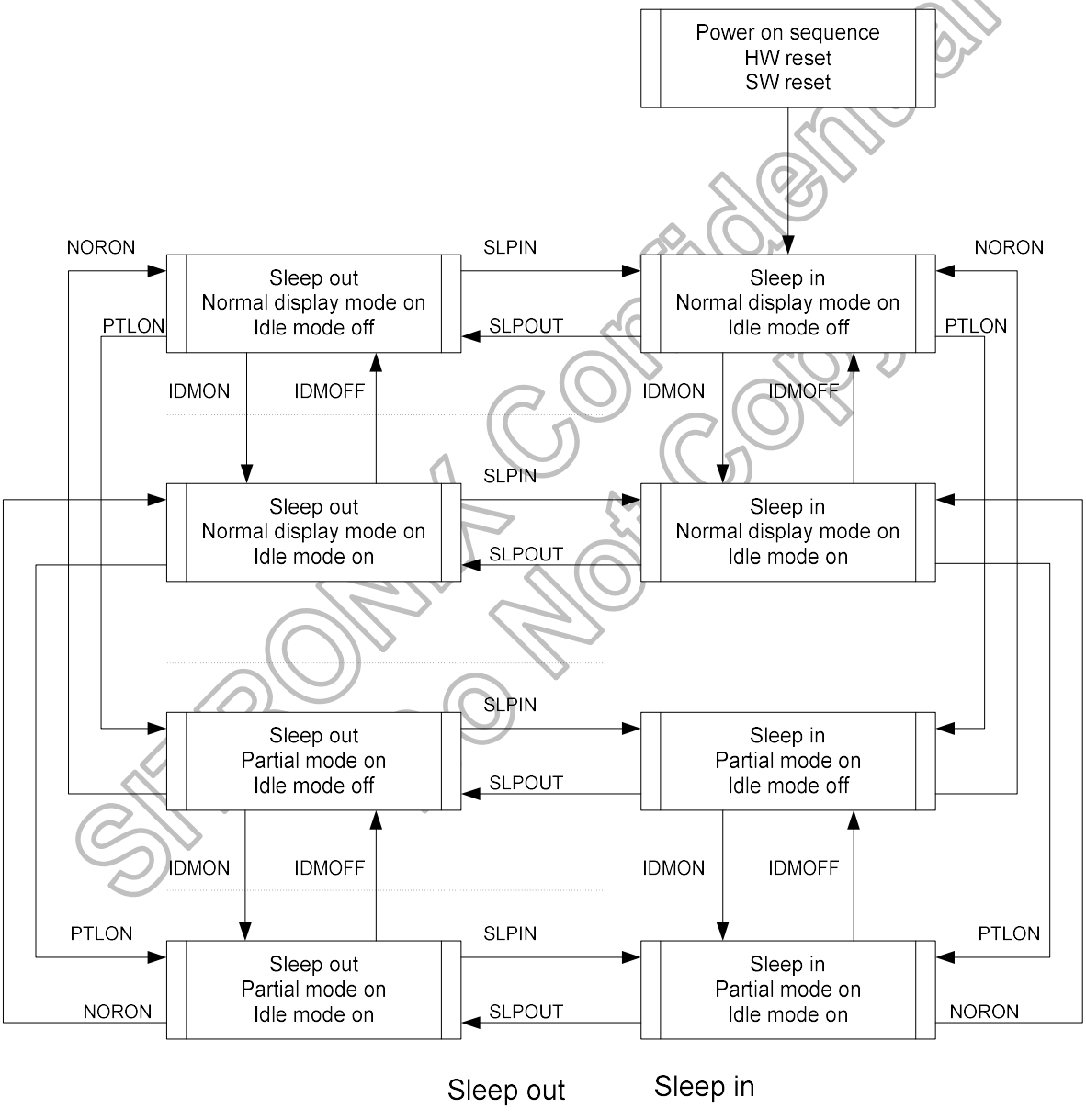


Figure 5.31: Power flow chart for different power modes

5.7 Reset function

5.7.1 Standard Command default value

Item	Register		After Power On	After Hardware Reset	After Software Reset
RDNUMPE	05h		00h	00h	00h
RDDPM	0Ah		08h	08h	08h
RDDMADCTR	0Bh		00h	00h	No Change
RDDCOLMOD	0Ch		70h	70h	No Change
RDDIM	0Dh		00h	00h	00h
RDDSM	0Eh		00h	00h	00h
RDDSDR	0Fh		00h	00h	00h
Sleep In/Out	10h/ 11h		In	In	In
Display On/Off	29h/ 28h		Off	Off	Off
Display mode (normal/partial)	13h/ 12h		Normal	Normal	Normal
Display Inversion On/Off	21h/ 20h		Off	Off	Off
All pixel On/Off	23/ 22h		Off	Off	Off
Display Idle Mode On/Off	39/ 38h		Off	Off	Off
Gamma setting	26H		GC0	GC0	GC0
Memory Data Access Control (MY/MX/RGB)	36H		0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	3AH		70h	70h	No Change
Display Brightness	51h/ 52h		00h	00h	00h
CTRL Display	53h/ 54h		00h	00h	00h
CABC Control	55h/ 56h		00h	00h	00h
ID1	DAH	NO OTP	48h	48h	48h
		OTPed	OTP Value	OTP Value	OTP Value
ID2	DBH	NO OTP	21h	21h	21h
		OTPed	OTP Value	OTP Value	OTP Value
ID3	DCH	NO OTP	1Fh	1Fh	1Fh
		OTPed	OTP Value	OTP Value	OTP Value

Table 5.7: Standard Command default value

5.7.2 Input Pins

Input pins	After Power On	After Hardware Reset	After Software Reset
RESX	Input valid	Input valid	Input valid
HS_DSI_D0P HS_DSI_D0P	Input valid	Input valid	Input valid
HS_DSI_D1P HS_DSI_D1P	Input valid	Input valid	Input valid
HS_DSI_D2P HS_DSI_D2P	Input valid	Input valid	Input valid
HS_DSI_D3P HS_DSI_D3N	Input valid	Input valid	Input valid
HS_DSI_CP HS_DSI_CN	Input valid	Input valid	Input valid

Table 5.8: Characteristics of input pins

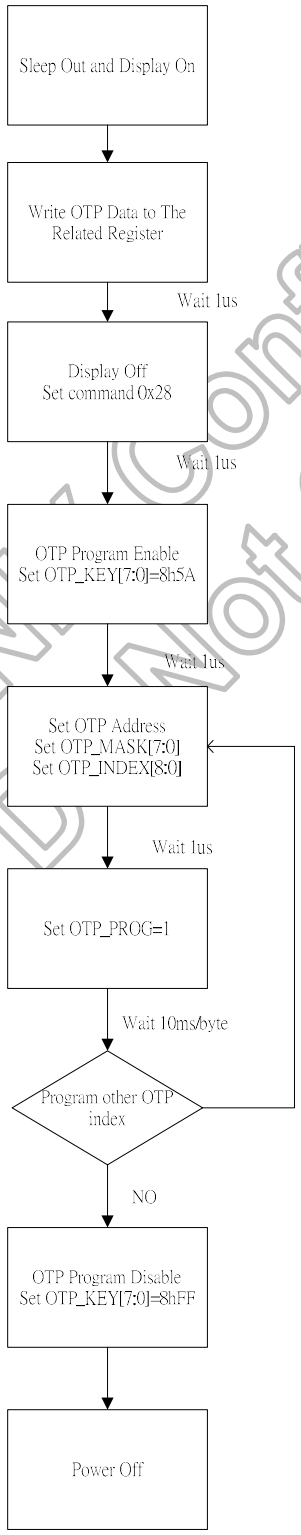
5.7.3 Output or Bi-directional Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
Source Output	VSSA	VSSA	VSSA
DSI_D0P DSI_D0P	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
CGOUTL1~22	VSSA	VSSA	VSSA
CGOUTR1~22	VSSA	VSSA	VSSA

Table 5.9: Characteristics of output or bi-direction pins

5.8 OTP Sequence

5.8.1 OTP Sequence



5.8.2 OTP Standard Programming Table

Programming Index (Hex)	D7	D6	D5	D4	D3	D2	D1	D0	Storage Index (Hex)
01	ID1_1[7:0]								01
	ID2_1[7:0]								02
	ID3_1[7:0]								03
	ID1_2[7:0]								04
	ID2_2[7:0]								05
	ID3_2[7:0]								06
	ID1_3[7:0]								07
	ID2_3[7:0]								08
	ID3_3[7:0]								09
	ID1_4[7:0]								0A
	ID2_4[7:0]								0B
	ID3_4[7:0]								0C
0D	VCOM_F1[7:0]								0D
	VCOM_B1[7:0]								0E
	VCOM_F2[7:0]								0F
	VCOM_B2[7:0]								10
	VCOM_F3[7:0]								11
	VCOM_B3[7:0]								12
	VCOM_F4[7:0]								13
	VCOM_B4[7:0]								14

5.9 CABC

This driver IC provides a dynamic backlight control function as CABC (Content adaptive brightness control) to reduce the power consumption of the luminance source. There are two module architectures for CABC operation as below figure.

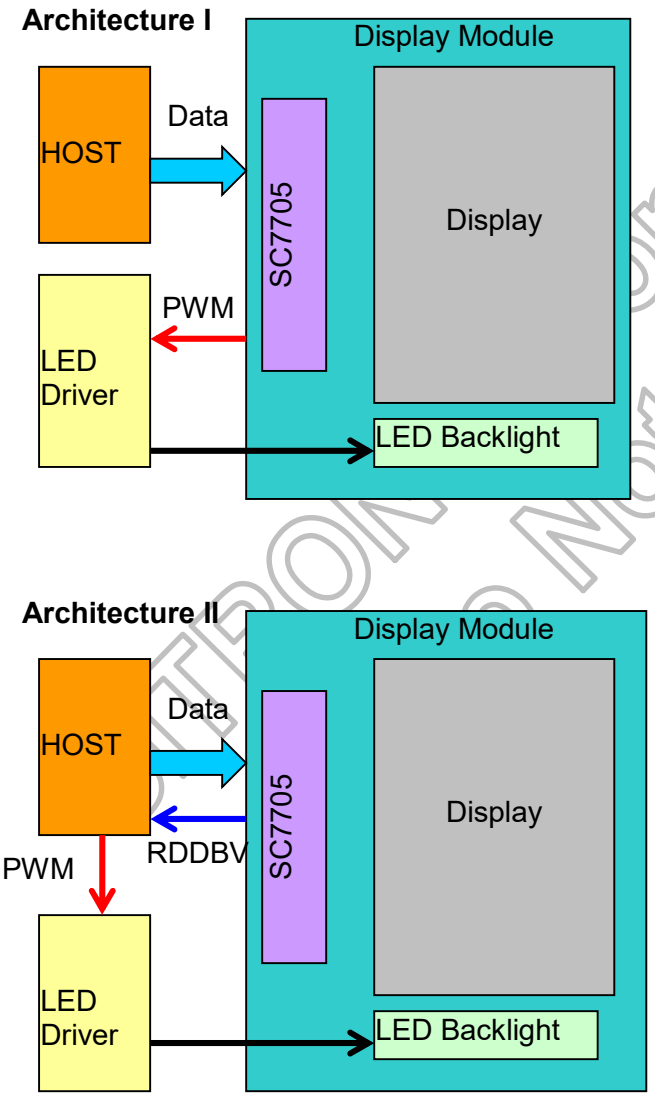
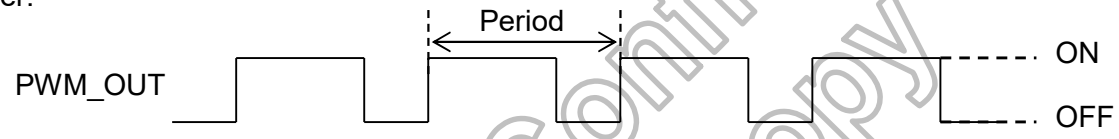


Figure 5.32: Two kinds of CABC Architecture

The driver IC will refer the gray scale content of display image to output a PWM waveform to LED driver for backlight brightness control. The PWM frequency can be adjusted by PWM_DIV parameters and the calculating equation as below:

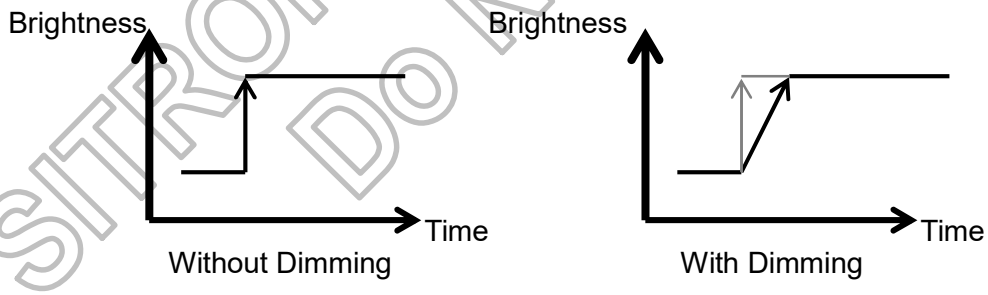
$$Fpwm\_out = \frac{36MHz}{(PWM\_PERIOD[7:0]+1)x255}$$

The figure in the following is the basic timing diagram which is applied SC7705 to control LED driver.



Display Backlight Dimming Control

A dimming function is used when changing from brightness level to another. This dimming function curve is the same in increment and decrement directions. Dimming function can be enabled and disabled by software register. The basic idea is described below.



6. Command Description

6.1 Command Table

Standard Command

(Hex)	Operation Code	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)
00h	NOP	W	0	0	0	0	0	0	0	0	No Operation	-
01h	SWRESET	W	0	0	0	0	0	0	0	1	Software Reset	-
04h	RDDIDIF	R	0	0	0	0	0	1	0	0	Read Display ID	-
			-	-	-	-	-	-	-	-	Dummy Read	-
			ID1[7:0]								ID1	48h
			ID2[7:0]								ID2	21h
			ID3[7:0]								ID3	1Fh
05h	RDNUMPE	R	0	0	0	0	0	1	0	1	Read Number of the Errors on DSI	-
			-	-	-	-	-	-	-	-	Dummy Read	-
			P[7:0]								-	00h
06h	RDRED	R	0	0	0	0	0	1	1	0	Read Red Color	-
			-	-	-	-	-	-	-	-	Dummy Read	-
			R7	R6	R5	R4	R3	R2	R1	R0	-	00h
07h	RDGREEN	R	0	0	0	0	0	1	1	1	Read Green Color	-
			-	-	-	-	-	-	-	-	Dummy read	-
			G7	G6	G5	G4	G3	G2	G1	G0	-	00h
08h	RDBLUE	R	0	0	0	0	1	0	0	0	Read Blue Color	-
			-	-	-	-	-	-	-	-	Dummy Read	-
			B7	B6	B5	B4	B3	B2	B1	B0	-	00h
0Ah	RDDPM	R	0	0	0	0	1	0	1	0	Read display power mode	-
			-	-	-	-	-	-	-	-	Dummy Read	-
			D7	D6	D5	D4	D3	D2	0	0	-	08h
0Bh	RDDMADCTL	R	0	0	0	0	1	0	1	1	Read display MADCTL	-
			-	-	-	-	-	-	-	-	Dummy Read	-
			D7	D6	D5	D4	D3	D2	0	0	-	00h
0Ch	RDDCOLMOD	R	0	0	0	0	1	1	0	0	Read display pixel format	-
			-	-	-	-	-	-	-	-	Dummy Read	-
			-	D6	D5	D4	-	-	-	-	-	70h
0Dh	RDDIM	R	0	0	0	0	1	1	0	1	Read display image mode	-
			-	-	-	-	-	-	-	-	Dummy Read	-
			D7	D6	D5	0	0	D2	D1	D0	-	00h
0Eh	RDDSM	R	0	0	0	0	1	1	1	0	Read display signal mode	-
			-	-	-	-	-	-	-	-	Dummy Read	-
			D7	D6	0	0	0	0	0	D0	-	00h
0Fh	RDDSDR	R	0	0	0	0	1	1	1	1	Read display self-diagnostic result	-
			-	-	-	-	-	-	-	-	Dummy Read	-
			D7	D6	0	0	0	0	0	D0	-	00h
10h	SLPIN	W	0	0	0	1	0	0	0	0	Sleep In	-
11h	SLPOUT	W	0	0	0	1	0	0	0	1	Sleep Out	-

(Hex)	Operation code	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)
13h	NORON	W	0	0	0	1	0	0	1	1	Normal Display Mode	-
20h	INVOFF	W	0	0	1	0	0	0	0	0	Display Inversion Off	-
21h	INVON	W	0	0	1	0	0	0	0	1	Display Inversion On	-
22h	ALLPOFF	W	0	0	1	0	0	0	1	0	All Pixel Off	-
23h	ALLPON	W	0	0	1	0	0	0	1	1	All Pixel On	-
28h	DISPOFF	W	0	0	1	0	1	0	0	0	Display Off	-
29h	DISPON	W	0	0	1	0	1	0	0	1	Display On	-
36h	MADCTL	W	0	0	1	1	0	1	1	0	Memory Access Control	-
			MY	MX	-	-	RGB	-	-	-		00h
38h	IDMOFF	W	0	0	1	1	1	0	0	0	Idle Mode Off	-
39h	IDMON	W	0	0	1	1	1	0	0	1	Idle Mode On	-
3Ah	COLMOD	W	0	0	1	1	1	0	1	0	Interface Pixel Format	-
			x	B6	B5	B4	-	-	-	-		70h
51h	WRDISBV	W	0	1	0	1	0	0	0	1	Write Display Brightness Value	-
			DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		00h
52h	RDRDISBV	R	0	1	0	1	0	0	1	0	Read Display Brightness Value	-
			-	-	-	-	-	-	-	-		-
			DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		00h
53h	WRCTRLD	W	0	1	0	1	0	0	1	1	Write CTRL Display	-
			-	-	BCTRL	-	-	DD	BL	-		00h
54h	RDCTRLD	R	0	1	0	1	0	1	0	0	Read CTRL Display	-
			-	-	-	-	-	-	-	-		-
			-	-	BCTRL	x	x	DD	BL	-		00h
55h	WRCABC	W	0	1	0	1	0	1	0	1	Write CABC Mode	-
			-	-	-	-	-	-	C1	C0		00h
56h	RDCABC	R	0	1	0	1	0	1	1	0	Read CABC Mode	-
			-	-	-	-	-	-	-	-		-
			-	-	-	-	-	-	C1	C0		00h
68h	RDABCSDR	R	0	1	0	1	0	1	1	0	Read ABC Self-Diagnostic Result	-
			-	-	-	-	-	-	-	-		-
			D7	D6	-	-	-	-	-	-		00h
70h	RDBWLB	R	0	1	1	1	0	0	0	0	Read Black/White Low Bits	-
			-	-	-	-	-	-	-	-		-
			Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0		-
71h	RDBkx	R	0	1	1	1	0	0	0	1	Read Bkx	-
			-	-	-	-	-	-	-	-		-
			Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2		-
72h	RDBky	R	0	1	1	1	0	0	1	0	Read Bky	-
			-	-	-	-	-	-	-	-		-
			Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2		-
73h	RDWx	R	0	1	1	1	0	0	1	1	Read Wx	-
			-	-	-	-	-	-	-	-		-
			Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2		-
74h	RDWy	R	0	1	1	1	0	1	0	0	Read Wy	-
			-	-	-	-	-	-	-	-		-
			Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2		-
75h	RDRGLB	R	0	1	1	1	0	1	0	1	Read Red/Green Low Bits	-
			-	-	-	-	-	-	-	-		-
			Rx1	Rx0	Ry1	Rx0	Gx1	Gx0	Gy1	Gy0		-
76h	RDRx	R	0	1	1	1	0	1	1	0	Read Rx	-
			-	-	-	-	-	-	-	-		-
			Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2		-

(Hex)	Operation code	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)
77h	RDRy	R	0	1	1	1	0	1	1	1	Read Ry	-
			-	-	-	-	-	-	-	-		-
			Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2		-
78h	RDGx	R	0	1	1	1	1	0	0	0	Read Gx	-
			-	-	-	-	-	-	-	-		-
			Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2		-
79h	RDRy	R	0	1	1	1	1	0	0	1	Read Gy	-
			-	-	-	-	-	-	-	-		-
			Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2		-
7Ah	RDBALB	R	0	1	1	1	1	0	1	0	Read Biue/AColour Low Bits	-
			-	-	-	-	-	-	-	-		-
			Bx1	Bx0	By1	Bx0	Ax1	Ax0	Ay1	Ay0		-
7Bh	RDBx	R	0	1	1	1	1	0	1	1	Read Bx	-
			-	-	-	-	-	-	-	-		-
			Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2		-
7Ch	RDBy	R	0	1	1	1	1	1	0	0	Read By	-
			-	-	-	-	-	-	-	-		-
			By9	By8	By7	By6	By5	By4	By3	By2		-
7Dh	RDAx	R	0	1	1	1	1	1	0	1	Read Ax	-
			-	-	-	-	-	-	-	-		-
			Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2		-
7Eh	RDAy	R	0	1	1	1	1	1	1	0	Read Ay	-
			-	-	-	-	-	-	-	-		-
			Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	Ay3	Ay2		-
A1h	Read_DDB_start	R	1	0	1	0	0	0	0	1	Read the DDB from the provided location.	-
			-	-	-	-	-	-	-	-		-
			-	-	-	-	-	-	-	-		00h
			-	-	-	-	-	-	-	-		00h
			-	-	-	-	-	-	-	-		00h
			-	-	-	-	-	-	-	-		00h
			1	1	1	1	1	1	1	1		FFh
A8h	Read_DDB_continue	R	1	0	1	0	1	0	0	0	Continue reading the DDB from the last read location.	-
			-	-	-	-	-	-	-	-		00h
			-	-	-	-	-	-	-	-		00h
			-	-	-	-	-	-	-	-		00h
			-	-	-	-	-	-	-	-		00h
AAh	RDFCS	R	1	0	1	0	1	1	0	0	Read First Checksum	
			-	-	-	-	-	-	-	-		00h
			FCS[7:0]									00h
AFh	RDCCS	R	1	0	1	0	1	1	0	0	Read Continue Checksum	
			-	-	-	-	-	-	-	-		00h
			CCS[7:0]									00h
DAh	RDID1	R	1	1	0	1	1	0	1	0	Read ID1	-
			-	-	-	-	-	-	-	-		-
			module's manufacturer[7:0]									48h
DBh	RDID2	R	1	1	0	1	1	0	1	1	Read ID2	-
			-	-	-	-	-	-	-	-		-
			LCD module/driver version [7:0]									21h
DCh	RDID3	R	1	1	0	1	1	1	0	0	Read ID3	-
			-	-	-	-	-	-	-	-		-
			LCD module/driver ID[7:0]									1Fh

6.2 Command Description

6.2.1 NOP (00h)

<table>
<tr><td>00 H</td><td colspan="10">NOP (No Operation)</td></tr>
<tr><td></td><td>R/W</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Parameter</td><td colspan="10">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="10">This command is an empty command; it does not have any effect on the display module.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Booster Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10">-</td></tr>
</table>

6.2.2 Software reset (01h)

01 H	SWRESET (Software Reset)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	0	0	0	1	01
Parameter	NO PARAMETER									
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) The display is blank immediately.									
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5m sec. If SW Reset is applied during Sleep Out mode, it will be necessary to wait 120m sec before sending Sleep Out command. SW Reset command cannot be sent during Sleep Out sequence.									

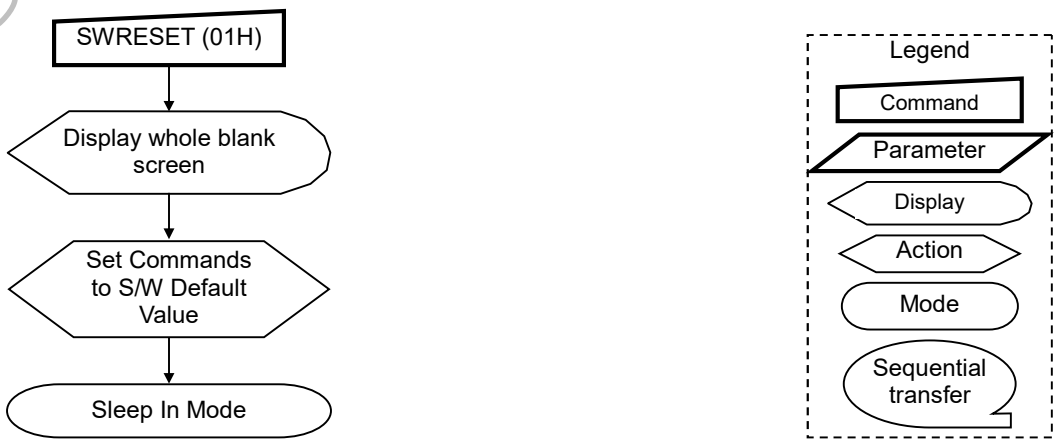
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



6.2.3 Read Display ID (04h)

04 H	RDDID (Read Display ID)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	0	1	0	0	04
Dummy Clock Cycle										
1st parameter	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	48
2nd parameter	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	21
3rd parameter	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	1F
Description	This read byte returns 24-bit display identification information.									
Restriction	-									

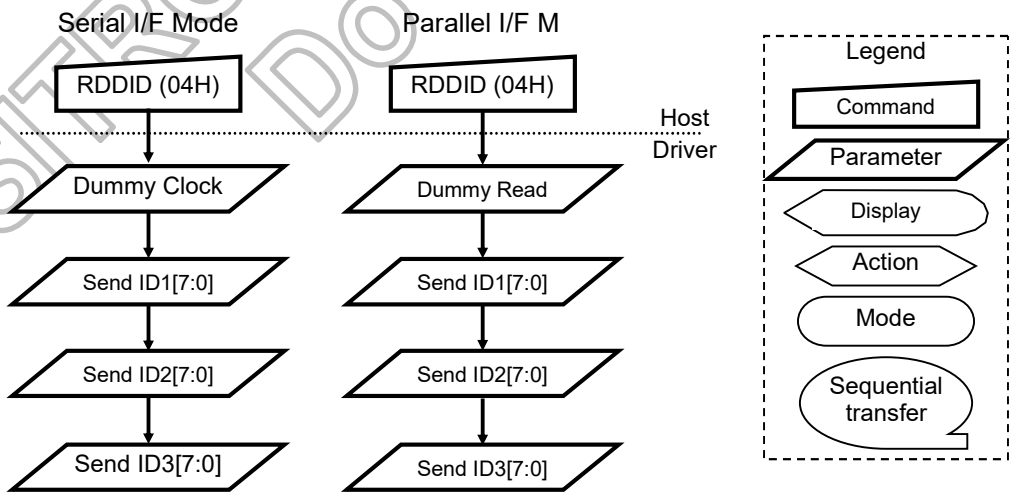
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	48,21,1F
S/W Reset	48,21,1F
H/W Reset	48,21,1F

Flow Chart



6.2.4 Read Number of the Errors on DSI (05h)

05 H	RDNUMPE (Read Number of the Errors on DSI)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	0	1	0	1	05
1st parameter	-	P7	P6	P5	P4	P3	P2	P1	P0	-
Description	The first parameter is telling a number of the errors on DSI.									
Restriction	-									

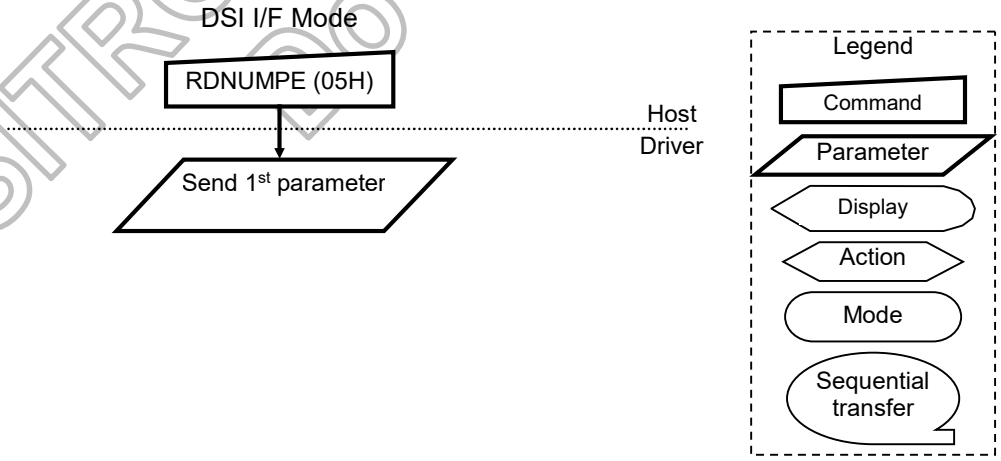
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.5 Read Red Color (06h)

06 H	RDRED (Read Red Color)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	0	1	1	0	06
1st parameter	-	R7	R6	R5	R4	R3	R2	R1	R0	-
Description	The first parameter is telling red color value of the first pixel of the frame when there is used in RGB I/F. 16 bit format: R5 is MSB and R1 is LSB. R7, R6 and R0 are set to '0'. 18 bit format: R5 is MSB and R0 is LSB. R7 and R6 are set to '0' 24 bit format: R7 is MSD and R0 is LSB									
Restriction	-									

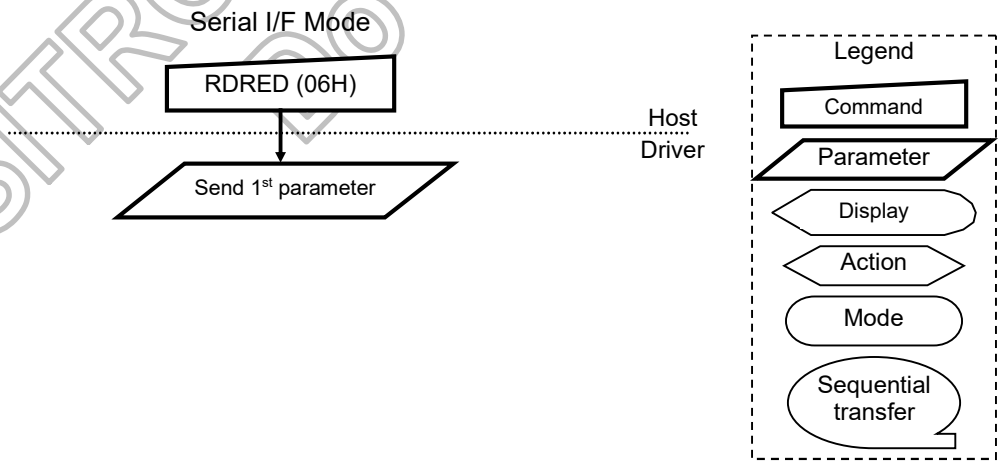
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.6 Read Green Color (07h)

07 H	RDGREEN (Read Green Color)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	0	1	1	1	07
1st parameter	-	G7	G6	G5	G4	G3	G2	G1	G0	-
Description	The first parameter is telling red color value of the first pixel of the frame when there is used in RGB I/F. 16 bit format: G5 is MSB and G0 is LSB. G7 and R6 are set to '0'. 18 bit format: G5 is MSB and G0 is LSB. G7 and R6 are set to '0' 24 bit format: G7 is MSD and G0 is LSB									
Restriction	-									

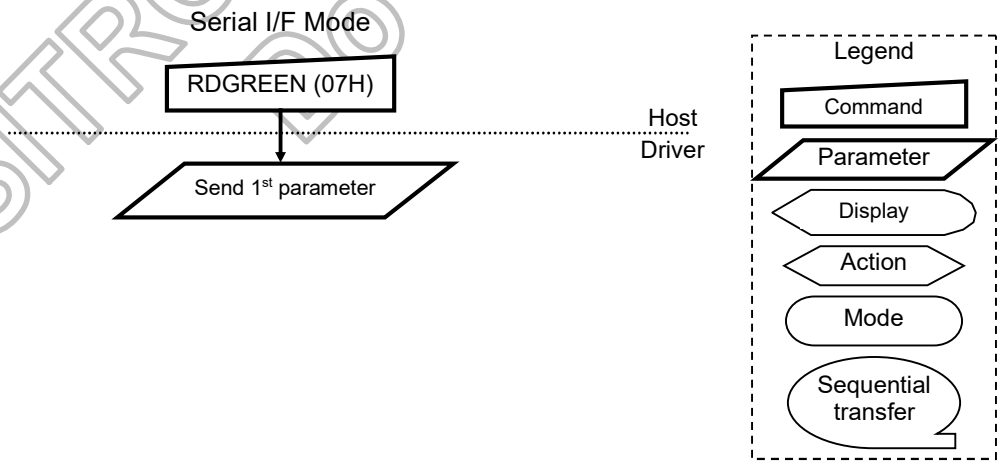
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.7 Read Blue Color (08h)

08 H	RDBLUE (Read Blue Color)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	1	0	0	0	08
1st parameter	-	B7	B6	B5	B4	B3	B2	B1	B0	-
Description	The first parameter is telling red color value of the first pixel of the frame when there is used in RGB I/F. 16 bit format: B5 is MSB and B1 is LSB. B7, B6 and B0 are set to '0'. 18 bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to '0' 24 bit format: B7 is MSD and B0 is LSB									
Restriction	-									

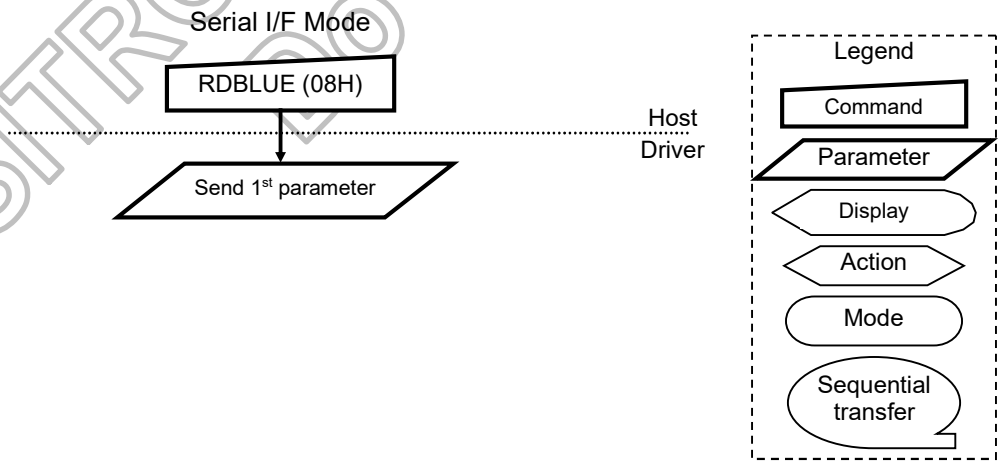
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.8 Read Display Power Mode (0Ah)

0A H	RDDPM (Read Display Power Mode)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	1	0	1	0	0A
	Dummy Clock Cycle									
1st parameter	-	D7	D6	D5	D4	D3	D2	0	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Booster Voltage Status	'1'=Booster on, '0'=Booster off
D6	Idle Mode On/Off	'1'=Idle Mode on, '0'=Idle Mode off
D5	Partial Mode On/Off	'1'=Partial Mode on, '0'= Partial Mode off
D4	Sleep In/Out	'1'=Sleep out , '0'=Sleep in
D3	Display Normal Mode On/Off	'1'=Display Normal on, '0'=Display Normal off
D2	Display On/Off	'1'=Display on, '0'=Display off
D1	Not Defined	Set to '0'
D0	Not Defined	Set to '0'

Restriction

-

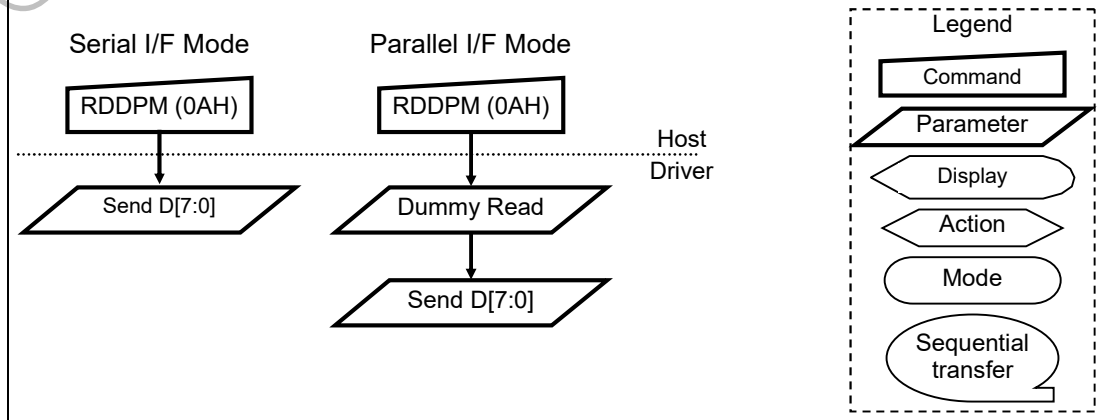
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

Flow Chart



6.2.9 Read Display MADCTR (0Bh)

0B H	RDDMADCTR (Read Display MADCTR)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	1	0	1	1	0B
Dummy Clock Cycle										
1st parameter	-	D7	D6	0	0	D3	D2	0	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Page Address Order (MY)	'0'=Increment, '1' = Decrement
D6	Column Address Order (MX)	'0'=Increment, '1' = Decrement
D5	Page/Column Exchange (MV)	Set to '0'
D4	Line Address Order (ML)	Set to '0'
D3	RGB/BGR Order	'0'=Increment, '1' = Decrement
D2	Display Data Latch Order (MH)	'0'=Increment, '1' = Decrement
D1	Flip horizontal	Set to '0'
D0	Flip vertical	Set to '0'

Restriction

-

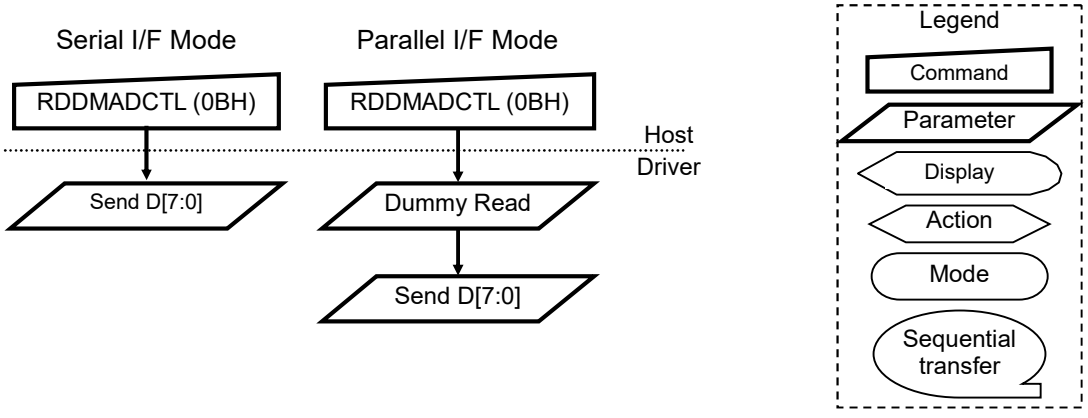
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.10 Read Display Pixel Format (0Ch)

0C H	RDDCOLMOD (Read Display COLMOD)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	1	1	0	0	0C
Dummy Clock Cycle										
1st parameter	-	D7	D6	0	0	D3	D2	0	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Reserved	Set to '0'
D6	RGB Interface Pixel format	'101' =16-bit/pixel
D5		'110' =18-bit/pixel
D4		'111' =24-bit/pixel
D3	Reserved	Set to '0'
D2	DBI Interface Pixel format	Set to '0'
D1		Set to '0'
D0		Set to '0'

Restriction

-

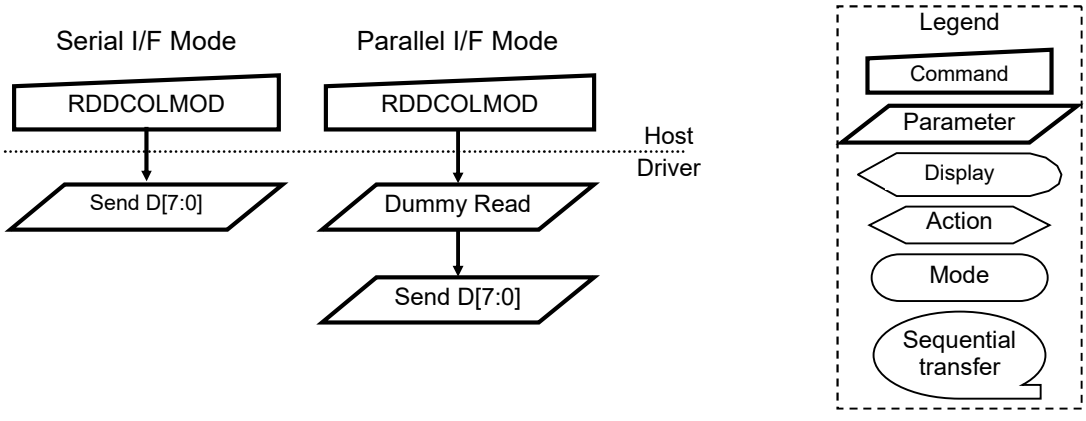
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	70h
S/W Reset	No Change
H/W Reset	70h

Flow Chart



6.2.11 Read Display Image Mode (0Dh)

0D H	RDDIM (Read Display Image Mode)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	1	1	0	1	0D
Dummy Clock Cycle										
1st parameter	-	D7	D6	0	0	D3	D2	0	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Vertical Scrolling On/Off	Set to '0'
D6	Horizontal Scrolling On/off	Set to '0'
D5	Inversion On/off	'1'= Inversion On, '0' = Inversion Off
D4	All Pixel On	'1'= White display, '0' = Normal display
D3	All Pixel Off	'1'= Black display, '0' = Normal display
D2	Gamma Curve Selection	'000'=GC0, '001'=GC1 '010'=GC2, '011'=GC3 '100' to '111' = not define
D1		
D0		

Restriction

-

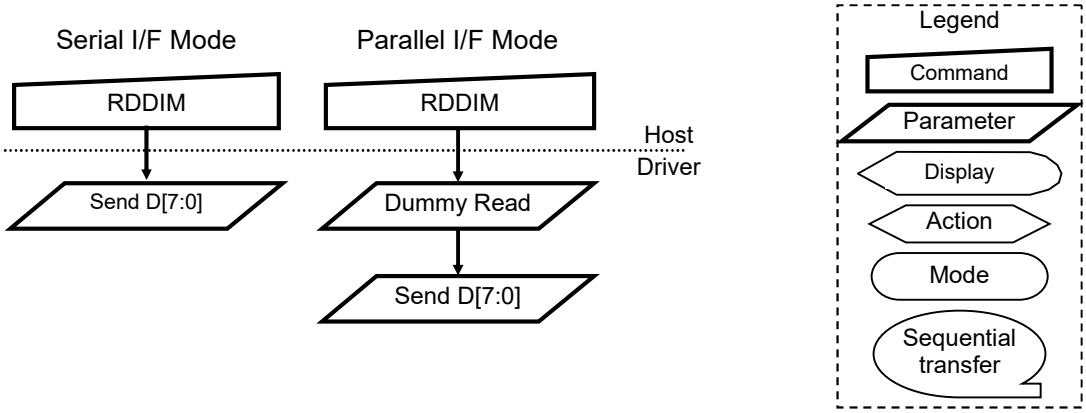
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.12 Read Display Signal Mode (0Eh)

0E H	RDDSM (Read Display Signal Mode)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	1	1	1	0	0E
Dummy Clock Cycle										
1st parameter	-	D7	D6	0	0	D3	D2	0	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Tearing Effect Line On/Off	Set to '0'
D6	Tearing Effect Line Mode	Set to '0'
D5	Horizontal Sync. On/Off	'1'= HS bit is '1', '0' = HS bit is '0'
D4	Vertical Sync. On/Off	'1'= VS bit is '1', '0' = VS bit is '0'
D3	Pixel Clock. On/Off	'1'= PCLK line is '1', '0' = PCLK line is '0'
D2	Data Enable On/Off	'1'= DE bit is '1', '0' = DE bit is '0'
D1	Not Define	Set to '0'
D0	Error on DSI	'1'= Error, '0' = No Error

Restriction

-

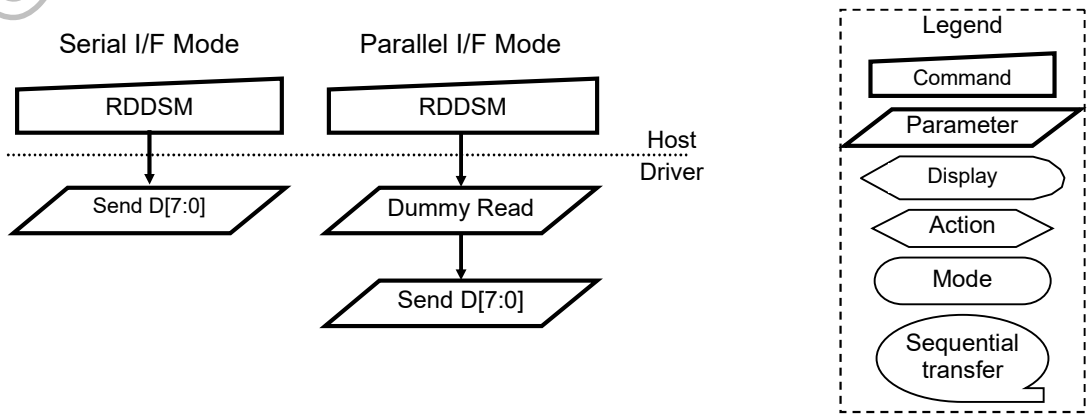
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.13 Read Display Self-Diagnostic Result (0Fh)

0F H	RDDSDR (Read Display Self-Diagnostic Result)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	0	0	0	1	1	1	1	0F
Dummy Clock Cycle										
1st parameter	-	D7	D6	0	0	0	0	0	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Register Loading Detection	See Section 5.4.1
D6	Functionality Detection	See Section 5.4.2
D5	Chip Attachment Detection	Set to '0'
D4	Display Glass Break Detection	Set to '0'
D3	Not Define	Set to '0'
D2	Not Define	Set to '0'
D1	Not Define	Set to '0'
D0	Checksums Comparison	'1'= Checksums are not the same '0'= Checksums are the same

Restriction

-

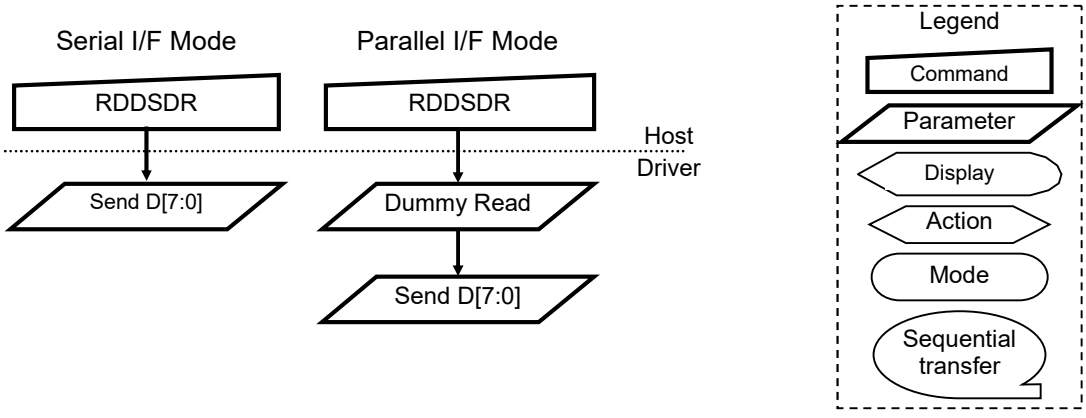
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart

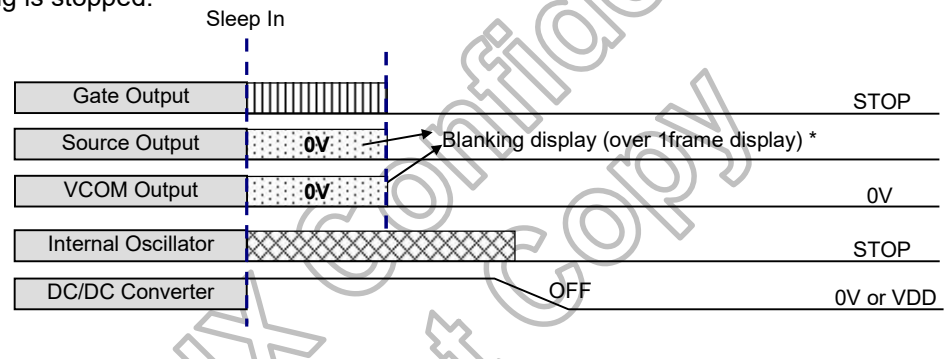


6.2.14 Sleep In (10h)

10 H	SLPIN (Sleep In)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	1	0	0	0	0	10
Parameter	No Parameter									

Description

This command causes the LCD module to enter the minimum power consumption mode.
In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.



Restriction

This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11H).
It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.
It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Register Availability

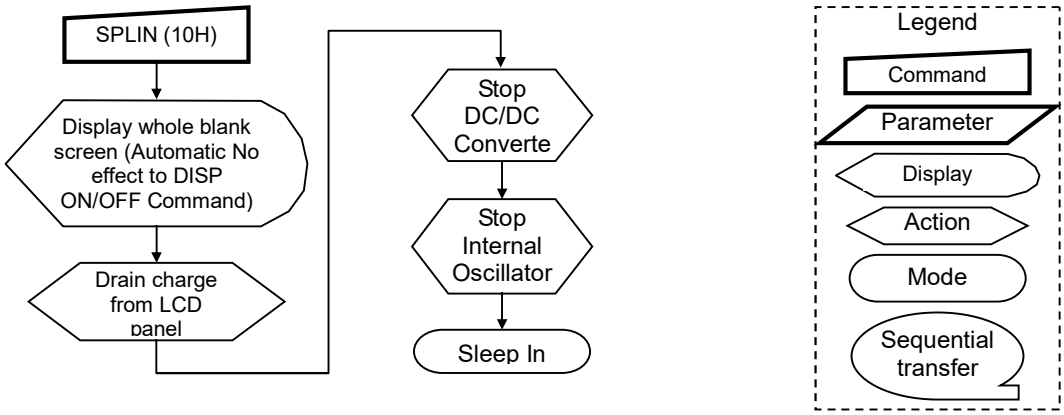
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

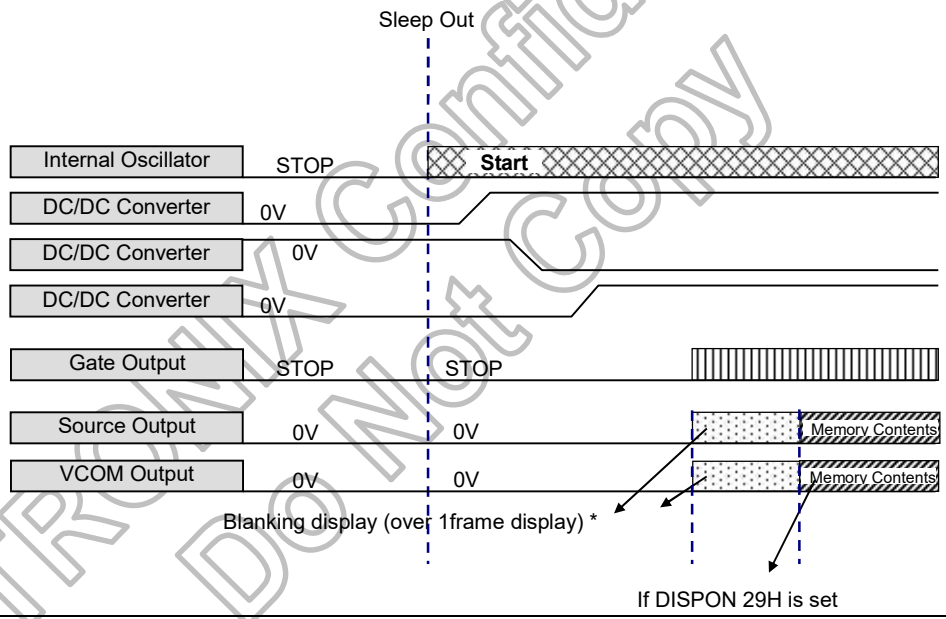
Status	Default Value
Power On Sequence	Sleep In mode
S/W Reset	Sleep In mode
H/W Reset	Sleep In mode

Flow Chart

It takes about 120msec to get into Sleep In mode after SLPIN command issued.



6.2.15 Sleep Out (11h)

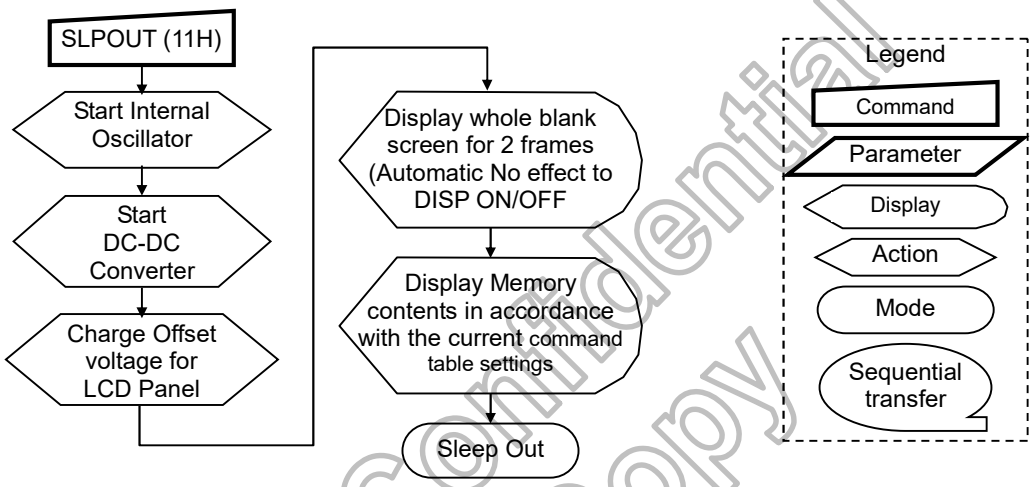
11 H	SLPOUT (Sleep Out)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	1	0	0	0	1	11
Parameter	No Parameter									
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.  									
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Sleep In mode
S/W Reset	Sleep In mode
H/W Reset	Sleep In mode

Flow Chart	It takes 120msec to become Sleep Out mode (booster on mode) after SLPOUT command issued.



6.2.16 Normal Display Mode On (13h)

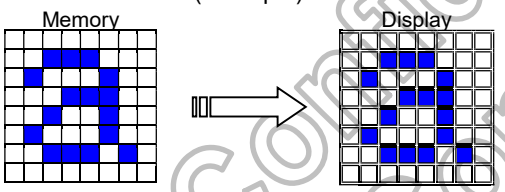
13 H	NORMON (Normal Display Mode On)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	1	0	0	1	1	13
Parameter	No Parameter									
Description	This command returns the display to normal mode. Normal display mode on means Partial mode off, Scroll mode Off.									
Restriction	This command has no effect when module is already in Normal Display mode.									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Normal mode ON
S/W Reset	Normal mode ON
H/W Reset	Normal mode ON

6.2.17 Display Inversion Off (20h)

20 H	INVOFF (Display Inversion Off)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	0	0	0	0	20
Parameter	No Parameter									
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. (Example) 									
Restriction	This command has no effect when module is already in inversion off mode									

Register Availability

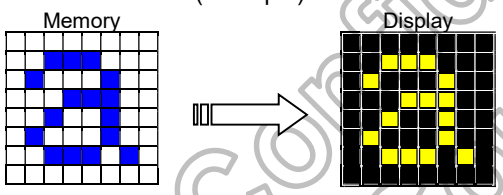
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart

6.2.18 Display Inversion On (21h)

21 H	INVON (Display Inversion On)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	0	0	0	1	21
Parameter	No Parameter									
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. (Example) 									
Restriction	This command has no effect when module is already in inversion on mode									

Register Availability

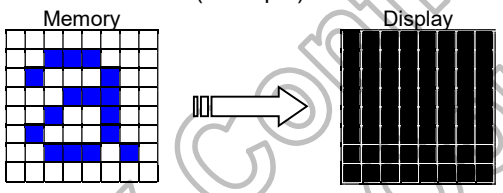
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart

6.2.19 All Pixel Off (22h)

22 H	ALLPOFF (All Pixel Off)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	0	0	1	0	22
Parameter	No Parameter									
Description	This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off. This command makes no change of contents of frame memory. This command does not change any other status. (Example) 									
Restriction	This command has no effect when module is already in all pixel off mode									

Register Availability

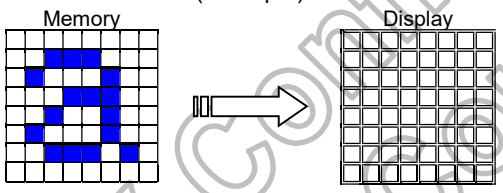
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	All pixel off
S/W Reset	All pixel off
H/W Reset	All pixel off

Flow Chart

6.2.20 All Pixel On (23h)

23 H	ALLPON (All Pixel On)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	0	0	1	1	23
Parameter	No Parameter									
Description	This command turns the display panel white in Sleep Out mode and a status of the Display On/Off –register can be on or off. This command makes no change of contents of frame memory. This command does not change any other status. (Example) 									
Restriction	This command has no effect when module is already in all pixel on mode									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	All pixel off
S/W Reset	All pixel off
H/W Reset	All pixel off

Flow Chart

6.2.21 Gamma Set (26h)

26 H	GAMSET (Gamma Set)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	0	1	1	0	26
Parameter	Write	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	-

Description

This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the table:

GC[7..0]	Parameter	Curve Selected
01h	GC0	Gamma Curve 1
02h	GC1	Reserved
04h	GC2	Reserved
08h	GC3	Reserved

Restriction

Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.

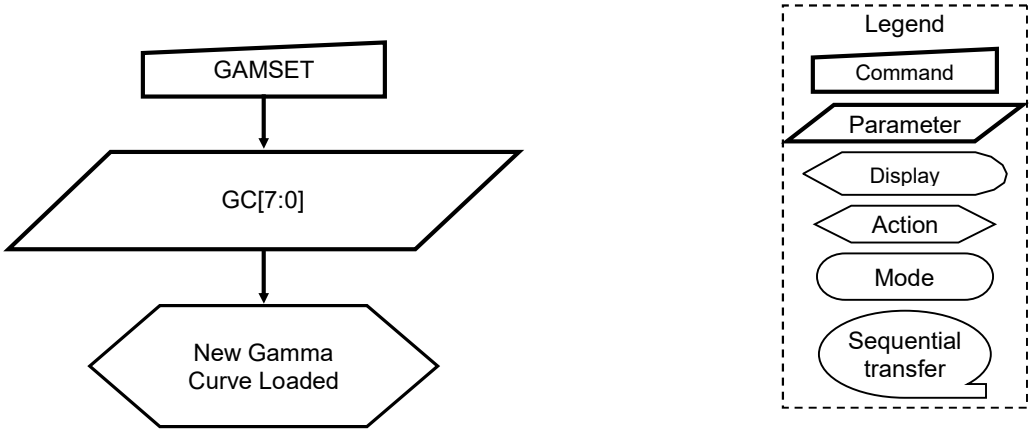
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

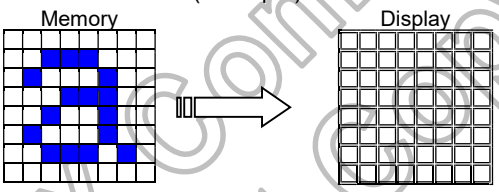
Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Flow Chart



6.2.22 Display Off (28h)

28 H	DISPOFF (Display off)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	1	0	0	0	28
Parameter	NO Parameter									
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. (Example) 									
Restriction	This command has no effect when module is already in display off mode.									

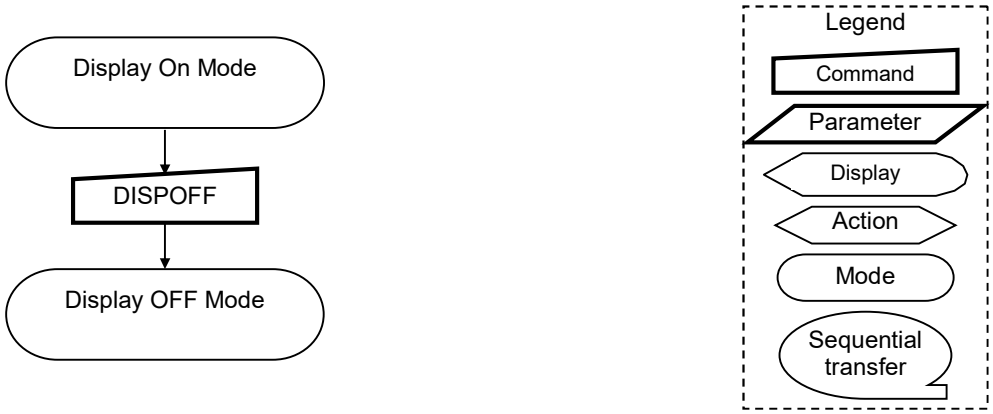
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

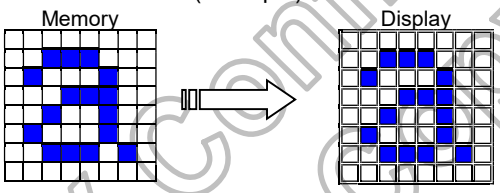
Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



6.2.23 Display On (29h)

29 H	DISPON (Display on)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	1	0	0	1	29
Parameter	NO Parameter									
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example) 									
Restriction	This command has no effect when module is already in display on mode.									

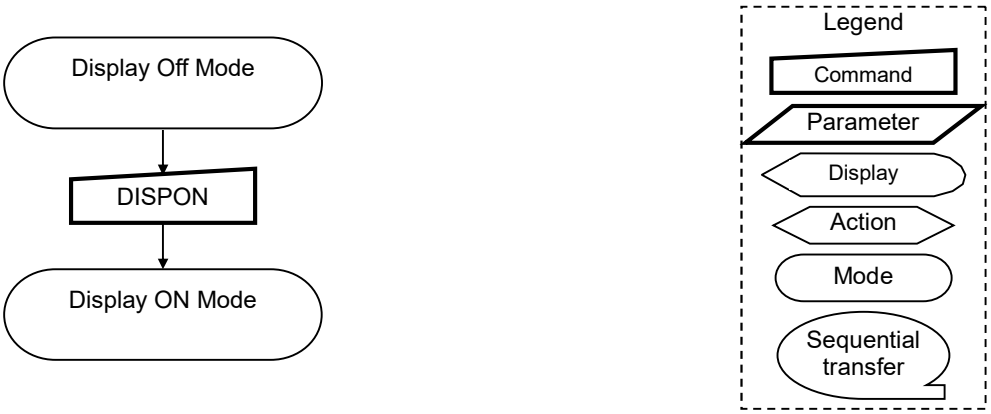
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



6.2.24 Memory Access Control (36h)

36 H	MADCTR (Memory Access Control)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	0	1	1	0	36
Parameter	-	MY	MX	-	-	RGB	SS	-	-	-

Description

This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.

Bit Assignment

BIT	NAME	DESCRIPTION
D7	PAGE ADDRESS ORDER (MY)	These 2 bits controls interface to display direction
D6	COLUMN ADDRESS ORDER (MX)	
D3	RGB-BGR ORDER (BGR)	Color selector switch control 0=RGB color sequence, 1=BGR color sequence
D2	Horizontal ORDER (SS)	LCD horizontal refresh direction control

Restriction

-

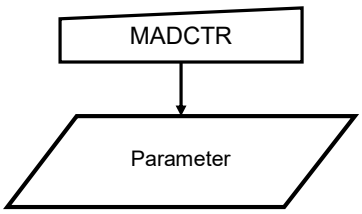
Register Availability

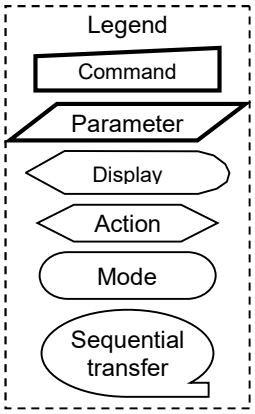
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	No Change
H/W Reset	00h

Flow Chart





6.2.25 Idle Mode Off (38h)

38 H	IDMOFF (Idle Mode Off)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	1	0	0	0	38
Parameter	No Parameter									
Description	This command is used to recover from idle mode on In the idle off mode, display panel can display maximum 16.7M colors									
Restriction	This command has no effect when module is already in idle off mode.									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart

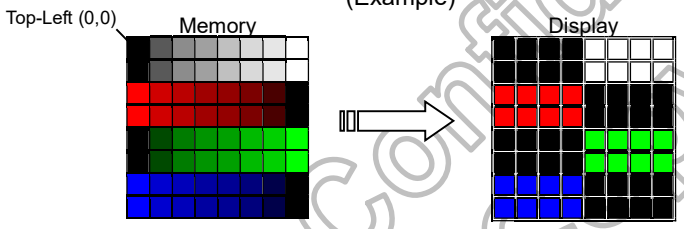
6.2.26 Idle Mode On (39h)

39 H	IDMON (Idle Mode on)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	1	0	0	1	39
Parameter	No Parameter									

Description

This command is used to enter idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.

(Example)



"x" Don't care

Color	R_7 R_6 R_5 R_4 R_3 R_2 R_1 R_0	G_7 G_6 G_5 G_4 G_3 G_2 G_1 G_0	B_7 B_6 B_5 B_4 B_3 B_4 B_1 B_0
Black	0xxx xxxx	0xxx xxxx	0xxx xxxx
Blue	0xxx xxxx	0xxx xxxx	1xxx xxxx
Red	1xxx xxxx	0xxx xxxx	0xxx xxxx
Magenta	1xxx xxxx	0xxx xxxx	1xxx xxxx
Green	0xxx xxxx	1xxx xxxx	0xxx xxxx
Cyan	0xxx xxxx	1xxx xxxx	1xxx xxxx
Yellow	1xxx xxxx	1xxx xxxx	0xxx xxxx
White	1xxx xxxx	1xxx xxxx	1xxx xxxx

Restriction

This command has no effect when module is already in idle on mode.

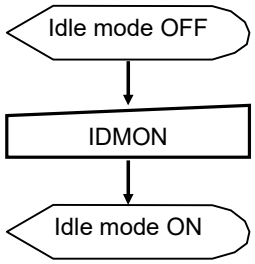
Register Availability

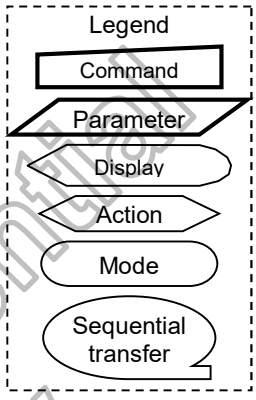
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart





6.2.27 Interface Pixel Format (3Ah)

3A H	COLMOD (Interface Pixel Format)								
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	1	0	1	0	3A
Parameter	Write	0	D6	D5	D4	0	0	0	0	101, 110, 111

Description

This command is used to define the format of RGB picture data, which is to be transfer via the system and RGB interface. The formats are shown in the table:

Interface Format	D6	D5	D4
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
24 Bit/Pixel	1	1	1

Restriction

There is no visible effect until the Frame Memory is written to.

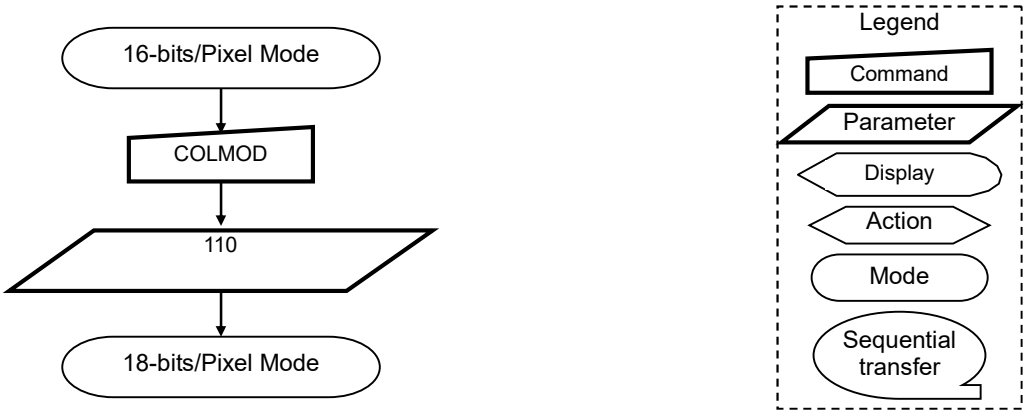
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	70h
S/W Reset	No change
H/W Reset	70h

Flow Chart



6.2.28 Write Display Brightness (51h)

51 H	WRDISBV (Write Display Brightness)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	0	0	0	1	51
Parameter	Write	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV1	-

Description

This command is used to adjust brightness value.
In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

DBV[7:0]	Brightness Ratio	Brightness %
00h	0/256	0%
01h	2/256	0.78%
:	:	:
FEh	255/256	99.6%
FFH	256/256	100%

Restriction

The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart

6.2.29 Read Display Brightness (52h)

52 H	RDDISBV (Read Display Brightness)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	0	1	0	0	1	0	52
	Dummy Cycle									
Parameter	Read	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV1	-
Description	This command is used to read brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.									
Restriction	-									

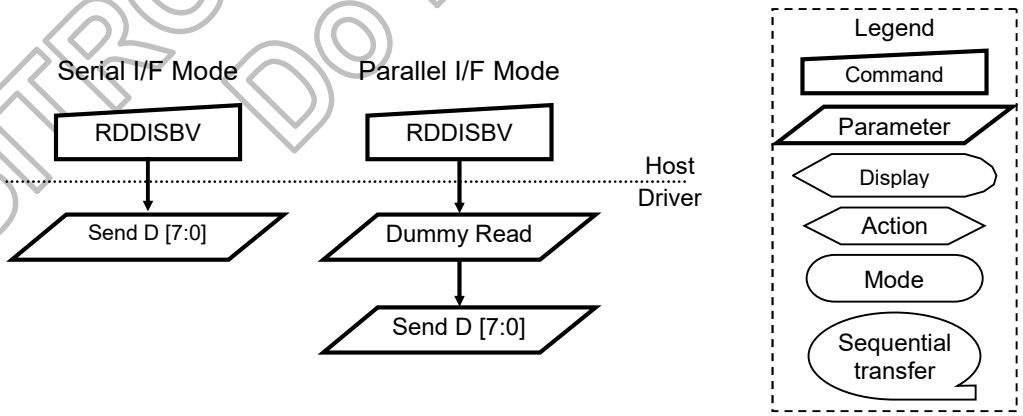
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.30 Write CTRL Display (53h)

53 H	WRCTRLD (Write CTRL Display Value)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	0	0	1	1	53
Parameter	Write	0	0	BCTRL	0	DD	BL	0	0	-

Description

This command is used to control display brightness.

I

Bits	Value
BCTRL	'0' off, DBV[7:0] is 00h; PWM keep low '1' On, DBV[7:0] is active; PWM output
DD	'0' Brightness dimming is off '1' Brightness dimming is on
BL	'0' Backlight Control is off '1' Backlight Control is on

Restriction

-

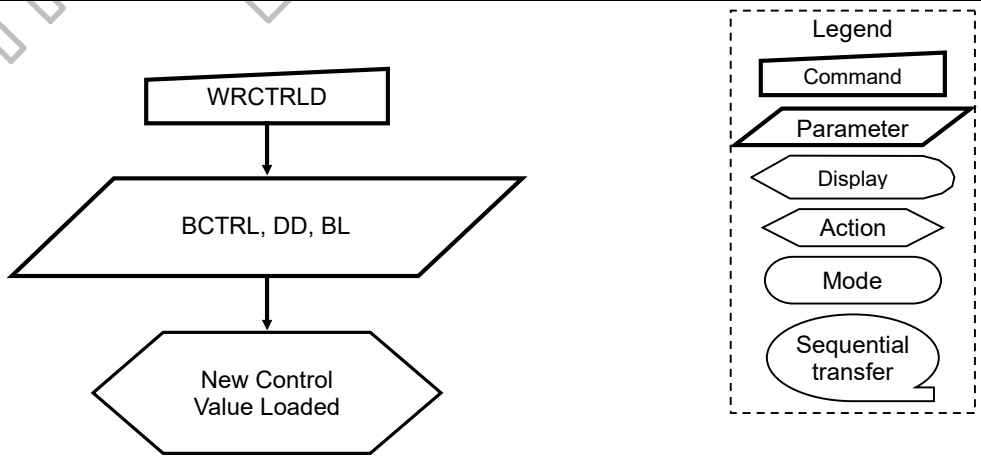
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.31 Read CTRL Display Value (54h)

54 H	RDCTRLD (Read CTRL Display Value)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	0	1	0	1	0	0	54
Dummy Cycle										
Parameter	Read	0	0	BCTRL	0	DD	BL	0	0	-
Description	This command is used to read brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.									
Restriction	-									

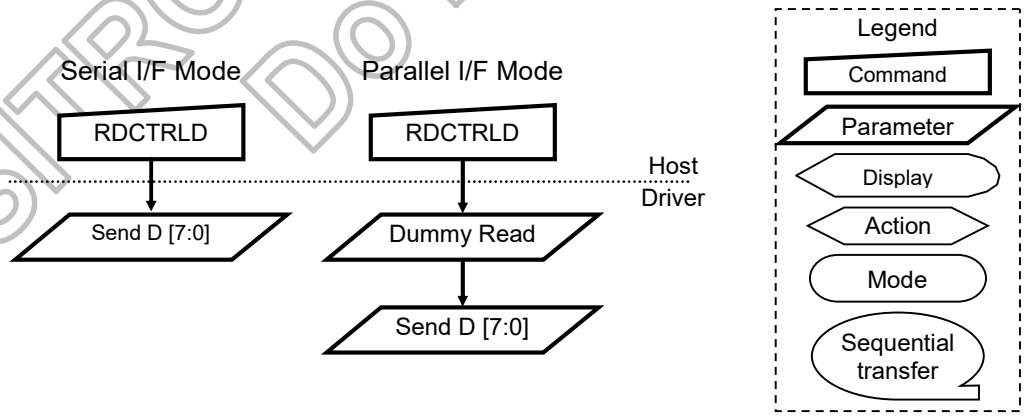
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.32 Write Content Adaptive Brightness Control (55h)

55 H	WRCABC (Write Content Adaptive Brightness Control)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	0	1	0	1	55
Parameter	Write	0	0	0	0	0	0	C1	C0	-

Description

This command is used to set parameters for image content based adaptive brightness control functionality.

I

C1	C0	Function
0	0	Off
0	1	User Interface Image (UI mode)
1	0	Still Picture Image (Still mode)
1	1	Moving Picture Image (Moving mode)

Restriction

This register is synchronized with V-sync by internal circuit.

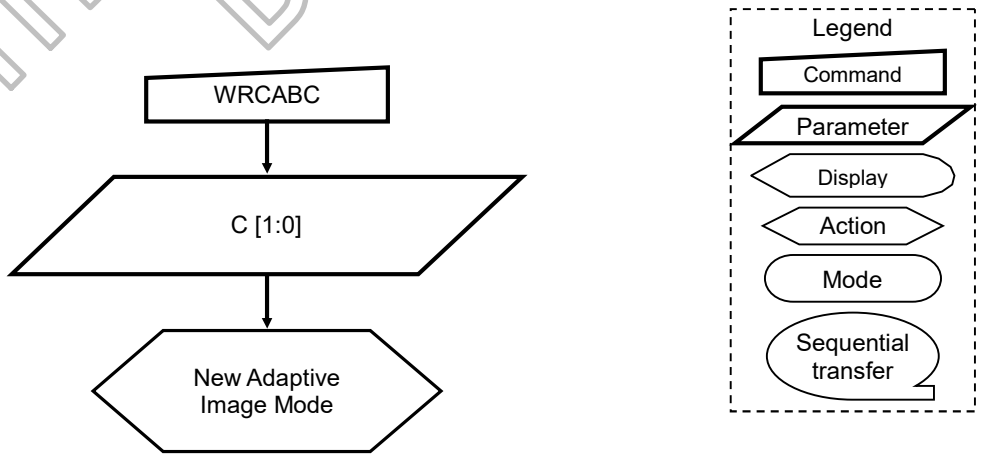
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.33 Read Content Adaptive Brightness Control (56h)

56 H	RDCABC (Read Content Adaptive Brightness Control)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	0	1	1	1	1	0	56
	Dummy Cycle									
Parameter	Read	0	0	0	0	0	0	C1	C0	-
Description	This command is used to read parameters for image content based adaptive brightness control functionality.									
Restriction	-									

Description:

C1	C0	Function
0	0	Off
0	1	User Interface Image (UI mode)
1	0	Still Picture Image (Still mode)
1	1	Moving Picture Image (Moving mode)

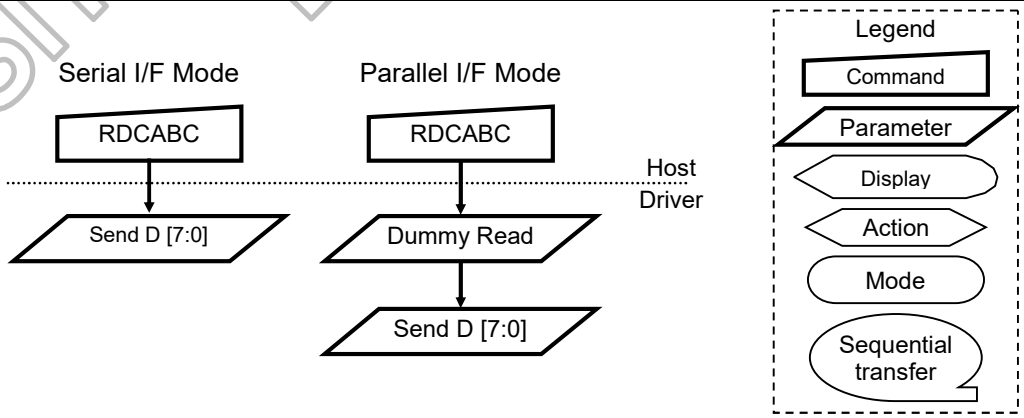
Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default:

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart:



6.2.34 Write CABC Minimum Brightness (5Eh)

5E H	WRCABCMB (Write CABC minimum brightness)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	1	1	1	0	5E
Parameter	Write	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	-
Description	This command is used to set the minimum brightness value of the display for CABC function In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.									
Restriction	-									

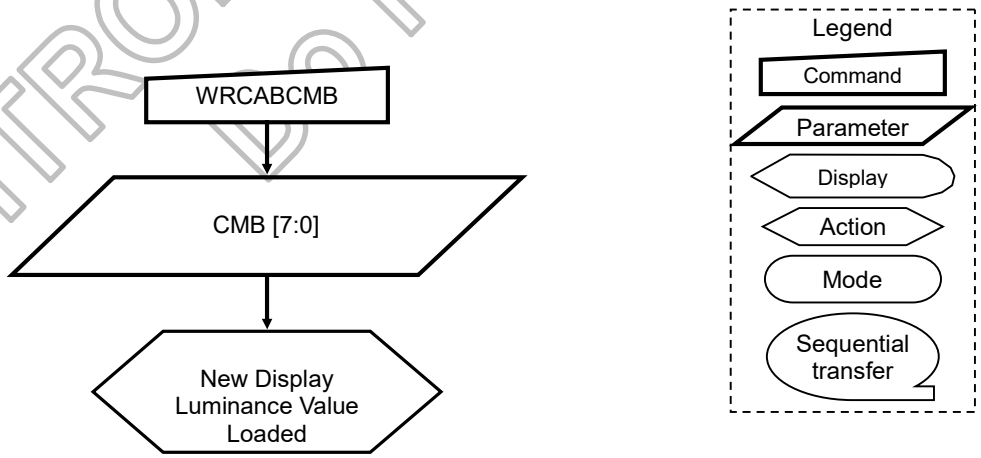
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.35 Read CABC minimum brightness (5Fh)

5F H	RDCABCMB (Read CABC minimum brightness)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	0	1	1	1	1	1	5F
Dummy Cycle										
Parameter	Read	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	-
Description	This command is used to read the minimum brightness value of the display for CABC function In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.									
Restriction	-									

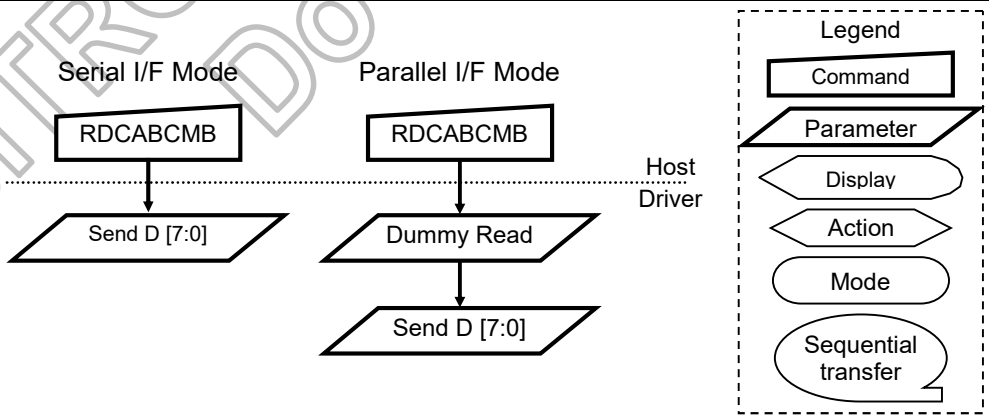
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.36 Read Black/White Low Bits (70h)

70 H	RDBWLB (Read Black White Low Bits)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	0	0	0	0	70
Dummy Cycle										
Parameter	Read	Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0	-
Description	This command returns the lowest bits of black and white color characteristic. Black: Bkx and Bky White: Wx and Wy									
Restriction	-									

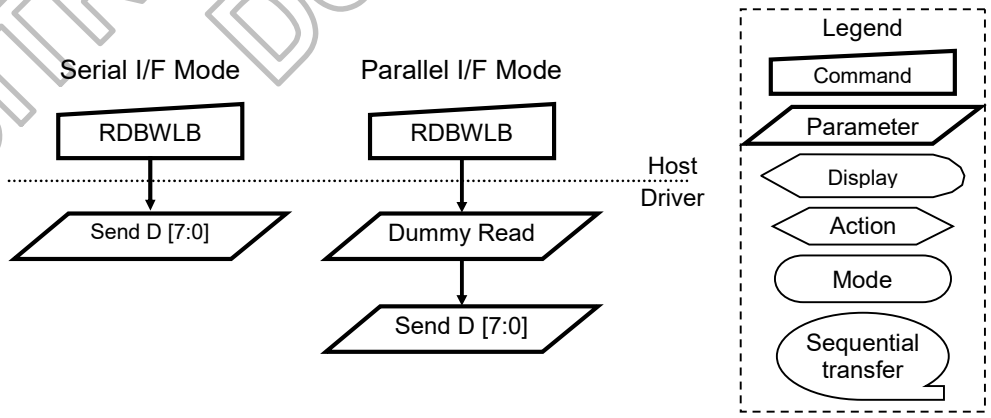
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.37 Read Bkx (71h)

71 H	RDBkx (Read Bkx)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	0	0	0	1	71
Dummy Cycle										
Parameter	Read	Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2	-
Description	This command returns the Bkx bits of black color characteristic.									
Restriction	-									

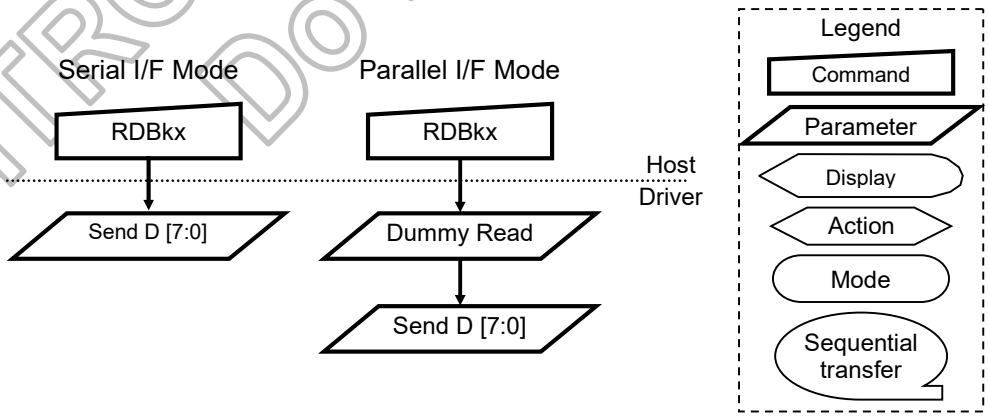
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.38 Read Bky (72h)

72 H	RDBky (Read Bky)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	0	0	1	0	72
Dummy Cycle										
Parameter	Read	Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2	-
Description	This command returns the Bky bits of black color characteristic.									
Restriction	-									

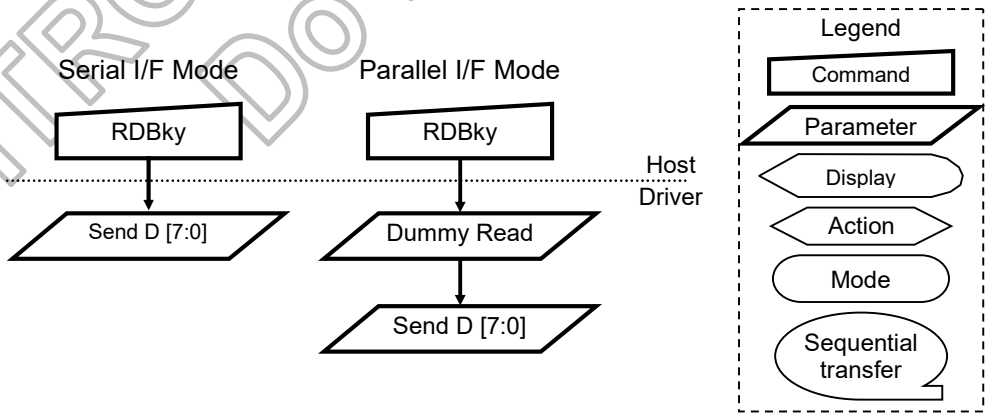
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.39 Read Wx (73h)

73 H	RDWx (Read Wx)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	0	0	1	1	73
	Dummy Cycle									
Parameter	Read	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2	-
Description	This command returns the Wx bits of White color characteristic.									
Restriction	-									

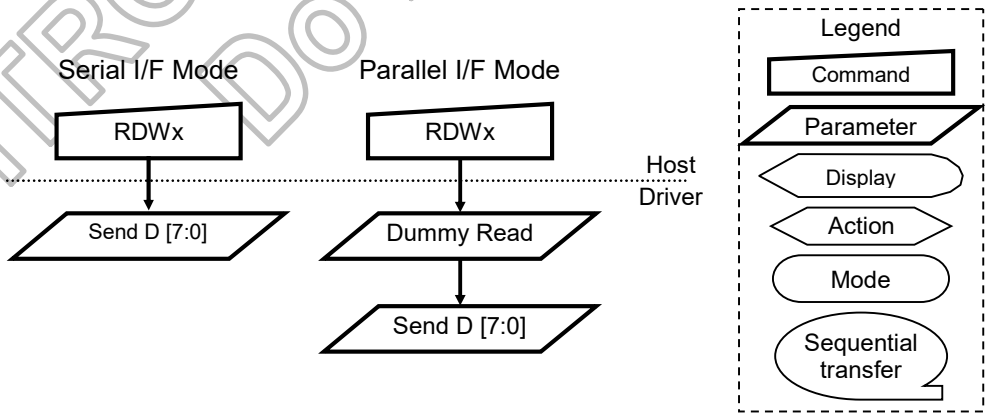
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.40 Read Wy (74h)

74 H	RDWy (Read Wy)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	0	1	0	0	74
Dummy Cycle										
Parameter	Read	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2	-
Description	This command returns the Wy bits of White color characteristic.									
Restriction	-									

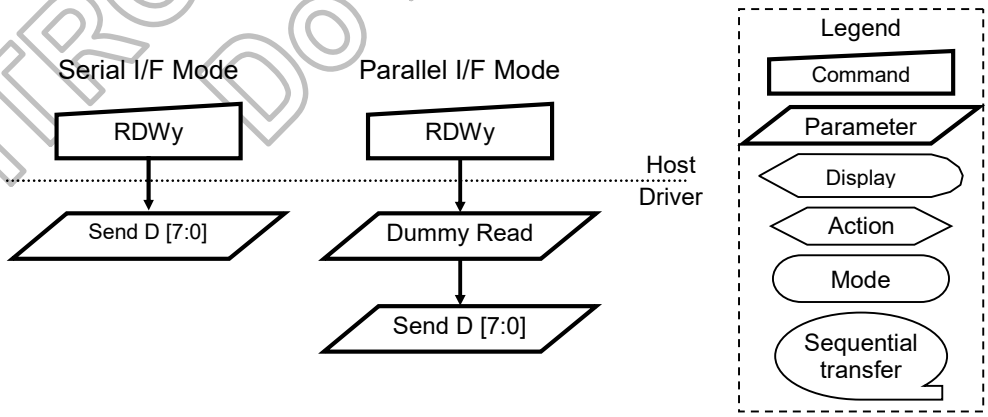
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.41 Read Red/Green Low Bits (75h)

75 H	RDRGLB (Read Red Green Low Bits)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	0	1	0	1	75
Dummy Cycle										
Parameter	Read	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0	-
Description	This command returns the lowest bits of Red and Green color characteristic. Red: Rx and Ry Green: Gx and Gy									
Restriction	-									

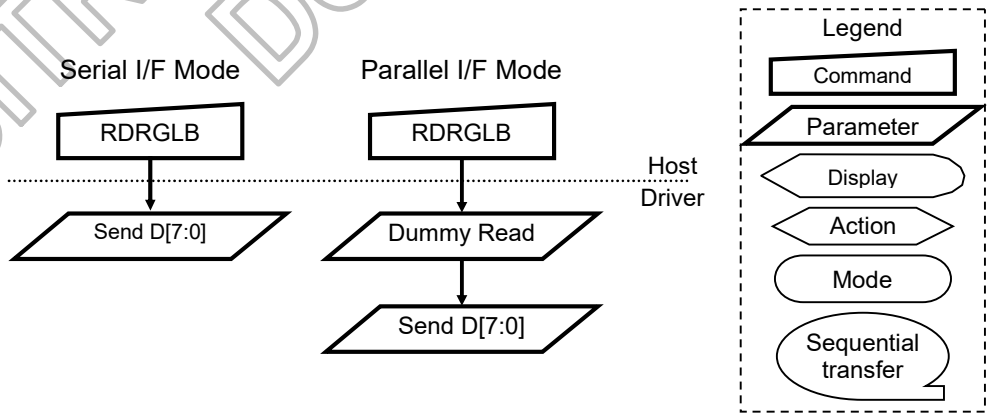
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.42 Read Rx (76h)

76 H	RDRx (Read Rx)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	0	1	1	0	76
Dummy Cycle										
Parameter	Read	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	-
Description	This command returns the Rx bits of Red color characteristic.									
Restriction	-									

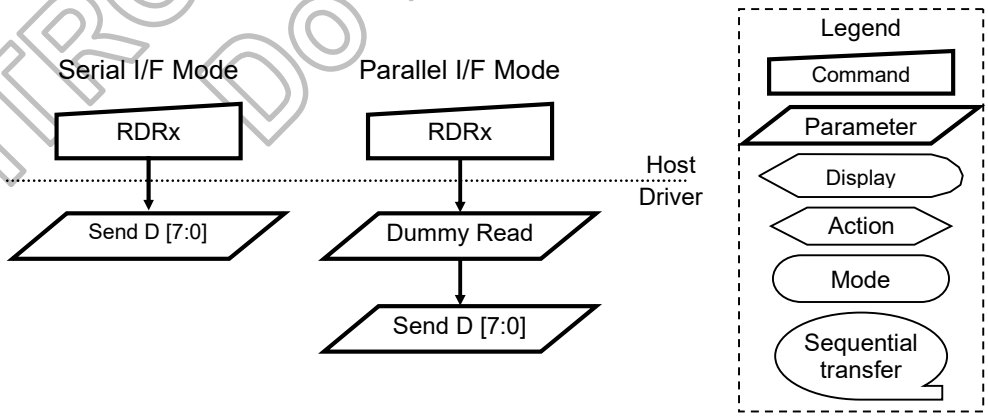
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.43 Read Ry (77h)

77 H	RDRy (Read Ry)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	0	1	1	1	77
	Dummy Cycle									
Parameter	Read	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2	-
Description	This command returns the Ry bits of Red color characteristic.									
Restriction	-									

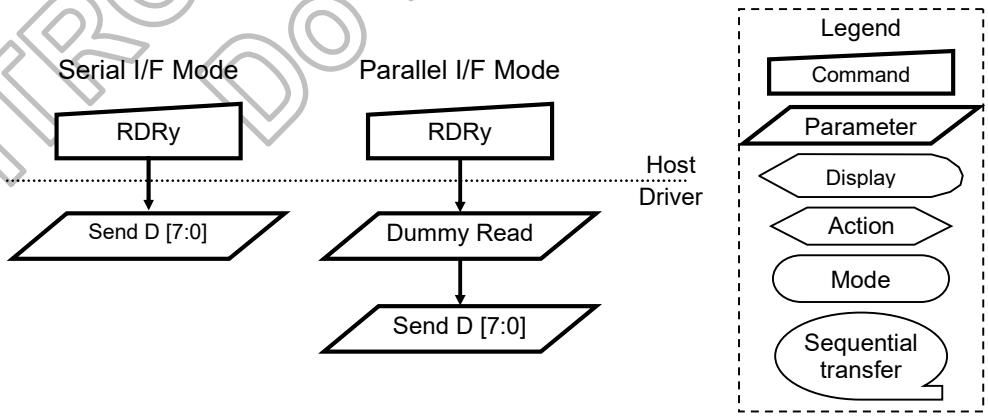
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.44 Read Gx (78h)

78 H	RDGx (Read Gx)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	1	0	0	0	78
Dummy Cycle										
Parameter	Read	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2	-
Description	This command returns the Gx bits of Green color characteristic.									
Restriction	-									

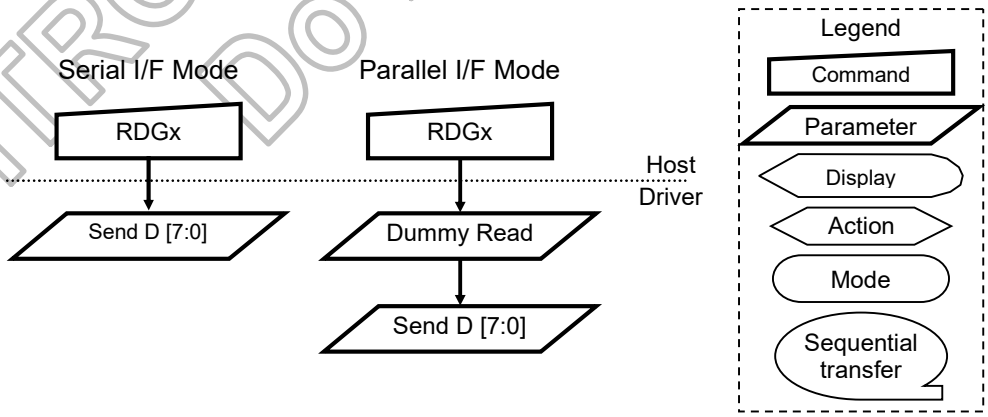
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.45 Read Gy (79h)

79 H	RDGy (Read Gy)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	1	0	0	1	79
	Dummy Cycle									
Parameter	Read	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2	-
Description	This command returns the Gy bits of Green color characteristic.									
Restriction	-									

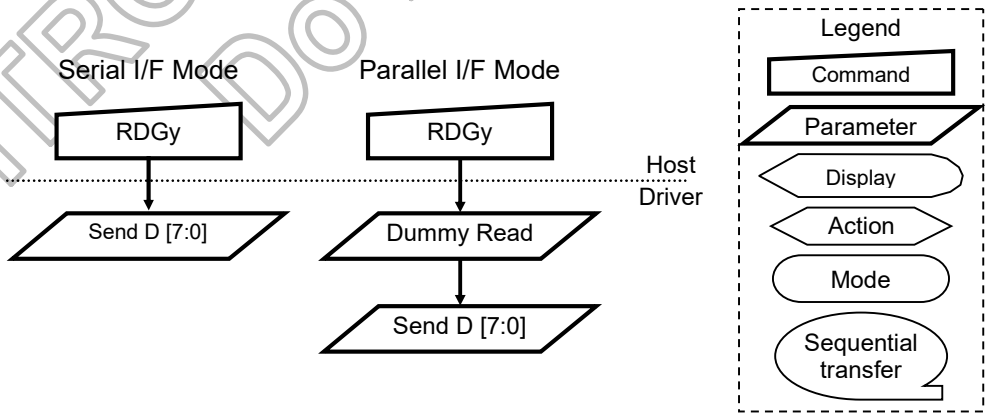
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.46 Read Blue/AColor Low Bits (7Ah)

7A H	RDBALB (Read Blue AColor Low Bits)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	1	0	1	0	7A
Dummy Cycle										
Parameter	Read	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0	-
Description	This command returns the lowest bits of Blue and AColor color characteristic. Blue: Bx and By A: Ax and Ay									
Restriction	-									

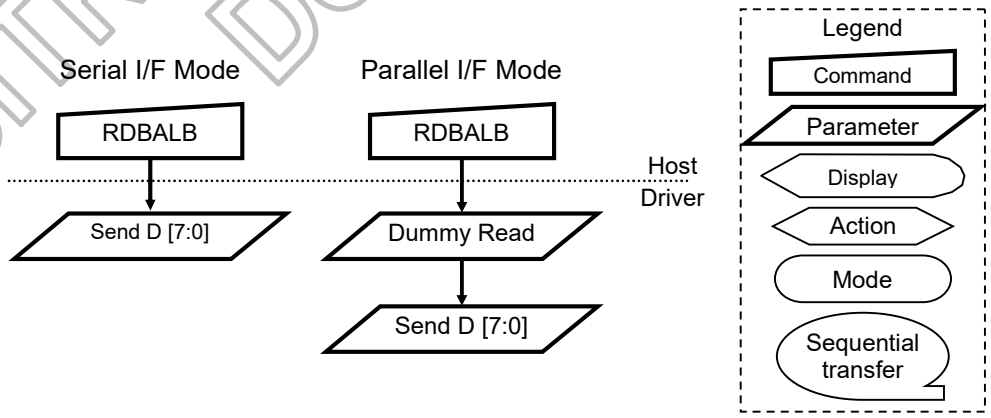
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.47 Read Bx (7Bh)

7B H	RDBx (Read Bx)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	1	0	1	1	7B
Dummy Cycle										
Parameter	Read	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2	-
Description	This command returns the Bx bits of Blue color characteristic.									
Restriction	-									

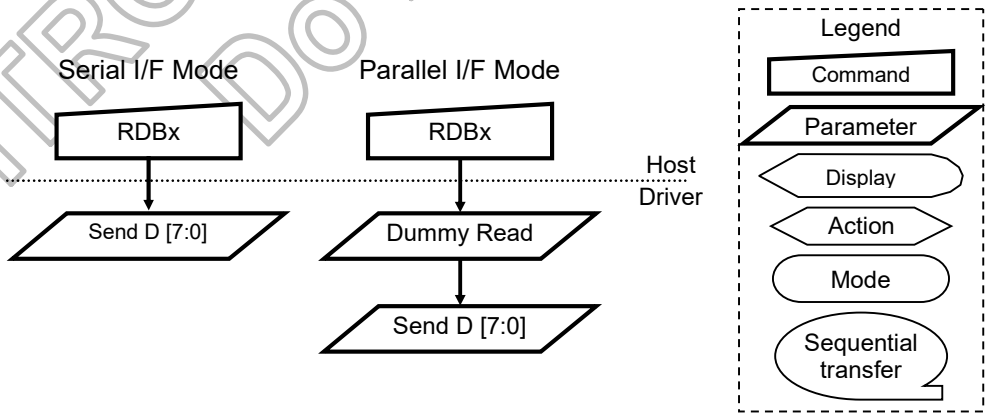
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.48 Read By (7Ch)

7C H	RDBy (Read By)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	1	1	0	0	7C
Dummy Cycle										
Parameter	Read	By9	By8	By7	By6	By5	By4	By3	By2	-
Description	This command returns the By bits of Blue color characteristic.									
Restriction	-									

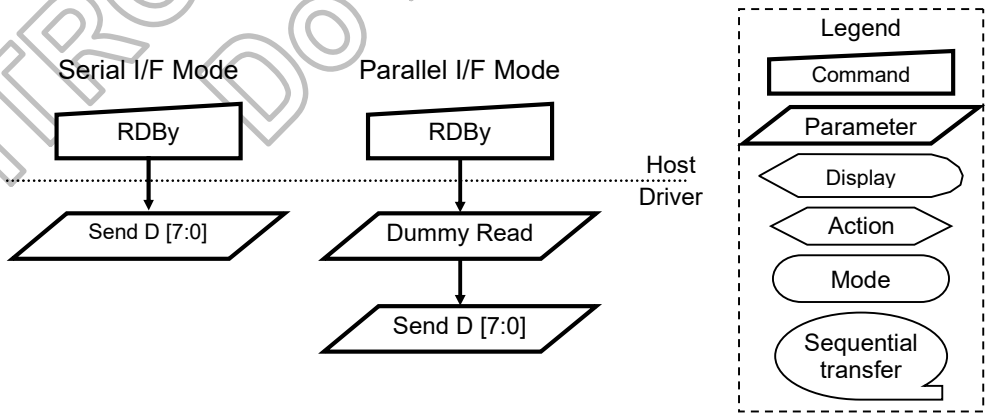
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.49 Read Ax (7Dh)

7D H	RDAx (Read Ax)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	1	1	0	1	7D
	Dummy Cycle									
Parameter	Read	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2	-
Description	This command returns the Ax bits of A color characteristic.									
Restriction	-									

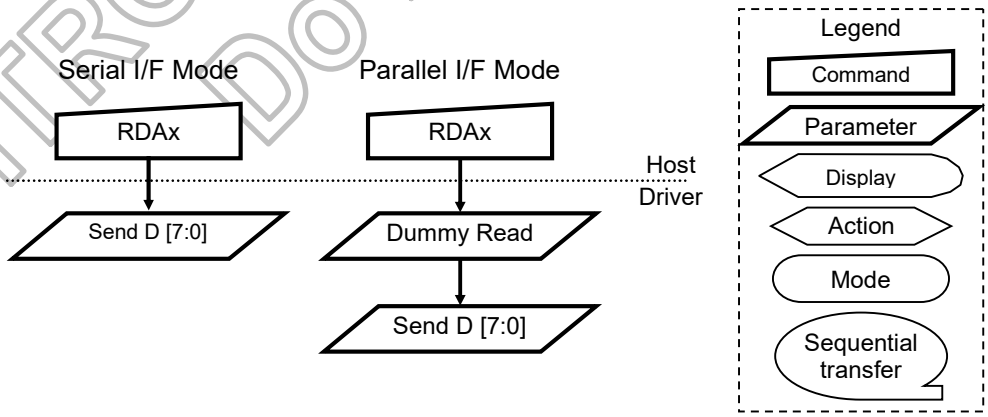
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.50 Read Ay (7Eh)

7E H	RDAy (Read Ay)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	0	1	1	1	1	1	1	0	7E
	Dummy Cycle									
Parameter	Read	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	Ay3	Ay2	-
Description	This command returns the Ay bits of A color characteristic.									
Restriction	-									

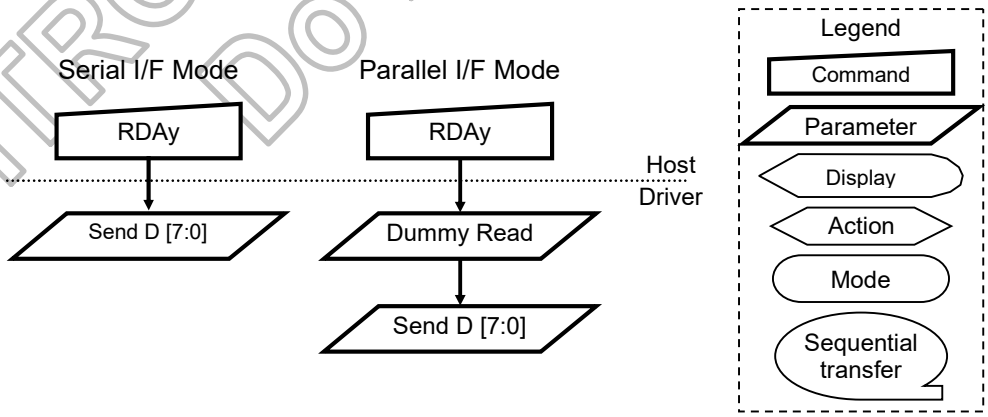
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.51 Read DDB Start (A1h)

A1 H	RDDDBS (Read DDB Start)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	1	0	1	0	0	0	0	1	A1
Dummy Cycle										
1st Parameter	Read	x	x	x	x	x	x	x	x	-
2nd Parameter		x	x	x	x	x	x	x	x	
3Rd Parameter		x	x	x	x	x	x	x	x	
4th parameter		x	x	x	x	x	x	x	x	
5th parameter		1	1	1	1	1	1	1	1	

Description

This command returns the supplier identification and display module mode/revision information.
Note: This information is not the same what “Read ID1 (DAh)”, “Read ID2 (DBh)” and “Read ID3 (DCh)”commands are returning.
Note: Parameter 0xFF is an “Exit Code”, this means that there is no more data in the DDB block.
This read sequence can be interrupted by any command and it can be continued by “Read DDB Continue (A8h)” command when the first parameter, what has been transferred, is the parameter, which has not been sent e.g. RDDDBS => 1st parameter has been sent => 2nd parameter has been sent=> interrupt => RDDDBC => 3rd parameter of the RDDDBS has been sent.

Restriction

-

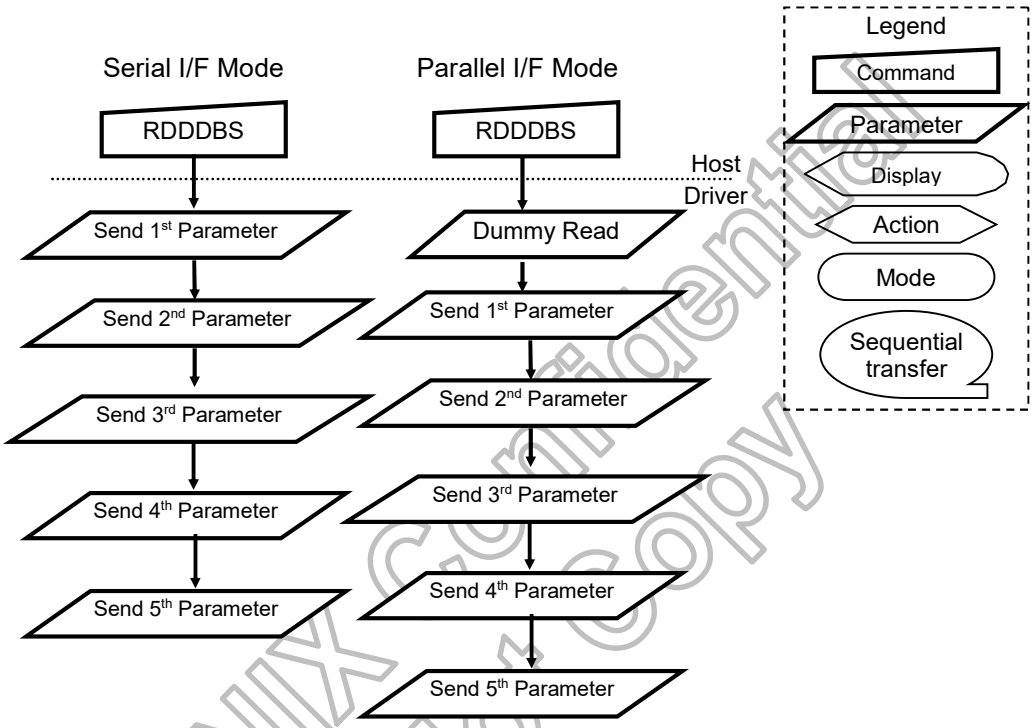
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.52 Read DDB Continue (A8h)

A8 H	RDDDBC (Read DDB Continue)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	1	0	1	0	1	0	0	0	A8
Dummy Cycle										
1st Parameter	Read	x	x	x	x	x	x	x	x	-
2nd Parameter		x	x	x	x	x	x	x	x	
3Rd Parameter		x	x	x	x	x	x	x	x	
4th parameter		x	x	x	x	x	x	x	x	
5th parameter		1	1	1	1	1	1	1	1	
Description	This command returns the supplier identification and display module mode/revision information from the point where RDDDBS command was interrupted by an other command. Note: Parameter 0xFF is an "Exit Code", this means that there is no more data in the DDB block.									
Restriction	-									

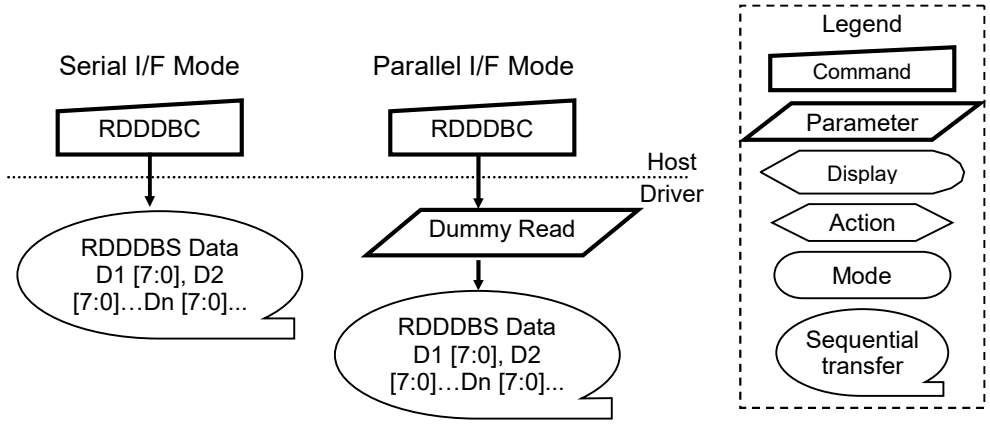
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

Flow Chart



6.2.53 Read First Checksum (AAh)

AA H	RDFCS (Read First Checksum)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	1	0	1	0	1	0	1	0	AA
Parameter	Read	FSC7	FSC6	FSC5	FSC4	FSC3	FSC2	FSC1	FSC0	-
Description	This command returns the first checksum what has been calculated from “Standard Command Set” area registers (not include “Manufacture Command Set) and the frame memory after the write access to those registers and/or frame memory has been done.									
Restriction	It will be necessary to wait 150ms after there is the last write access on “Standard Command Set” area registers before there can read this checksum value.									

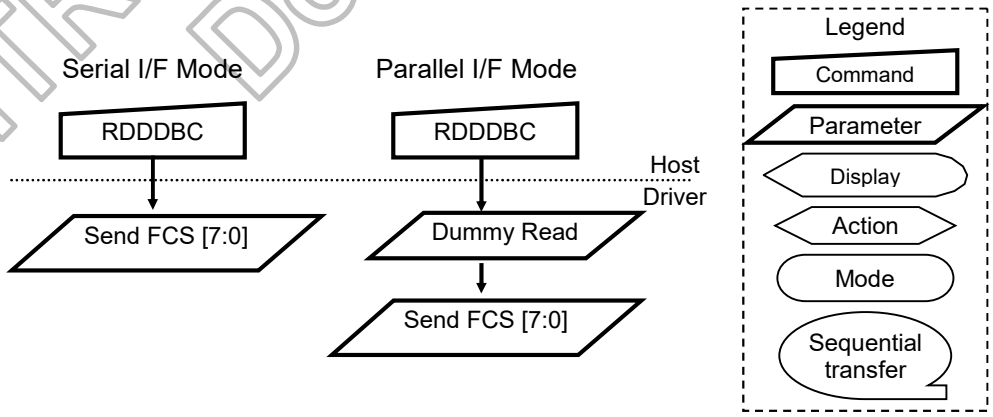
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.54 Read Continue Checksum (AFh)

AF H	RDCCS (Read Continue Checksum)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	1	0	1	0	1	1	1	1	AF
Parameter	Read	CSC7	CSC6	CSC5	CSC4	CSC3	CSC2	CSC1	CSC0	-
Description	This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from “Standard Command Set” area registers and the frame memory after the write access to those registers and/or frame memory has been done									
Restriction	It will be necessary to wait 300ms after there is the last write access on “Standard Command Set” area registers before there can read this checksum value.									

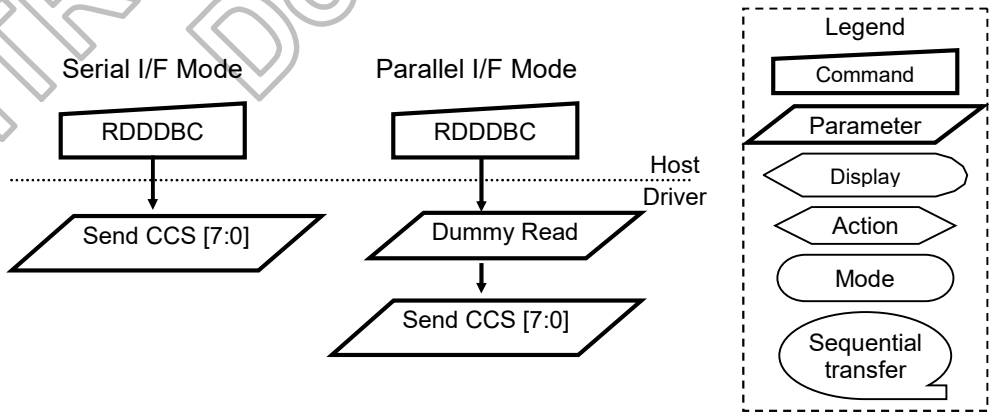
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



6.2.55 Read ID1 Value (DAh)

DA H	RDID1 (Read ID1 Value)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	1	1	0	1	1	0	1	0	DA
Dummy Cycle										
Parameter	Read	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-
Description	This read byte identifies the LCD module's manufacturer.									
Restriction	-									

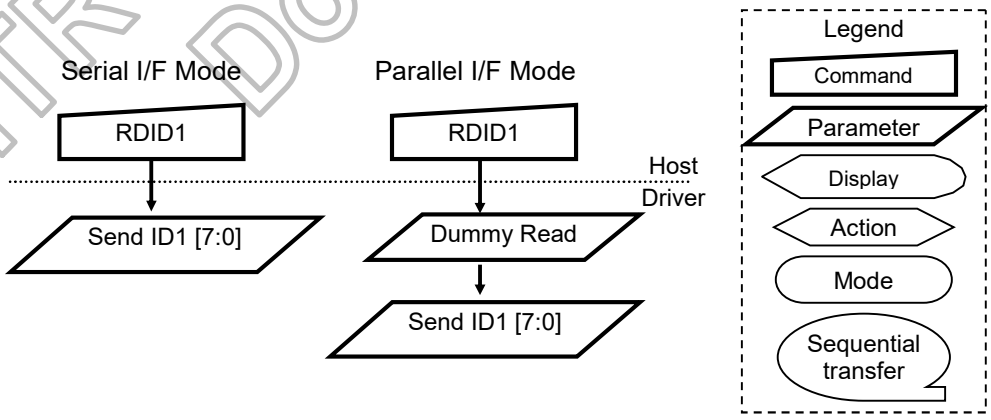
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	48h	OTP Value
S/W Reset	48h	OTP Value
H/W Reset	48h	OTP Value

Flow Chart



6.2.56 Read ID2 Value (DBh)

DB H	RDID2 (Read ID2 Value)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	1	1	0	1	1	0	1	1	DB
Dummy Cycle										
Parameter	Read	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
Description	This read byte identifies the LCD module version.									
Restriction	-									

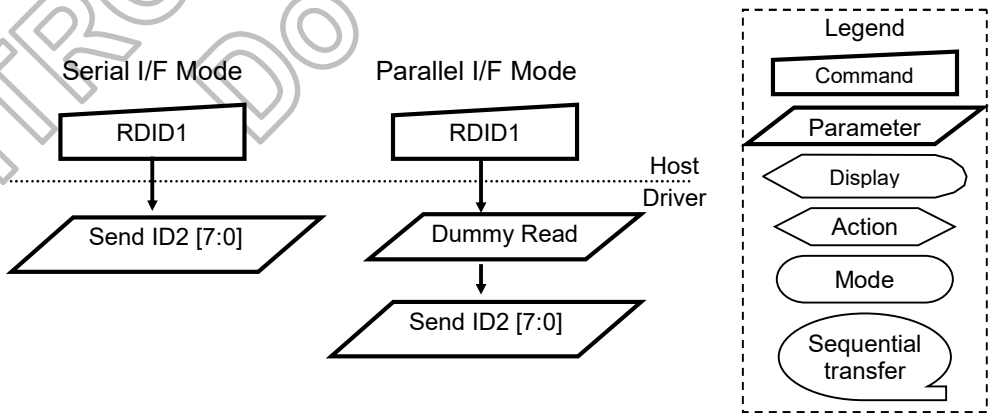
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	21h	OTP Value
S/W Reset	21h	OTP Value
H/W Reset	21h	OTP Value

Flow Chart



6.2.57 Read ID3 Value (DCh)

DC H	RDID3 (Read ID3 Value)									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Read	1	1	0	1	1	1	0	0	DC
	Dummy Cycle									
Parameter	Read	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-
Description	This read byte identifies the LCD module/driver.									
Restriction	-									

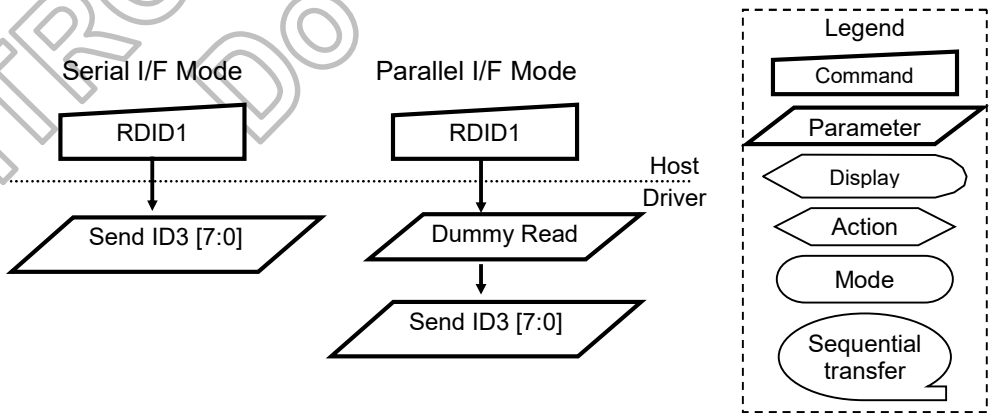
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
	Before OTP	After OTP
Power On Sequence	1Fh	OTP Value
S/W Reset	1Fh	OTP Value
H/W Reset	1Fh	OTP Value

Flow Chart



7. Electrical Characteristics

7.1 Absolute maximum ratings

Item	Symbol	Unit	Spec.		
			Min.	Typ.	Max.
Power Supply Voltage 1	IOVCC~VSSD	V	-0.3	-	+5.5
Power Supply Voltage 2	VCI ~ VSSA	V	-0.3	-	+5.5
Power Supply Voltage 3	VSP ~ VSSA	V	-0.3	-	+6.6
Power Supply Voltage 4	VSSA ~ VSN	V	-0.3	-	+6.6
Power Supply Voltage 5	VGH ~ VGL	V	-0.3	-	+35
Logic Input Voltage	V_{IN}	V	-0.3	-	IOVCC+0.3
Logic Output Voltage	Vo	V	-0.3	-	IOVCC+0.3
Differential Input Voltage	DSI_CP/DSI_CN DSI_D0P/DSI_D0P, DSI_D1P/DSI_D1N	V	-0.3	-	2.0
Operating Temperature	Topr	℃	-40	-	+85
Storage Temperature	Tstg	℃	-55	-	+110

Table 7.1: Absolute maximum ratings

7.2 DC characteristics

7.2.1 Basic Characteristics

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Power & Operating Voltages						
Logic Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	3.3	V
Analog Operating voltage	VCI	Operation voltage	2.5	2.8	3.3	
Input / Output						
Logic High level input voltage	VIH	-	0.7IOVCC	-	IOVCC	V
Logic Low level input voltage	VIL	-	VSSD	-	0.3IOVCC	
Logic High level output voltage	VOH	IOH = -1.0mA	0.8IOVCC	-	IOVCC	
Logic Low level output voltage	VOL	IOL = +1.0mA	VSSD	-	0.2IOVCC	
Input leakage current	IIL	-	-1	-	1	μA
DC/DC Converter Operation						
VSP booster voltage	VSP	IVSP=1mA	4.5		6.2	V
VSN booster voltage	VSN	IVSN=-1mA	-6.2		-4.5	
VCL booster voltage	VCL	Ivcl=-1mA	-3.3		-2.5	
VGH booster voltage	VGH	Ivgh=1mA	10		20	
VGL booster voltage	VGL	Ivgl=-1mA	-15		-7.5	
VGH and VGL difference	|VGH-VGL|	-	-	-	32	
Oscillator tolerance	OSC	25℃	-3		3	%
Source Driver						
Gamma reference voltage	VSPR	-	3.3		5.6	V
	VSNR	-	-5.6		-3.3	
Output voltage deviation	DVOS	VSSD+1.0 ~ VSPROUT-1.0	-	-	+/- 20	mV
		VSSD+0.1V ~ VSSD+1.0 VSPR-1.0 ~ VSPR-0.1V	-	-	+/- 50	mV
Output offset voltage	Voff	-		-	+/-50	mV

7.2.2 DSI DC Characteristics

LP Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX(CLK, D0)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX(CLK, D0)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX(CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX(D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX(D0)	-50	-	50	mV
Logic high level input current	V_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic low level input current	V_{IL}	LP-CD, LP-RX	-10	-	-	uA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-D0+/1	-	-	300	Vps

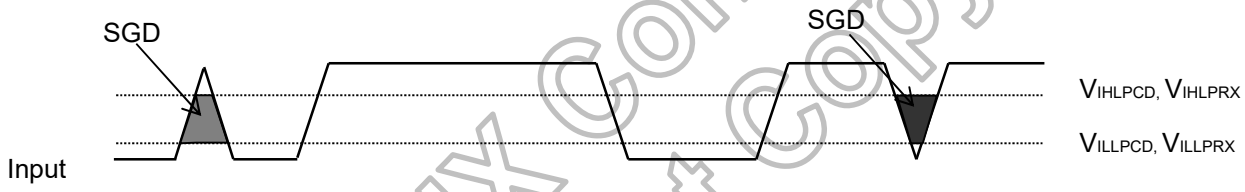


Figure 7.1: Input glitch rejections of low-power receivers

High Speed Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Input common mode	V_{CMCLK} V_{CMDATA}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	70	-	330	mV
Input common mode variation <450 MHZ	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-50	-	50	mV
Input common mode variation >450 MHZ	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	100	mV
Low-level differential Input threshold	V_{THLCLK} $V_{THLDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-70	-	-	mV
High-level differential Input threshold	V_{THHCLK} $V_{THHDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	70	mV
Single ended input low voltage	V_{ILHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-40	-	-	mV
Single ended input high voltage	V_{IHHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	80	100	125	Ω
Single-ended threshold voltage for termination enable	V_{TERMEN}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	450	mV
Termination capacitor	C_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	-	pF

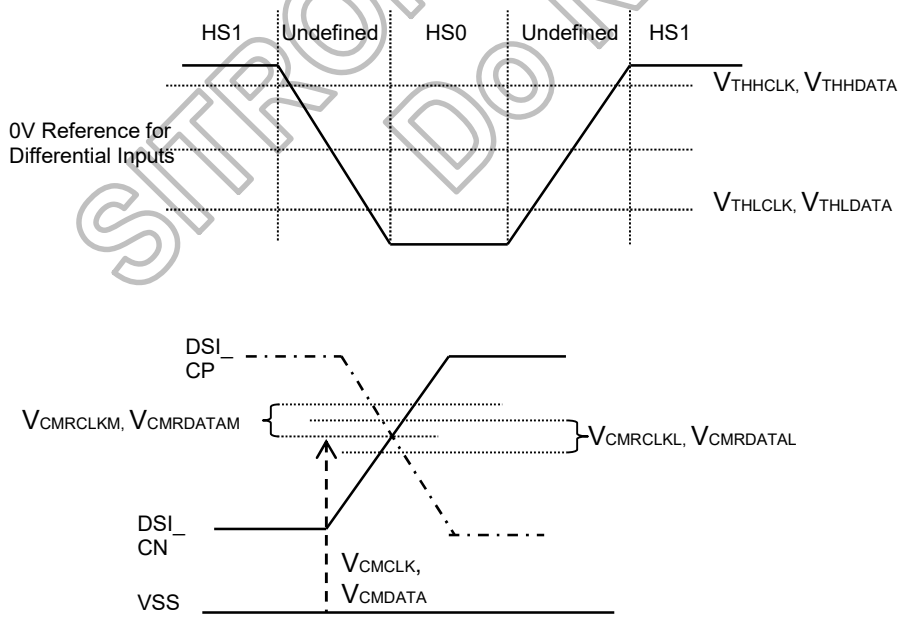


Figure 7.2: Differential voltage range and Command mode voltage

7.3 AC characteristics

7.3.1 Serial Interface Characteristics

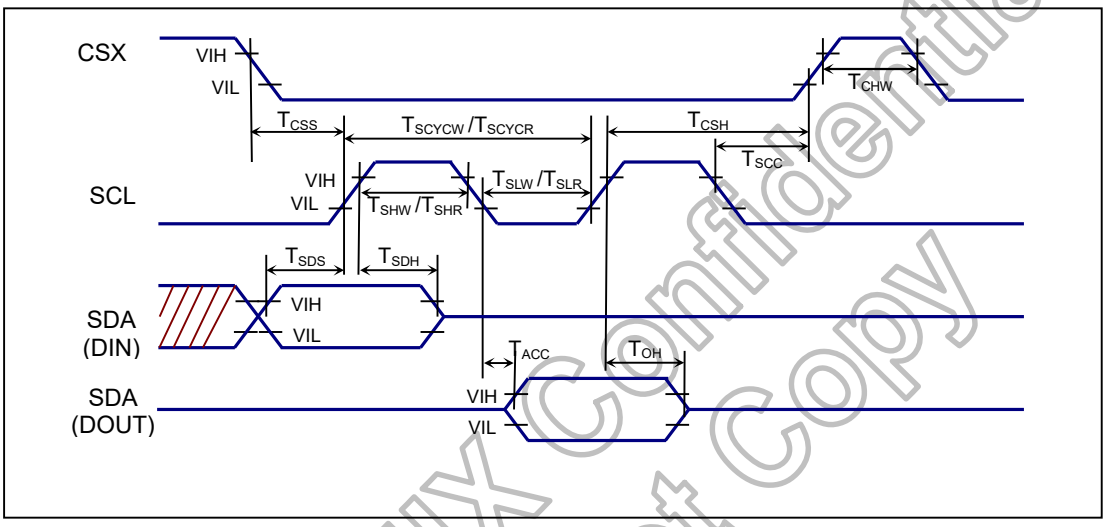


Figure 7.3: Serial Interface Characteristics

(VSSA=0V, IOVCC=1.8V, VCI=2.8V, T_A = 25°C)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	t_{CSS}	Chip select setup time (Write)	15	-	ns	-
	t_{CSS}	Chip select setup time (Read)	60	-		
	t_{CSH}	Chip select hold time (Write)	15	-		
	t_{CSH}	Chip select hold time (Read)	65	-		
DCX	t_{AST}	Address setup time	0	-	ns	-
	t_{AHT}	Address hold time (Write/Read)	10	-		
SCL (Write)	t_{WC}	Write cycle	66	-	ns	-
	t_{WRH}	Control pulse “H” duration	15	-		
	t_{WRL}	Control pulse “L” duration	15	-		
SCL (Read)	t_{RC}	Read cycle	150	-	ns	-
	t_{RDH}	Control pulse “H” duration	60	-		
	t_{RDL}	Control pulse “L” duration	60	-		
SDA (Input)	t_{DS}	Data setup time	10	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	t_{DH}	Data hold time	10	-		
SDA (Output)	t_{ACC}	Read access time	-	100	ns	
	t_{OH}	Output disable time	10	-		

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Table 7.2: Serial Interface Characteristics

7.3.2 DSI Interface Timing Characteristics

High Speed Mode

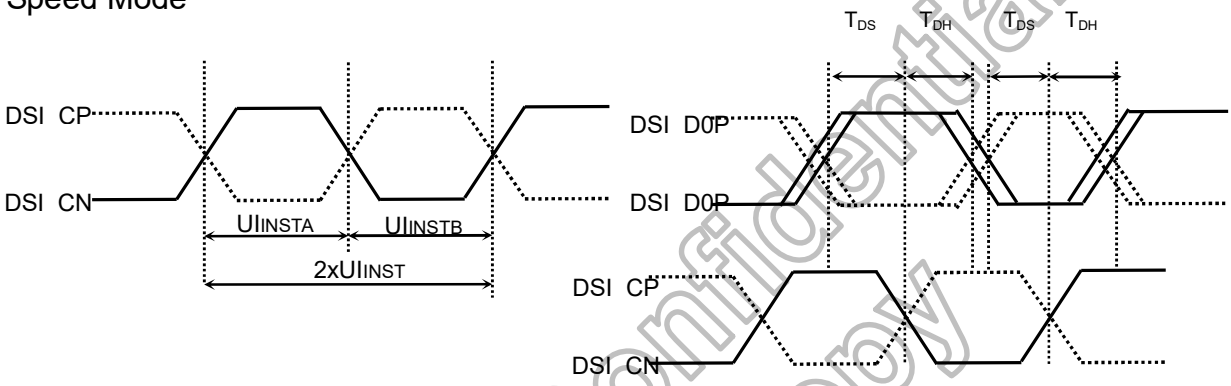


Figure 7.4: DSI clock timing Characteristics

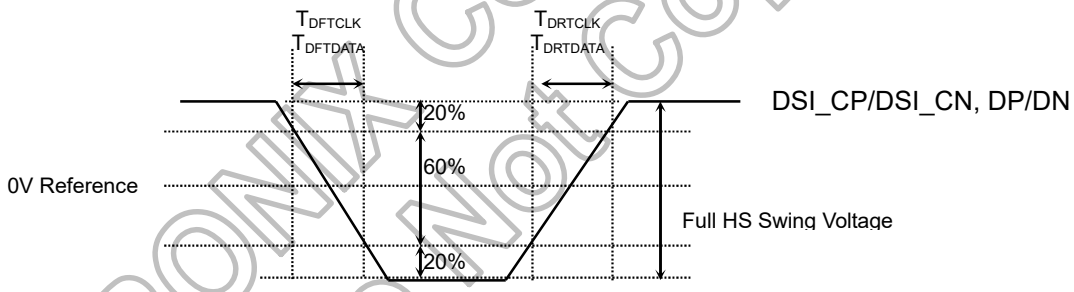


Figure 7.5: Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	2xUINST	TBD	-	25	ns
	UI instantaneous	UINSTA UINSTB	TBD	-	12.5	ns
DP/DN	Data to clock setup time	TDS	0.15xUI	-	-	ps
	Data to clock hold time	TDH	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	TDRTCLK	150	-	0.3UI	ps
	Differential fall time for clock	TDFTCLK	150	-	0.3UI	ps
DP/DN	Differential rise time for data	TDRTDATA	150	-	0.3UI	ps
	Differential fall time for data	TDFTDATA	150	-	0.3UI	ps

Table 7.3: DSI High Speed Mode characteristics

Low Power Mode

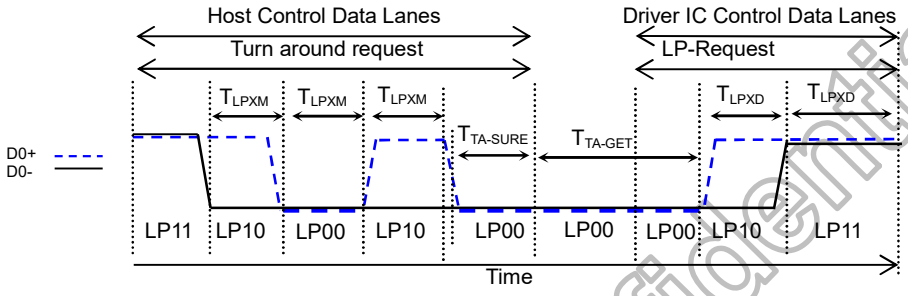


Figure 7.6: BTA from HOST to Display module Timing

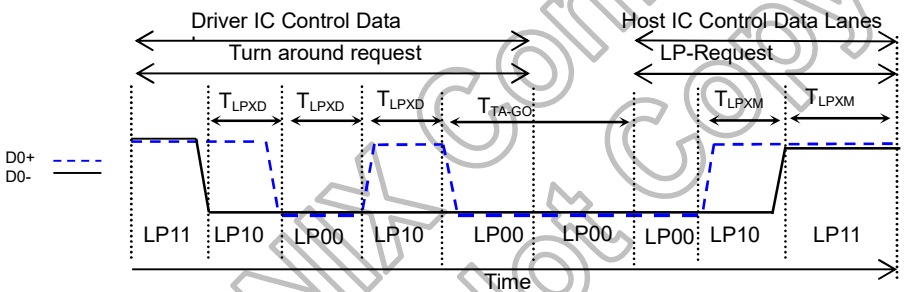


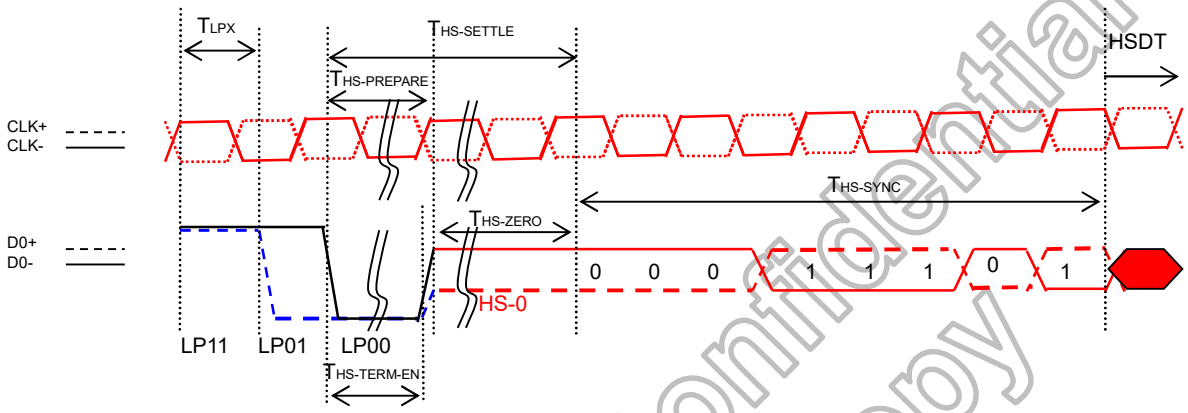
Figure 7.7: BTA from Display module Timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→ Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module →Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	2xT_{LPXD}	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

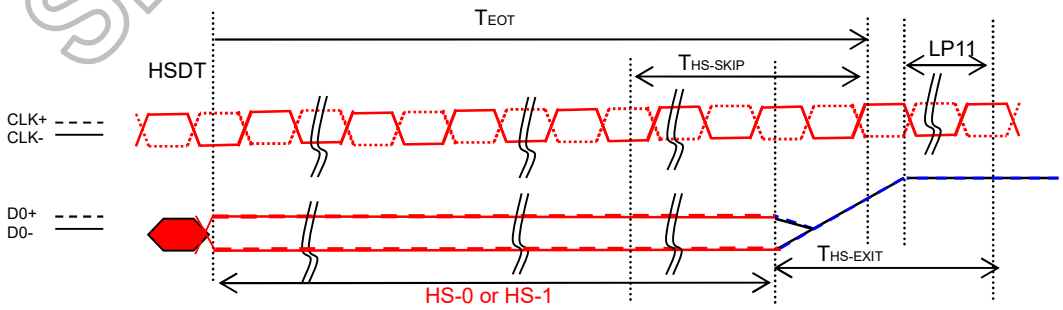
Table 7.4: DSI Low Power Mode characteristics

DSI BURSTS



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T_{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	$T_{HS-TERM-EN}$	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

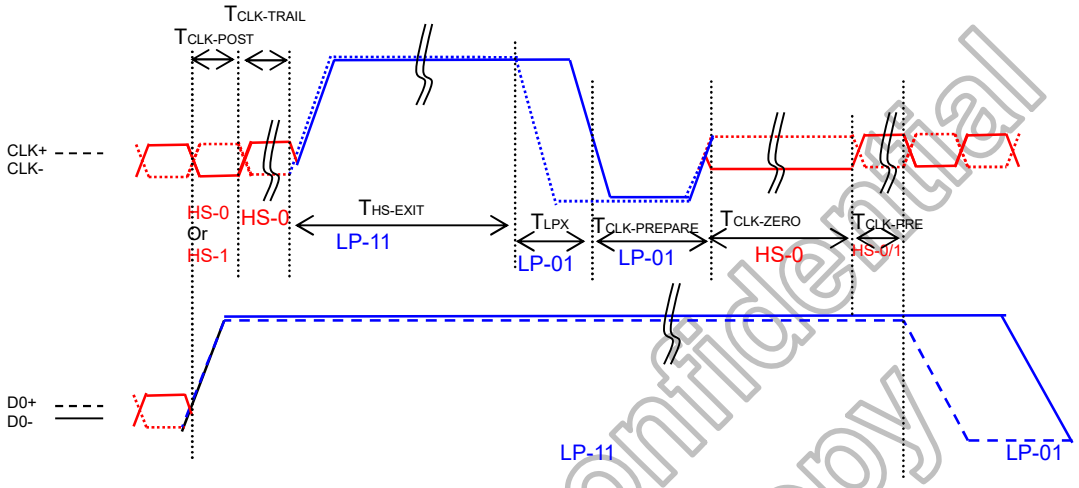
Table 7.5: DSI Low Power Mode to High Speed Mode Timing



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	$T_{HS-SKIP}$	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	$T_{HS-EXIT}$	100	-	-	ns

Table 7.6: DSI Low Power Mode to High Speed Mode Timing



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns
	Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	$T_{CLK-PREPARE}$	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	$T_{CLK-TERM-EN}$	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	8xUI			

Table 7.7: Clock Lanes High Speed Mode to/from Low Power Mode Timings

7.3.3 Reset input timing

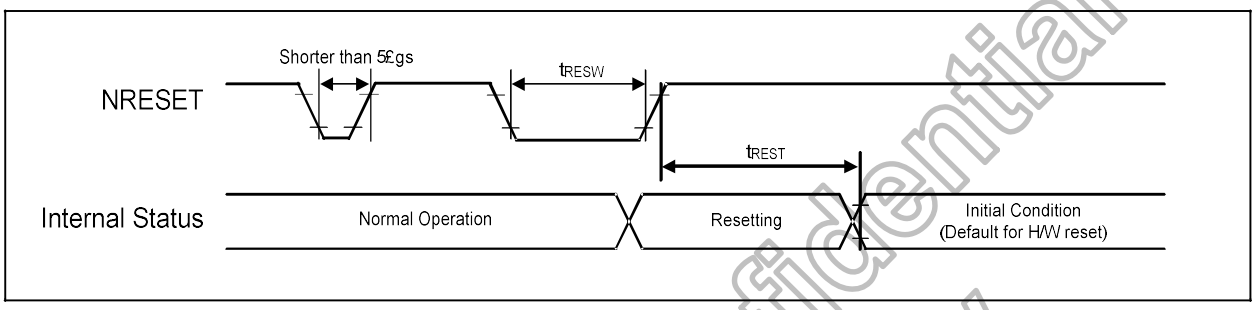


Figure 7.8: Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	5	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table 7.8: Reset input timing

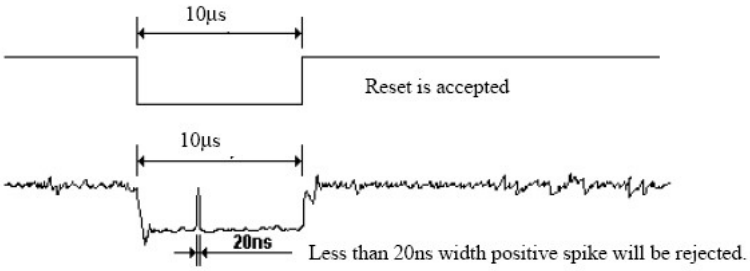
Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.

(4) Spike Rejection also applies during a valid reset pulse as shown as below:



(5) It is necessary to wait 5msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. Reference Application

8.1 Interface

The display, which is using DSI interface or RGB with SPI interface, is connected to the MPU as it is illustrated below.

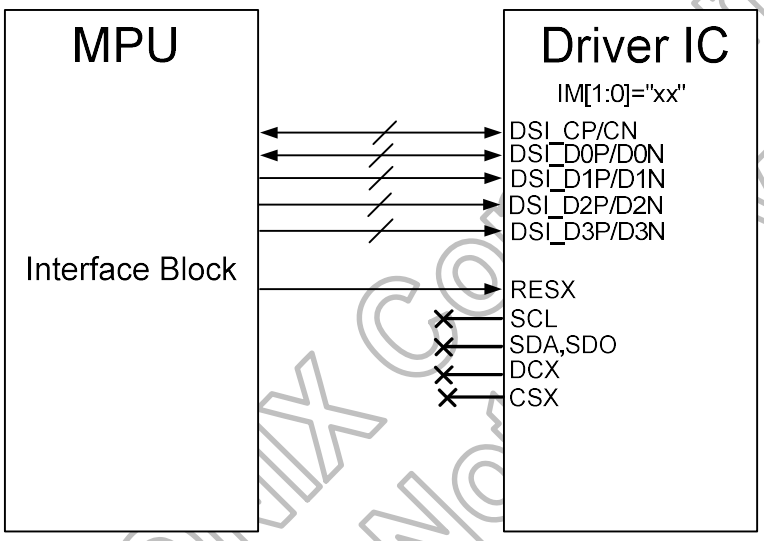
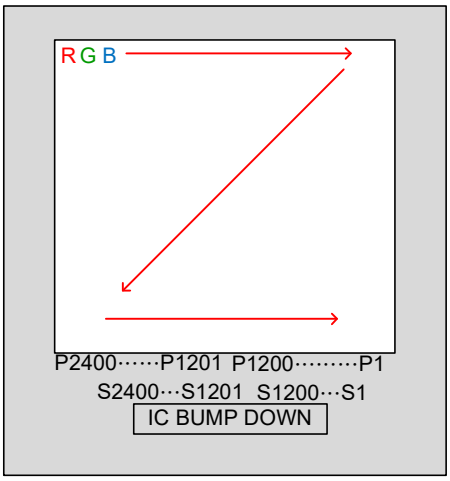
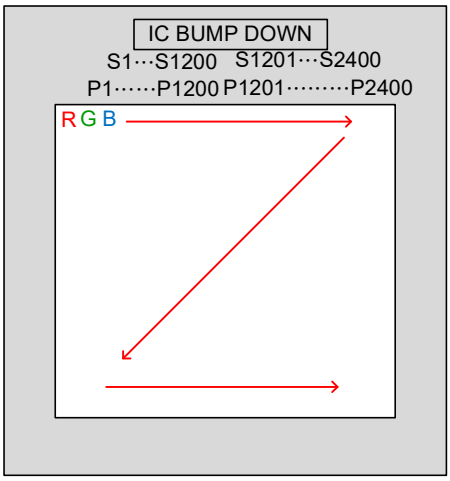


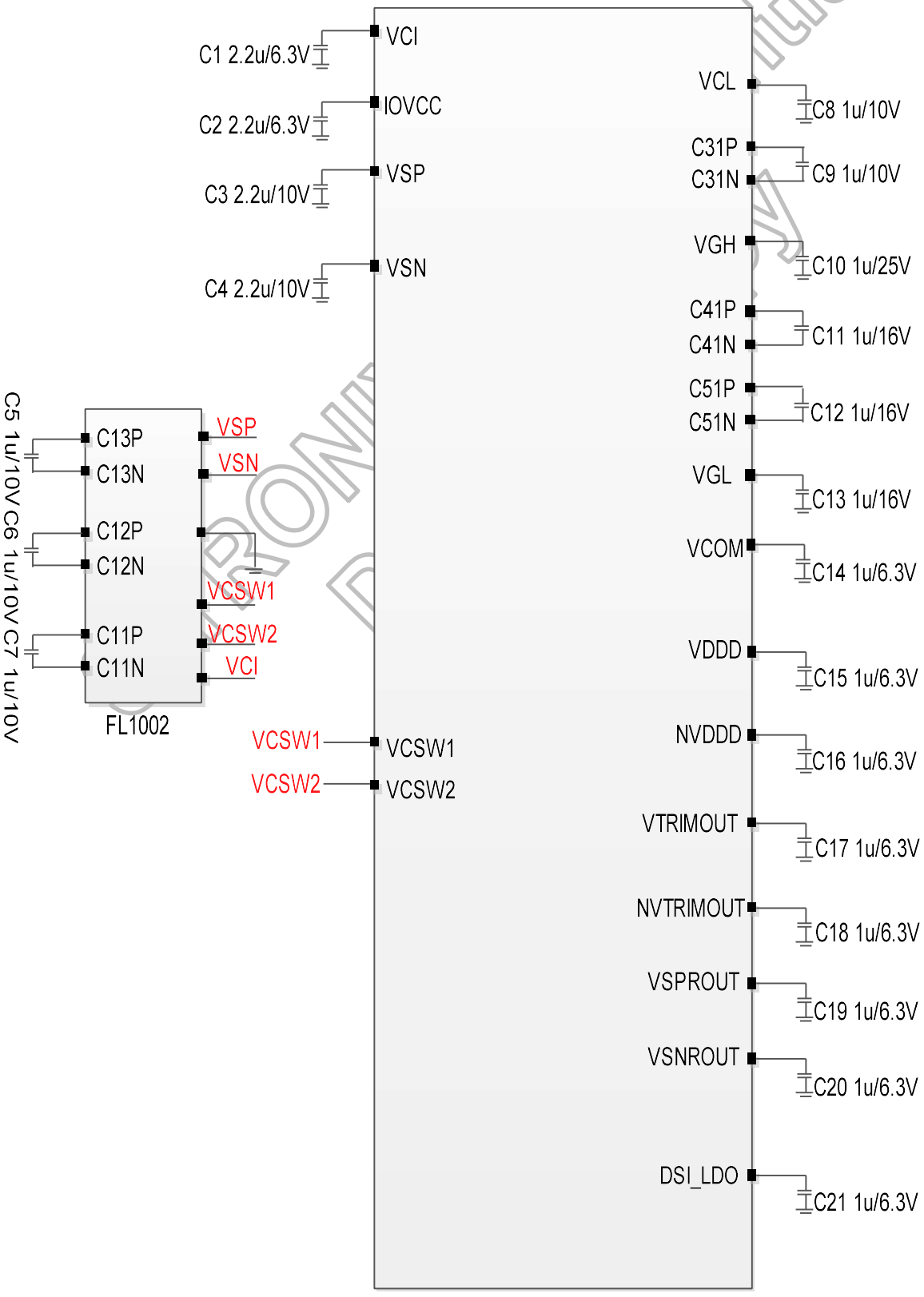
Figure 8.1: Interface for DSI Interface

8.2 Connections with Panel

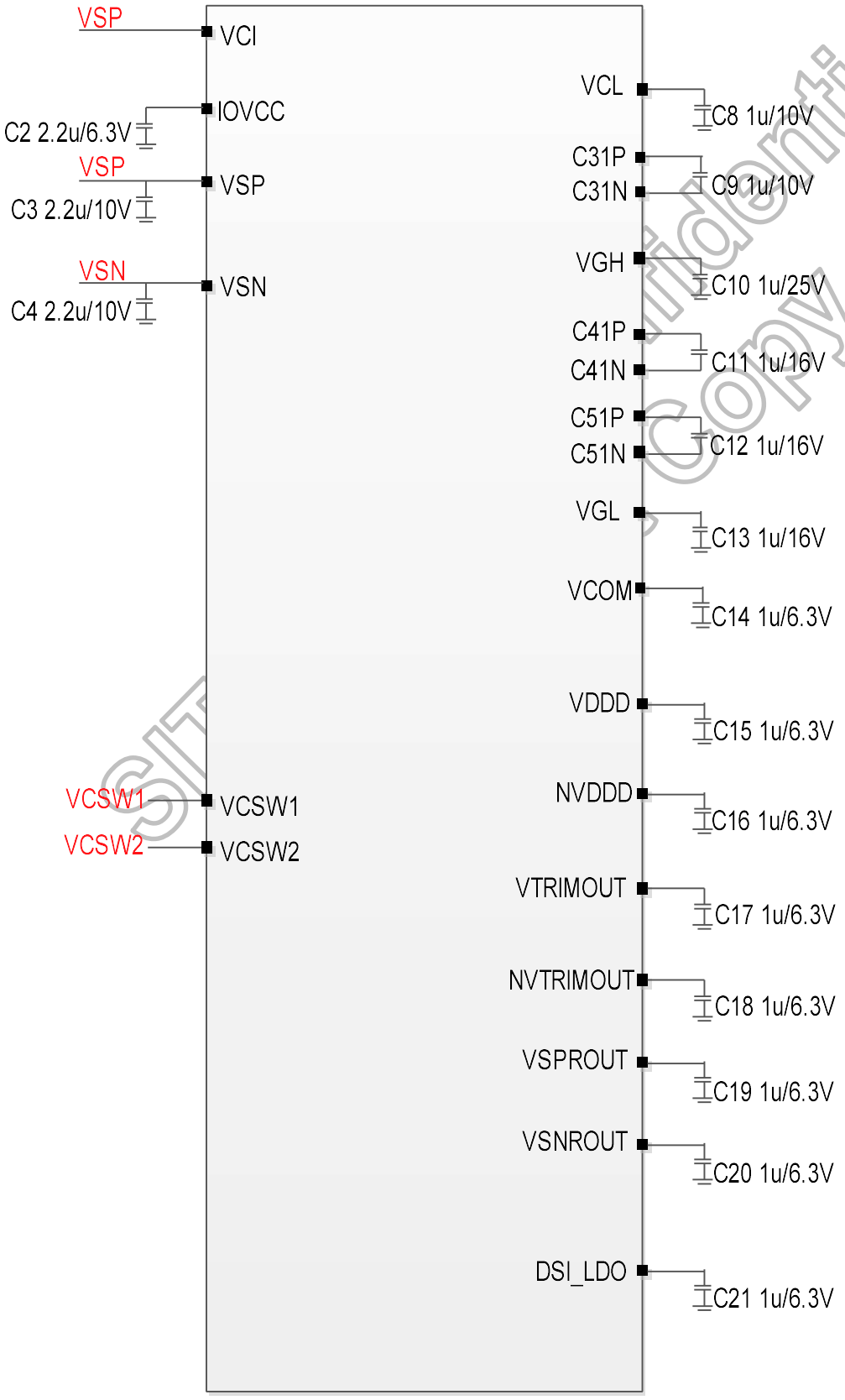
	
IC on Bottom Side of Module	IC on Bottom Side of Module
SS_PANEL='1' RGB_PANEL='1'	SS_PANEL='0' RGB_PANEL='0'

8.3 DC/DC Converter

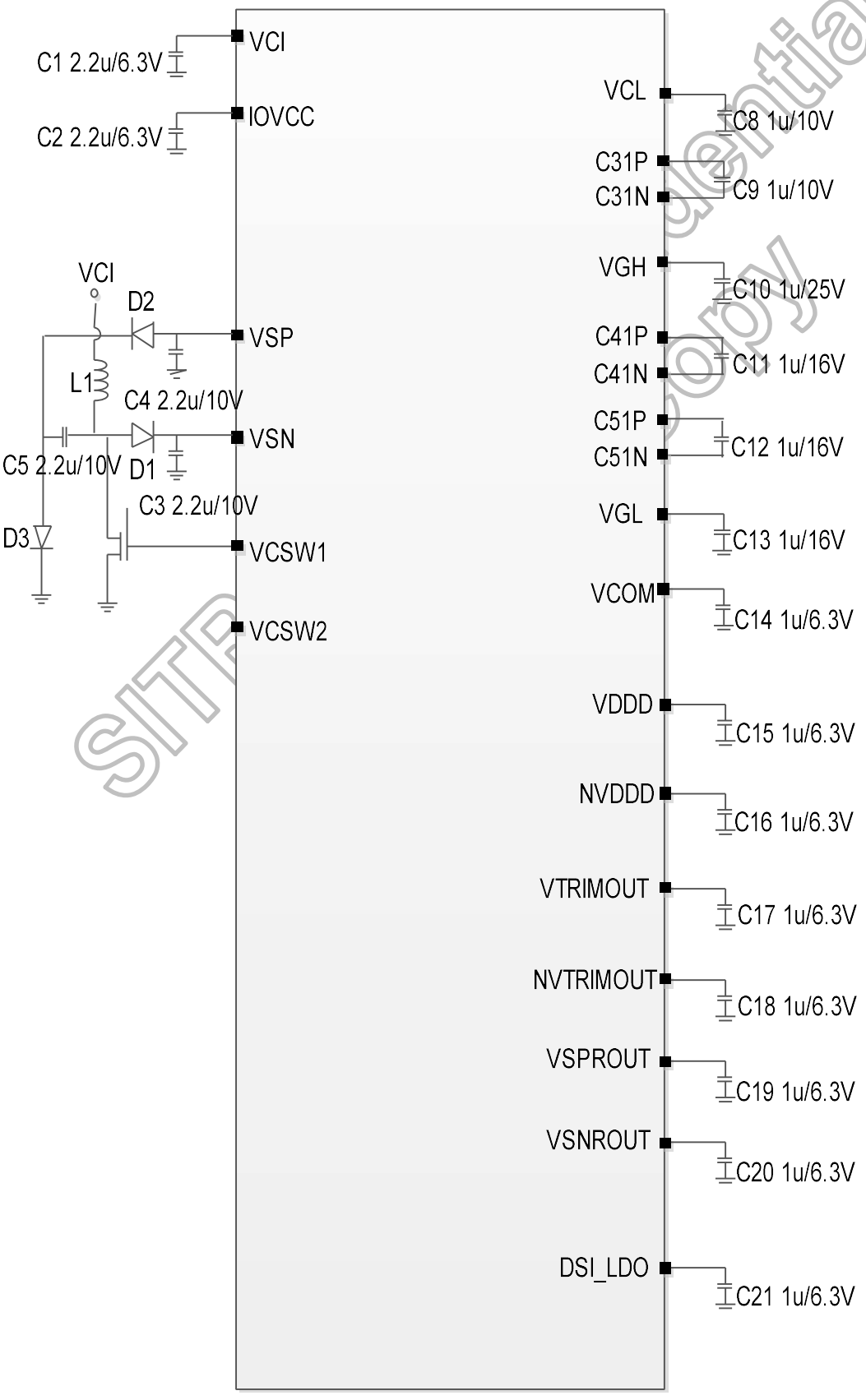
8.3.1 External Power IC(FL1002)



8.3.2 Three Power Mode



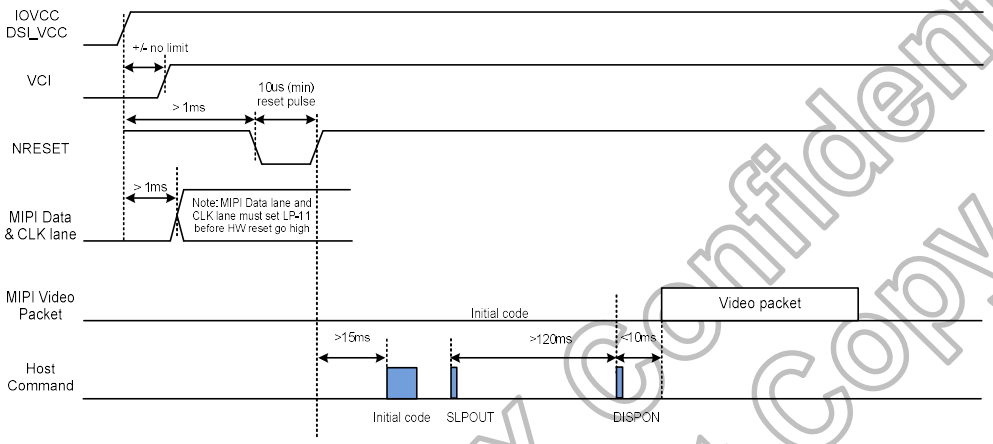
8.3.3 PFM Type C



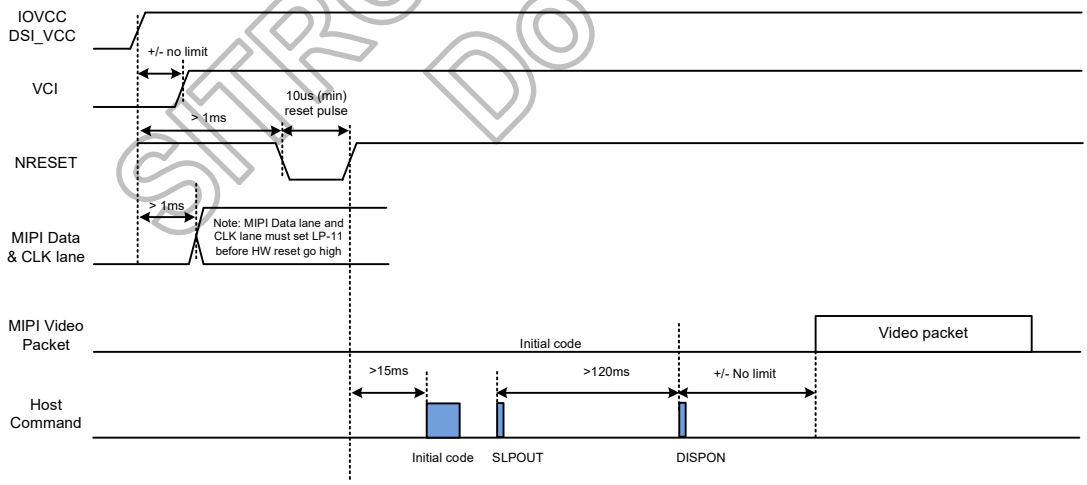
8.4 DSI Power On/Off Timing

8.4.1 Power on Timing

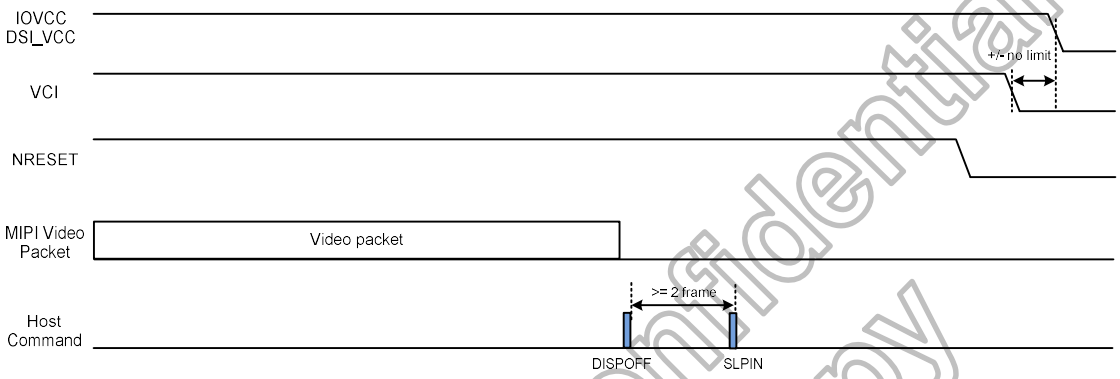
ESD_WHITE_EN=0



ESD_WHITE_EN=1



8.4.2 Power off Timing



8.5 Maximum layout resistance

Name	Type	Maximum layout resistance	Unit
IOVCC	Power supply	10	Ω
VCI	Power supply	5	Ω
VSSD	Power supply	10	Ω
VSSA	Power supply	10	Ω
DSI_VCC	Power supply	10	Ω
DSI_VSS	Power supply	10	Ω
VCSW1	Output	30	Ω
VCSW2_	Output	30	Ω
IM1,IM0,LANSEL	Input	100	Ω
DCX,SCL,CSX,RESX	Input	100	Ω
T_HSYNC,T_VSYNC,T_DE ,T_PCLK	Input	100	Ω
SDA	Input/Output	100	Ω
SDO, GPO[3:0]	Output	100	Ω
T_DB[7:0]	Input	100	Ω
VOUT,HOUT, PWM	Output	100	Ω
VCOM	Output	10	Ω
DSI_D0P	Input/Output	8	Ω
DSI_D0N	Input/Output	8	Ω
DSI_CP	Input	8	Ω
DSI_CN	Input	8	Ω
DSI_D1P/D2P/D3P	Input	8	Ω
DSI_D1N/D2N/D3P	Input	8	Ω
VDDD, NVDDDOUT	Capacitor Connection	10	Ω
VSP,VSN	Capacitor Connection	10	Ω
VSPROUT, VSNROUT	Capacitor Connection	10	Ω
VTRIMOUT, NVTRIMOUT	Capacitor Connection	10	Ω
VGL	Capacitor Connection	10	Ω
VGH	Capacitor Connection	10	Ω
VCL	Capacitor Connection	10	Ω
DSI_LDO	Capacitor Connection	10	Ω
OSC_OUT	Input	100	Ω
C31P,C31N,	Capacitor Connection	5	Ω
C41P,C41N,	Capacitor Connection	5	Ω
C51P,C51N,	Capacitor Connection	5	Ω
TEST[4:1], PM1, PM0	Input	100	Ω
VTESTOUTP, VTESTOUTN	Output	100	Ω
GOUT1~22_L	Output	30	Ω
GOUT1~22_R	Output	30	Ω