PCIe-6323 Specifications

2023-05-15

Contents

PCIe-6323 Specifications

The following specifications are typical at 25 °C, unless otherwise noted. For more information about the PCIe-6323, refer to the X Series User Guide available from ni.com/manuals.

Analog Input

Number of channels	16 differential or 32 single ended
ADC resolution	16 bits
DNL	No missing codes guaranteed
INL	Refer to the AI Absolute Accuracy section.
Sample rate	
Single channel maximum	250 kS/s
Multichannel maximum (aggregate)	250 kS/s
Minimum	No minimum
Timing resolution	10 ns
Timing accuracy	50 ppm of sample rate
Input coupling	DC
Input range	±0.2 V, ±1 V, ±5 V, ±10 V

Maximum working voltage for analog inputs (signal + common mode)	±11 V of AI GND
CMRR (DC to 60 Hz)	100 dB
Input impedance	
Device on	
AI+ to AI GND	>10 GΩ in parallel with 100 pF
AI- to AI GND	>10 GΩ in parallel with 100 pF
Device off	
AI+ to AI GND	1,200 Ω
AI- to AI GND	1,200 Ω
Input bias current	±100 pA
Crosstalk (at 100 kHz)	
Adjacent channels	-75 dB
Non-adjacent channels	-90 dB
Small signal bandwidth (-3 dB)	700 kHz
Input FIFO size	4,095 samples
Scan list memory	4,095 entries
Data transfers	DMA (scatter-gather), programmed I/O
Overvoltage protection for all analog input and sense channels	
Device on	±25 V for up to two AI pins

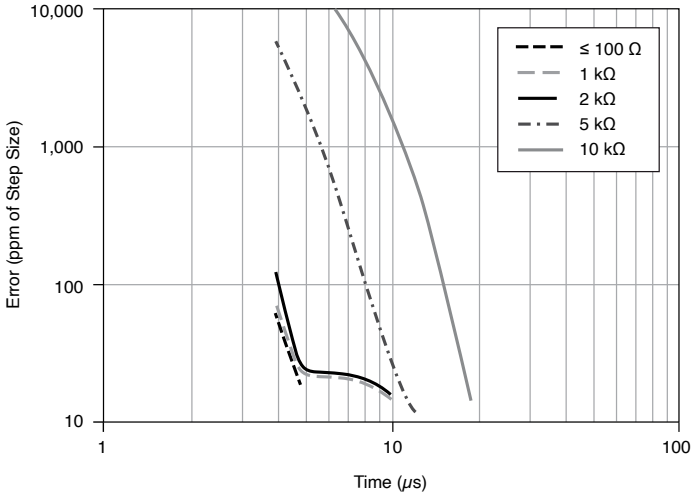
Device off	±15 V for up to two AI pins
Input current during overvoltage condition	±20 mA max/AI pin

Settling Time for Multichannel Measurements

Accuracy, full-scale step, all ranges	
±90 ppm of step (±6 LSB)	4 µs convert interval
±30 ppm of step (±2 LSB)	5 µs convert interval
±15 ppm of step (±1 LSB)	7 µs convert interval

Typical Performance Graph

Figure 1. Settling Error versus Time for Different Source Impedances



AI Absolute Accuracy

Table 1. AI Absolute Accuracy

Nominal Range Positive Full Scale	Nominal Range Negative Full Scale	Residual Gain Error (ppm of Reading)	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	Random Noise, σ (µVrms)	Absolute Accuracy at Full Scale (µV)
10	-10	65	13	24	229	2,220
5	-5	72	13	25	118	1,140
1	-1	78	17	37	26	257
0.2	-0.2	105	27	93	12	69

For more information about absolute accuracy at full scale, refer to the AI Absolute Accuracy Example section.

Gain tempco	7.3 ppm/°C
Reference tempco	5 ppm/°C
INL error	60 ppm of range

Note Accuracies listed are valid for up to two years from the device external calibration.

AI Absolute Accuracy Equation

AbsoluteAccuracy = **Reading** · **(GainError)** + **Range** · **(OffsetError)** + **NoiseUncertainty**

- **GainError** = **ResidualGainError** + **GainTempco** · **(TempChangeFromLastInternalCal)** + **ReferenceTempco** · **(TempChangeFromLastExternalCal)**
- **OffsetError** = **ResidualOffsetError** + **OffsetTempco** · **(TempChangeFromLastInternalCal)** + **INLError**

- **NoiseUncertainty** = $\frac{\text{Random Noise} \quad 3}{\sqrt{10,000}}$ for a coverage factor of 3 σ and averaging 10,000 points.

AI Absolute Accuracy Example

Absolute accuracy at full scale on the analog input channels is determined using the following assumptions:

- **TempChangeFromLastExternalCal** = 10 °C
- **TempChangeFromLastInternalCal** = 1 °C
- **number_of_readings** = 10,000
- **Coveragefactor** = 3 σ

For example, on the 10 V range, the absolute accuracy at full scale is as follows:

- **GainError** = 65 ppm + 7.3 ppm · 1 + 5 ppm · 10 = 122 ppm
- **OffsetError** = 13 ppm + 24 ppm · 1 + 60 ppm = 97 ppm
- **NoiseUncertainty** = $\frac{229\ \mu\text{V} \quad 3}{\sqrt{10,000}}$ = 6.9 µV
- **AbsoluteAccuracy** = 10 V · (**GainError**) + 10 V · (**OffsetError**) + **NoiseUncertainty** = 2,220 µV

Analog Output

Number of channels	4
DAC resolution	16 bits
DNL	±1 LSB
Monotonicity	16 bit guaranteed

Maximum update rate	
1 channel	900 kS/s
2 channels	840 kS/s per channel
3 channels	775 kS/s per channel
4 channels	719 kS/s per channel
Timing accuracy	50 ppm of sample rate
Timing resolution	10 ns
Output range	±10 V
Output coupling	DC
Output impedance	0.2 Ω
Output current drive	±5 mA
Overdrive protection	±15 V
Overdrive current	15 mA
Power-on state	±20 mV
Power-on/off glitch	2 V for 500 ms
Output FIFO size	8,191 samples shared among channels used
Data transfers	DMA (scatter-gather), programmed I/O

AO waveform modes	Non-periodic waveform, periodic waveform regeneration mode from onboard FIFO, periodic waveform regeneration from host buffer including dynamic update
Settling time, full-scale step, 15 ppm (1 LSB)	6 µs
Slew rate	15 V/µs
Glitch energy	
Magnitude	100 mV
Duration	2.6 µs

AO Absolute Accuracy

Absolute accuracy at full-scale numbers is valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration.

Table 2. AO Absolute Accuracy

Nominal Range Positive Full Scale	Nominal Range Negative Full Scale	Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco (ppm/°C)	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	INL Error (ppm of Range)	Absolute Accuracy at Full Scale (µV)
10	-10	80	11.3	5	53	4.8	128	3,271

Note Accuracies listed are valid for up to two years from the device external calibration.

AO Absolute Accuracy Equation

AbsoluteAccuracy = **OutputValue** · **(GainError)** + **Range** · **(OffsetError)**

- **GainError** = **ResidualGainError** + **GainTempco** · **(TempChangeFromLastInternalCal)** + **ReferenceTempco** · (**TempChangeFromLastExternalCal)**
- **OffsetError** = **ResidualOffsetError** + **OffsetTempco** · **(TempChangeFromLastInternalCal)** + **INLError**

Digital I/O/PFI

Static Characteristics

Number of channels	48 total, 32 (P0.<0..31>), 16 (PFI <0..7>/P1, PFI <8..15>/P2)
Ground reference	D GND
Direction control	Each terminal individually programmable as input or output
Pull-down resistor	50 kΩ typical, 20 kΩ minimum
Input voltage protection	±20 V on up to two pins

Caution Stresses beyond those listed under the **Input voltage protection** specification may cause permanent damage to the device.

Waveform Characteristics (Port 0 Only)

Terminals used	Port 0 (P0.<0..31>)
Port/sample size	Up to 32 bits
Waveform generation (DO) FIFO	2,047 samples

Waveform acquisition (DI) FIFO	255 samples
DO or DI Sample Clock frequency	0 to 1 MHz, system and bus activity dependent
Data transfers	DMA (scatter-gather), programmed I/O
Digital line filter settings	160 ns, 10.24 µs, 5.12 ms, disable

PFI/Port 1/Port 2 Functionality

Functionality	Static digital input, static digital output, timing input, timing output
Timing output sources	Many AI, AO, counter, DI, DO timing signals
Debounce filter settings	90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable high and low transitions; selectable per input

Recommended Operating Conditions

Input high voltage (V_{IH})	
Minimum	2.2 V
Maximum	5.25 V
Input low voltage (V_{IL})	
Minimum	0 V
Maximum	0.8 V
Output high current (I_{OH})	

P0.<0..31>	-24 mA maximum
PFI <0..15>/P1/P2	-16 mA maximum
Output low current (I_{OL})	
P0.<0..31>	24 mA maximum
PFI <0..15>/P1/P2	16 mA maximum

Digital I/O Characteristics

Positive-going threshold (VT+)	2.2 V maximum
Negative-going threshold (VT-)	0.8 V minimum
Delta VT hysteresis (VT+ - VT-)	0.2 V minimum
I_{IL} input low current (V_{IN} = 0 V)	-10 µA maximum
I_{IH} input high current (V_{IN} = 5 V)	250 µA maximum

Figure 2. P0.<0..31>: I_{OH} versus V_{OH}

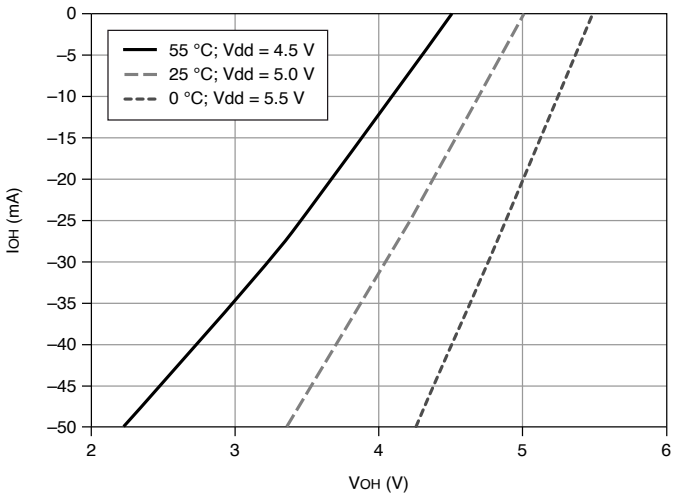


Figure 3. P0.<0..31>: I_{OL} versus V_{OL}

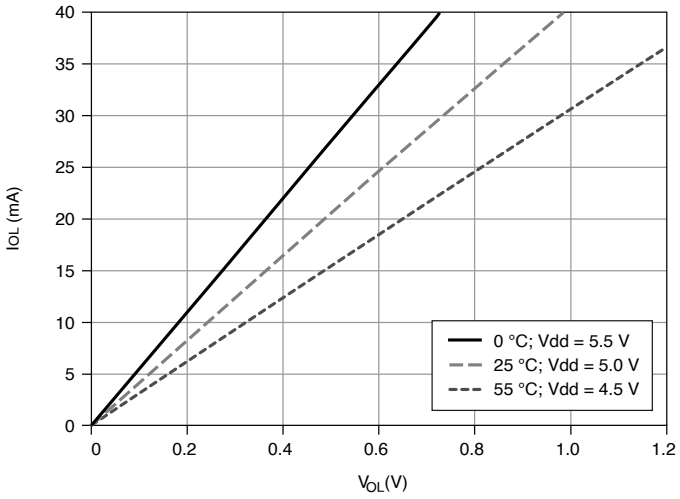


Figure 4. PFI <0..15>/P1/P2: I_{OH} versus V_{OH}

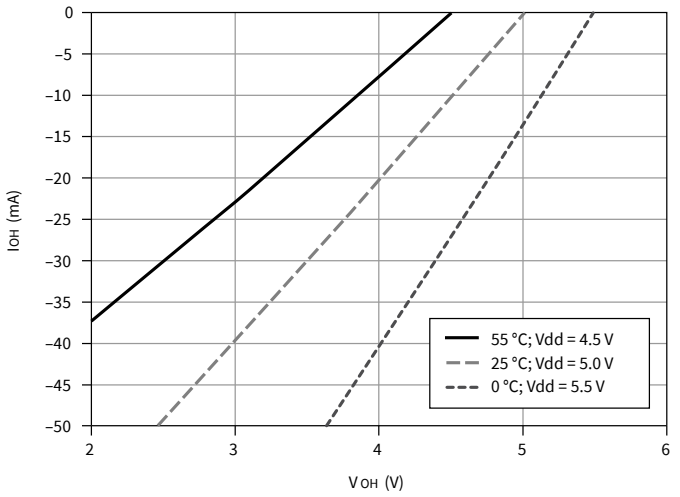
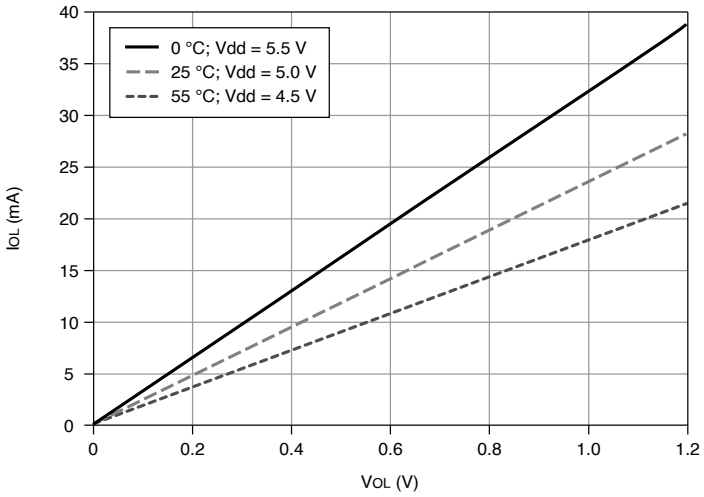


Figure 5. PFI <0..15>/P1/P2: I_{OL} versus V_{OL}



General-Purpose Counters

Number of counter/timers	4
Resolution	32 bits
Counter measurements	Edge counting, pulse, pulse width, semi-period, period, two-edge separation
Position measurements	X1, X2, X4 quadrature encoding with Channel Z reloading; two-pulse encoding
Output applications	Pulse, pulse train with dynamic updates, frequency division, equivalent time sampling
Internal base clocks	100 MHz, 20 MHz, 100 kHz
External base clock frequency	0 to 25 MHz
Base clock accuracy	50 ppm

Inputs	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down, Sample Clock
Routing options for inputs	Any PFI, RTSI, many internal signals
FIFO	127 samples per counter
Data transfers	Dedicated scatter-gather DMA controller for each counter/timer, programmed I/O

Frequency Generator

Number of channels	1
Base clocks	20 MHz, 10 MHz, 100 kHz
Divisors	1 to 16
Base clock accuracy	50 ppm

Output can be available on any PFI or RTSI terminal.

Phased-Locked Loop (PLL)

Number of PLLs	1

Table 3. Reference Clock Locking Frequencies

Reference Signal	Locking Input Frequency (MHz)
RTSI <0..7>	10, 20
PFI <0..15>	10, 20

Output of PLL	100 MHz Timebase; other signals derived from 100 MHz Timebase including 20 MHz and 100 kHz Timebases

External Digital Triggers

Source	Any PFI, RTSI
Polarity	Software-selectable for most signals
Analog input function	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase
Analog output function	Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase
Counter/timer functions	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down, Sample Clock
Digital waveform generation (DO) function	Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase
Digital waveform acquisition (DI) function	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase

Device-to-Device Trigger Bus

Input source	RTSI <0..7>
Output destination	RTSI <0..7>

Output selections	10 MHz Clock, frequency generator output, many internal signals
Debounce filter settings	90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable high and low transitions; selectable per input

Bus Interface

Form factor	x1 PCI Express, specification v1.1 compliant
Slot compatibility	x1, x4, x8, and x16 PCI Express slots
DMA channels	8, can be used for analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1, counter/timer 2, counter/timer 3

Power Requirements

Caution The protection provided by the device can be impaired if the device is used in a manner not described in the **X Series User Manual.**

Without disk drive power connector installed	
+3.3 V	1.4 W
+12 V	8.6 W
With disk drive power connector installed	
+3.3 V	1.4 W
+12 V	3 W

+5 V	15 W

Current Limits

Caution Exceeding the current limits may cause unpredictable behavior by the device and/or PC.

Without disk drive power connector installed	
P0/PFI/P1/P2 and +5 V terminals combined	1 A max
With disk drive power connector installed	
+5 V terminal (connector 0)	1 A max
+5 V terminal (connector 1)	1 A max
P0/PFI/P1/P2 combined	1 A max

Physical Characteristics

Printed circuit board dimensions	9.9 × 16.8 cm (3.9 × 6.6 in.) (half-length)
Weight	114 g (4.0 oz)
I/O connector	2 68-pin VHDCI

Table 4. Mating Connectors

Manufacturer, Part Number	Description
MOLEX 71430-0011	68-Pos Right Angle Single Stack PCB-Mount VHDCI (Receptacle)
MOLEX 74337-0016	68-Pos Right Angle Dual Stack PCB-Mount VHDCI (Receptacle)

Manufacturer, Part Number	Description
MOLEX 71425-3001	68-Pos Offset IDC Cable Connector (Plug) (SHC68-*)
Disk drive power connector	Standard ATX peripheral connector (not serial ATA)

Calibration

Recommended warm-up time	15 minutes
Calibration interval	2 years

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Caution The protection provided by the DAQ device can be impaired if it is used in a manner not described in the **X Series User Manual**.

Channel to earth	11 V, Measurement Category I

Note Measurement Categories CAT I and CAT O (Other) are equivalent. These test and measurement circuits are not intended for direct connection to the MAINs building installations of Measurement Categories CAT II, CAT III, or CAT IV.

Environmental

Operating temperature	0 to 50 °C

Storage temperature	-40 to 70 °C
Operating humidity	10 to 90% RH, noncondensing
Storage humidity	5 to 95% RH, noncondensing
Pollution Degree	2
Maximum altitude	2,000 m

Indoor use only.

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)
- 2011/65/EU; Restriction of Hazardous Substances (RoHS)

- 2014/53/EU; Radio Equipment Directive (RED)
- 2014/34/EU; Potentially Explosive Atmospheres (ATEX)

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Engineering a Healthy Planet** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）

- **中国 RoHS**— NI 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 NI 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

Device Pinout

Figure 6. NI PCIe-6323 Pinout