



# dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04

## dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 Family Silicon Errata and Data Sheet Clarification

The dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 family devices that you have received conform functionally to the current Device Data Sheet (DS70291D), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 silicon.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (A4).

Data Sheet clarifications and corrections start on page 10, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site ([www.microchip.com](http://www.microchip.com)).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICkit 3.
2. From the main menu in MPLAB IDE, select Configure>Select Device, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (Debugger>Select Tool).
4. Perform a "Connect" operation to the device (Debugger>Connect). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

**Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 silicon revisions are shown in Table 1.

**TABLE 1: SILICON DEVREV VALUES**

| Part Number      | Device ID <sup>(1)</sup> | Revision ID for Silicon Revision <sup>(2)</sup> |        |        |        |
|------------------|--------------------------|---|--------|--------|--------|
|                  |                          | A1  | A2     | A3     | A4     |
| dsPIC33FJ32MC302 | 0x0601                   | 0x3001  | 0x3002 | 0x3002 | 0x3003 |
| dsPIC33FJ32MC304 | 0x0603                   |   |        |        |        |
| dsPIC33FJ64MC202 | 0x0611                   |   |        |        |        |
| dsPIC33FJ64MC204 | 0x0613                   |   |        |        |        |
| dsPIC33FJ64MC802 | 0x0619                   |   |        |        |        |
| dsPIC33FJ64MC804 | 0x061B                   |   |        |        |        |

**Note 1:** The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

**2:** Refer to the "dsPIC33F/PIC24H Flash Programming Specification" (DS70152) for detailed information on Device and Revision IDs for your specific device.

**TABLE 1: SILICON DEVREV VALUES (CONTINUED)**

| Part Number       | Device ID <sup>(1)</sup> | Revision ID for Silicon Revision <sup>(2)</sup> |        |        |        |
|-------------------|--------------------------|---|--------|--------|--------|
|                   |                          | A1  | A2     | A3     | A4     |
| dsPIC33FJ128MC202 | 0x0621                   | 0x3001  | 0x3002 | 0x3002 | 0x3003 |
| dsPIC33FJ128MC204 | 0x0623                   |   |        |        |        |
| dsPIC33FJ128MC802 | 0x0629                   |   |        |        |        |
| dsPIC33FJ128MC804 | 0x062B                   |   |        |        |        |

**Note 1:** The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

**2:** Refer to the “dsPIC33F/PIC24H Flash Programming Specification” (DS70152) for detailed information on Device and Revision IDs for your specific device.

**TABLE 2: SILICON ISSUE SUMMARY**

| Module            | Feature            | Item Number | Issue Summary  | Affected Revisions <sup>(1)</sup> |    |    |    |
|-------------------|--------------------|-------------|--|-----------------------------------|----|----|----|
|                   |                    |             |  | A1                                | A2 | A3 | A4 |
| UART              | IR Mode            | 1.          | The 16x baud clock signal on the BCLK pin is present only when the module is transmitting.   | X                                 | X  | X  | X  |
| UART              | High-Speed Mode    | 2.          | When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.  | X                                 | X  | X  | X  |
| SPI               | Transmit Operation | 3.          | The SPI Transmit Buffer Full (SPITBF) flag does not get set immediately after writing to the buffer.   | X                                 | X  | X  | X  |
| SPI               | Frame Mode         | 4.          | The SPI module will generate incorrect frame synchronization pulses in Frame Master mode if FRMDLY = 1.  | X                                 | X  | X  | X  |
| I <sup>2</sup> C™ | SFR Writes         | 5.          | The BCL bit in I2CSTAT can only be cleared with Word instructions, and can be corrupted with byte instructions and bit operations.   | X                                 | X  | X  | X  |
| I <sup>2</sup> C  | 10-bit Addressing  | 6.          | When the I <sup>2</sup> C module is configured for 10-bit addressing using the same address bits (A10 and A9) as other I <sup>2</sup> C devices, A10 and A9 bits may not work as expected.             | X                                 | X  | X  | X  |
| I <sup>2</sup> C  | 10-bit Addressing  | 7.          | When the I <sup>2</sup> C module is configured as a 10-bit slave with an address of 0x102, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02.                           | X                                 | X  | X  | X  |
| I <sup>2</sup> C  | —                  | 8.          | With the I <sup>2</sup> C module enabled, the PORT bits and external Interrupt Input functions (if any) associated with SCL and SDA pins will not reflect the actual digital logic levels on the pins. | X                                 | X  | X  | X  |
| I <sup>2</sup> C  | 10-bit Addressing  | 9.          | The 10-bit slave does not set the RBF flag or load the I2CxRCV register, on address match if the Least Significant bits (LSbs) of the address are the same as the 7-bit reserved addresses.            | X                                 | X  | X  | X  |
| I <sup>2</sup> C  | —                  | 10.         | After the ACKSTAT bit is set when receiving a NACK, it may be cleared by the reception of a Start or Stop bit.   | X                                 | X  | X  | X  |
| UART              | Interrupts         | 11.         | The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.   | X                                 | X  | X  | X  |

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

| Module                     | Feature                           | Item Number | Issue Summary   | Affected Revisions <sup>(1)</sup> |    |    |    |
|----------------------------|-----------------------------------|-------------|---|-----------------------------------|----|----|----|
|                            |                                   |             |   | A1                                | A2 | A3 | A4 |
| UART                       | IR Mode                           | 12.         | When the UART module is operating in 8-bit mode (PDSEL = 0x) and using the IrDA <sup>®</sup> encoder/decoder (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h. | X                                 | X  | X  | X  |
| Comparator                 | Output Pin                        | 13.         | When CMCON<CxOUTEN> bit is set, the Comparator output pin cannot be used as a general purpose I/O pin even if the Comparator is disabled.   | X                                 | X  | X  | X  |
| Internal Voltage Regulator | Sleep Mode                        | 14.         | When the VREGS bit (RCON<8>) is set to a logic '0' the device may reset and higher Sleep current may be observed.   | X                                 | X  | X  | X  |
| PSV Operations             | —                                 | 15.         | An address error trap occurs in certain addressing modes when accessing the first four bytes of any PSV page.   | X                                 | X  | X  | X  |
| ECAN                       | Sleep Mode                        | 16.         | The WAKIF bit in the CxINTF register cannot be cleared by software instruction after the device is interrupted from Sleep due to activity on the CAN bus.                               | X                                 | X  | X  | X  |
| ECAN                       | Receive Operation                 | 17.         | The ECAN module may not store the received data in the correct location.  | X                                 | X  | X  |    |
| CPU                        | EXCH Instruction                  | 18.         | The EXCH instruction does not execute correctly.  | X                                 | X  | X  | X  |
| PWM                        | Debug Mode                        | 19.         | PTMR does not keep counting down after halting code execution in Debug mode.  | X                                 | X  | X  | X  |
| PWM                        | DOZE Mode                         | 20.         | The Motor Control PWM module generates more interrupts than expected when DOZE mode is used and the output postscaler value is different than 1:1.                                      | X                                 | X  | X  | X  |
| SPI                        | Transmit Operation                | 21.         | Writing to the SPIxBUF register as soon as TBF bit is cleared will cause SPI module to ignore written data.   | X                                 | X  | X  | X  |
| UART                       | Break Character Generation        | 22.         | The UART module will not generate back-to-back Break characters.  | X                                 | X  | X  | X  |
| QE1                        | Timer Gated Accumulation Mode     | 23.         | When Timer Gated Accumulation is enabled, the QE1 does not generate an interrupt on every falling edge.   | X                                 | X  | X  | X  |
| QE1                        | Timer Gated Accumulation Mode     | 24.         | When Timer Gated Accumulation is enabled, and an external signal is applied, the POSCNT increments and generates an interrupt after a match with MAXCNT.                                | X                                 | X  | X  | X  |
| Audio DAC                  | Voltage Specifications            | 25.         | The Audio DAC positive and negative output differential voltages may not meet the specifications listed in the data sheet.  | X                                 | X  | X  |    |
| ADC                        | Current Consumption in Sleep Mode | 26.         | If the ADC module is in an enabled state when the device enters Sleep Mode, the power-down current (IPD) of the device may exceed the device data sheet specifications.                 | X                                 | X  | X  | X  |
| JTAG                       | Boundary Scan                     | 27.         | On 28-pin devices, Boundary Scan does not function correctly for pin 7.   | X                                 | X  | X  | X  |
| RTCC                       | Operation During Reset            | 28.         | The RTCC module gets reset on any device Reset, instead of getting reset only on a POR or BOR.  | X                                 | X  | X  | X  |

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

## Silicon Errata Issues

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

### 1. Module: UART

When the UART is configured for IR interface operations (UxMODE<9:8> = 11), the 16x baud clock signal on the BCLK pin is present only when the module is transmitting. The pin is idle at all other times.

#### Work around

Configure one of the output compare modules to generate the required baud clock signal when the UART is receiving data or in an Idle state.

#### Affected Silicon Revisions

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

### 2. Module: UART

When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.

This issue does not affect the other UART configurations.

#### Work around

Use the 16x baud rate option (BRGH = 0) and adjust the baud rate accordingly.

#### Affected Silicon Revisions

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

### 3. Module: SPI

The SPI Transmit Buffer Full (SPITBF) flag does not get set immediately after writing to the buffer.

#### Work around

After a write to the SPI buffer, poll the SPITBF flag until the flag gets set, indicating that the transmit buffer is not full. Afterwards, poll the SPITBF flag again until the flag gets cleared, indicating that the transmit has started and that the transmit buffer is empty and another write can occur.

#### Affected Silicon Revisions

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

### 4. Module: SPI

The SPI module will generate incorrect frame synchronization pulses when configured in Frame Master mode if the start of data is selected to coincide with the start of the frame synchronization pulse (FRMEN = 1, SPIFSD = 0, FRMDLY = 1). However, the module functions correctly in Frame Slave mode, and also in Frame Master mode if FRMDLY = 0.

#### Work around

If DMA is not being used, manually drive the SSx pin (x = 1 or 2) high using the associated PORT register, and then drive it low after the required 1 bit-time pulse-width. This operation needs to be performed when the transmit buffer is written.

If DMA is being used, and if no other peripheral modules are using DMA transfers, use a timer interrupt to periodically generate the frame synchronization pulse (using the method described above) after every 8 or 16-bit periods (depending on the data word size, configured using the MODE16 bit).

If FRMDLY = 0, no work around is needed.

#### Affected Silicon Revisions

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

### 5. Module: I<sup>2</sup>C

The BCL bit in I2CSTAT can only be cleared with Word instructions, and can be corrupted with byte instructions and bit operations.

#### Work around

Use Word instructions to clear BCL.

#### Affected Silicon Revisions

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**6. Module: I<sup>2</sup>C**

If there are two I<sup>2</sup>C devices on the bus, one of them is acting as the Master receiver and the other as the Slave transmitter. If both devices are configured for 10-bit Addressing mode, and have the same value in the A10 and A9 bits of their addresses, then when the Slave select address is sent from the Master, both the Master and Slave acknowledge it. When the Master sends out the read operation, both the Master and the Slave enter into Read mode and both of them transmit the data. The resultant data will be the ANDing of the two transmissions.

**Work around**

In all I<sup>2</sup>C devices, the addresses as well as bits A10 and A9 should be different.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**7. Module: I<sup>2</sup>C**

When the I<sup>2</sup>C module is configured as a 10-bit slave with an address of 0x102, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02; however, the module acknowledges both address bytes.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**8. Module: I<sup>2</sup>C**

With the I<sup>2</sup>C module enabled, the PORT bits and external interrupt input functions (if any) associated with the SCL and SDA pins do not reflect the actual digital logic levels on the pins.

**Work around**

If the SDA and/or SCL pins need to be polled, these pins should be connected to other port pins in order to be read correctly. This issue *does not* affect the operation of the I<sup>2</sup>C module.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**9. Module: I<sup>2</sup>C**

In 10-bit Addressing mode, some address matches don't set the RBF flag or load the receive register I2CxRCV, if the lower address byte matches the reserved addresses. In particular, these include all addresses with the form XX0000XXXX and XX1111XXXX, with the following exceptions:

- 001111000X
- 011111001X
- 101111010X
- 111111011X

**Work around**

Ensure that the lower address byte in 10-bit Addressing mode does not match any 7-bit reserved addresses.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**10. Module: I<sup>2</sup>C**

When the I<sup>2</sup>C module is operating in either Master or Slave mode, after the ACKSTAT bit is set when receiving a NACK, it may be cleared by the reception of a Start or Stop bit.

**Work around**

Store the value of the ACKSTAT bit immediately after receiving a NACK from the master.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**11. Module: UART**

The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.

**Work around**

Read the error flags in the UxSTA register whenever a byte is received to verify the error status. In most cases, these bits will be correct, even if the UART error interrupt fails to occur.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**12. Module: UART**

When the UART is operating in 8-bit mode (PDSEL = 0x) and using the IrDA encoder/decoder (IREN = 1), the module incorrectly transmits a data payload of 80h as 00h.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**13. Module: Comparator**

If CMCON<CxOUTEN> bit is set and the comparator module CMCON<CxEN> bit is disabled, the remappable comparator output pins, C1OUT and C2OUT, cannot be used as general purpose I/O pins.

**Work around**

When the comparator module is disabled the CMCON<CxOUTEN> bit should be reset so that the remappable comparator output pins C1OUT and C2OUT are not driven onto the output pad.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**14. Module: Internal Voltage Regulator**

When the VREGS bit (RCON<8>) is set to a logic '0', the device may reset and a higher Sleep current may be observed.

**Work around**

Ensure VREGS bit (RCON<8>) is set to a logic '1' for device Sleep mode operation.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**15. Module: PSV Operations**

An address error trap occurs in certain addressing modes when accessing the first four bytes of an PSV page. This only occurs when using the following addressing modes:

- MOV.D
- Register Indirect Addressing (Word or Byte mode) with pre/post-decrement

**Work around**

Do not perform PSV accesses to any of the first four bytes using the above addressing modes. For applications using the C language, MPLAB C30 version 3.11 or higher, provides the following command-line switch that implements a work around for the erratum.

```
-merrata=psv_trap
```

Refer to the `readme.txt` file in the MPLAB C30 v3.11 tool suite for further details.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**16. Module: ECAN**

The WAKIF bit in the CxINTF register cannot be cleared by software instruction after the device is interrupted from Sleep due to activity on the CAN bus.

When the device wakes up from Sleep due to CAN bus activity, the ECAN module is placed in operational mode. The ECAN Event interrupt occurs due to the WAKIF flag. Trying to clear the flag in the Interrupt Service Routine (ISR) may not clear the flag. The WAKIF bit being set will not cause repetitive Interrupt Service Routine execution.

**Work around**

Although the WAKIF bit does not clear, the device Sleep and ECAN Wake function continue to work as expected. If the ECAN event is enabled, the CPU will enter the Interrupt Service Routine due to the WAKIF flag getting set. The application can maintain a secondary flag, which tracks the device Sleep and Wake events.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**17. Module: ECAN**

The ECAN module may not store received data in the correct location. When this occurs, the receive buffers will become corrupted. In addition, it is also possible for the transmit buffers to become corrupted. This issue is more likely to occur as the CAN bus speed approaches 1 Mbps.

**Work around**

Do not use the DMA with ECAN in Peripheral Indirect mode. Use the DMA in Register Indirect mode, Continuous mode enabled and Ping Pong mode disabled. The receive DMA channel count should be set to 8 words. The transmit DMA channel count should be set for the actual message size (maximum of 7 words for Extended CAN messages and 6 words for Standard CAN Messages). To simplify application error handling while using this mode, only one TX buffer should be used. While message filtering is not affected, messages will not be stored at distinct RX buffers. Instead all messages are stored contiguously in memory. The start of this memory is pointed to by the receive DMA channel. The application must still clear RXFUL flags and other interrupt flags. The application must manage the RX buffer memory.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  |    |  |  |  |  |

**18. Module: CPU**

The EXCH instruction does not execute correctly.

**Work around**

If writing source code in assembly, the recommended work around is to replace:

```
EXCH Wsource, Wdestination
```

with:

```
PUSH Wdestination
```

```
MOV Wsource, Wdestination
```

```
POP Wsource
```

If using the MPLAB C30 C compiler, specify the compiler option: `-merrata=exch` (*Project > Build Options > Projects > MPLAB C30 > Use Alternate Settings*).

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**19. Module: PWM**

If the PTDIR bit is set (when PTMR is counting down), and the CPU execution is halted (after a breakpoint is reached), PTMR will start counting up, as if PTDIR was zero.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**20. Module: PWM**

When the device is operated in DOZE mode and the Motor Control PWM module has a postscaler set to any value different than 1:1 (PTOPS > 0 in PxTCON register), the Motor Control PWM module generates more interrupts than expected.

**Work around**

Do not use DOZE mode with the Motor Control PWM if the time base output postscaler is different than 1:1 (PTOPS > 0 in PxTCON register).

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**21. Module: SPI**

Writing to the SPIxBUF register as soon as the TBF bit is cleared will cause the SPI module to ignore the written data. Applications which use SPI with DMA will not be affected by this erratum.

**Work around**

After the TBF bit is cleared, wait for a minimum duration of one SPI Clock before writing to the SPIxBUF register.

Alternately, do one of the following:

- Poll the RBF bit and wait for it to get set before writing to the SPIxBUF register
- Poll the SPI Interrupt flag and wait for it to get set before writing to the SPIxBUF register
- Use an SPI Interrupt Service Routine (ISR)
- Use DMA

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**22. Module: UART**

The UART module will not generate consecutive break characters. Trying to perform a back-to-back Break character transmission will cause the UART module to transmit the dummy character used to generate the first Break character instead of transmitting the second Break character. Break characters are generated correctly if they are followed by non-Break character transmission.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**23. Module: QEI**

When the TQCS and TQGATE bits in the QEIXCON register are set, a QEI interrupt should be generated after an input pulse on the QEA input. This interrupt is not generated in the affected silicon.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**24. Module: QEI**

When the TQCS and TQGATE bits in the QEIXCON register are set, the POSCNT counter should not increment but erroneously does, and if allowed to increment to match MAXCNT, a QEI interrupt will be generated.

**Work around**

To prevent the erroneous increment of POSCNT while running the QEI in Timer Gated Accumulation mode, initialize MAXCNT = 0.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**25. Module: Audio DAC**

The Audio DAC positive differential output voltage and negative differential output voltage (parameters DA01 and DA02, respectively) may not meet the specifications listed in the data sheet.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  |    |  |  |  |  |

**26. Module: ADC**

If the ADC module is in an enabled state when the device enters Sleep mode as a result of executing a PWRSAV #0 instruction, the device power-down current (IPD) may exceed the specifications listed in the device data sheet. This may happen even if the ADC module is disabled by clearing the ADON bit prior to entering Sleep mode.

**Work around**

In order to remain within the IPD specifications listed in the device data sheet, the user software must completely disable the ADC module by setting the ADC Module Disable bit in the corresponding Peripheral Module Disable register (PMDx), prior to executing a PWRSAV #0 instruction.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

**27. Module: JTAG**

On 28-pin devices, JTAG Boundary Scan does not function correctly for pin 7. Both pins 6 and 7 respond to stimulus applied to pin 7.

**Work around**

Do not include pin 7 in the JTAG Boundary Scan chain for 28-pin devices.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |



**28. Module: RTCC**

The RTCC module gets reset on any device Reset, instead of getting reset only on a POR or BOR.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | A3 | A4 |  |  |  |  |
|----|----|----|----|--|--|--|--|
| X  | X  | X  | X  |  |  |  |  |

## Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70291D):

**Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

### 1. Module: DC Characteristics: I/O Pin Input Specifications

The maximum value for parameter DI19 ( $V_{IL}$  specifications for SDAx and SCLx pins) was stated incorrectly in Table 31-9 of the current device data sheet. Also, parameters DI28 and DI29 ( $V_{IH}$  specifications for SDAx and SCLx pins) were not stated. The correct values are shown in bold type in Table 3.

**TABLE 3: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS**

| DC CHARACTERISTICS |          |                    | Standard Operating Conditions: 3.0V to 3.6V<br>(unless otherwise stated)<br>Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial<br>$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended |     |              |          |                       |
|--------------------|----------|--------------------|---|-----|--------------|----------|-----------------------|
| Param No.          | Symbol   | Characteristic     | Min   | Typ | Max          | Units    | Conditions            |
| DI18               | $V_{IL}$ | Input Low Voltage  |   |     |              |          |                       |
|                    |          | <b>SDAx, SCLx</b>  | $V_{SS}$  | —   | $0.3 V_{DD}$ | V        | SMBus disabled        |
| DI19               |          | <b>SDAx, SCLx</b>  | $V_{SS}$  | —   | <b>0.8</b>   | V        | SMBus enabled         |
| DI28               | $V_{IH}$ | Input High Voltage |   |     |              |          |                       |
|                    |          | <b>SDAx, SCLx</b>  | <b><math>0.7 V_{DD}</math></b>  | —   | <b>5.5</b>   | <b>V</b> | <b>SMBus disabled</b> |
| DI29               |          | <b>SDAx, SCLx</b>  | <b>2.1</b>  | —   | <b>5.5</b>   | <b>V</b> | <b>SMBus enabled</b>  |

## **APPENDIX A: REVISION HISTORY**

### Rev A Document (3/2009)

Initial release of this document; issued for revision A1, A2 and A3 silicon.

Includes silicon issues 1-2 (UART), 3-4 (SPI), 5-10 (I<sup>2</sup>C), 11-12 (UART), 13 (Comparator), 14 (Internal Voltage Regulator), 15 (PSV Operations), 16-17 (ECAN), 18 (CPU), 19-20 (PWM) and 21 (SPI).

This document replaces the following errata document:

- DS80372, “dsPIC33FJ32MC302/304, dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04 Rev. A1/A2/A3 Silicon Errata”

### Rev B Document (4/2009)

Corrected part numbers.

### Rev C Document (8/2009)

Added silicon issues 22 (UART) and 23-24 (QEI).

### Rev D Document (1/2010)

Added Rev. A4 silicon information.

Added silicon issue 25 (Audio DAC).

### Rev E Document (6/2010)

Updated silicon issue 18 (CPU).

Added silicon issues 26 (ADC), 27 (JTAG) and 28 (RTCC), and data sheet clarification 1 (DC Characteristics: I/O Pin Input Specifications).

**NOTES:**

---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

#### **Trademarks**

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC<sup>32</sup> logo, rfPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.


FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Octopus, Omniscient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICTail, REAL ICE, rLAB, Select Mode, Total Endurance, TSHARC, UniWinDriver, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2010, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

ISBN: 978-1-60932-278-6

*Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

**QUALITY MANAGEMENT SYSTEM**  
**CERTIFIED BY DNV**  
**== ISO/TS 16949:2002 ==**



## Worldwide Sales and Service

### AMERICAS

#### Corporate Office

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://support.microchip.com>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

#### Atlanta

Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

#### Boston

Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

#### Chicago

Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

#### Cleveland

Independence, OH  
Tel: 216-447-0464  
Fax: 216-447-0643

#### Dallas

Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

#### Detroit

Farmington Hills, MI  
Tel: 248-538-2250  
Fax: 248-538-2260

#### Kokomo

Kokomo, IN  
Tel: 765-864-8360  
Fax: 765-864-8387

#### Los Angeles

Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608

#### Santa Clara

Santa Clara, CA  
Tel: 408-961-6444  
Fax: 408-961-6445

#### Toronto

Mississauga, Ontario,  
Canada  
Tel: 905-673-0699  
Fax: 905-673-6509

### ASIA/PACIFIC

#### Asia Pacific Office

Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon  
Hong Kong  
Tel: 852-2401-1200  
Fax: 852-2401-3431

#### Australia - Sydney

Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

#### China - Beijing

Tel: 86-10-8528-2100  
Fax: 86-10-8528-2104

#### China - Chengdu

Tel: 86-28-8665-5511  
Fax: 86-28-8665-7889

#### China - Chongqing

Tel: 86-23-8980-9588  
Fax: 86-23-8980-9500

#### China - Hong Kong SAR

Tel: 852-2401-1200  
Fax: 852-2401-3431

#### China - Nanjing

Tel: 86-25-8473-2460  
Fax: 86-25-8473-2470

#### China - Qingdao

Tel: 86-532-8502-7355  
Fax: 86-532-8502-7205

#### China - Shanghai

Tel: 86-21-5407-5533  
Fax: 86-21-5407-5066

#### China - Shenyang

Tel: 86-24-2334-2829  
Fax: 86-24-2334-2393

#### China - Shenzhen

Tel: 86-755-8203-2660  
Fax: 86-755-8203-1760

#### China - Wuhan

Tel: 86-27-5980-5300  
Fax: 86-27-5980-5118

#### China - Xian

Tel: 86-29-8833-7252  
Fax: 86-29-8833-7256

#### China - Xiamen

Tel: 86-592-2388138  
Fax: 86-592-2388130

#### China - Zhuhai

Tel: 86-756-3210040  
Fax: 86-756-3210049

### ASIA/PACIFIC

#### India - Bangalore

Tel: 91-80-3090-4444  
Fax: 91-80-3090-4123

#### India - New Delhi

Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

#### India - Pune

Tel: 91-20-2566-1512  
Fax: 91-20-2566-1513

#### Japan - Yokohama

Tel: 81-45-471- 6166  
Fax: 81-45-471-6122

#### Korea - Daegu

Tel: 82-53-744-4301  
Fax: 82-53-744-4302

#### Korea - Seoul

Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or  
82-2-558-5934

#### Malaysia - Kuala Lumpur

Tel: 60-3-6201-9857  
Fax: 60-3-6201-9859

#### Malaysia - Penang

Tel: 60-4-227-8870  
Fax: 60-4-227-4068

#### Philippines - Manila

Tel: 63-2-634-9065  
Fax: 63-2-634-9069

#### Singapore

Tel: 65-6334-8870  
Fax: 65-6334-8850

#### Taiwan - Hsin Chu

Tel: 886-3-6578-300  
Fax: 886-3-6578-370

#### Taiwan - Kaohsiung

Tel: 886-7-536-4818  
Fax: 886-7-536-4803

#### Taiwan - Taipei

Tel: 886-2-2500-6610  
Fax: 886-2-2508-0102

#### Thailand - Bangkok

Tel: 66-2-694-1351  
Fax: 66-2-694-1350

### EUROPE

#### Austria - Wels

Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

#### Denmark - Copenhagen

Tel: 45-4450-2828  
Fax: 45-4485-2829

#### France - Paris

Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

#### Germany - Munich

Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

#### Italy - Milan

Tel: 39-0331-742611  
Fax: 39-0331-466781

#### Netherlands - Druenen

Tel: 31-416-690399  
Fax: 31-416-690340

#### Spain - Madrid

Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

#### UK - Wokingham

Tel: 44-118-921-5869  
Fax: 44-118-921-5820