BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION)

CLASS: BTECH
BRANCH: ECE+CS+IT+EEE

SEMESTER: III
SESSION: MO/2022

SUBJECT: EC203 DIGITAL SYSTEM DESIGN

TIME: 2 HOURS

FULL MARKS: 25

INSTRUCTIONS:
1. The total marks of the questions are 25.
2. Candidates attempt for all 25 marks.
3. Before attempting the question paper, be sure that you have got the correct question paper.
4. The missing data, if any, may be assumed suitably.
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

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| Q1 (a) | i) If $N^2=(760)_8$, then what is the value of N if N is a base-6 number?<br>ii) Convert the decimal number 0.356 into its hexadecimal equivalent. | [1+1] | 1 | 1 |
| Q1 (b) | i) What are the advantages of 2's complement representation?<br>ii) Let $R_1$, $R_2$, and $R_3$ are 4-bit registers that store signed numbers in 2's complement form. Say, $R_1$=1100 and $R_2$=1010, and the result of $(R_1+R_2)$ is stored in $R_3$. Does $R_3$ contain a valid data? Justify your answer. | [1+2] | 1 | 2 |
| Q2 (a) | Explain the working of a two-input TTL NOR gate with diagram. | [2] | 2 | 2 |
| Q2 (b) | i) What are the advantages of CMOS logic family?<br>ii) Write a VHDL program for implementing a function F=ABC+AB+C. | [1+2] | 2 | 2 |
| Q3 (a) | Convert the following Boolean function into canonical form (POS)<br>Y(A, B, C)=(A+B)(B+C')(A+C) | [2] | 1 | 3 |
| Q3 (b) | Minimize the following Boolean function using K-Map<br>$Y(A,B,C,D) = \sum m(1,3,5,8,9,11,15) + d(2,13)$ | [3] | 1 | 3 |
| Q4 (a) | Realize the logic function obtained in Q3(b) using NAND gates. | [2] | 1 | 2 |
| Q4 (b) | Minimize the following Boolean function using K-Map<br>$F(A,B,C,D) = \prod M(1,2,3,8,9,10,11,14).d(7,15)$ | [3] | 1 | 3 |
| Q5 (a) | Design a 4-bit parity bit checker circuit with diagram. | [2] | 2 | 1 |
| Q5 (b) | What is Full adder? Design a Full adder circuit using Half adder. | [3] | 2 | 1 |

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