BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI (MID SEMESTER EXAMINATION)

CLASS: BRANCH: ECE/EEE/CSE/IT SEMESTER: III/ADD SESSION: MO/16

[2]

SUBJECT: EC3201-DIGITAL ELECTRONICS

FULL MARKS: 25 TIME: 1.5 HOURS

INSTRUCTIONS:

- 1. The total value of the questions are 30 marks.
- 2. Candidates may attempt for all 30 marks.
- In those cases where the marks obtain exceed 25 marks. The excess will be ignored.
- 4. Before attempting the question paper, be sure that you have got the correct question paper.
- 5. The missing data, If any, may be assumed suitably.
- Q1. (a) Simplify the following function using the don't care conditions in SOP form using K-map? [3] $F(A,B,C,D) = \sum (0,6,8,13,14)$

 $d(A,B,C,D) = \sum (2,4,10)$

- (b) Convert the following numbers to signed 10's complement form and find the following [2]
 - (i) (+9742) +(-641)
- (ii) (-9742) +(-641)
- Q2. (a) Simplify the following Boolean function in SOP form by means of the Quine-McCluskey [3]

 $F(A,B,C,D,E) = \sum (0.1,2,8,9,15,17,21,24,25,27,31)$

(b) Implement the following function with NAND gate. Use only 4 gates. Only the normal inputs [2] are available.

P(w,x,y,z) = w'xz + w'yz + x'yz' + wxy'zd(w, x, y, z = wyz

- Q3. (a) Design a full adder circuit using two half adders?
 - (b) Implement the following Boolean function using 8 X 1 multiplexer, the selection lines of the [2] multiplexer should be connected to inputs A,B and C?

F(A,B,C,D) =(2,5,6,7,10,11,12,13,14)

Q4. (a) A combinational circuit is defined by the following three functions:

F1 = x'y' + xyz'F2 = x' + yF3 = xy + x'y'

Design the circuit with a decoder and external gates

- A majority circuit is a combinational circuit whose output is equal to 1 if the input [3] variables have more 1's than 0's. The output is 0 otherwise. Design a 3 input majority circuit by finding the circuit's truth table, Boolean equation and logic diagram.
- Q5_(a) Design J-K flip-flop. What is race-around condition in It? [3] [2] (b) Design a synchronous MOD-8 up counter?
- Write short notes on:
- (i) Master Slave Flip Flop. (iii) 4-bit right shift register

21.09.16**E

