BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BE
BRANCH: CSE/EEE/ECE/IT

SEMESTER : III
SESSION : MO/17

SUBJECT: EC3201 DIGITAL ELECTRONICS

TIME: 3. Hours

FULL MARKS: 60

INSTRUCTIONS:
1. The question paper contains 7 questions each of 12 marks and total 84 marks.
2. Candidates may attempt any 5 questions maximum of 60 marks.
3. The missing data, if any, may be assumed suitably.
4. Before attempting the question paper, be sure that you have got the correct question paper.
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

Q.1(a) Show that a positive logic AND gate is a negative logic OR gate. [2]

Q.1(b) Distinguish between minterm and maxterm. Express the function $Y = \bar{A}C + B\bar{D}$ in canonical POS form. [4]

Q.1(c) Simplify the following Boolean function using Quine McCluskey method and obtain the minimal SOP expression: [6]

$$Y = \sum_m(0,2,5,7,8,10,13,15)$$

Q.2(a) Distinguish between encoder and decoder. [2]

Q.2(b) Design a 16:1 multiplexer using two 8:1 multiplexers and external gates. [4]

Q.2(c) Explain the carry propagate and carry generate conditions in carry look ahead adder. Develop the logic diagram of a look ahead carry generator for 4-bit parallel addition. [6]

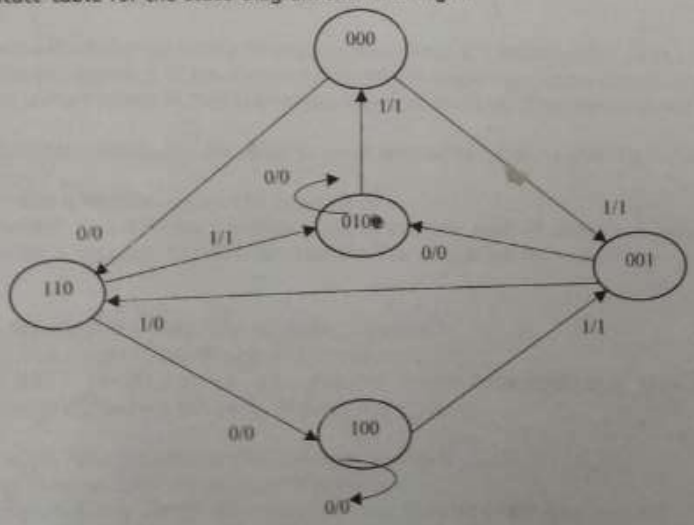
Q.3(a) Implement D flip flop with NAND gates and obtain its characteristic equation. [2]

Q.3(b) Develop a 3-bit bidirectional shift register with D flip flops and explain its working. [4]

Q.3(c) Explain the operation of a 3-bit asynchronous UP/Down counter with J-K flip flops using truth table. What are its advantages and disadvantages? [6]

Q.4(a) What is state assignment problem in sequential circuit? [2]

Q.4(b) Obtain the state table for the state diagram shown in Fig.1. [4]



Q.4(c) Design a sequential circuit with J-K flip-flop to satisfy the following state equations: [6]

$$A(t+1) = A'D + A'B'C + ACD + AC'B$$
$$B(t+1) = A'D' + C + A'BC$$
$$C(t+1) = C,\ D(t+1) = B'$$

PTO

Q.5(a)	What is a transmission gate? Where is it used?	[2]
Q.5(b)	Show the circuit of a three input NAND gate using CMOS transistors and explain its working.	[4]
Q.5(c)	Explain the working principle of 3-input TTL NAND gate with totem pole output driver. What is the advantage of this configuration? Why the diode is used in the output section?	[6]
Q.6(a)	What is meant by hysteresis voltage in a Schmitt trigger?	[2]
Q.6(b)	A transistorized astable multivibrator is required to provide a train of pulses of 4 μs wide at a repetition rate of 100 kHz. Determine the values of capacitors that are to be used if the component values $R_1 = R_2 = 25\ k\Omega$.	[4]
Q.6(c)	Explain the operation of monostable multivibrator built by OP AMP with its waveforms.	[6]
Q.7(a)	Distinguish between volatile and non- volatile memory with examples.	[2]
Q.7(b)	Explain with circuit diagram the read, write and refresh operation of dynamic RAM cell.	[4]
Q.7(c)	How does the architecture of PLA differ from PAL? Implement the following functions using a PLA:	[6]

$$F_1(A,B,C) = \sum(0,4,5,6) \quad , \quad F_2(A,B,C) = \sum(2,3,7)$$

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