BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BE
BRANCH: ECE/CSE/EEE/IT

SEMESTER : III
SESSION : MO/19

SUBJECT: EC203 DIGITAL SYSTEM DESIGN

TIME: 3 HOURS

FULL MARKS: 50

INSTRUCTIONS:
1. The question paper contains 5 questions each of 10 marks and total 50 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
4. Before attempting the question paper, be sure that you have got the correct question paper.
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

Q.1(a) Write the entity declaration and architecture declaration of half subtractor in VHDL code. [5]
Q.1(b) Explain with circuit diagram the working principle of 3-input TTL NAND gate with totem pole output [5]
driver. Justify the need of totem pole output stage.

Q.2(a) Construct a combinational circuit for the following Boolean function using NOR gates only: [5]
$F = \prod (3.5.6.7)$
Q.2(b) Evaluate the simplification of the following Boolean function and obtain the minimal-POS expression [5]
by Karnaugh map:
$F = \prod (0.1.3.4.5.7.9.12.14) \prod_d (2.6.11)$

Q.3(a) Write the drawback of parallel binary adder for addition operation. Show how it can be overcome in [5]
Carry look ahead adder.
Q.3(b) Show how the following function is implemented with a multiplexer taking B,C and D as selection [5]
lines:
$(A.B.C.D) = \sum_m (1.3.5.7.9.10.13.15)$

Q.4(a) (i) Construct SR flip flop with NAND gates and obtain its characteristic equations. [5]
(ii) Design an asynchronous Mod-12 up counter using JK flip flops.
Q.4(b) Distinguish between the programmable logic devices PLA and PAL. Implement the following functions [5]
using a PAL:
$F_1 (A.B.C) = \sum (1.2.5)$, $F_2 (A.B.C) = \sum (0.3.7)$, $F_3 (A.B.C) = \sum (2.4.6)$

Q.5(a) Draw the architecture of SAP-1 computer and explain the functions of each block in the left-hand side [5]
of the W bus.
Q.5(b) List the instructions of SAP-1 and describe their operation with examples. [5]

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