BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BE
BRANCH: CSE/EEE/IT/ECE

SEMESTER : III
SESSION : MO/18

SUBJECT: EC3201-DIGITAL ELECTRONICS

TIME: 03:00

FULL MARKS: 60

INSTRUCTIONS:
1. The question paper contains 7 questions each of 12 marks and total 84 marks.
2. Candidates may attempt any 5 questions maximum of 60 marks.
3. The missing data, if any, may be assumed suitably.
4. Before attempting the question paper, be sure that you have got the correct question paper.
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

Q.1(a) Distinguish between Canonical forms and Standard forms of Boolean functions. [2]
(b) What is the advantage of multilevel gate network? Apply 2-input NAND gates only to implement the function $= (AB + \bar{C})D + EF$. [4]
(c) Determine the prime-implicants and essential prime-implicants of the following Boolean function using Quine McCluskey method and obtain the minimal SOP expression: [6]

$$Y = \sum_{m}(0,1,6,9,10,11,12,14) + \sum_{d}(3,15)$$

Q.2(a) How does an encoder differ from a multiplexer? [2]
(b) Design a full subtractor circuit with a decoder and logic gates. [4]
(c) Show how the following function is implemented with a multiplexer taking A,B and C as selection lines: [6]

$$Y(A,B,C,D) = \Sigma_m(0,2,5,7,8,10,13,15)$$

Q.3(a) What is race-around condition in J-K flip-flop? [2]
(b) Explain with circuit diagram the working principle of a 4-bit parallel -in serial- out shift register. [4]
(c) What is the advantage of synchronous counter over asynchronous one? With the help of excitation table , design the synchronous counter for the following counting sequence using J-K flip-flops: 0–1–2–3–4–5–0---- [6]

Q.4(a) What are the requirements of state reduction and state assignment in sequential circuits? [2]
(b) Construct the state table for the state diagram shown in Fig.1. [4]
(c) Design a sequential circuit with J-K flip-flop to satisfy the following state equations: [6]

$$A(t+1) = \bar{A}CD + \bar{A}B\bar{D} + AB\bar{C} + AC\bar{D}$$
$$B(t+1) = \bar{A}C + \bar{D} + \bar{A}B\bar{C}$$
$$C(t+1) = B,\ D(t+1) = \bar{D}$$

Q.5(a) Compare TTL logic with CMOS in digital system. [2]
(b) What is the limiting factor for the speed of operation of TTL gate? Show how it can be overcome in a 3-input TTL NAND gate with totem pole output driver. [4]
(c) Design a CMOS logic circuit to realize the function $F = \Sigma_m(0,1,2,4,6,8,10,12,14)$ [6]

Q.6(a) List the applications of astable, monostable and bistable multivibrators. [2]
(b) In a symmetrical collector coupled astable multivibrator using transistors the component values are $R_1 = R_2 = 35\ K\Omega$ and $C1 = C2 = 0.02\ \mu F$. Determine the frequency of oscillation. [4]
(c) Explain with circuit diagram the operation of Schmitt trigger using OP AMP. Sketch its input-output characteristics for increasing and decreasing the input signal. What is hysteresis voltage? [6]

Q.7(a) What are the advantages of an EEPROM over an EPROM? [2]
(b) How does a static RAM cell differ from a dynamic RAM cell? Explain with circuit diagram the read and write operation of dynamic RAM cell. Why refresh operation is required in dynamic RAMs? [4]
(c) Distinguish between FPGA and PLD devices. Design a logic circuit using PLA to convert a 3-bit Binary code to Gray code. [6]