BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION)

CLASS: BE
BRANCH: EEE/ECE/CSE/IT

SEMESTER: III
SESSION : MO/2018

SUBJECT : EC3201 DIGITAL ELECTRONICS

TIME: 1.5 HOURS

FULL MARKS: 25

INSTRUCTIONS:
1. The total marks of the questions are 30.
2. Candidates may attempt for all 30 marks.
3. In those cases where the marks obtained exceed 25 marks, the excess will be ignored.
4. Before attempting the question paper, be sure that you have got the correct question paper.
5. The missing data, if any, may be assumed suitably.

Q1 (a) Simplify the following Boolean function to a minimum number of literals : [2]
$$Y = (B + BC)(B + \bar{B}C)(B + D)$$
 (b) Explain the term universal gate. Construct the logic circuit for the function $Y = B(A + CD) + A\bar{C}$ using 2-input NOR gates only. [3]

Q2 (a) Formulate the Boolean function $F = \bar{A}B + \bar{C}$ into a Canonical SOP form. [2]
 (b) Simplify the following Boolean function and obtain the minimal-POS expression by Karnaugh map: [3]
$$F = \prod(0,4,5,7,10,12) \prod_d (2,8,13,15)$$

Q3 (a) Show how a full adder circuit is implemented using a decoder and logic gates. [2]
 (b) Perform the BCD-addition of 75 with 58. Construct the logic circuit for this BCD addition using 4-bit binary adders and logic gates. [3]

Q4 (a) Develop a 4-to-2 priority encoder which has highest priority for highest order input. [2]
 (b) Construct a multiplexer for the implementation of the following Boolean function: [3]
$$Y(A, B, C, D) = \sum(1,2,3,6,8,10,12,14)$$
where the variable 'A' is used as input for the multiplexer.

Q5 (a) Distinguish between level triggering and edge triggering. [2]
 (b) Construct the excitation table for J-Kflip-flop and D flip-flop. Using the excitation table, convert a J-K flip-flop into a D flip-flop. [3]

Q6 (a) Design a 4-bit parallel-input-parallel-output shift register and explain its working. [2]
 (b) A synchronous down counter is required to count the following sequence: [3]
'3-1-0-3... Design the counter with J-K flip-flop.