BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION)

CLASS: BE
BRANCH: ECE/EEE/CSE/IT

SEMESTER: III/ADD
SESSION: MO/2017

SUBJECT: EC3201 DIGITAL ELECTRONICS

TIME: 1.5 HOURS

FULL MARKS: 25

INSTRUCTIONS:
1. The total marks of the questions are 30.
2. Candidates may attempt for all 30 marks.
3. In those cases where the marks obtained exceed 25 marks, the excess will be ignored.
4. Before attempting the question paper, be sure that you have got the correct question paper.
5. The missing data, if any, may be assumed suitably.

Q1 (a) Simplify the function: $Y = A + \bar{A}B + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}D$. [2]
(b) Why NAND and NOR gates are called universal gates? Construct the logic circuit for the function $Y = (\overline{A} + \overline{B})C + (\overline{D} + \overline{E})F$ using 2-input NAND gates only. [3]

Q2 (a) Distinguish between (i) Canonical SOP form and canonical POS form; and (ii) Standard form and non-standard form of Boolean functions. [2]
(b) Find the minimized Boolean expression of the following Boolean function F in SOP using don't care conditions, d: [3]
$F = \bar{B}\bar{C}\bar{D} + B\bar{C}\bar{D} + AB\bar{C}\bar{D}$: $d = \bar{B}C\bar{D} + \bar{A}B\bar{C}D$

Q3 (a) Construct the truth table for full subtractor and build the logic circuit using half subtractor and logic gates. [2]
(b) Perform the BCD-addition of 79 with 68. Draw a logic circuit for the BCD adder using 4-bit binary adders. [3]

Q4 (a) Distinguish between (i) Encoder & Multiplexer, (ii) Decoder & Demultiplexer. [2]
(b) Construct a multiplexer for the implementation of the following Boolean function: [3]
$$F(w, x, y, z) = \sum(1,2,5,7,9,13,14)$$
where the variable 'w' is used as input for the multiplexer.

Q5 (a) Explain the role of 'Preset' and 'Clear' in S-R flip-flop. [2]
(b) Construct a Master-Slave J-K flip-flop with NAND gates and explain how the race around condition is eliminated in it. [3]

Q6 (a) Design a 3-bit parallel-input serial-output shift register and explain its working. [2]
(b) A MOD-3 synchronous counter is required to count the following sequence: 0-1-2-0... [3]
Design the counter with J-K flip-flop.

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