BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(SHORT SEMESTER EXAMINATION)

CLASS: BE
BRANCH: ALL

SEMESTER : SS/2019
SESSION : 2018-19

SUBJECT: EC3201 DIGITAL ELECTRONICS

TIME: 3:00 HOURS

FULL MARKS: 100

INSTRUCTIONS:
1. The question paper contains 7 questions each of 20 marks and total 140 marks.
2. Candidates may attempt any 5 questions maximum of 100 marks.
3. The missing data, if any, may be assumed suitably.
4. Before attempting the question paper, be sure that you have got the correct question paper.
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

Q.1(a) Define minterms and maxterms in switching functions. [4]
Q.1(b) Implement the function $F = B(A+CD) + A\bar{C}$ using NAND gate only. [6]
Q.1(c) Simplify the following Boolean function using Karnaugh map method and obtain (i) minimal SOP and (ii) minimal POS expressions: [10]
$$Y = \Sigma_m (0,2,5,6,8,10) + \Sigma_d (7,9,14,15)$$

Q.2(a) Implement a full adder with two half adders and logic gate. [4]
Q.2(b) Design a 16:1 multiplexer using two 8:1 multiplexers and external gates. [6]
Q.2(c) Distinguish between multiplexer and encoder. Implement the following function with a multiplexer: [10]
$$Y = \Sigma (1,3,4,6,9,10,11,14)$$

Q.3(a) What is race around condition in sequential circuit? How it can be overcome? [4]
Q.3(b) What is the difference between register and counter? Explain with circuit diagram the working principle of 4-bit shift register. [6]
Q.3(c) Distinguish between synchronous and asynchronous counters. Develop a 4- bit UP-DOWN asynchronous counter. [10]

Q.4(a) Distinguish between excitation table and state table in sequential circuit. [4]
Q.4(b) What is state reduction problem in sequential circuit? [6]
Q.4(c) A sequential circuit has one input X, one output Y and two S-R flip flops denoted by A and B. The four flip- flop input functions and one circuit output are as follows: [10]
$S_A = B\bar{X}$, $R_A = \bar{B}X$, $S_B = A\bar{X}$, $Y = A\bar{B}X$

Q.5(a) Define the terms: (i) Fan-in (ii) Fan out (iii) Propagation delay (iv) Power dissipation. [4]
Q.5(b) Explain the working principle of 3-input TTL NAND gate with open collector output. [6]
Q.5(c) Draw the circuit of a 2-input CMOS NOR gate and explain the operation. [10]

Q.6(a) What is the difference between as table and monostable multivibrators? [4]
Q.6(b) In an as table multivibrator, the duty cycle D= 25% and the ON period T_1= 2 ms. Determine the frequency of oscillation for the multivibrator. [6]
Q.6(c) Explain with circuit diagram the operation of monostable multivibrator using transistors. Sketch the input output waveforms. [10]

Q.7(a) What is the difference between EPROM and EEPROM? [4]
Q.7(b) Draw the circuit of a static MOS RAM cell and explain its working. [6]
Q.7(c) What is the difference between FPGA and FPLA? Implement the following functions using PLA: [10]
$F_1 = \Sigma(3,4,6,7)$, $F_2 = (0,2,4,7)$

::::::28/06/2019::::::