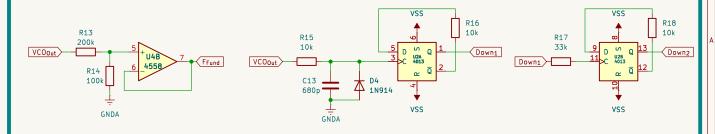


#### 1. Input + Boost Doesn't have to be exact. "Big" is fine. BLUE We just wanna make sure we smush the signal a bunch and cut off the high-highs. D2 BLUE (Any common op amp is probably fine) C9 220p R12 R9 510k R5 33k 220p 510k GNDS GNDA

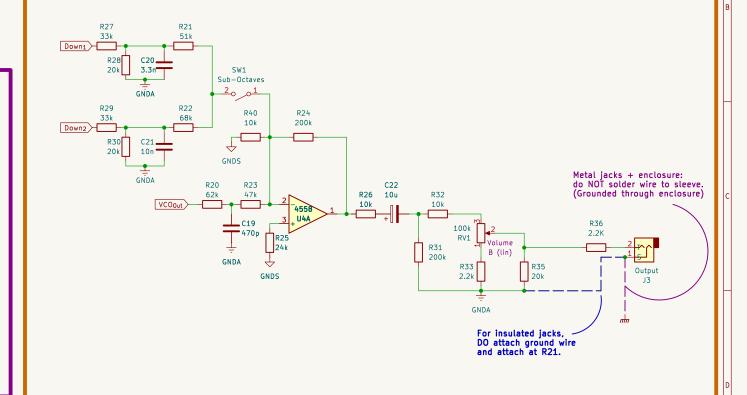
### PLL Notes:

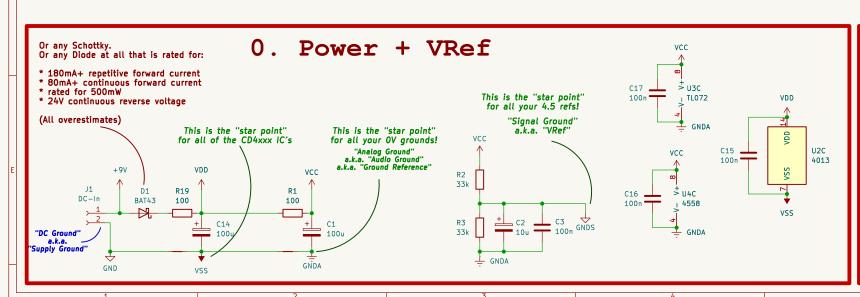
- 1. RV4 + RV2 make noise when:
  both up/down/full-opposite.
  (Only one extreme == usable).
  Play with sizes/ranges!
- RV4 and C12 set the center frequency:
   If R4 gets smaller; make C12 bigger.
   Increase R37 = less droop/slide/wah.
- 4. Fiddle with the diodes and stuff!
- 5. P.S. Signals ARE also at PC1/PCP, BTW.
- 6. When PCP = HIGH + PC1 = LOW 4+ times in a row: you are at frequency lock!
- 7. If you put a counter/divider between CompII out and VCOIn, the PLL will shift the frequency UP as much as the divider divides. Use one half of the CD4013 in the loop instead: octave up!

## 3. Octaves and VCO



# 4. Summing Stage & Output





# **WARNINGS:**

- LUNCHTIME HACK / ALPHA!
- Keep the volume low while experimenting. This circuit can produce very high or loud tones if adjusted live!
- Breadboard before you solder anything! This is hastily documented and NOT double checked! (Yet)

#### NOTES:

- Connect ground symbols at respective star grounds
- You can omit VSS and just use GNDA as audio ground (I think the signal will swamp out any noise anyway)
- Octave down is optional: just exclude CD4013
- This was another lunch hack: don't judge.
- Do hack!