

2. PLL + Control

- 470n = more rumble/glitch (less "charge up" after silence)
- 150nF - 330n = between 470nF and 100nF...
- 22nF-100nF = crisper highs, less rumbley lows
- 10nF or less = more nasal + gets static

Omit entirely for cleanest tracking!
(But also less sustain)
My current preference is 100nF
It's 470nF in the video

4. Auto-Adj

3. Suboctaves

The circuit diagram illustrates the generation of suboctaves using two 74VHC123 monostable multistablers. The first multistabler (U2A) is triggered by the VCOout signal through a 10k resistor (R15). Its timing network consists of a 680pF capacitor (C13) and a 1N914 diode (D4) connected to ground (GNDA). The output of U2A (Q1) is labeled 'Down1' and is connected to the input of the second multistabler (U2B) through a 33k resistor (R17). The output of U2B (Q2) is labeled 'Down2' and is connected to the input of the final output stage through a 47k resistor (R45). The final output stage is a buffer or inverter (U2C) that produces the 'SubOctaves' signal. The timing network for U2C consists of a 68nF capacitor (C25) and a 47k resistor (R42) connected to ground (GNDS). The circuit also includes several other resistors (R16, R18, R21, R22, R27, R28, R29, R30, R43, R44) and capacitors (C20, C21, C24) to ensure proper timing and signal integrity.

[illegible]

PLL Notes:

1. RV4 + RV2 make noise when:
both up/down/full-opposite.
(Only one extreme == usable).
Play with sizes/ranges!
2. RV4 and C12 set the center frequency:
If R4 gets smaller; make C12 bigger.
3. Increase R37 = less droop/slide/wah.
4. Fiddle with the diodes and stuff!
5. P.S. Signals ARE also at PC1/PCP, BTW.
6. When PCP = HIGH + PC1 = LOW 4+ times
in a row: you are at frequency lock!
7. If you put a counter/divider between
CompII out and VCOIn, the PLL will
shift the frequency UP as much as the
divider divides. Use one half of the
CD4013 in the loop instead: octave up!

4. Summing Stage & Output

SW1
Sub-Octaves

SubOctaves 2 1

VCOBuff

R20 62k

R23 47k

R24 200k

R26 10k

C22 10u

R32 10k

100k

RV1

2

Volume B (lin)

R31 200k

R33 2.2k

R35 20k

R36 2.2k

Output J3

GNDA

GNDS

4558 U4A

2 1

3

R25 24k

GNDS

4558 U4B

5 6 7

VCOOut

R13 200k

R14 100k

GNDA

VCOBuff

C19 470p

GNDA

For insulated jacks, DO attach ground wire and attach at R21.

Metal jacks + enclosure: do NOT solder wire to sleeve. (Grounded through enclosure)

[illegible]

WARNINGS :

- LUNCHTIME HACK / ALPHA!
- Keep the volume low while experimenting. This circuit can produce very high or loud tones if adjusted live!
- Breadboard before you solder anything! This is hastily documented and NOT double checked! (Yet)

NOTES:

- Connect ground symbols at respective star grounds
- You can omit VSS and just use GNDA as audio ground
(I think the signal will swamp out any noise anyway)
- Octave down is optional: just exclude CD4013
- This was another lunch hack: don't judge.
- Do hack!