

2. PLL + Control

- 470n = more rumble/glitch (less "charge up" after silence)
- 150nF - 330n = between 470nF and 100nF...
- 22nF-100nF = crisper highs, less rumibly lows
- 10nF or less = more nasal + gets static

Omit entirely for cleanest tracking!
(But also less sustain)
My current preference is 100nF
It's 470nF in the video

The circuit diagram shows the internal components of the PLL+Control section. A U1 4046 VCO chip is the central component. Its Refin pin (3) is connected to VDD. The SigIn pin (4) is connected to a network consisting of a boosted signal through resistor R8 (2.2k), capacitor C11 (100n), and capacitor C10 (560p) to ground. The FOUT pins (2 and 13) are connected to the CompII input. The VCOIn pin (9) is connected to a 'Center' input through resistor R1 (10k). The VCOOut pins (14 and 1) are connected to the output. Other pins like PC1, PC2, PCP, SFout, ZOUT, and Inh are either unconnected or connected to VSS/VDD as indicated by the schematic.

Experiment with any/all of this.
The only thing you ****need**** is
a path to ground from the negative
side of C23.

3. Octaves and VCO

The first diagram shows a voltage divider with R13 (200k) and R14 (100k) connected to VCO0out. The midpoint is connected to the non-inverting input of a U4B 4558 op-amp. The op-amp is configured as a voltage follower with its output connected to Ffund.

The second diagram shows a voltage divider with R15 (10k) connected to VCO0out. The midpoint is connected to the D input of a u2A 4013 flip-flop. The flip-flop is configured as a monostable multivibrator with its output connected to Down1.

The third diagram shows a voltage divider with R17 (33k) connected to Down1. The midpoint is connected to the D input of a u2B 4013 flip-flop. The flip-flop is configured as a monostable multivibrator with its output connected to Down2.

1. Input + Boost

Doesn't have to be exact. "Big" is fine.
We just wanna make sure we smush the
signal a bunch and cut off the high-highs.

(Any common op amp is probably fine)

PLL Notes:

1. RV4 + RV2 make noise when:
both up/down/full-opposite.
(Only one extreme == usable).
Play with sizes/ranges!
2. RV4 and C12 set the center frequency:
If R4 gets smaller; make C12 bigger.
3. Increase R37 = less droop/slide/wah.
4. Fiddle with the diodes and stuff!
5. P.S. Signals ARE also at PC1/PCP, BTW.
6. When PCP = HIGH + PC1 = LOW 4+ times
in a row: you are at frequency lock!
7. If you put a counter/divider between
CompII out and VCOIn, the PLL will
shift the frequency UP as much as the
divider divides. Use one half of the
CD4013 in the loop instead: octave up!

4. Summing Stage & Output

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Metal jacks + enclosure:
do NOT solder wire to sleeve.
(Grounded through enclosure)

For insulated jacks,
DO attach ground wire
and attach at R21.

0. Power + VRef

Or any Schottky.
Or any Diode at all that is rated for:

- * 180mA+ repetitive forward current
- * 80mA+ continuous forward current
- * rated for 500mW
- * 24V continuous reverse voltage

(All overestimates)

This is the "star point" for all of the CD4xxx IC's

This is the "star point" for all your 0V grounds!

"Analog Ground" a.k.a. "Audio Ground" a.k.a. "Ground Reference"

"DC Ground" a.k.a. "Supply Ground"

This is the "star point" for all your 4.5 refs!

"Signal Ground" a.k.a. "VRef"

1

2

3

4

WARNINGS :

- LUNCHTIME HACK / ALPHA!
- Keep the volume low while experimenting. This circuit can produce very high or loud tones if adjusted live!
- Breadboard before you solder anything! This is hastily documented and NOT double checked! (Yet)

NOTES: <ul style="list-style-type: none"> - Connect ground symbols at respective star grounds - You can omit VSS and just use GNDA as audio ground (I think the signal will swamp out any noise anyway) - Octave down is optional: just exclude CD4013 - This was another lunch hack: don't judge. - Do hack! 		
<p>WARNING: HACK! NOT CHECKED FOR ERRORS (yet).</p> <p>Pink Circles = Fiddle with these! (Fiddle with any)</p> <p>Andrew T. Canaday (povins), D.B. Buchholz (QuickButterfly_4571)</p> <p>Sheet: /</p> <p>File: OSM.kicad_sch</p>		
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