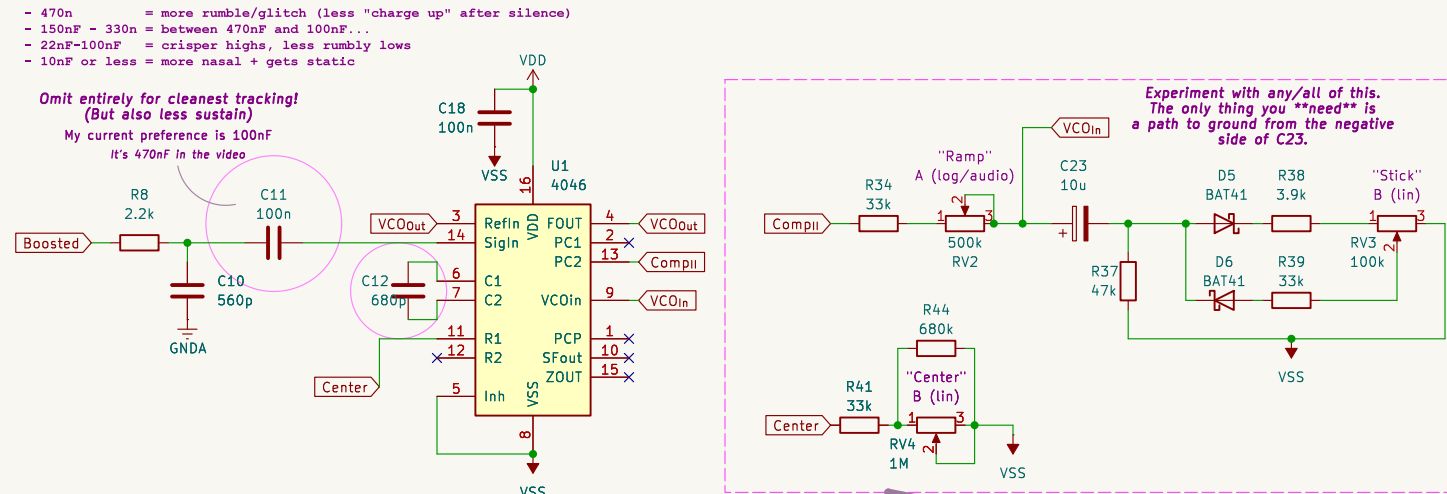


## 2. PLL + Control

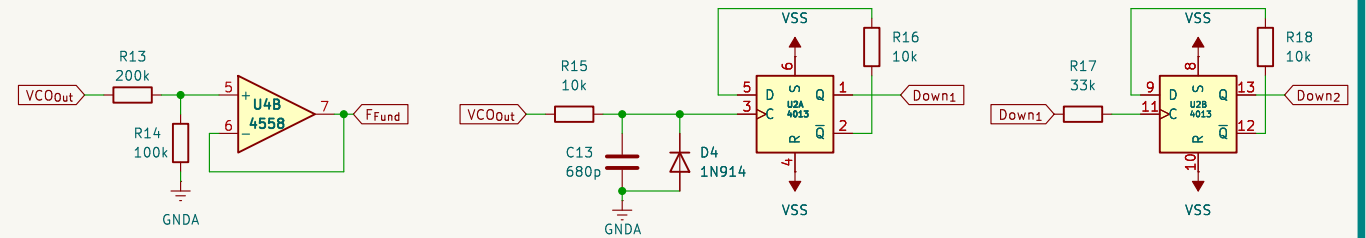
- 470n = more rumble/glitch (less "charge up" after silence)  
 - 150nF - 330n = between 470nF and 100nF...  
 - 22nF-100nF = crisper highs, less rumbley lows  
 - 10nF or less = more nasal + gets static

Omit entirely for cleanest tracking!  
 (But also less sustain)  
 My current preference is 100nF  
 It's 470nF in the video

Experiment with any/all of this.  
 The only thing you **need** is  
 a path to ground from the negative  
 side of C23.



### 3. Octaves and VCO



# 1. Input + Boost

Doesn't have to be exact. "Big" is fine.  
We just wanna make sure we smush the  
signal a bunch and cut off the high-highs.

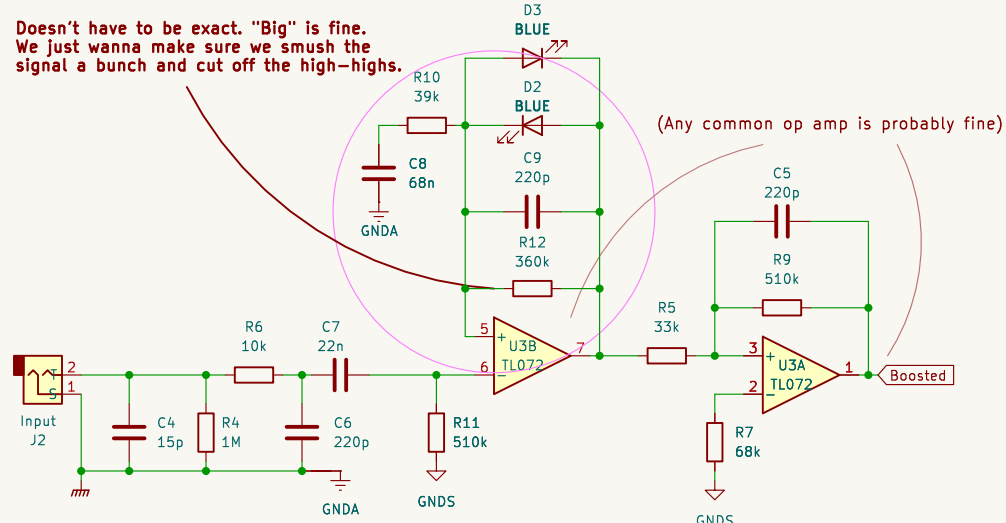
Input J2

Output Boosted

Components:

- Resistors: R4 (1M), R6 (10k), R10 (39k), R11 (510k), R12 (360k), R9 (510k)
- Capacitors: C4 (15p), C6 (220p), C7 (22n), C8 (68n), C9 (220p), C5 (220p)
- Op-Amps: U3A (TL072), U3B (TL072)
- Diodes: D2 (BLUE), D3 (BLUE)

Grounds: GNDA, GNDS, GND



# PLL Notes:

1. RV4 + RV2 make noise when:  
both up/down/full-opposite.  
(Only one extreme == usable).  
Play with sizes/ranges!
2. RV4 and C12 set the center frequency:  
If R4 gets smaller; make C12 bigger.
3. Increase R37 = less droop/slide/wah.
4. Fiddle with the diodes and stuff!
5. P.S. Signals ARE also at PC1/PCP, BTW.
6. When PCP = HIGH + PC1 = LOW 4+ times  
in a row: you are at frequency lock!
7. If you put a counter/divider between  
CompII out and VCOIn, the PLL will  
shift the frequency UP as much as the  
divider divides. Use one half of the  
CD4013 in the loop instead: octave up!

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## 4. Summing Stage & Output

Down1

Down2

SW1  
Sub-Octaves

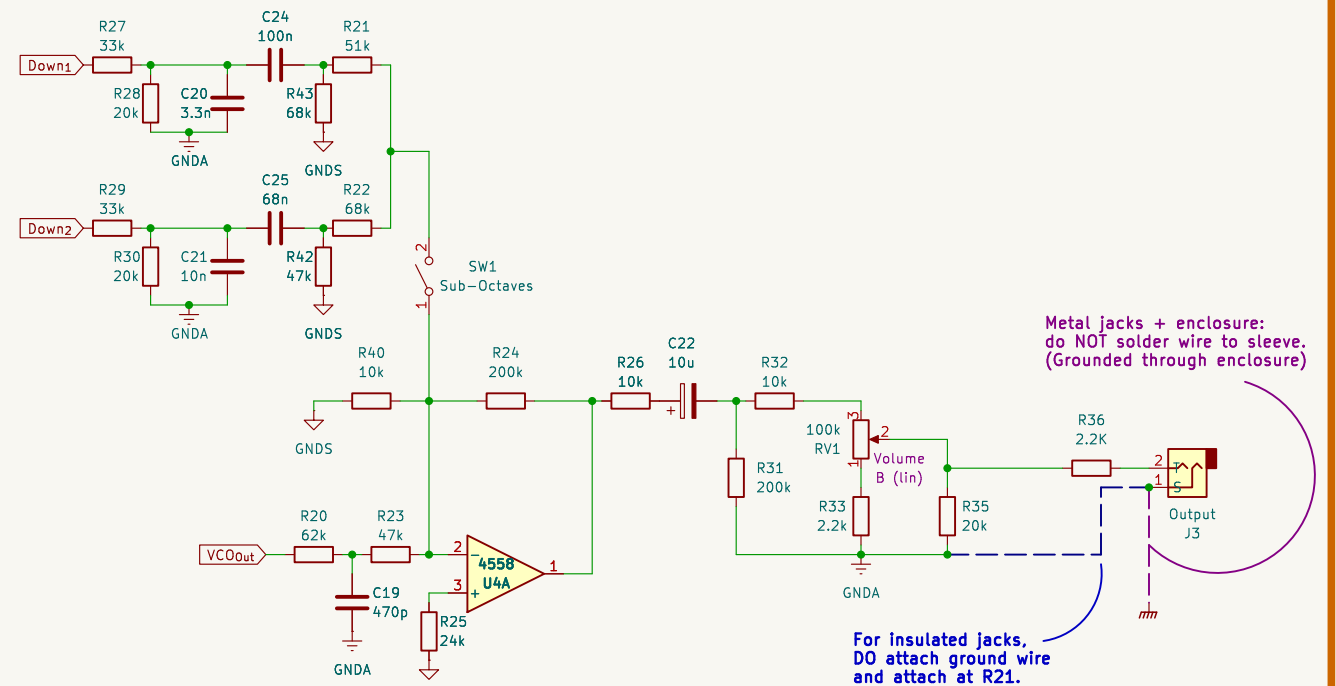
VCOOut

4558  
U4A

Output J3

Metal jacks + enclosure:  
do NOT solder wire to sleeve.  
(Grounded through enclosure)

For insulated jacks,  
DO attach ground wire  
and attach at R21.



# 0. Power + VRef

Or any Schottky.  
Or any Diode at all that is rated for:

- \* 180mA+ repetitive forward current
- \* 80mA+ continuous forward current
- \* rated for 500mW
- \* 24V continuous reverse voltage

(All overestimates)

This is the "star point" for all of the CD4xxx IC's

This is the "star point" for all your 0V grounds!

"Analog Ground" a.k.a. "Audio Ground" a.k.a. "Ground Reference"

This is the "star point" for all your 4.5 refs!

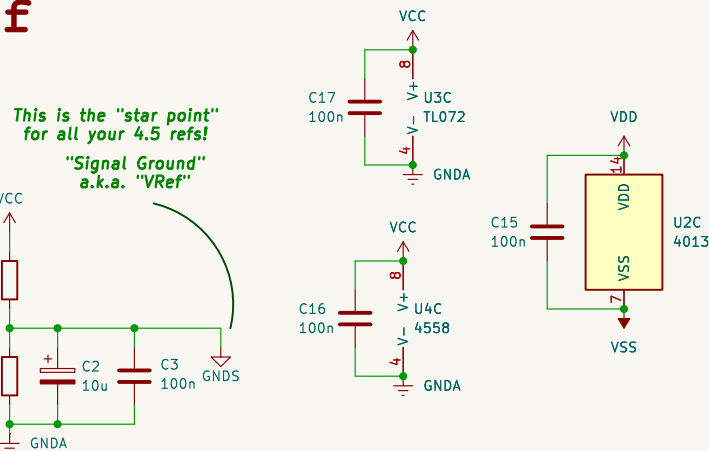
"Signal Ground" a.k.a. "VRef"

1

2

3

4



# WARNINGS :

- LUNCHTIME HACK / ALPHA!
- Keep the volume low while experimenting. This circuit can produce very high or loud tones if adjusted live!
- Breadboard before you solder anything! This is hastily documented and NOT double checked! (Yet)

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<b>NOTES:</b> <ul style="list-style-type: none"> <li>- Connect ground symbols at respective star grounds</li> <li>- You can omit VSS and just use GNDA as audio ground (I think the signal will swamp out any noise anyway)</li> <li>- Octave down is optional: just exclude CD4013</li> <li>- This was another lunch hack: don't judge.</li> <li>- Do hack!</li> </ul>		
<p>WARNING: HACK! NOT CHECKED FOR ERRORS (yet).</p> <p>Pink Circles = Fiddle with these! (Fiddle with any)</p> <p><b>Andrew T. Canaday (povins), D.B. Buchholz (QuickButterfly4571)</b></p> <p>Sheet: /</p> <p>File: OSM.kicad_sch</p>		
<p><b>Title: Olangrall's Sex Machine</b></p>		
Size: B	Date: 2025-01-17	Rev: 0.0.3a
KiCad E.D.A. 8.0.7		Id: 1/1

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KiCad E.D.A. 8.0.7

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