QuickLogic® ArcticPro™ 2 – GF 22FDX Data Sheet

Highlights

Low Power

- Ultra-low power eFPGA, architected for integration in SoCs targeting mobile applications
- Low leakage for extended battery life

Efficient Logic Utilization

- Super logic cell (SLC) with four logic cells in each logic cluster
- Supports combinatorial and sequential logic within each logic cell
- Logic cell output can be feedback to input of any logic cell within the SLC
- Shared register clock, set, and reset signals for better place and route efficiency
- Registered and nonregistered interface signals

Fast Time-to-Market

- Reduces development time and costs

Flexible Reconfigurable Logic

- Sizes ranging from 8x8 up to 64x64 SLC arrays
- Reconfigurable SRAM technology

Advanced Clock Network

- Multiple low skew clock networks
  - Six programmable global clock networks
- Quadrant and/or multiple sub-quadrant based clock networks depending on the size of the device

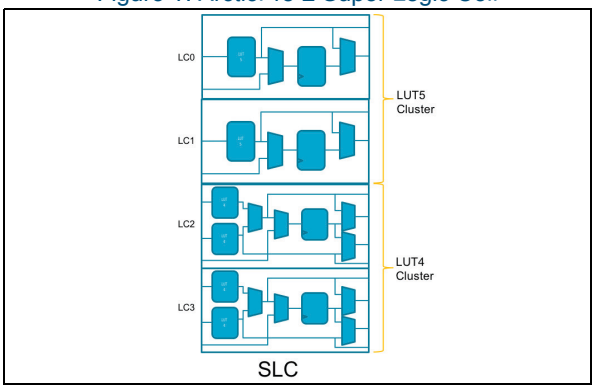
Configuration Controller

- Serial Peripheral Interface (SPI) Master and Slave
- APB3 for system on a chip (SOC) integration

Introduction

ArcticPro 2 was specifically architected to meet the increasingly complex needs of mobile device OEMs. With special attention paid to efficient logic cell utilization, smallest size, and lowest power consumption during the design process, ArcticPro 2 is the ideal solution for OEMs who require a configurable logic solution for their application. ArcticPro 2 operates seamlessly with any processor available on the market today to address emerging connectivity, sensor control, and custom applications.

Figure 1: ArcticPro 2 Super Logic Cell



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Programmable Logic Architectural Overview

Super Logic Cells

The SLC is a building block of the ArcticPro 2. If the logic cluster or highway network within the SLC is not used, it is powered off to save static power. Each SLC consists of the following:

- Two Separate Logic Clusters - Each SLC has four logic cells that are organized into two logic clusters. The logic cluster details are:
  - LC0 and LC1 contain two 5-input *Look-Up Tables* (LUTs), one register, and multiple muxes that enable the logic cell to perform different functions (for example: combinatorial, sequential, or both)
  - LC2 and LC3 contain of four 4-input LUTs.

  Direct input selection to the register allows combinatorial and sequential logic to be used separately. Multiple outputs per logic cell are strategically selected to either feedback within the same SLC or to travel to another SLC. A shared register clock, set, and reset signals for all four logic cells help reduce routing congestion.
- Street network – Routes signals from the global routing network (highway), as well as the feedback network, to the inputs of the logic cells.
- Feedback network – Allows some of the local logic cell outputs, as well as selected outputs from the four immediate orthogonal neighbor logic cells, to be routed back to the local logic cell inputs.
- Highway network – Routes signals from one SLC to other SLCs.
- Clock mux – Allows high fan-out signal to get on the clock tree and then routes to any input of the logic cells, except QCK.
- QCK mux – provides a dedicated clock path to the clock input of the logic cell registers.
- SLC-level power gating (SLC_PG) block – Controls the power gating of the logic cluster or the highway network inside the SLC.

Table 1 shows the SLC power characteristics.

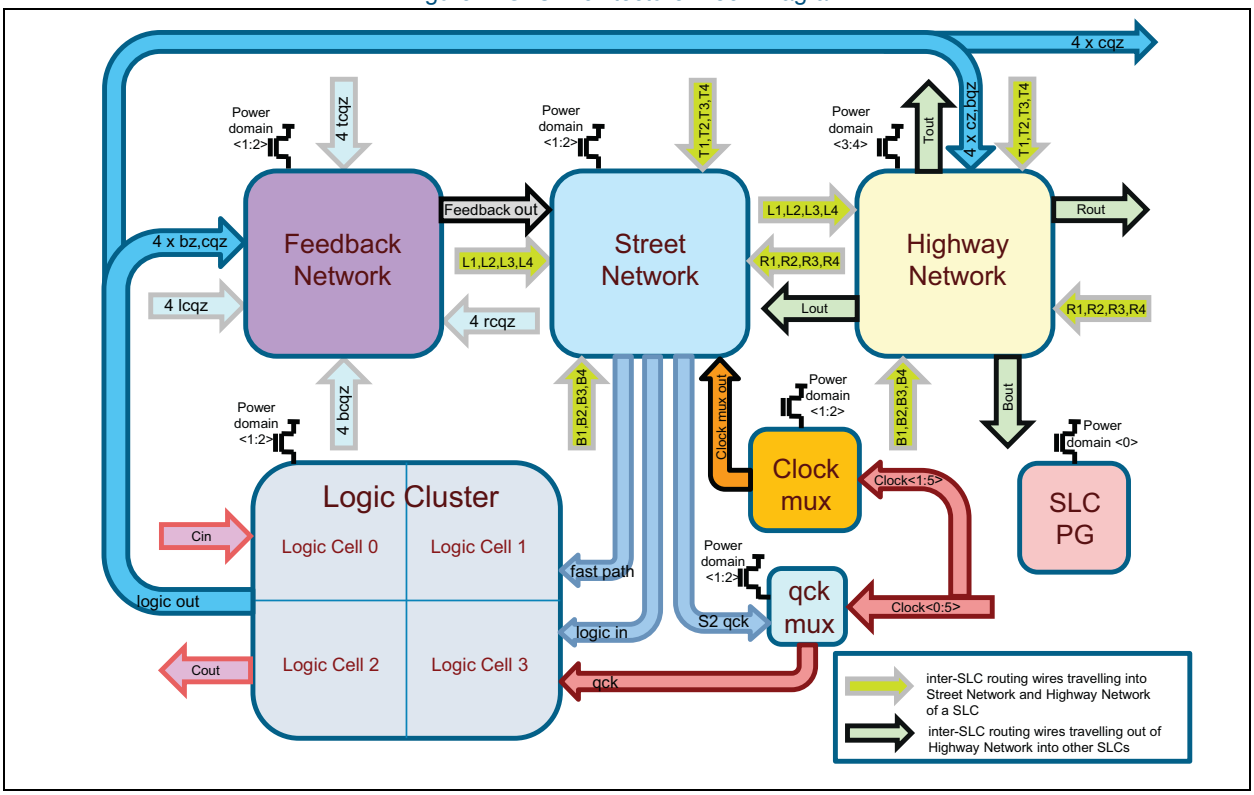
Table 1: SLC Power Characteristics

Parameters	Description	Power Used[a]	Unit
SLC Enable Power	Power consumption for SLC enable	1.76	uW
SLC in VLP	Power consumption in retention mode	0.3224	uW
SLC Power Down	Power consumption when SLC is unused	0.4712	uW
Interface Buffer Enable	Interface buffer power consumption in active	0.692	uW
Interface Buffer Disable	Interface buffer when unused	0.1864	uW
Interface Buffer in VLP	Interface buffer in retention	0.2176	uW
Dynamic Power	Based on 16-counter design	4.8	uW per MHz

a. The data is based on 25°C.

Figure 2 illustrates the SLC architecture and how it functions.

Figure 2: SLC Architecture Block Diagram



Distributed Clock Networks

Global Clocks

The ArcticPro 2 clock network architecture consists of a minimum of two levels of H-tree structure for the purpose of minimizing clock skew. For larger SLC array size, the H-tree structure can go up to four levels. The first level of the clock network spans from the clock input to the global clock muxes located at the center of the SLC array. From the global clock muxes, the clock tree network is extended to the middle of the quadrant, then sub-quadrant, and sub-sub-quadrant of the SLC array. Eventually, the clock network reaches each SLC through the fishbone structure of column clocks.

There are a total of six clock inputs for each ArcticPro 2 IP. From the global clock muxes, the clock output can be individually enabled or disabled as they enter into the four quadrant-level clock networks. A similar enable/disable feature can also be found in selected clock networks at the sub-quadrant and column clock levels. Locally generated signals can be selected and placed onto the clock network at any global, quadrant, sub-quadrant, or sub-sub-quadrant of the clock tree through the different levels of clock muxes.

Figure 3 shows the clock network.

Figure 3: Clock Network

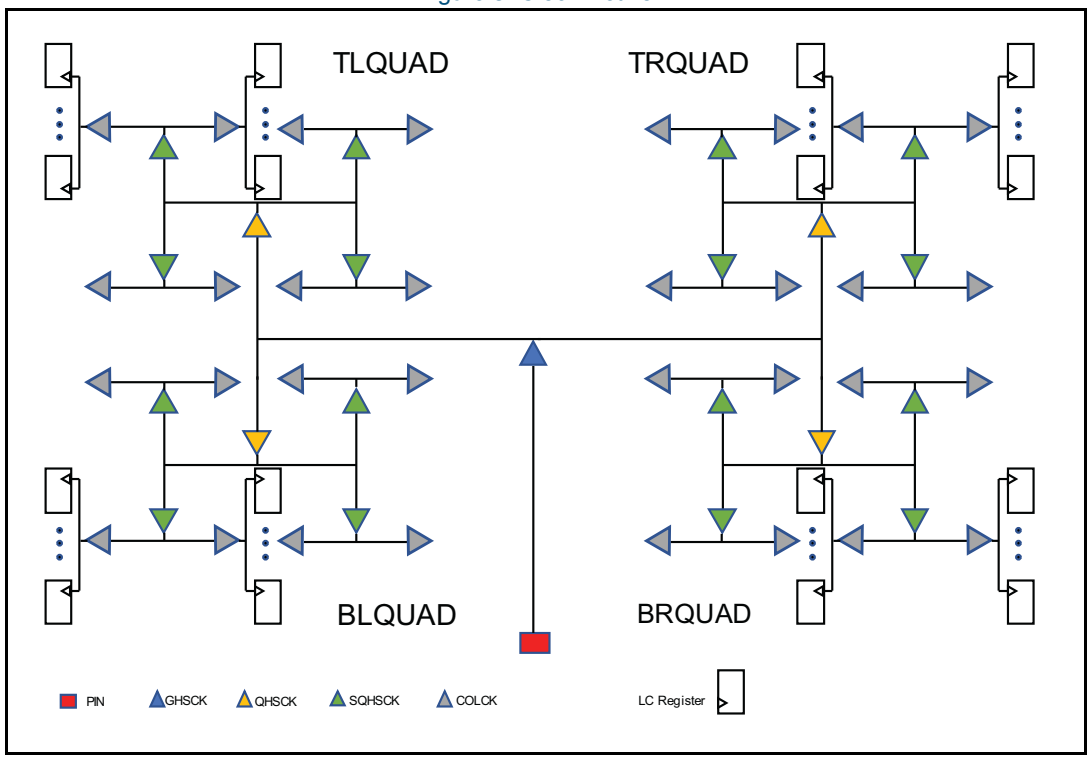


Table 2: Clock Tree Propagation Delay[a,b]

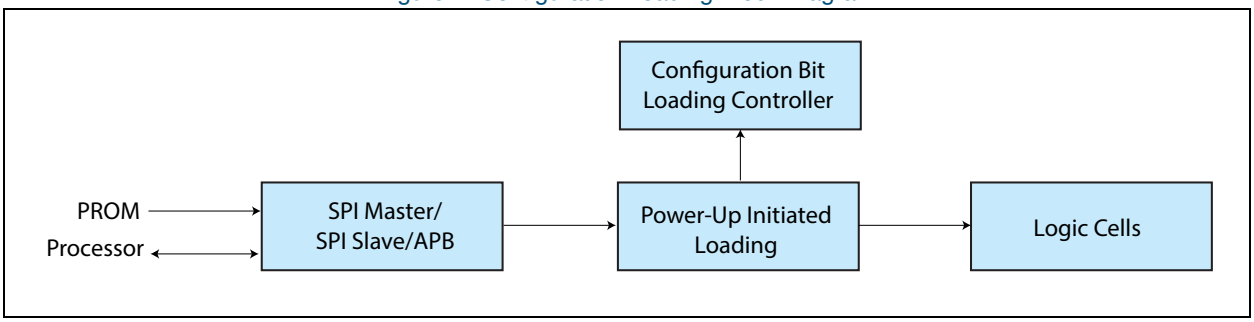
Method	Description	Propagation Delay (ns)		
		Min.[c]	Typ.	Max.[d]
$t_{PIN-QHSCK}$	From the external clock signals to the input of QHSCK (including GHSCK)	0.551	0.887	1.856
$t_{GHSCK-SQHSCK}$	From the input of QHSCK to the input of SQHSCK (including the buffers in QHSCK)	0.265	0.426	0.891
$t_{SQHSCK-COLCK}$	From the input of SQHSCK to the input of COLCK (including the buffers in SQHSCK)	0.117	0.188	0.393
$t_{COLCK-REG}$	From the input of COLCK to the input of LC register (including the buffers in COLCK)	0.162	0.261	0.546

a. Data based on an ArcticPro 2 test chip with an array size of 32x32 SLCs.
b. Timing is applicable to all points with expected minimum skew of 100 ps due to H-Tree clock tree structure.
c. Minimum conditions: FF, 125°C, 0.88V.
d. Maximum conditions: SS, -40°C. 0.72V.

ArcticPro 2 Configuration Loading

The ArcticPro 2 is reconfigurable. The configuration of an ArcticPro 2 must be loaded each time the device is powered on. As shown in **Figure 4**, the ArcticPro 2 provides three interfaces for configuring the logic cells within the device. These interfaces are SPI Master, SPI Slave, and Advanced Peripheral Bus (APB).

Figure 4: Configuration Loading Block Diagram



SPI Modes of Operation

The configuration controller of the ArcticPro 2 device can operate as a SPI Master or SPI Slave. When operating in SPI Master mode, the ArcticPro 2 device reads data from a Programmable Read-Only Memory (PROM). When operating in SPI Slave mode, the ArcticPro 2 receives data from a processor.

The SPI Slave interface is implemented in hard logic, and consumes significantly less power than a fabric-implemented SPI Master interface.

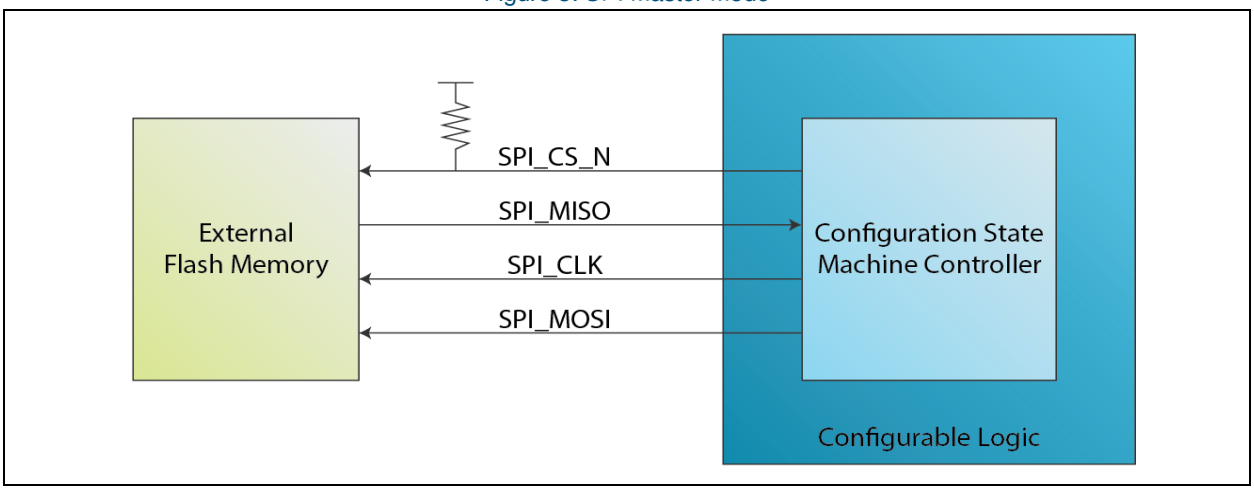
Operation in SPI Master mode or SPI Slave mode is determined by detecting either a logical high or low voltage on the SPI_CS_N pin upon de-assertion of SPI_RST_N.

- When SPI_CS_N is high, the ArcticPro 2 SPI controller enters SPI Master mode.
- When SPI_CS_N is low, the ArcticPro 2 SPI controller enters SPI Slave mode.

SPI Master Mode

In SPI Master mode (shown in **Figure 5**), SPI_RST_N must be asserted to hold the ArcticPro 2 in a reset state until the PROM is fully powered up and ready to be read. Upon de-assertion of SPI_RST_N, the ArcticPro 2 is set to SPI Master mode, takes control of the SPI pins, and starts initiating the required SPI commands.

Figure 5: SPI Master Mode



Configuration loading of the ArcticPro 2 requires a PROM of adequate size. The ArcticPro 2 SPI Master SPI clock frequency can operate up to 20 MHz during configuration. It is important to note that the VCCIO of the SPI pins for programming and normal operation must match the VCCIO of the PROM.

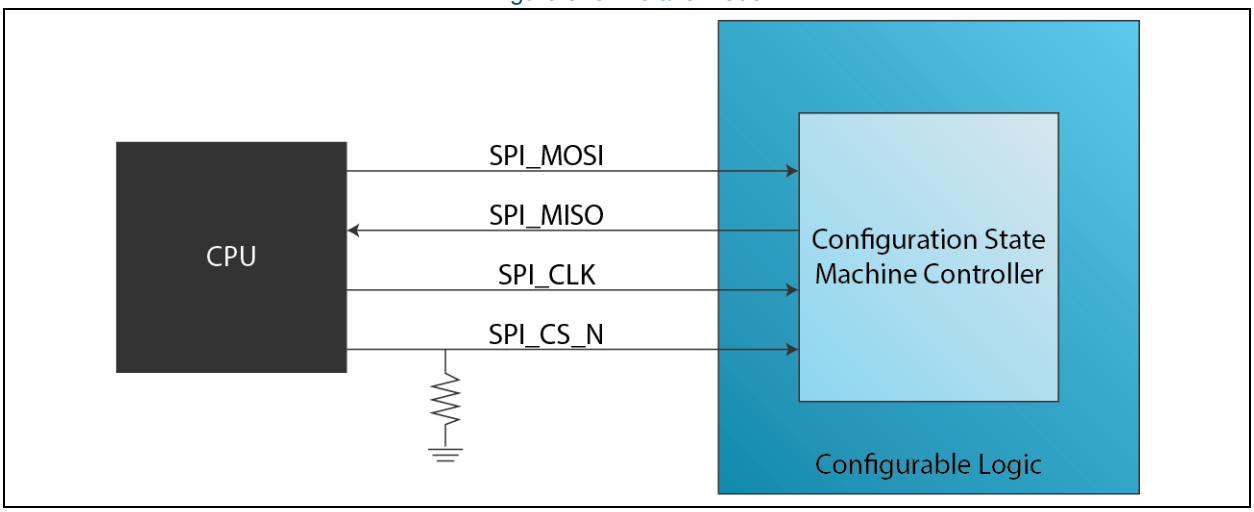
Upon completion of the loading, the PROM can be placed in a deep power down mode. To put the PROM into deep power down mode, the SPI Master sends a power down command after the last byte of data is received.

The PROM loading file used to program the external flash is generated by QuickLogic's QuickWorks software tools. The configuration data is constructed to work with the corresponding commands from the ArcticPro 2 SPI Master.

SPI Slave Mode

When the ArcticPro 2 is powered up in SPI Slave mode (shown in **Figure 6**), the SPI Master takes control of the SPI pins.

Figure 6: SPI Slave Mode



The configuration bit file, required for specifying the SPI Master commands, is generated by QuickLogic QuickWorks software tools. The resulting binary file combined with software drivers supplied by QuickLogic can be used for configuration loading of the ArcticPro 2.

Advanced Peripheral Bus (APB) Configuration

The processor can also configure the ArcticPro 2 device through the AMBA APB3 interface with a 32-bit data bus. (For more information about APB3, refer the ARM® Limited, *AMBA™ Specification*). Since APB3 is an internal bus, it can operate at a much higher frequency than SPI interfaces.

Configuration Verification Check Sum

To achieve higher system robustness, ArcticPro 2 uses a checksum algorithm to guarantee data integrity. Upon receiving the data from the PROM, a check sum mechanism is used to ensure the ArcticPro 2 configuration is intact. The final checksum is compared to those in the PROM checksum. If the checksums match, the CFG_DONE pin will go high. If the check sum does not match, the configuration controller retries configuration up to five times.

Power Management Unit

The ArcticPro 2 device is divided into four different power islands. Each power island consists of one-forth of the overall device size. In this case, each quadrant consist of a total of 16 x 16 SLC (256 SLC).

The size of the power island must not be too small, because a limited number of SLC can constrain the size of the user design being fit into the quadrant. An adequate quadrant size for fitting a variety of designs is 16 x 16 SLC, which is about 80% of the programmable fabric.

In addition to the power islands, the ArcticPro 2 device has a very low power (VLP) mode (retention mode) feature.

The power island implementation typically only involves the SLC array. However, there are exceptions:

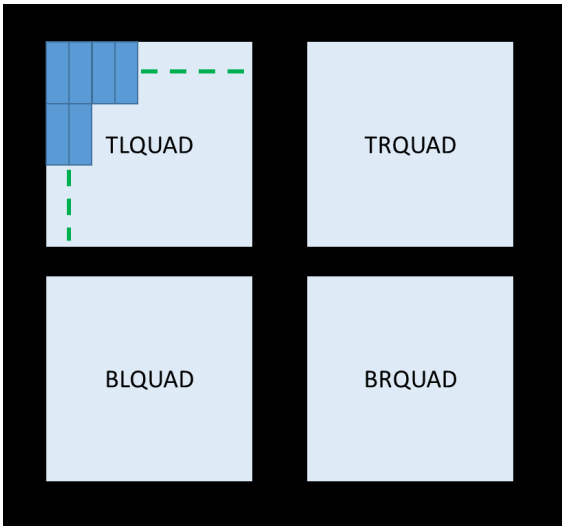
- Clock Cells

  All street/high networks of the clock cells are powered off, but the clock circuitry remains powered on. These include GHSCKMUX (2 instances), QHSCKMUX (4 instances), and SQHSCKMUX (16 instances).

- Interface Buffer SLCs

  All interface buffer SLCs are powered on.

Figure 7: SLC Array Floorplan



Clock tree-related circuits are always on, despite the size, due to the complexity of the power island implementation. While the leakage of the clock tree circuitry can be slightly higher, dynamic power is handled by a dynamically controllable signal in almost all levels of HSCKM.

eFPGA Power-Down Mode

The programmable Fabric can be independently powered down to save power in the device. During the power-down mode, the programmable Fabric powers down completely. This includes the logic cell, clock tree, macro interface, and configuration bits. Upon wake-up, the FPGA must be reconfigured.

Table 3 shows the power characteristics.

Table 3: Power-Down Mode Power Saving

Parameter	Percentage
Full chip	95

VLP Mode

The ArcticPro 2 has a unique feature, referred to as VLP mode, which reduces power consumption by placing the device in standby. The VLP mode can be operated at device level and at SLC quadrant level. Specifically, VLP mode can bring the programmable fabric standby current down. VLP mode is controlled through a register. The VLP mode is active high, so VLP mode is activated by pulling the register to VDD.

When the ArcticPro 2 goes into VLP mode, all register values in the programmable fabric are preserved. As the ArcticPro 2 exits out of VLP mode, the data from the registers will be used to recover the functionality of the platform.

VLP mode powers down all logic components while keeping the configuration bits alive. VLP does not power-down the interface buffer to the SLC. Each quadrant can be put in VLP mode independently as well as in combination of power-down/VLP mode, but not both at the same time. VLP mode does not involve the configuration controller.

The VLP mode characteristics are specified in **Table 4** through **Table 5**. Data is calculated with V_{MIN} = 0.72V at 25°C.

Table 4: VLP Characteristics

Parameter	Time	Unit
VLP mode enabled	1.136	uS
Wake Up from VLP mode	23.92	uS

Table 5: VLP Mode Power Saving

Parameter	Percentage
Full chip	48
Quadrant	12

Electrical Specifications

DC Characteristics

The DC characteristics are specified in **Table 6** through **Table 7**. Data is based on typical process, 0.8V, and 25 C with no back bias.

Table 6: Recommended Operating Range

Symbol	Parameter	Min.	Max.	Unit
VCC	Supply Voltage	0.72	0.88	V
TJ	Junction Temperature	-40	125.0	°C

Table 7: DC Characteristics[a]

Symbol	Parameter	Min.[b]	Typ.	Max.[c]	Units
I_{VCC}	Quiescent Current	0.2	2.96	108	mA
I_{VLP}	Standby Current with Retention	0.213	1.89	56	mA

a. Data based on an ArcticPro 2 test chip with an array size of 32x32 SLCs. The design is based on 32x32 SLCs with 100% SLC utilization. The data includes routing and interface buffers.
b. Minimum conditions: SS, -40°C. 0.72V.
c. Maximum conditions: FF, 125°C, 0.88V.

AC Timing Parameters

The critical components of the ArcticPro 2 eFPGA timing parameters are specified in **Figure 8** and **Figure 3** and **Table 8** through **Table 10**. Data is based on typical process, 0.8V, and 25 C with no back bias.

Figure 8: ArcticPro 2 Logic Cell Block Diagram

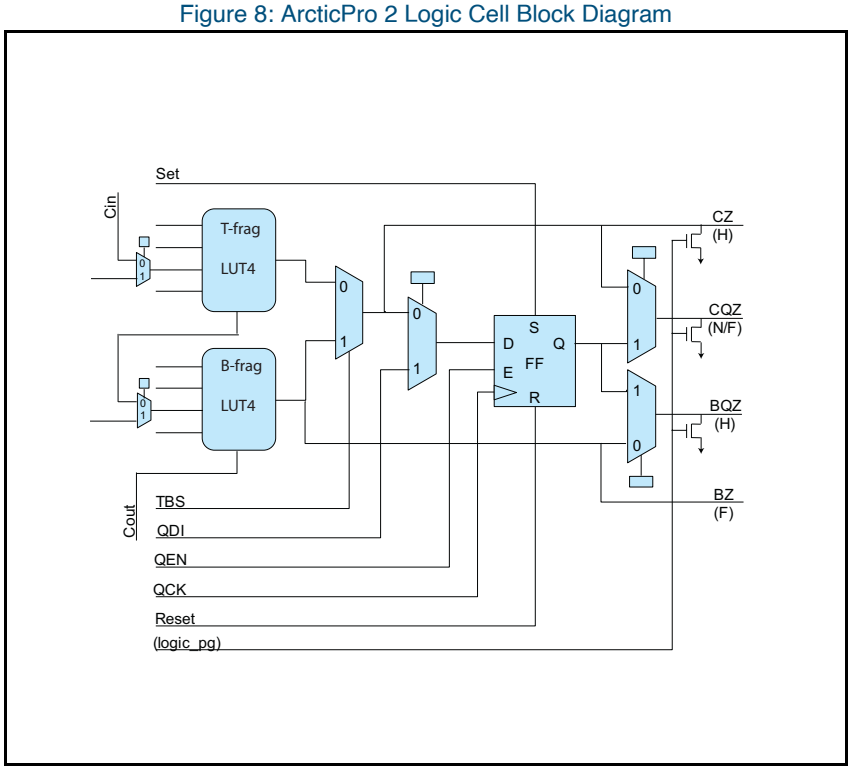


Table 8: Logic Cell Critical Path AC Parameters[a]

Symbol	Parameter	Propagation Delay (ps)			Power Consumption (nW/MHz)		
		Min.[b]	Typ.	Max.[c]	Min.[b]	Typ.	Max.[a]
$t_{PDTB-CZ}$	T/B frag input to CZ output delay (worst)	238	382	–	4.98	13	–
$t_{PDTB-CQZ}$	T/B frag input to CQZ output delay (worst)	268	431	–	9.19	24	–
t_{PDB-BZ}	B-frag input to CZ output delay (worst)	206	332	–	3.83	10	–
$t_{PDTB-BQZ}$	B-frag input to CQZ output delay (worst)	238	382	–	4.98	13	–
t_{CLK}	Clock to CQZ/BQZ output	128	206	–	4.98	13	–
t_{SU}	Setup time	27	44	–	–	–	–
t_{H}	Hold time	31	50	–	–	–	–
t_{CWHI}	Clock high time	34	55	–	–	–	–
t_{CWLO}	Clock low time	31	50	–	–	–	–
t_{SET}	Set to Q output delay	62	99	–	0.61	1.6	–
t_{SW}	Set pulse width	62	100	–	–	–	–
t_{RESET}	Reset to Q delay	39	63	–	0.57	1.5	–
t_{RW}	Reset pulse width	44	70	–	–	–	–
t_{ES}	Register enable setup time	37	60	–	–	–	–
t_{EH}	Register enable hold time	–	–	–	–	–	–
t_{QDI}	Register direct input delay	80	129	–	–	–	–
$t_{CIN-COUT}$	Carry in to carry out delay within a LUT4	104	168	–	2.68	7	–

a. Data based on an ArcticPro 2 test chip with an array size of 32x32 SLCs.
b. Minimum conditions: FF, 125°C, 0.88V.
c. Maximum conditions: SS, -40°C. 0.72V.

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Table 9: Designs for ArcticPro 2 Silicon Validation for a 32x32 Configuration Test Chip

Design	Description	Frequency (MHz)			Power[a](mW)
		Min.[a]	Typ.	Max.[b]	
16-bit counter	16-bits synchronous up counter	171	250	361	0.868
256-bit shift register	256-bit synchronous shift register	318	448	741	1.11
8-bit adder	8-bit adder	490	704	1131	0.855

a. Minimum conditions: SS, 40°C, 0.72V.
b. Maximum conditions: FF, 125°C. 0.88V.

NOTE: The total power is measured for Nominal conditions at 10MHz.

Table 10: Total Time for Device Configuration in Various Modes (Calculated)[a]

Method	Description	Clock Frequency (MHz)	System Clock Frequency (MHz)	eFPGA Configuration Time (ms)
SPI Slave	External host to transfer data to eFPGA	20	80	29
SPI Master	Internal host load data from external memory	40	80	14.5
PIF8	Parallel interface 8-bit mode (test mode)	80	80	1.02

a. Data based on an ArcticPro 2 test chip with an array size of 32x32 SLCs.

Contact Information

Phone: (408) 990-4000 (US)
+(44) 1932-21-3160 (Europe)
+(886) 26-603-8947 (Taiwan)
+(86) 139-0517-5302 (China)
+(81) 3-5875-0547 (Japan)
+(82) 31-601-4225 (Korea)
E-mail: info@quicklogic.com
Sales: America-sales@quicklogic.com
Europe-sales@quicklogic.com
Asia-sales@quicklogic.com
Japan-sales@quicklogic.com
Korea-sales@quicklogic.com
Support: www.quicklogic.com/support
Internet: www.quicklogic.com

Revision History

Revision	Date	Originator and Comments
1.0	February 2017	Initial Release
1.1	October 2017	K.C. Yap and Kathleen Bylsma Updated Electrical Specifications.
1.2	January 2018	K.C. Yap, Lisa Pham and Kathleen Bylsma Added AC Timing Characteristics section.
1.3	February 2018	K.C. Yap and Kathleen Bylsma Updated Table 3. Logic Cell Critical Path AC Parameters, changed Power Consumption Units to nW/MHz. Updated Table 5. Designs for ArcticPro II Silicon Validation, changed shift register to 256-bit and added frequency and power values.
1.4	March 2018	K.C. Yap and Kathleen Bylsma Added conditions, minimum and maximum values to Tables 2 through 5.
1.5	September 2018	Lisa Pham and Khalid Hasnain Added the following tables: **Table 1**, **Table 3**, **Table 4**, and **Table 5**. Updated **Table 7** and **Table 9**.

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