gf22 FLL

(FLL version 3.3)

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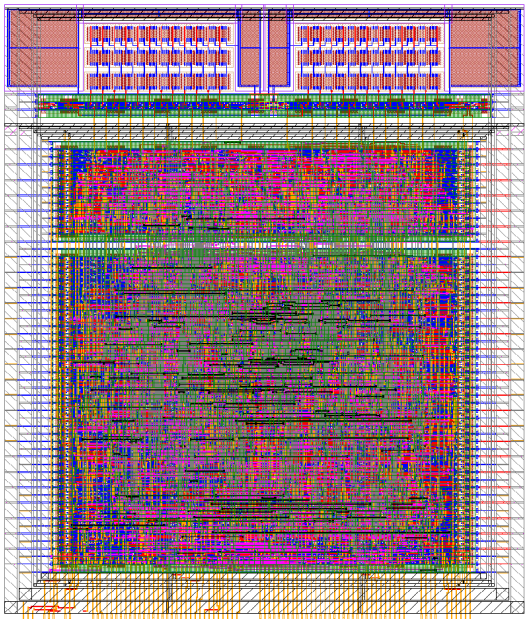
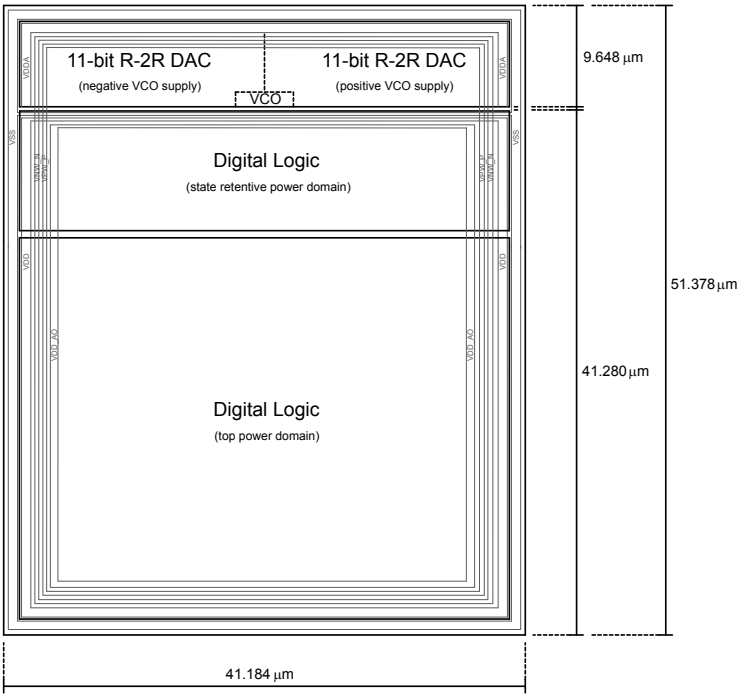




I. Specification Summary

Technology	gf 22 nm CMOS						
Pdk	V1.3_1.0						
Top Metal Layer	C3						
Signal Pins Layer	C1						
Power / Ground Pin Layer	C2, C3						
Poly Orientation	Vertical						
Area (analog)	$1'538.15$						μm^2
Area (digital)	$5'127.16$						μm^2
Area (total)	$6'665.31$						μm^2
	min	nom	max	min	nom	max	unit
Supply voltage (digital)	0.59	0.65	0.72	0.72	0.8	0.88	V
Supply voltage (analog)	0.59	0.65	0.72	0.72	0.8	0.88	V
	min	typ	max	min	typ	max	unit
Max reference frequency					50		MHz
Max FLL frequency				1.5	1.7		GHz
Max FLL frequency (digital)	0.52	1.54		1.5	2.5		GHz
Max DCO output frequency (analog)					3.3		GHz
Startup FLL frequency					17.5		MHz
Frequency resolution (w/o dithering)							MHz
Frequency resolution (with dithering)							kHz
Max. clock rate (config. interf.)	89	95		95	97		MHz
							unit
Power (analog, avg. across DCO range)							μW
Power (digital, stand-alone mode, $f_{DCO} \approx 35$ MHz, $f_{FLL} = 1/2 * f_{DCO}$)						5.2	μW
Power (digital, normal mode, $f_{DCO} = 1000$ MHz, $f_{FLL} = 1/2 * f_{DCO}$)						124.1	μW
Power (digital, normal mode, $f_{DCO} = 2000$ MHz, $f_{FLL} = 1/2 * f_{DCO}$)						248.7	μW
Power (digital, normal mode, $f_{DCO} = 3000$ MHz, $f_{FLL} = 1/2 * f_{DCO}$)						374.2	μW
Power (digital, stand-alone mode, $f_{DCO} \approx 1000$ MHz, $f_{FLL} = 1/2 * f_{DCO}$)						119.4	μW
Power (digital, stand-alone mode, $f_{DCO} \approx 2000$ MHz, $f_{FLL} = 1/2 * f_{DCO}$)						243.9	μW
Power (digital, stand-alone mode, $f_{DCO} \approx 3000$ MHz, $f_{FLL} = 1/2 * f_{DCO}$)						369.7	μW
Leakage Power (digital)						0.74	μW
Power (retention) (total)							nW

II. Pin Description

Pin	Direction	Description
FLLCLK	out	FLL clock out
FLLOE	in	FLL clock output enable (active high)
REFCLK	in	reference clock input
LOCK	out	FLL lock signal (active high)
CFGREQ	in	configuration port handshake
CFGACK	out	configuration port handshake
CFGAD[0:1]	in	config address
CFGD[0:31]	in	config data in
CFGQ[0:31]	out	config data out
CFGWEB	in	config reg write enable (active low)
RSTB	in	global async reset (active low)
RET	in	async state retention signal (active high)
PWD	in	async power down (active high)
TM	in	test mode (active high)
TE	in	scan enable (active high)
TD	in	scan in 1
TQ	out	scan out 1
JTD	in	scan in 2 (JTAG)
JTQ	out	scan out 2 (JTAG)
VDD	inout	digital supply (0.8 or 0 V)
VDD_AO	inout	always-on supply for retention (0.8 V)
VSS	inout	digital/analog ground
VNW_N	inout	digital/analog body bias connection nMOS (nominal 0.0 V)
VPW_P	inout	digital/analog body bias connection pMOS (nominal 0.0 V)
VDDA	inout	analol supply (0.8 V)

III. TESTING

The FLL features a scan test interface for fabrication testing using ATPG (automatic test pattern generation). There are two scan chains: Chain 1 contains the most important configuration registers (optimized for JTAG use) with input pin JTD and output pin JTQ. Chain 2 contains all the remaining registers in the block except for the flip-flops in the clock divider unit. The clock divider unit is not scan testable.

Pin	Direction	Description
TM	in	increase testability (active high, tie low during normal operation)
TE	in	scan enable (active high, tie low during normal operation)
JTD	in	serial scan data input chain 1 (optimized for JTAG)
JTQ	out	serial scan data output chain 1 (optimzed for JTAG)
TD	in	serial scan data input chain 2
TQ	out	serial scan data output chain 2
REFCLK	in	scan chain shift clock
RSTB	in	reset signal (active low)

The JTAG scan chain has 83 bits and traces trough:

```
JTD (input)
cfgreg_1[0]
   ⋮
cfgreg_1[31]
cfgreg_2[0]
   ⋮
cfgreg_2[27]
cfgreg_2[29]
   ⋮
cfgreg_2[31]
intreg_2[6]
   ⋮
intreg_2[25]
JTQ (output)
```

IV. Configuration Register Map

The register map includes 3 registers that control the operation of the FLL and 1 registers to monitor its status.

Address	Access	Reset	Description: Bit range	Function
0x0	R		Status register I:	
		0x0000	31-16	n/a
		0x0000	15-0	current multiplication factor (i.e., current frequency)
0x1	R/W		Configuration register I:	
		0b0	31	Operation mode select (0=stand-alone, 1=normal)
		0b1	30	FLL output gated by LOCK signal (active high)
		0x1	29-26	FLL output clock divider setting (default: divide-by-2, see Section VI for details)
		0x088	25-16	DCO input code for stand-alone mode
		0x05F5	15-0	Target clock multiplication factor for normal mode
0x2	R/W		Configuration register II:	
		0b0	31	Dithering enable (active high)
		0b0	30	Open-loop-when-locked (active high)
		0b0	29	Config clock select in STA mode (0=DCOCLK, 1=REFCLK)
		0b0	28	n/a
		0x200	27-16	lock tolerance: margin around the target multiplication factor within which the output clock is considered stable
		0x10	15-10	In normal mode: no. of stable REFCLK cycles until LOCK assert. In stand-alone mode: upper 6-bit of LOCK assert counter target.
		0x10	9-4	In normal mode: no. of unstable REFCLK cycles until LOCK de-assert. In stand-alone mode: lower 6-bit of LOCK assert counter target.
		0x7	3-0	FLL loop gain setting (default: $2^{-7} = 1/256$)
0x3	R/W		Integrator register:	
		0x00	31-26	n/a
		0x088	25-16	Integrator state: integer part (DCO input bits)
		0x000	15-9	Integrator state: fractional part (dither unit input)
		0x0	8-0	n/a

V. Configuration Interface Protocol

The configuration registers are clocked with the reference clock while the configuration interface maybe driven with any asynchronous clock. Thus, the asynchronous configuration interface uses a 4 phase handshake protocol to read and write from the configuration registers.
The CFGREQ is synchronized with the reference clock on the rising edge and is propagated through a chain of 4 flip-flops. The CFGACK is the output of the last flip-flop in the chain. The configuration data present at the CFGD port is latched into the configuration register selected by CFGAD with the 3rd rising edge of the reference clock after the CFGREQ has been asserted. CFGAD is also latched into a register with the 3rd rising edge of the reference clock after the CFGREQ has been asserted. The stored version of the CFGAD selects the configuration register output to appear at the CFGQ port.

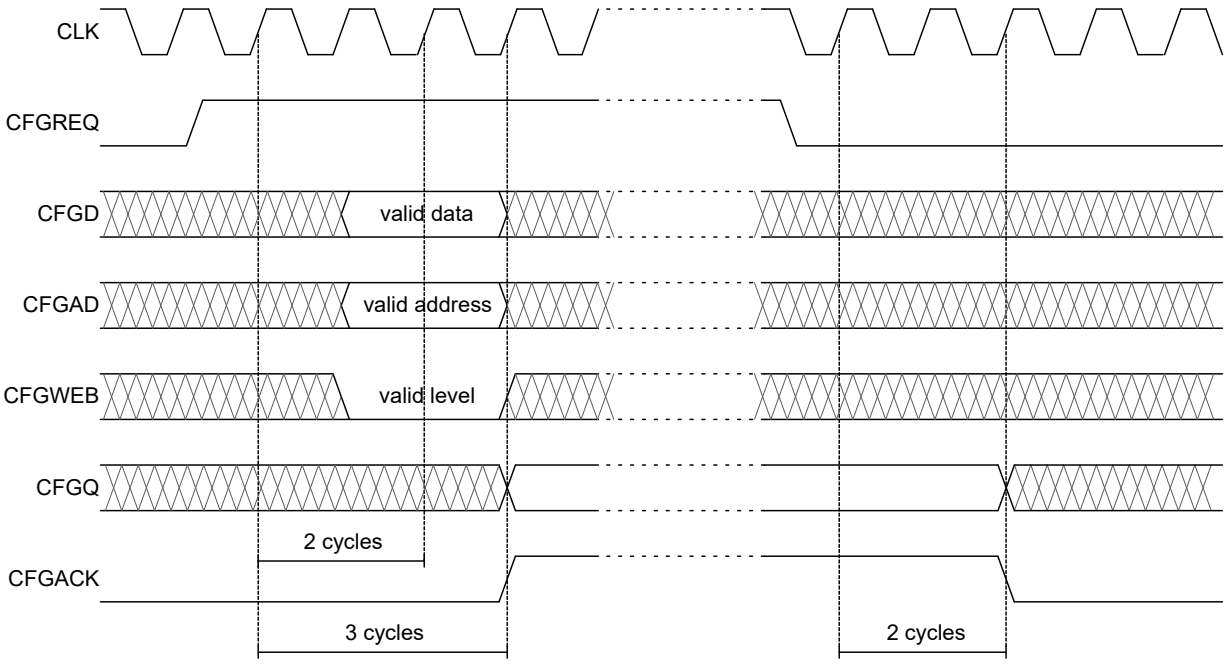


Fig. 1: Waveform and timing of the interface protocol.

VI. Setting the FLL output frequency

A. Normal mode

In the Normal mode, the output frequency is regulated such that it is a function of the reference clock frequency f_{ref}, the multiplication factor M (set in the configuration register I) and of the feedback clock divider D_{out} settings (set in the configuration register I). The output frequency in the Normal mode can be calculated as follows:

$$f_{out,Normal} = f_{ref} \cdot \frac{M}{D_{out}}$$

The relationship between the clock divider value in the configuration register and D_{out} is as follows:

Divider setting	D_{out}	duty-cycle	internal DCO frequency
0	1	arbitrary	$M \cdot f_{ref}$
1	1	50%	$2 \cdot M \cdot f_{ref}$
2	2	50%	$2 \cdot M \cdot f_{ref}$
3	4	50%	$2 \cdot M \cdot f_{ref}$
4	8	50%	$2 \cdot M \cdot f_{ref}$
5	16	50%	$2 \cdot M \cdot f_{ref}$
6	32	50%	$2 \cdot M \cdot f_{ref}$
7	64	50%	$2 \cdot M \cdot f_{ref}$
8	128	50%	$2 \cdot M \cdot f_{ref}$

B. Stand-alone mode

The FLL can be operated in an unregulated stand-alone mode, if the operation mode select bit in configuration register I is cleared. In this mode, the control loop is not operational and the frequency is unregulated. No reference clock is required, and the output frequency of the FLL is directly determined via the input word of the DCO. The configuration interface remains operational, i.e., all configuration register are accessible for read and write operations. The DCO input word can directly be set in configuration register I (see Section IV for the register bit map, and Section X-A for the DCO frequency transfer function). The effective output frequency is determined by the DCO transfer function $\mathrm{TF}(d)$, where d is the digital DCO input word, the clock frequency select setting in stand-alone mode S (set in the configuration register I), and the FLL output divider setting D_{out} (set in the configuration register I). The output frequency in the Stand-alone mode can be estimated as follows:

$$f_{out,Stand-alone} = \frac{\mathrm{TF}(S)}{D_{out}}$$

The relationship between the clock divider value in the configuration register and D_{out} is as follows:

Divider setting	D_{out}	duty-cycle
0	1	arbitrary
1	2	50%
2	4	50%
3	8	50%
4	16	50%
5	32	50%
6	64	50%
7	128	50%
8	256	50%

VII. Hardware Architecture

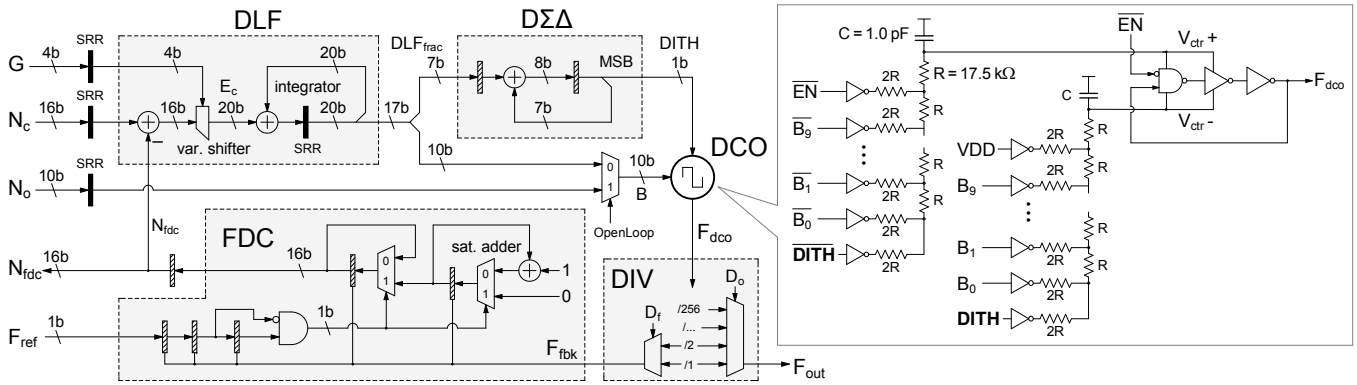


Fig. 2: Architecture of the FLL. Detail of the DCO comprising of 2 dither-enabled R-2R DACs and a 3-inverter ring-oscillator. SRR = state-retentive registers.

The FLL hardware architecture is illustrated in Figure 2. The FLL is composed of a digitally-controlled oscillator (DCO), a frequency-to-digital converter (FDC), a digital loop filter (DLF), a digital $\Sigma\Delta$-modulator (D$\Sigma\Delta$), and a binary clock divider (DIV). The loop realizes an integral-type controller minimizing the error signal given by the difference between the desired clock multiplication factor $\mathrm{N_c}$ (i.e., the setpoint of the loop in closed-loop mode) and the effective multiplication factor $\mathrm{N_{fdc}}$. The resulting loop feedback frequency $\mathrm{F_{fbk}}$ is $\mathrm{N_c}$-times higher than the reference frequency $\mathrm{F_{ref}}$, while the DCO output frequency $\mathrm{F_{dco}}$ is either equal or double the feedback frequency, depending on the divider setting.

The DLF is a multiply-and-accumulate unit implementing an integrator with configurable gain G using fixed-point arithmetic with 10 integer bits and 16 fractional bits. The gain is configurable between 2^{-10} and 2^{-1}. The integer bits of the integrator are the input code to the DCO bits $\mathrm{B_0}$ to $\mathrm{B_9}$, whereas the 7 most significant fractional bits are fed to the D$\Sigma\Delta$ for the generation of the dithering pattern.

The D$\Sigma\Delta$ is a digital, error-feedback-type 1^{st}-order $\Sigma\Delta$-modulator with one-bit quantization. The D$\Sigma\Delta$ generates a 128 bit-periodic 1-bit signal DITH having an average value equal to the fractional number represented by the 7 bit input $\mathrm{DLF_{frac}}$. The dithering scheme using a 7 bit fractional increases the nominal DCO resolution to 17 bit.

The DCO consists of two R-2R DACs and a short voltage controlled ring-oscillator. The detailed schematic of the DCO is shown in the inset of Figure 2. The 3-inverter ring-oscillator is composed from one voltage controlled NAND-gate, two voltage controlled inverters and two level-restoring inverters. All the employed digital gates are unaltered cells from a standard cell library. The R-2R DACs are realized with twenty-four 15 kΩ poly-silicon unit resistors providing 11 bit of nominal resolution. Since each DAC only needs to operate in one half of the supply swing, only half of the dynamic range is actually required. During operation, the MSBs of the upper and lower DAC are fixed to VDD and GND, respectively. The active-low enable signal EN is part of the power-down scheme and is equal to GND during normal operation. Thus, the required input code word is 10 bit wide. The DAC outputs are buffered by large capacitors to protect the ring-oscillator from supply ripples, filter thermal noise from the DAC resistor structure, and provide 1^{st}-order low-pass filtering.

The FDC is implemented as a synchronous digital counter driven by the DCO output clock signal. It counts the number of rising clock edges of the DCO output clock occurring within one reference clock period

$\mathrm{N_{fdc}}$. This number is an approximation of the instantaneous clock multiplication factor. The measurement uncertainty is at most one DCO clock cycle, i.e., the measurement error is approximately $1/\mathrm{N_{fdc}}$. Since we are targeting multiplication factors of hundreds to thousands, the FDC measurement error can be considered insignificant. The FDC counter is sampled and reset at each falling edge of the reference clock, which allows us to maintain a single-edge triggered DLF while having a short FDC delay of only half a reference clock period. Consequently, the DCO is updated roughly in the middle of an FDC measurement window, and therefore the FDC output value corresponds to the average between the DCO output frequency of the previous and the current reference clock period.

The binary clock divider (DIV) consists of three subsequent divider stages; two independent asynchronous divide-by-2 stages to handle the possibly high output clock rates of the DCO, followed by a synchronous divide-by-64 stage. Glitch-free clock muxes allow to select and switch between any of the available divided versions of the DCO clock seamlessly. Unused stages are clock gated to save power. The source of the feedback clock to the FDC $\mathrm{F_{fbk}}$ can be selected to be either the DCO directly or the first asynchronous divide-by-2 stage. The clock divide factor for the FLL output clock signal $\mathrm{F_{out}}$ is independently configurable from the feedback clock path, and can be any power of 2, up to a factor of 256.

VIII. Power Modes

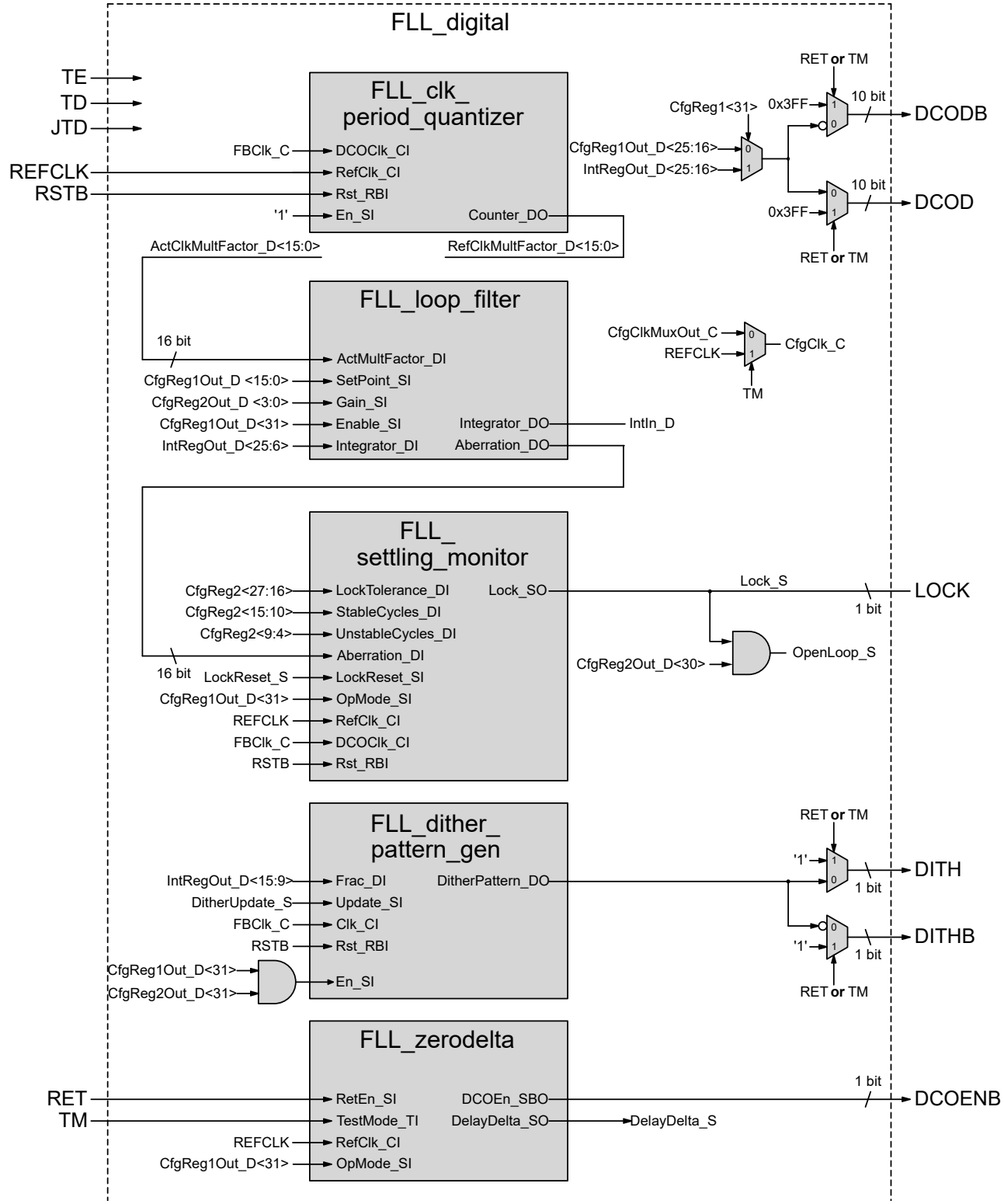
The FLL is partitioned into two power domains: one domain containing the retentive registers (the registers labelled SRR for state-retentive register in Figure 2), the secend domain containing the DCO and the rest of the digital logic.

This division allows the FLL to be operated in tow different power modes: the ACTIVE mode in which the complete FLL is powered-up and producing a clock signal; and, the SLEEP mode in which the configuration registers and the integrator register remain powered-up, while the rest of the digital logic including the DCO are being powered-down. In the SLEEP mode, the configuration registers and the integrator register retain their state, which allows the FLL to wake-up and instantly return to the operating point it was in before going to sleep.

For the FLL to transition savely to the SLEEP mode, the VDD power supply must remain active for at least three reference clock cycles after the retention signal (RET,active-high) has been asserted. To return safely to the ACTIVE mode the VDD power supply must be activeted and remain stable for at least three reference clock cycles before de-asserting RET. The retained state is immediately effective after the de-assertion of RET, however the loop will stay in open-loop configuration during the first three reference clock cycles after de-asserting RET, and will then change automatically to the closed-loop configuration. This makes sure that the loop state is not corrupted by the state of the period quantizer which is unkown after returning from SLEEP state.

The re-start time is on the order of the start-up time in open-loop mode since the DCO input value corresponds to the settled loop.

IX. Digital Control and Loop Logic — FLL_digital



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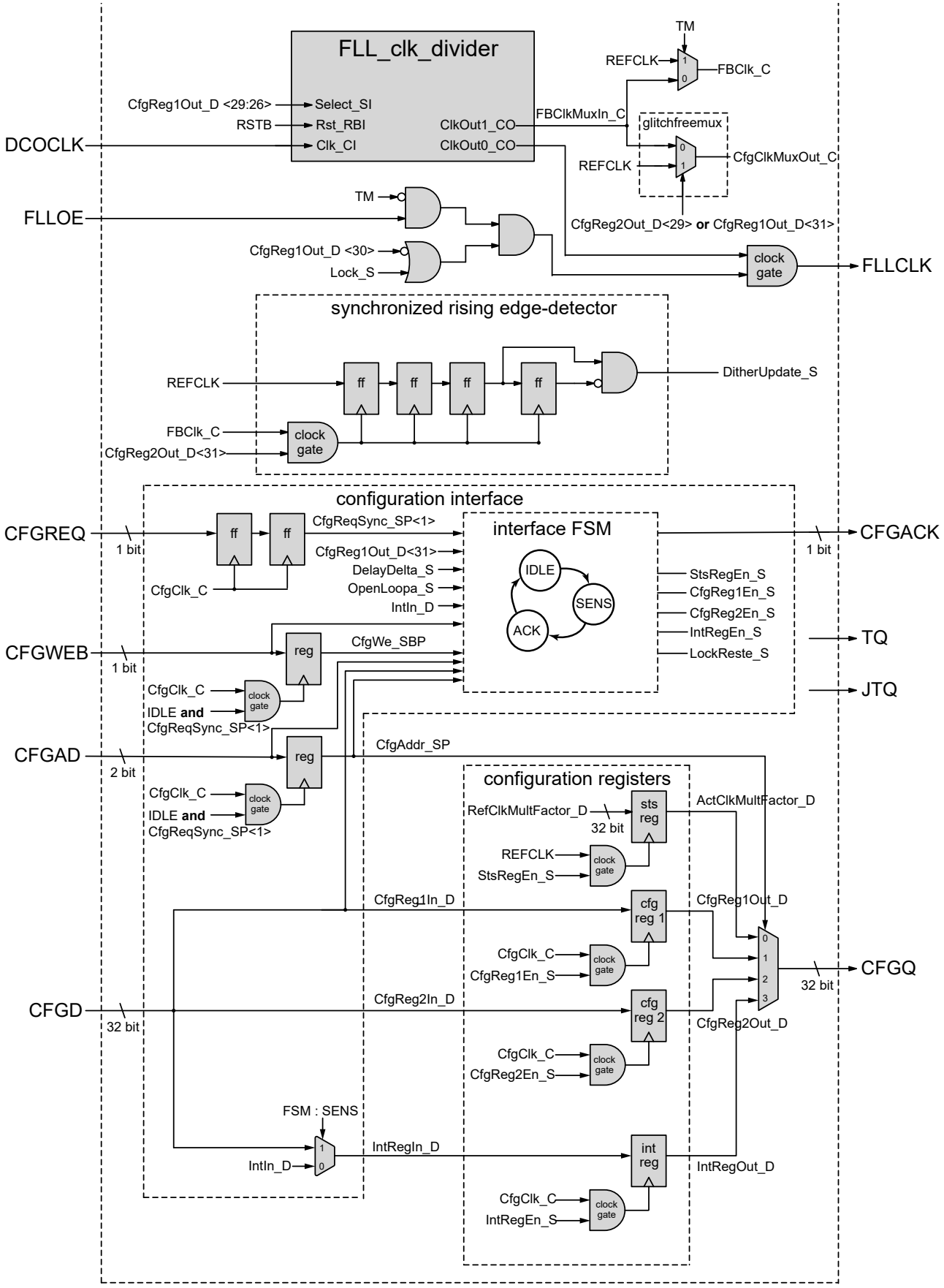

Complete block diagram of the digital section.

A. Asynchronous Clock Divider — `FLL_clk_divider`

The `FLL_clk_clkdivider` unit is a configurable clock divider that enables both the feedback clock and the FLL output clock to be a powers-of-two fraction of the DCO clock. The clock divider is composed of two asynchronous glitch-free divide-by-2 dividers connected back-to-back to bring the frequency to a save level to allow further division to be realized with a synchornous counter-based divider in the worst case. The feedback clock will not be divided by more than a factor of 2. The output clocks are selected via glitch-free muxes. The division factor for the FLL output clock can be selected via configuration register I (see Section IV for the corresponding bit map), and can be changed during operation without risk of glitching on both the freedback and FLL output clock lines. The default divider settings is divide-by-2, which is the smallest possible division factor that results in a 50% duty cycle.

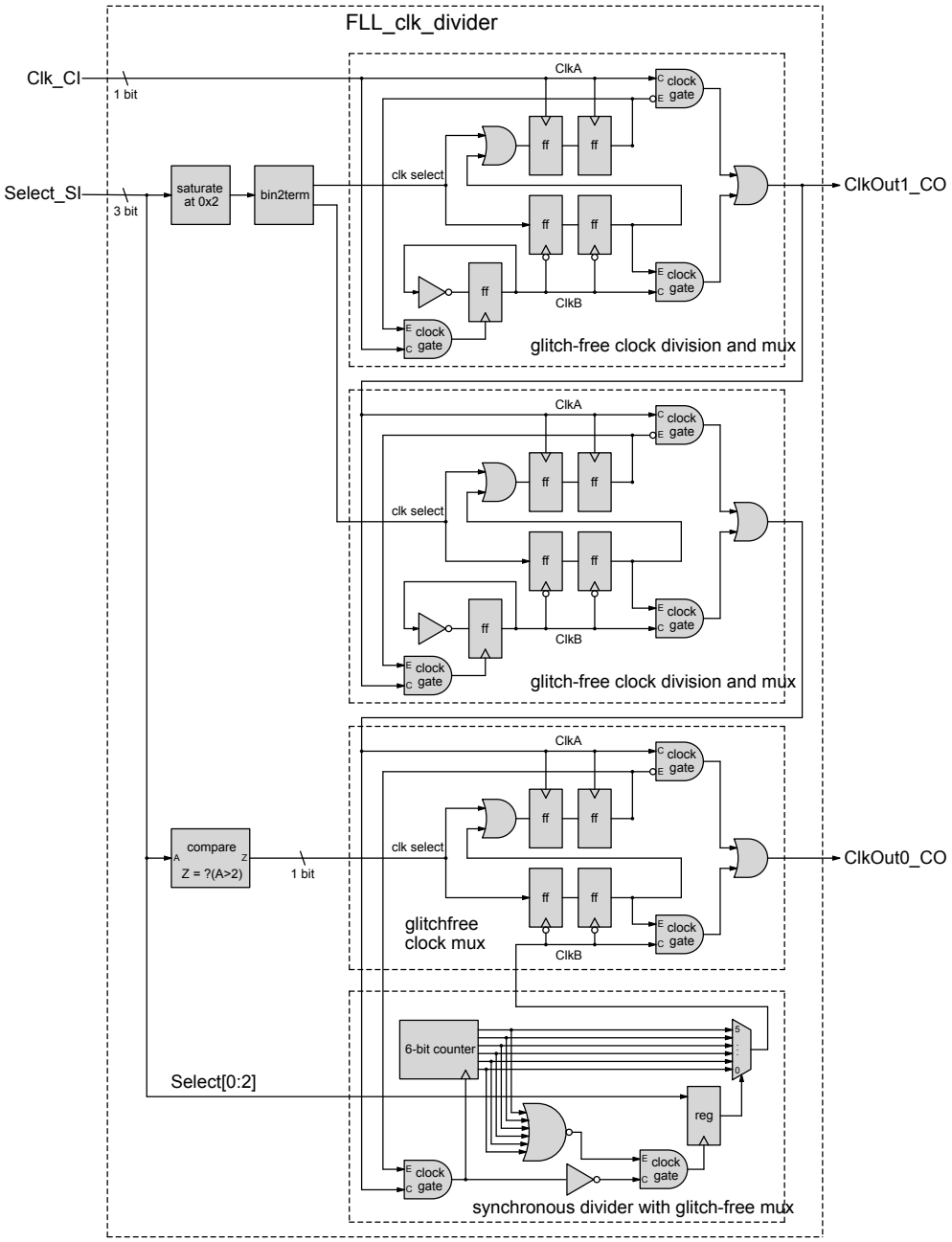

Fig. 3: Block diagram of the asynchronous clock divider.

B. Glitchfree clockmultiplexer — `FLL_glichfree_clkmux`

The `FLL_glitchfree_clkmux` unit is used to switch between the reference and the feedback clock as clock source for the FLL configuration interface. The selection occurs automatically depending on the operating mode of the FLL. In the stand-alone mode, the interface is clocked by the feedback clock to be able to set the FLL configuration in case there is no reference clock available. In the normal mode, the interface operates with the reference clock. It can be assumed that the reference clock is present in this mode, since otherwise the control loop would not be functional.

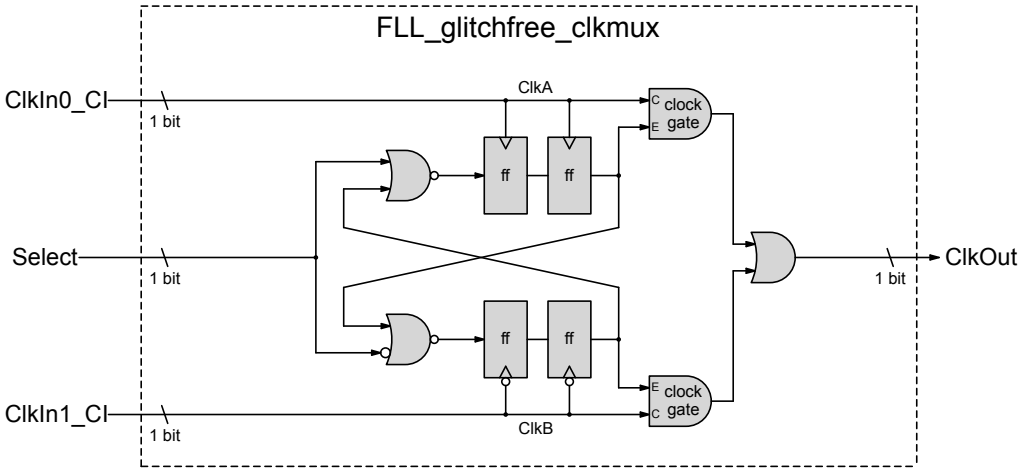

Fig. 4: Block diagram of the glitchfree clockmultiplexer for the configuration interface clock.

C. *Settling Monitor* — `FLL_settling_monitor`

The `FLL_settling_monitor` unit monitors the FLL output frequency, and provides a `LOCK` signal that indicates that the target frequency has been reached and is stable. The block diagram of the unit is shown in Figure 5.

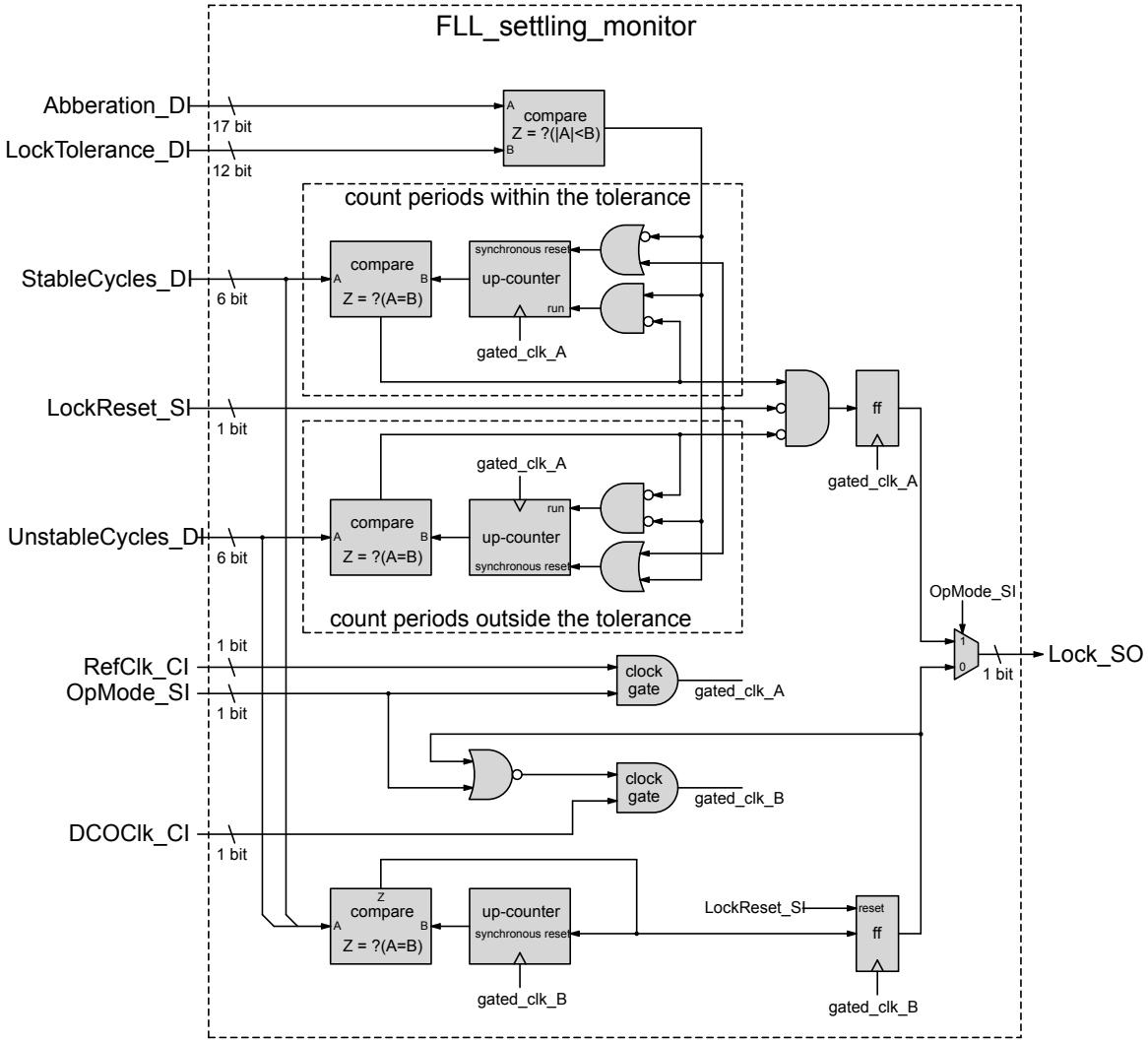

Fig. 5: Block diagram of the DCO frequency monitoring facilities.

In normal operation mode, the `LOCK` signal indicates whether the frequency is within the tolerance specified by the user via the configuration register II (see Section IV for the detailed register bitmap). Figure 5 and Figure 6 illustrate the lock signal behavior and the various timing quantities associated with it in the Normal operation mode of the FLL.

In the stand-alone mode, the `LOCK` signal is asserted after a predefined number of cycles after start-up of the FLL or after the frequency setting has been modified in configuration register I. The number of cycles is given by the number obtained via concatenating the value for the unstable cycles and stable cycles specified in configuration register II (see Section IV for the detailed register bitmap). Figure 5 and Figure 6 illustrate the lock signal behavior and the timing quantities associated with it in the Stand-alone operation mode of the FLL.

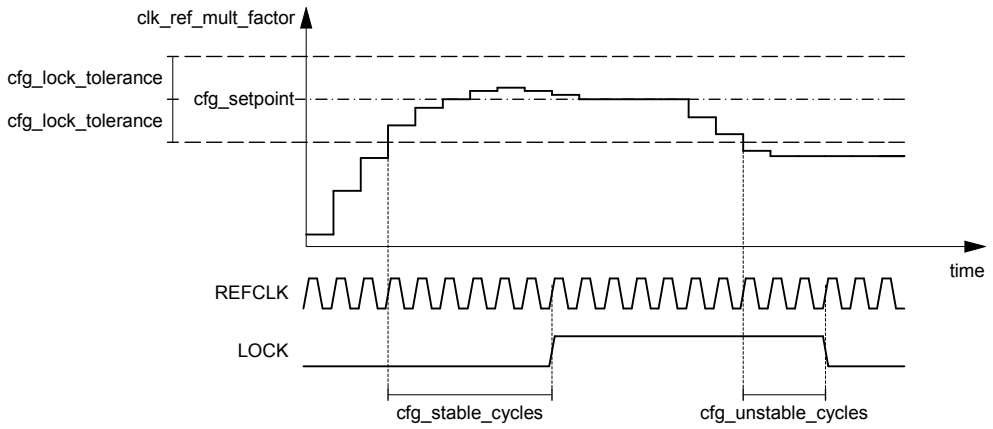

Fig. 6: Lock signal waveform (in Normal mode): Lock assertion and lock deassertion due to deviation of the DCO frequency beyond the tolerance limit set by the user.

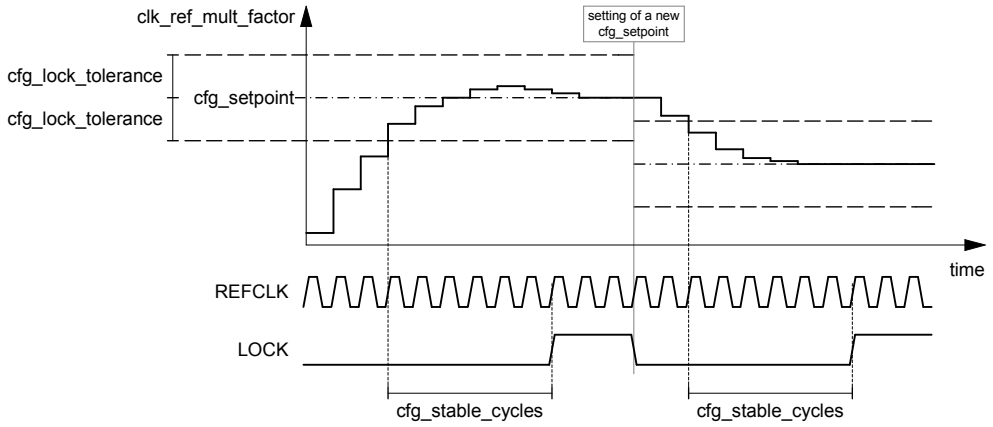

Fig. 7: Lock signal waveform (in Normal mode): Lock assertion and lock deassertion due to setting a new FLL output frequency.

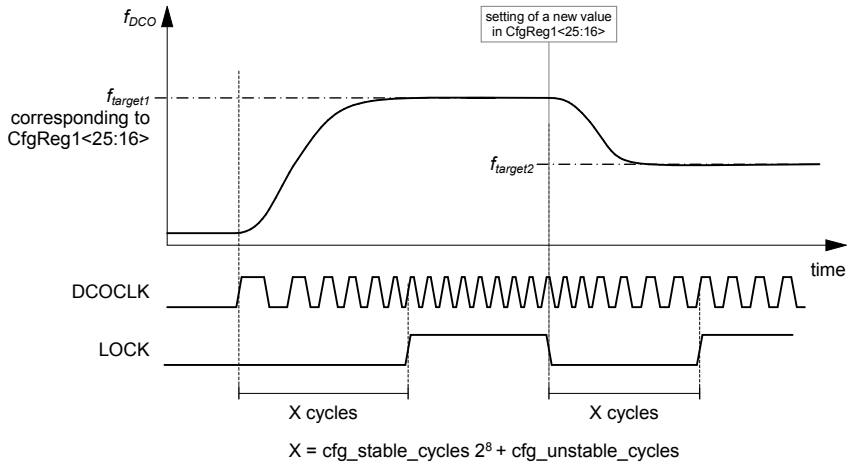

Fig. 8: Lock signal waveform (in Stand-alone mode): Lock assertion and lock deassertion due to setting a new FLL output frequency.

D. Zero Delta — `FLL_zerodelta`

The `FLL_zerodelta` accomplishes two tasks:
1) Delay the DCO enable signal with respect to the retention signal going low (i.e., switching to active operation), such that the ring-oscillator starts up in a known state.
2) Delay the integrator update after changing the operating mode from stand-alone to normal mode or after deasserting the retention signal. The delay avoids that incorrect period quantizer values are considered for the loop update. The period quantizer will produce invalid measurements immediately after wake-up from sleep mode, or when changing from stand-alone mode to normal mode after the setpoint has been changed. The delay is achieved by forcing the error signal in the loop filter unit to zero for a few reference clock cycles (three cycles in the current implementation).

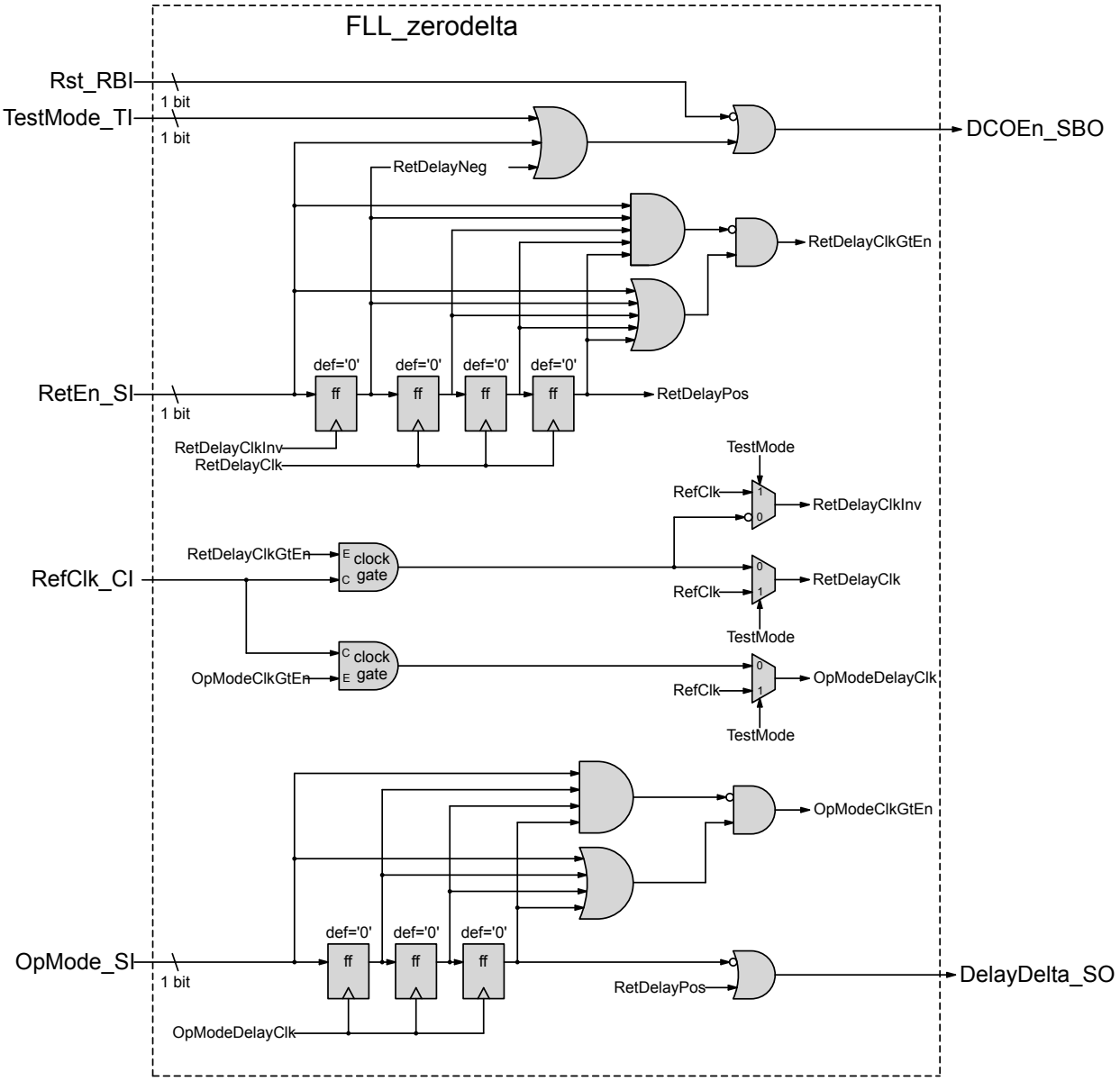

Fig. 9: Block diagram of the Zero_Delta unit.

X. Analog Section

A. DCO Transfer Function

Figure **??** shows the frequency transfer function of the DCO. The frequency transfer function under typical conditions (i.e., TT, 25C, 0.8V) for low input codes $x \in \{87, 386\}$ can be approximated by the third order fit given by

$$f_{DCO} = 107.683 - 2.526 \cdot x + 0.016899 \cdot x^2 - 0.000014555 \cdot x^3 \quad [\text{MHz}].$$

The frequency transfer function under typical conditions (i.e., TT, 25C, 0.8V) for input codes $x \in \{387, 1023\}$ can be approximated by the second order fit given by

$$f_{DCO} = -1210.565 - 6.962 \cdot x - 0.001157 \cdot x^2 \quad [\text{MHz}].$$