AEC FPGA Project

Revision: *1.10*

Date: *27 Mar 2021*

QuickLogic Corporation

1 Requirement:

2 Pinout:

Sl. No.	Signal Name	PAD Number	Direction	Description
FLL				
1	I2S_bitclk_in		Input	

3 FPGA Interrupts:

Sl. No.	FPGA Interrupts to M4	Interrupt Description
1	FB_INTERRUPT_0	Local clock slow down
2	FB_INTERRUPT_1	Local clock speed up
3	FB_INTERRUPT_2	I2S Interrupt
4	FB_INTERRUPT_3	Reserved

Note: The I2S Interrupt is a combination of the following interrupts, logically OR'ed together:

- I2S Disconnected Interrupt
- I2S DMA Done Interrupt
- I2S Decimation Done Interrupt
- I2S Decimation DMA Start Interrupt
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To determine the source of an I2S Interrupt, firmware must inspect the I2S Slave RX register module's Interrupt Status register. Refer to the I2S Slave RX Register document in QuickLogic's s3-gateware repository, under the /ip_modules/I2S_slave_rx/ directory. The individual interrupts that may trigger an I2S Interrupt as described above may be individually enabled via the register at offset 0x100C in the I2S Slave RX IP module (offset 0x100C from the FPGA's address offset + the I2S Slave RX module's offset). Likewise, the status of the individual interrupts may be seen in the register at offset 0x1008 in the I2S Slave RX IP module (offset 0x1008 from the FPGA's address offset + the I2S Slave RX module's offset).

The source of each interrupt may also be cleared by writing to the interrupt status register as described in the I2S Slave RX Register Document. Further details are listed below:

- I2S Disconnected Interrupt
    - Enabled via Interrupt Enable Register (0x100C), bit 3
    - Status/Clear via Interrupt Status Register (0x1008), bit 3
- I2S DMA Done Interrupt
    - Enabled via Interrupt Enable Register (0x100C), bit 0
    - Status/Clear via Interrupt Status Register (0x1008), bit 0
- I2S Decimation Done Interrupt
    - Enabled via Interrupt Enable Register (0x100C), bit 2
    - Status/Clear via Interrupt Status Register (0x1008), bit 2
- I2S Decimation DMA Start Interrupt
    - Active when the Decimation RX FIFO level (viewable at offset 0x1010) is greater than or equal to the DMA Count Register (0x1028). Note that unlike the other interrupts listed above, this interrupt does not have an enable/status bit.

4 FPGA Clocks

The FPGA clock C16 should be set to 6MHz (1024*6000). The FPGA clock C21 should be set to 3MHz (1024*3000). The 6MHz clock is used by the decimation filter, and the 3MHz clock is used as the local I2S bit clock.

5 Address Map Specification

5.1 Memory Map

The EOS 3B system maps the FPGA IP into the address range of 0x40020000 to 0x4003FFFF. This address range provides 128K bytes of address range for FPGA based IP. The following tables further define the registers within this range.

Table 1-1: FPGA IP Register Space

Register	Block	Space Allocated	Remarks
0x40020000 – 0x400200FF	FPGA IP Registers	256 bytes	
0x40020100 – 0x40020FFF	Reserved		
0x40021000 – 0x40021FFF	FLL_I2S	4096 bytes	
0x40022000 – 0x40023FFF	I2S Slave RX (includes pre-decimator RAM) ~~(includes decimator)~~	8192 bytes	
0x40024000 – 0x40025FFF	Decimator (includes coefficient RAM)	8192 bytes	
0x40026000 – 0x4003FFFF	Reserved		

5.2 Register Address Table

The following sections will outline the expected allocation of registers and describe their operations.

5.2.1 FPGA Registers Address Table

Table 1-2 shows the expected allocation of FPGA Registers address space.

Table 1-2: FPGA IP Register Table

Register	Block	Reset Value	Remarks
0x40020000	IP Device ID	0xABCD0200	Read only
0x40020004	IP Revision number	0x0100	Read only Version
0x40020008 – 0x400200FF	Not Used	0x0	Reserved.

5.2.2 FLL_I2S Register Map

The FLL_I2S module has a base address that starts at offset 0x1000 from the FPGA's base address (0x40020000 + 0x1000). The register map for the FLL_I2S Controller is described in a separate document, and can be found along with the RTL source code for the FLL_I2S module (currently in QuickLogic's s3-gateware repository on github, under ip_modules).

5.2.3 I2S RAM and I2S Slave Register Map

The I2S RX Slave module has a base address that starts at offset 0x2000 from the FPGA's base address (0x40020000 + 0x2000). The register map for the I2S Slave Controller is described in a separate document, and can be found along with the RTL source code for the I2S Slave module (currently in QuickLogic's s3-gateware repository on github, under ip_modules).

5.2.4 Decimator and Decimator Coefficient RAM Register Map

The Decimator 3to1 module has a base address that starts at offset 0x4000 from the FPGA's base address (0x40020000 + 0x4000). The register map for the Decimator is described in a separate document, and can be found along with the RTL source code for the Decimator 3to1 module (currently in QuickLogic's s3-gateware repository on github, under ip_modules).

6 Revision History

Date	Revision	Author	Description
21 Jan 2021	1.00	Randy O.	Initial Release
16 Feb 2021	1.01	Randy O.	Added clock requirements. Re-arranged some of the module offsets to be more clear. Removed information that can be found in the I2S slave IP module register document since it can be confusing to include that information in this document.
27 Mar 2021	1.10	Randy O.	Separated the I2S RX + Decimator IP module into 2 modules (I2S RX, and Decimator).

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QuickLogic Corporation

2220 Lunday Ave.

San Jose CA. 95131, USA