I2S Slave RX FPGA IP

Revision: *1.10*

Date: *25 Mar 2021*

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1 Theory of Operation

This I2S slave IP connects to I2S Master in the AP. This I2S slave IP works only in receive mode. The data received by the I2S slave is transferred to the M4 SRAM by the SDMA block.

There is an additional FIR decimator block which is also included in the path. The FIR decimator factor is 3. I2S data sampled at 48khz is down sampled to 16khz.

2 Features

- ➢ The I2S Slave IP is based on the Philips I2S serial protocol
- ➢ Supports 16-bit data width I2S data.
- ➢ Supports Sampling rate of 48KHz.
- ➢ Slave in RX mode only supported
- ➢ Decimation 48Khz to 16Khz is supported for Left channel only.
- ➢ Supports DMA

3 Dependency

The C16 clock frequency should be set to 6Mhz (1024 * 6000). This is used by the Decimator.

C21 should be set to 3MHz (1024 * 3000). This is used as the local I2S bit clock.

4 I2S Interface

4.1 Overview

The bus consists of a serial data line (sd), a word select line (ws), and a serial clock (sclk). The serial data line is time multiplexed to allow the transfer of two data streams (such as, left and right stereo data). I2S slave (Rx Mode) configuration:
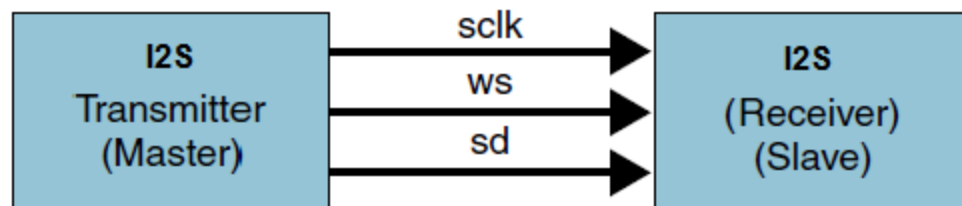

Figure 3-1: I2S slave Rx mode

4.2 I/O signals

i2s_sclk: Interface clock

i2s_ws : Word Select Line

i2s_din: Data In

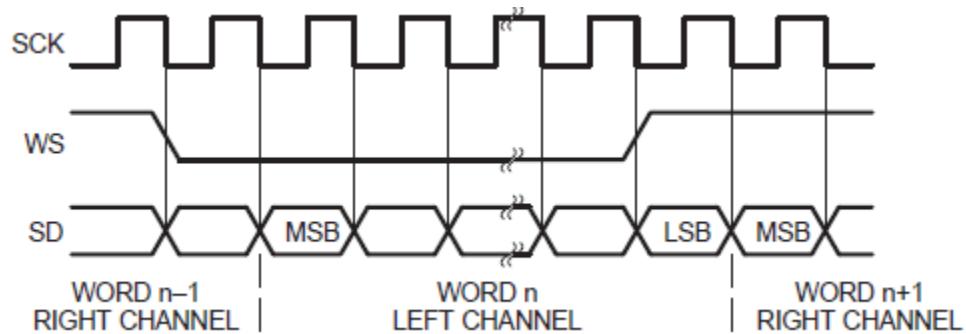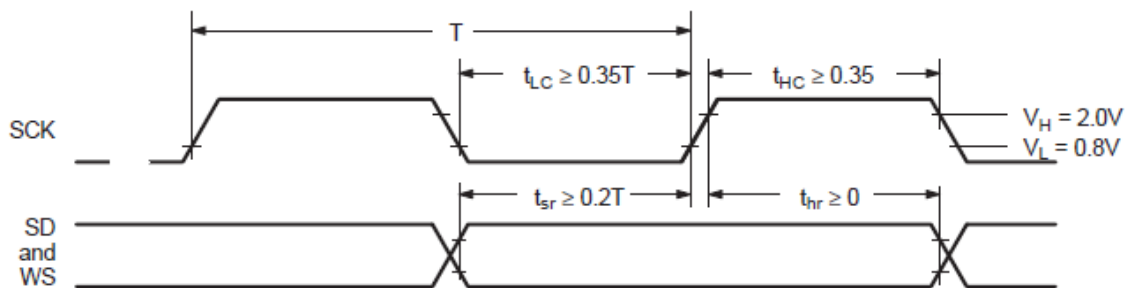## 1.1 I2S Timing Diagrams

Figure 3-2: Basic Interface Timing

T   =   clock period
T_r =   minimum allowed clock period for transmitter
T   > T_r

Figure 3-3: Timing for I2S receiver

5 I2S Slave IP block diagram:
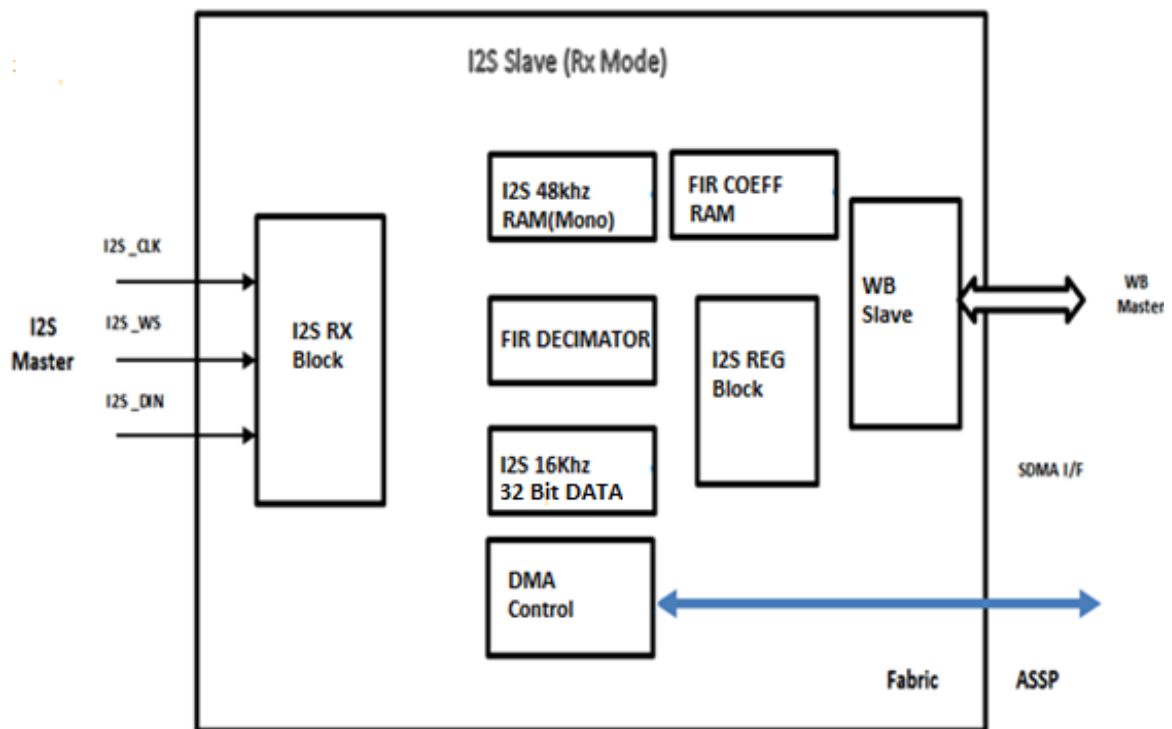
Figure 4-1: I2S Slave IP Block Diagram

o Block description

4.2.1 I2S Rx Block:

The audio data Mono is received serially from a data input line. The receiving is timed with respect to the serial clock (sclk) and the word select line (ws). The serial data is latched into the receiver on the leading edge of the serial clock signal.

4.2.2 RAM Block

The IP utilizes 2 RAM blocks for Storing I2S 48khz data and FIR Coefficients. Each of these RAM blocks are 512x16 in size.

4.2.2.1 I2S 48khz RAM(Mono)

The I2S data sampled at 48Khz is written to this block by the I2S Rx Block. This RAM is read accessible by the FIR filter only. This RAM block may be cleared via the Wishbone interface (writing any data to a RAM location will result in a write of all 0's to that RAM location).

The FIR decimation filter if enabled will read from the pre-decimation RAM and perform decimation.

4.2.2.2 FIR Coefficient RAM

This RAM stores the pre-calculated FIR coefficients. The FIR coefficients are calculated in matlab.

Following equation is used for calculating coefficients for 121 Tap FIR filter.

b1 = fir1(120, 0.90/3, kaiser(121, 6.3));

*b2 = round(b1*32768);*

The M4 should write the coefficient values in the FIR Coefficient RAM during the initialization phase. Since the RAM is 512x16 in size, only the lower 16 bits of each 32-bit write from the Wishbone interface will be written to the Coefficient RAM. The coefficients need not be modified thereafter.

4.2.3 I2S slave register block:

This block supports the I2S slave register and the DMA registers. Details provided in the Address Map specification section.

FIR decimator registers are part of this register map.

4.2.4   FIR Decimation block:

This block has 121 tap coefficient FIR filter with built-in decimator. The decimator decimates by a factor of 3. Input data which is sampled at 48khz is down sampled to 16khz. FIR decimation filter utilizes RAM as a delay element and operates at a rate of ~5Mhz by doing fast access per sample.

The coefficient RAM is initialized by host. The filter uses coefficient RAM for calculating the final decimated sample value.

When I2S clock stops and there are no I2S data writes to RAM, FIR decimator detects this condition and uses Zero data for calculating decimated sample values. After FIR decimator has pushed all zeroes in the virtual delay elements and I2S writes have stopped then FIR decimator stops its operation, decimation enable bit is cleared and an interrupt is generated.

When host receives decimation done interrupt it needs to clear the I2S 48khz RAM buffer by writing 0x0, 16-bit data to this RAM.

4.2.5   DMA control block:

This block generates the DMA Request to the SDMA block when there is 1 Word of DMA data is available in the decimation RAM. DMA complete is indicated by DMA done signal from Assp. Once the DMA done is received then DMA done interrupt is generated to the M4.

4.2.6   Wishbone Slave Interface:

This block is a communication bridge between M4 and fabric design.

Address Map Specification

4.3 Memory Map

The EOS 3B system maps the FPGA IP into the address range of 0x40020000 to 0x4003FFFF. This address range provides 128K bytes of address range for FPGA based IP. Each instantiation of this I2S Slave Rx IP module should be allocated a base address within the FPGA's address space. The register offsets described in this document are all relative to the I2S_slave_rx IP's base address that you have chosen for your design. The I2S_slave_rx IP module currently uses 4096 bytes of address space, although this address space may not be fully utilized.

Table 5-1: Fabric IP Register Space

Register	Block	Space Allocated	Remarks
0x0000 – 0x07FF	I2S Pre decimator RAM		
0x1000 – 0x1FFF	I2S Slave IP+Decimator		
0x2000 – 0x2FFF	FIR coefficient RAM		

4.4 I2S Slave Register Address Table

Error! Reference source not found. The table below shows the expected allocation of I2S Slave Register address space.

Table 5-2: I2S Slave Register Table

Register	Register Name	Reset Value	Description
0x0000– 0x07FF	FI2SRAM	0x0	FIR I2S 48Khz. Pre-decimation I2S data.
0x1000	IER	0x0	I2S Enable Register
0x1004	ACSLIPR [DEPRICATED]	0x0	ACSLIP Reset Register
0x1008	ISR	0x0	Interrupt Status Register

Register	Register Name	Reset Value	Description
0x100C	IEN	0x0	Interrupt Enable Register
0x1010	DFSTS	0x0	Decimation FIFO Status Register
0x1014	DFDREG	0x0	Decimation Data Register 16 bit
0x1018	ACSLIP [DEPRICATED]	0x0	ACSLIP Register
0x101C	DFRST	0x0	Decimation FIFO reset.
0x1020	DER	0x0	DMA Enable Register
0x1024	DSR	0x0	DMA Status Register
0x1028	DCNT	0x2	DMA Count Register
0x102C	ACSLTMR [DEPRICATED]	0xF	ACSLIP Timer Register.
0x1030	FDCR	0x0	FIR Decimation control.
0x1034	FDSR	0x0	FIR Decimator Status Register
0x1038	Reserved	0x0	Reserved
0x103C–0x13FF	Reserved	0x0	Reserved
0x2000–0x2FFF	FCRAM	0x0	FIR decimator coefficient RAM.

4.5   I2S Slave Register Description:

4.5.1   FIR I2S 48Khz RAM(0x0000-0x07FF)

Register Address location: 0x0000-0x07FF

Reset Value: 0x0

Table 5-12: FIR decimation RAM

Name	Bit(s)	Type	Description
Reserved	[31:16]	R	Returns 0
RAW I2S 48Khz Data(Non-Decimated)	[15:0]	R	Lower 16 bits of the Decimation RAM. NOTE: This RAM does not appear to be readable from the Wishbone interface.

4.5.2 I2S Enable Register(0x1000)

Register Address location: 0x1000

Reset Value: 0x00

Table 5-3: I2S Enable Register

Name	Bit(s)	Type	Description
Reserved	[31:4]	R	Returns 0
COERAMRD_AC	3	R/W	Setting this bit to 1 enables the read access to Coefficient Ram from Wb interface cutting off the FIR decimator read access. Added for initial Software debug. Needs to be set to 0 after reading the RAM for FIR decimation.
ACSLIP_ena [DEPRICATED]	2	R/W	Write 1 for enabling the ACSLIP register counter.
I2S_48khz_write_access	1	R/W	Write 1 to get write access to 48khz RAM. Firmware needs to clear this bit after initializing the RAM to all zeros.
I2S Enable	0	R/W	0 - Disable I2S Slave 1 - Enable I2S Slave

4.5.3 ACSLIP Reset Register(0x1004)

Register Address location: 0x1004

Reset Value: 0x00

Table 5-4: RX FIFO Reset Register

Name	Bit(s)	Type	Description
Reserved	[31:1]	R	Returns 0
ACSLIP reset [DEPRICATED]	0	R/W	1 – ACSLIP Register is reset. Software needs to clear this bit to 0. Default value is 1.

4.5.4 Interrupt Status Register(0x1008)

Register Address location: 0x1008

Reset Value: 0x00

Table 5-5: Interrupt Status Register

Name	Bit(s)	Type	Description
Reserved	[31:6]	R	Returns 0
I2S_CON_INT	5	R/W	I2S Clock started (I2S Connected) FW needs to clear the interrupts, write 0 to clear.
ACSLIP_INT [DEPRICATED]	4	R/W	ACSLIP interrupt. FW needs to clear the interrupt, write 0 to clear
I2S_DIS_INT	3	R/W	I2S Clock stopped (I2S Disconnected) FW needs to clear the interrupt, write 0 to clear
DES_CMPL	2	RO	Decimation Complete. FW needs to clear the interrupt, write 0 to clear
DES_DAT_AVL	1	RO	Data Available in the Decimation Rx FIFO. For each 16bit data availability an interrupt is generated.
DMA_DONE_INT	0	R/W	DMA complete interrupt FW needs to clear the interrupt, write 0 to clear

4.5.5 Interrupt Enable Register(0x100C)

Register Address location: 0x100C

Reset Value: 0x00

Table 5-6: Interrupt Enable Register

Name	Bit(s)	Type	Description
Reserved	[31:6]	R	Returns 0
I2S_CON_INT_EN	5	R/W	I2S Clock started interrupt Enable 0 – disable 1 - enable
ACSLIP_INT_EN [DEPRICATED]	4	R/W	ACSLIP timer interrupt Enable 0 – disable 1 – enable
I2S_DIS_INT_EN	3	R/W	I2S Clock stopped interrupt Enable 0 – disable 1 – enable
DEC_D_AVL_INT_EN	2	R/W	Decimation data available. 0 – disable 1 – enable
DEC_DN_INT_EN	1	R/W	Decimation Done interrupt. 0 – disable 1 – enable
DMA_DONE_INT_EN	0	R/W	Dma done interrupt. 0 – disable 1 – enable

4.5.6　Decimation Rx FIFO Status Register(0x1010)

Register Address location: 0x1010

Reset Value: 0x00000000

Table 5-8: Decimation Rx Fifo Status register

Name	Bit(s)	Type	Description
DFSTS	[31:18]	R	Decimation fifo status register
DRxFIFOFUL	[17]	R	Decimation Rx FIFO Full.
DRxFIFOEMP	[16]	R	Decimation Rx FIFO empty.
DRxFIFOLVL	[15:0]	R	Decimation Rx FIFO level.

4.5.7　Decimation Rx FIFO Data Register(0x1014)

Register Address location: 0x1014

Reset Value: 0x00000000

Table 5-8: Decimation Rx Fifo Data register

Name	Bit(s)	Type	Description
DFDREG	[31:16]	R	Decimation Odd Data
	[15:0]	R	Decimation Even Data

4.5.8　ACSLIP Register(0x1018) [DEPRICATED]

Register Address location: 0x1018

Reset Value: 0x00000000

This counter counts in positive direction for I2S Clock and count in negative direction for Mic clock.

Table 5-8: ACSLIP register

Name	Bit(s)	Type	Description
ACSLIP [DEPRICATED]	[31:0]	R	ACSLIP register

4.5.9 Decimation Fifo Reset(0x101C)

Register Address location: 0x101C

Reset Value: 0x0

Table 5-12: Reserved

Name	Bit(s)	Type	Description
DFRST	[31:0]	W	Write 0x1 to reset the FIFO. This bit is auto clear.

4.5.10 DMA Enable Register(0x1020)

Register Address location: 0x1020

Reset Value: 0x0

Table 5-11: DMA Enable Register

Name	Bit(s)	Type	Description
Reserved	[31:1]	R	Returns 0
DMA_EN	0	R/W	0 – Disable 1 – Enable HW clears this bit when the DMA transfer is done

4.5.11 DMA Status Register(0x1024)

Register Address location: 0x1024

Reset Value: 0x0

Table 5-12: DMA Status Register

Name	Bit(s)	Type	Description
Reserved	[31:1]	R	Returns 0
DMA_REQ	0	R	Fabric IP generates the DMA Request to the SDMA block
DMA_ACTIVE	0	R	DMA Active signal from the SDMA block
DMA_DONE	0	R	1 – DMA is completed
DMA_Busy	0	R	0 – DMA not in progress 1 – DMA in progress

4.5.12 DMA Count Register(0x1028)

Register Address location: 0x1028

Reset Value: 0x4

Table 5-13: DMA Count Register

Name	Bit(s)	Type	Description
Reserved	[31:9]	R	Returns 0
DMA_CNT	[8:0]	R/W	DMA count register (in 16-bit word length) Reset value: 0x2 (Two 16 Bit Data) FW need to write the DMA count while setting up the SDMA register. This register gives the DMA count in 16 bit word.

4.5.13 ACSLIP Timer(0x102C) [DEPRICATED]

Register Address location: 0x102C

Reset Value: 0x0

Table 5-12: Reserved

Name	Bit(s)	Type	Description
Reserved	[31:16]	R	Returns 0
ACSLIP_INT_TIMER [DEPRICATED]	[15:0]	R/W	Divisor value for internal 16 Khz clock(). This will act as a reference for generation of ACSLIP interrupt. Default values is 0x1DF (30 ms Timer interrupt) .

4.5.14 FIR Decimation Control Register(0x1030)

Register Address location: 0x1030

Reset Value: 0x0

Table 5-11: FIR decimation control Register

Name	Bit(s)	Type	Description
Reserved	[31:1]	R	Returns 0
FIR_DECI_INT_EN	1	W	0 – Disable 1 – Enable
FIR_DECI_EN	0	R/W	0 – Disable 1 – Enable Enable FIR decimation. Cleared by the Hardware automatically at the end of Decimation cycle.

4.5.15 Reserved (0x1034)

Register Address location: 0x1034

Reset Value: 0x0

Table 5-11: FIR decimation Status Register

Name	Bit(s)	Type	Description
Reserved	[31:0]	R	Returns 0

4.5.16 Reserved(0x1038)

Register Address location: 0x1038

Reset Value: 0x0

Table 5-12: Reserved

Name	Bit(s)	Type	Description
Reserved	[31:0]	R	Reserved

4.5.17 Reserved(0x103C-0x13FF)

Register Address location: 0x103C-0x13FF

Reset Value: 0x0

Table 5-12: Reserved

Name	Bit(s)	Type	Description
Reserved	[31:0]	R	Reserved

4.5.18 FIR COEFF RAM(0x2000-0x27FF)

Register Address location: 0x2000-0x27FF

Reset Value: 0x0

Table 5-12: FIR Coefficient RAM

Name	Bit(s)	Type	Description
Reserved	[31:16]	R/W	Unused
FIR coefficient Data	[15:0]	W	Lower 16 bits of the coefficient RAM.

5   Programming Sequence:

5.1.1   Decimation Data Read sequence

a. AP interrupts S3B (M4) through the SW interrupt register indicating I2S master is ready to send data.

b. M4 runs the ISR routine to set up the I2S slave to receive the Audio data

1. Power on the fabric block if it is in power down mode

2. Enable and setup the fabric clocks (C16 = 5Mhz and C21)

3. Set up the SDMA to DMA the data from the fabric FIR decimation Buffer Port to the M4 SRAM

    - Source address from the fabric DFDREG (0x1014).
    - DREQ will be generated for each 32 bit Decimation data available, the DMA count register(DCNT 0x1028) is set to default value of 0x1 which indicates availability of one 32 bit data. The register can be set to higher count values as well to do burst transfers of 32 bit data.

    - Destination address, M4SRAM location allocated for Audio buffer incremented on every 32-bit data received

    - SDMA channel dedicated for this I2S slave path is Channel 12

4. Enable the fabric interrupt in the NVIC

5. Enable the I2S DMA done fabric interrupt in the interrupt controller

- I2S DMA done interrupt done is tied on the fb_intr[2]

- Set up FB_INTR_TYPE, its level interrupt (0x40004888 = 0x0)

- Set up FB_INTR_POL, its high polarity (0x4000488C = 0x4)

- Set up FB_INTR_EN_M4, interrupt enable to M4 (0x40004894 = 0x4)

6. Set up the fabric register to receive the Decimated data

- Set up the DMA count, write DMA_CNT (in 16- bit words) to DMA count register (0x1028). The count register is by default set to 2. Since DMA request is generated for two 16 bit data packed in 32 bit.

- Clear the DMA done intr (if any) write 0 to bit[0] of the interrupt status register (0x1008)

- Enable DMA done interrupt, bit[0] = 1 of the interrupt enable register (0x100C)

- Enable the DMA, write 0x1 to 0x1020, HW clears this bit when the DMA transfer is done

  - Enable Write access to FIR I2S 48khz RAM. Write 0x1000 = 0x2
  - Clear the RAM. Write (0x0800-0x0FFF) =0x0. (This process of zero data initialization of the I2S 48khz RAM needs to be done after the decimation process is completed)
  - Initialize the FIR COEFF RAM memory(0x2000-0x2FFF)= 121 Tap pre-calculated coefficient data. After writing meaningful 121, 32 bit data(lower 16 bit valid), write 0s.

- Enable the FIR decimator and interrupt:
  - Write 0x1030 = 0x3

- Enable the FB I2S slave:
  - Write 0x1000 = 0x1(Here the wishbone write access to I2S RAM is also released so that I2S block can write data to this RAM).

c. Now I2S slave in the fabric is ready to receive the I2S data

d. Interrupt AP, indicating S3 device is ready to receive the I2S data and I2S master in the AP can start transmitting the Audio data

e. FB I2S Slave receives the I2S Audio data and stores in the FIR I2S 48khz RAM . FIR decimator reads this Data and uses coefficient RAM data to calculate the decimated Samples. When two 16 bit sample value are available then fabric generates DMA_REQ to the SDMA indicating SDMA to start the DMA transfer.

f. SDMA starts DMA transfer of audio data from the Decimation Rx FIFO data to M4 SRAM. Dreqs are generated based on the threshold set in DCNT(0x1028)

g. Once the DMA transfer is completed, fabric generates DMA done interrupt to M4 indicating that DMA transfer is complete and M4 can process the received data.

h. M4 runs the ISR routine to process the DMA done interrupt, M4 clears the DMA done interrupt by writing 0 to bit [0] of the interrupt status register (0x1008)

i. M4 sets up the next DMA transfer by configuring the SDMA engine

j. M4 enables the DMA by writing 0x1 to 0x1020

k. Fabric will generate the DMA_Req again when it has data in FIR decimation data reg.

l. The process repeats till the AP indicates to M4 to disable the I2S slave in the fabric.

m. At the end of Decimation (When no I2S data is available), Fabric generates FIR decimation Done interrupt. This bit is indicated in FIR decimation status register. After receiving this interrupt the Host needs to disable I2S enable & get write access to I2S 48khz RAM and initialize the RAM to zero. The write access bit after clearing needs to be set to 0.

n. The host can then re enable the entire flow by

    a. Write 0x1030 = 0x3.
    b. Write 0x1000 = 0x1 (Clear I2S 48khz RAM before each Decimation run).

6 Revision History

Date	Revision	Author	Description
27 Jan 2021	1.00	Randy O	Initial Release
10 Mar 2021	1.01	Randy O	Corrected the required clock freq's for C16 and C21. Re-arranged some of the RAM descriptions to be less confusing, and added some RAM size information.
25 Mar 2021	1.10	Randy O	Separated the I2S receiver and Decimation Filter into separate IP modules.

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