FLL_I2S FPGA IP

Revision: *1.00*

Date: *03 Nov 2020*

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1 Theory of Operation

The FLL_I2S IP module is a simple Frequency-Locked Loop controller. It can be used to detect frequency differences between a local clock (slave) and an external clock (master). Based on the frequency difference, if any, the FLL_I2S IP module will generate interrupts to the M4 processor in the S3 device so that the local clock speed can be adjusted. This enables the S3 device to be used as an I2S slave, and synchronize its local (slave) clock to the external (master) clock.

Note that the S3's high-speed internal oscillator will be locked to its own local 32.768KHz oscillator. Therefore, it cannot be locked to an external I2S master's clock. However, the local high-speed clock can be digitally controlled, manually, by software running in the S3 device. By using interrupts coming from this FLL_I2S IP module, the M4 software can adjust its own local clock to match an external clock source.

This IP module contains a few control registers. There is a Control register that can be activated to turn on the FLL. There is a Sample Time register that can be used to control the length of time (in local clock periods) over which the clock speed measurements are made. There is also a Gap Timer that can be used to control the length of time (in local clock periods) between each sample.

Once enabled, the FLL will count down from the Sample Time register value, to zero, in the local clock domain. Simultaneously it will count down from the Sample Time register value in the external (master) clock domain. Once the sample period is over, the count value in the external (master) clock domain will indicate whether the external clock domain is faster, slower, or the same as the local clock. The Gap counter will then count down from the Gap Timer value, to zero. Once the Gap counter reaches zero, another sample will be initiated, and the process will repeat until the FLL is disabled.

Simultaneous to the above, an I2S word count will be maintained in both the local and external clock domains. The I2S Word Size is a parameter in the IP module (default value = 64), which can be over-ridden if needed when the module is instantiated. Depending on the relative clock speeds, the word counts in each clock domain may be the same, or different, over time. The FLL control logic will compare the word counts between the two clock domains, as well as the relative clock speeds as shown by the Sample Counters described in the previous paragraph, and determine if it needs to generate a "speed up" interrupt, a "slow down" interrupt, or neither. Therefore, the FLL will try to maintain the same word count in each clock domain while also matching the local clock frequency to the external clock frequency.

2 Address Map Specification

2.1 Memory Map

The EOS 3B system maps the FPGA IP into the address range of 0x40020000 to 0x4003FFFF. This address range provides 128K bytes of address range for FPGA based IP. Each instantiation of this FLL_I2S IP module should be allocated a base address within the FPGA's address space. The register offsets described in this document are all relative to the FLL_I2S IP's base address that you have chosen for your design. The

FLL_I2S IP module currently uses 256 bytes of address space, although this address space may not be fully utilized.

2.1.1 FLL_I2S Address Table

Table 1 shows the allocation of the FLL_I2S module's address space.

Table 1: FLL_I2S Register Table

Register	Register Name	Reset Value	Description
0x00	Control Register	0x0	Enable bit to turn on the FLL.
0x04	Sample Time	0x0400	Number of local clock periods per sample.
0x08	Gap Timer	0x0400	Number of local clock periods between samples.
0x0C – 0xFF	Reserved	0x0	

2.2 Description of Registers

The following sections will detail the registers for the FLL_I2S IP module.

2.2.1 Conventions

Access Tag	Name	Meaning
R	Read	field may be read by the user/sw
W	Write	field may be written by the user/sw
U	Update	field may be updated by hardware
S	Set	field may be set by the user
C	Clear	field may be cleared by the user
RO	Read Only	field can only be read by the user/sw

2.2.2 FLL_I2S Registers

2.2.2.1 [0x00] Control Register

Bit 0 of this register allows the FLL to operate. Other bits are reserved.

Table 2: Control Register

Name	Bit(s)	Type	Description
CONTROL[0]	[0]	R/W	FLL Enable. 1=enabled, 0=disabled. Reset value = 0.
CONTROL[31:1]	[31:1]	R	Reserved.

2.2.2.2 [0x04] Sample Time

This register specifies the length of time, in local clock periods, per sample. During the sample time, the number of clocks in the external clock domain will be counted to determine if the two clock domains are frequency locked, or not.

Table 3: Sample Time

Name	Bit(s)	Type	Description
SAMPLE_TIME[31:0]	[31:0]	R/W	Sample Time, specified in local clock periods. Reset value = 0x0400.

2.2.2.3 [0x08] Gap Timer

This register specifies the length of time, in local clock periods, between samples.

Table 4: Gap Timer

Name	Bit(s)	Type	Description
GAP_TIMER[31:0]	[31:0]	R/W	Gap Timer, specified in local clock periods. Reset value = 0x0400.

3 Revision History

Date	Revision	Author	Description
03 Nov 2020	1.00	Randy O	Initial Release

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