UART FPGA IP

Revision: *1.01*

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1 Requirement:

2 Pinout:

Sl. No.	Signal Name	PAD Number	Direction	Description
UART				
4	UART_TX		Output	
5	UART_RX		Input	

3 FPGA Interrupts:

Sl. No.	FPGA Interrupts to M4	Interrupt Description
1	FB_INTERRUPT_0	Reserved
2	FB_INTERRUPT_1	Reserved
3	FB_INTERRUPT_2	UART 0 INTR
4	FB_INTERRUPT_3	Reserved

4 Address Map Specification

4.1 Memory Map

The EOS 3B system maps the FPGA IP into the address range of 0x40020000 to 0x4003FFFF. This address range provides 128K bytes of address range for FPGA based IP. The following tables further define the registers within this range.

Table 1-1: FPGA IP Register Space

Register	Block	Space Allocated	Remarks
0x40020000 – 0x400200FF	FPGA IP Registers	256 bytes	
0x40020100 – 0x40020FFF	Reserved	0x0	
0x40021000 – 0x400217FF	UART 0	512 Words	
0x40021800 – 0x4003FFFF	Reserved	0x0	

4.2 Register Address Table

The following sections will outline the expected allocation of registers and describe their operations.

4.2.1 FPGA Registers Address Table

Table 1-2 shows the expected allocation of FPGA Registers address space.

Table 1-2: FPGA IP Register Table

Register	Block	Reset Value	Remarks
0x40020000	IP Device ID	0xABCD0001	Read only
0x40020004	IP Revision number	0x0100	Read only Version
0x40020008 – 0x400200FF	Not Used	0x0	

4.2.2 UART 0 Address Table

Table 1-3 shows the expected allocation of UART Register address space. This selection reflects the goal of backward compatibility with the UART 16550 commonly used for serial communications.

Table 1-3: UART Register Table

Register	Register Name	Reset Value	Description
0x40021000	Receiver Buffer Register		Receive Data (Read Only) *Note: Divisor Latch Access Bit (DLAB) = "0"*
0x40021000	Transmit Buffer Register		Transmit Data (Write Only) *Note: Divisor Latch Access Bit (DLAB) = "0"*
0x40021000	Divisor Latch (LSB)		Reference Clock divisor's LSB *Note: Divisor Latch Access Bit (DLAB) = "1"*
0x40021004	Interrupt Enable Register		Enables various interrupt conditions. *Note: Divisor Latch Access Bit (DLAB) = "0"*
0x40021004	Divisor Latch (MSB)		Reference Clock divisor's MSB *Note: Divisor Latch Access Bit (DLAB) = "1"*
0x40021008	Interrupt Identification Register		(Read Only)
0x40021008	FIFO Control Register		(Write Only)
0x4002100C	Line Control Register		
0x40021010	Modem Control Register		
0x40021014	Line Status Register		
0x40021018	Modem Status Register		
0x4002101C	Scratch Register	0x00	
0x40021020 – 0x400217FF	Reserved	0x00	

4.3 Description of Registers

The following sections will detail the registers for each address space.

4.3.1 Conventions

Access Tag	Name	Meaning
R	Read	field may be read by the user/sw
W	Write	field may be written by the user/sw
U	Update	field may be updated by hardware
S	Set	field may be set by the user
C	Clear	field may be cleared by the user
RO	Read Only	field can only be read by the user/sw

4.3.2 FPGA IP Registers

4.3.2.1 IP Device ID register

Register Address location: 0x40020000

Reset Value: 0xABCD0001

Table 3-2.1: ID Value Register

Name	Bit(s)	Type	Description
IP Device ID	[31:0]	RO	0xABCD0001 : Read only

4.3.2.2 IP revision number register

Register Address location: 0x40020004

Reset Value: 0x0100

Table 3-2.2: Revision Number Register

Name	Bit(s)	Type	Description
Revision Number	[15: 0]	RW	0x0100 : Read only
Not Used	[31:16]	RO	Return “0” when read

4.3.3 UART Registers

4.3.3.1 Receive Buffer Register / Transmitter Holding Register

Data received by the UART's Rx logic may be read from this location. Data for transmission by the UART's Tx logic should be written to this location.

Note: These registers are only available if the "*Divisor Latch Access Bit*" (*DLAB*) of the Line Control Register (Ref. 0x4002100C) is set to "0".

Register Address location: 0x40021000

Reset Value: 0x00

Table 3-4.1: Receive Buffer/Transmission Holding Register

Name	Bit(s)	Type	Description
Receive Buffer	[7:0]	R	Receive Data from the Rx logic
Transmitter Holding	[7:0]	W	Data for transmission by the Tx logic.
Reserved	[31:8]	R	Returns "0"

4.3.3.2 Divisor Latch (LSB) Register

The Divisor Latch (LSB) register holds the lower byte of the reference clock divisor.

Note: These registers are only available if the "*Divisor Latch Access Bit*" (*DLAB*) of the Line Control Register (Ref. 0x4002100C) is set to "1".

Register Address location: 0x40021000

Reset Value: 0x00

Table 3-4.2: Divisor Latch (LSB) Register

Name	Bit(s)	Type	Description
Divisor Latch (LSB)	[7:0]	R/W	Reference Clock divisor LSB byte.
Reserved	[31:8]	R	Returns "0"

4.3.3.3 Interrupt Enable Register

This register enables/disables various interrupt conditions.

Note: These registers are only available if the "*Divisor Latch Access Bit*" (*DLAB*) of the Line Control Register (Ref. 0x4002100C) is set to "0".

Register Address location: 0x40021004

Reset Value: 0x00

Table 3-4.3: Interrupt Enable Register

Name	Bit(s)	Type	Description
Received Data	[0]	R/W	Enable Received Data Available Interrupt
Transmit Data	[1]	R/W	Enable Transmitter Holding Register Empty Interrupt
Receiver Line Status	[2]	R/W	Enable Receiver Line Status Interrupt
Modem Status	[3]	R/W	Enable Modem Status Interrupt
Reserved	[31:4]	R	Returns "0"

4.3.3.4 Divisor Latch (MSB) Register

The Divisor Latch (MSB) register holds the lower byte of the reference clock divisor.

Note: These registers are only available if the "*Divisor Latch Access Bit*" (*DLAB*) of the Line Control Register (Ref. 0x4002100C) is set to "1".

Register Address location: 0x40021004

Reset Value: 0x00

Table 3-4.4: Divisor Latch (MSB) Register

Name	Bit(s)	Type	Description
Divisor Latch (MSB)	[7:0]	R/W	Reference Clock divisor MSB byte.
Reserved	[31:8]	R	Returns "0"

4.3.3.5 Interrupt Identification Register

The Interrupt Identification register returns the status of various interrupt sources. More specifically, this register provides the user with four interrupt status bits. Performing a read cycle on the Interrupt Identification register will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. Whenever the interrupt status register is read, the interrupt status is cleared. However, it should be noted that only the currently pending interrupt is cleared by the read. A lower level interrupt may be seen after re-reading the interrupt status bits. Table shows the data values (bits [3:0] of the Interrupt Identification Register) for the four prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

Table 3-4.5: Interrupt Sources

Priority	Bit [3]	Bit [2]	Bit [1]	Bit [0]	Source of Interrupt
-	0	0	0	1	None
1	0	1	1	0	Receiver Line Status Register
2	0	1	0	0	Received Data Ready
2	1	1	0	0	Received Data Time-Out
3	0	0	1	0	Transmitter Holding Register Empty
4	0	0	0	0	Modem Status Register

Register Address location: 0x40021008

Reset Value: 0x00

Table 3-4.5a: Interrupt Identification Register

Name	Bit(s)	Type	Description
Interrupt Pending	[0]	R	“0” when an interrupt is pending (i.e. Bit[0] in Table)
Interrupt ID	[3:1]	R	Selects interrupt sources (i.e. Bit [3:1] in Table)
Reserved	[4]	R	Returns “0”
512 Byte FIFO Enabled	[5]	R	Enable Modem Status Interrupt
FIFOs Enabled	[7:6]	R	
Reserved	[31:8]	R	Returns “0”

4.3.3.6 FIFO Control Register

The FIFO Control register enables the FIFO operation of the UART.

Register Address location: 0x40021008

Reset Value: 0x00

Table 3-4.6: Interrupt Identification Register

Name	Bit(s)	Type	Description
FIFO Enable	[0]	W	Enables FIFO operations 0 – FIFOs Disabled 1 – FIFOs Enabled
Receive FIFO Reset	[1]	W	Selects interrupt sources
Transmit FIFO Reset	[2]	W	Returns “0”
DMA Mode Select	[3]	W	Enable the use of the Tx Ready and Rx Ready signals in conjunction with the each FIFO operation.
Reserved	[4]	W	
512 FIFO Enabled	[5]	W	Enables extended FIFO operation 0 – 16-Byte Mode 1 – 512 Byte Mode
Receive Trigger	[7:6]	W	Selects the FIFO level for trigging an interrupt Refer to Table.
Reserved	[31:8]	R	Returns “0”

Table 3-4.6a: RX FIFO Trigger Level Selection

FCR[7]	LCR[6]	RX FIFO Trigger Levels (Bytes)	
		16-Byte Operation	512-Byte Operation
0	0	1	1
0	1	4	128
1	0	8	256
1	1	14	496

4.3.3.7 Line Control Register

Register Address location: 0x4002100C

Reset Value: 0x00

Table3-4.7: Line Control Register

Name	Bit(s)	Type	Description
Word Length Select	[1:0]	R/W	Word Length

			These two bits specify the word length to be transmitted or received. (Refer to Table)
Number of Stop Bits	[2]	R/W	Stop Bit(s) The length of Stop bits is specified by this bit in conjunction with the word length. (Refer to Table)
Parity Enable	[3]	R/W	Parity Enable 0 – No Parity 1 – A parity bit is generated during the transmission, receiver checks the data and parity for transmission errors.
Even Parity Select	[4]	R/W	Even parity. If the parity bit is enabled with LCR[3] set to a logic 1, LCR[4] selects the even or odd parity format. (Refer to Table) 0 – Odd parity is generated by forcing an odd number of logic 1s in the transmitted data. The receiver must be programmed to check the same format (normal default condition). 1 – Even parity is generated by forcing an even number of logic 1s in the transmitted data. The receiver must be programmed to check the same format.
Stick Parity	[5]	R/W	Set parity. If the parity bit is enabled, LCR[5] selects the forced parity format. (Refer to Table) Programs the parity conditions as follows: 0 – parity is not forced (normal default condition) LCR[5] – logic 1 and LCR[4] = logic 0: parity bit is forced to a logic 1 for the transmit and receive data LCR[5] – logic 1 and LCR[4] = logic 1: parity bit is forced to a logic 0 for the transmit and receive data
Break Control	[6]	R/W	Set Break. When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR[6] to a logic 0. 0 – no TX break condition (normal default condition) 1 – forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition
Divisor Latch Access Bit	[7]	R/W	Divisor latch enable. The internal baud rate counter latch and Enhanced Feature mode enable. 0 – Divisor latch disabled (normal default condition) 1 – Divisor latch and enhanced feature register enabled
Reserved	[31:8]	R	Returns “0”

Table 3-4.7a: Parity Selection

LCR[5]	LCR[4]	LCR[3]	Parity Selection
X	X	0	No Parity
0	0	1	Odd Parity
0	1	1	Even Parity
1	0	1	Force Parity “1”
1	1	1	Force Parity “0”

Table 3-4.7b: Stop Bit Length

LCR[2]	Word Length (Bits)	Stop Bit Length (Bit Times)
0	5, 6, 7, 8	1
1	5	1 ½
1	6, 7, 8	2

Table 3-4.7c: Word Length

LCR[1]	LCR[0]	Word Length (Bits)
0	0	5
0	1	6
1	0	7
1	1	8

4.3.3.8 Modem Control Register

Register Address location: 0x40021010

Reset Value: 0x00

Table 3-4.8: Modem Control Register

Name	Bit(s)	Type	Description
Data Terminal Ready	[0]	R/W	DTRn 0 – Force DTR output to a logic 1 (normal default condition) 1 – Force DTR output to a logic 0
Request To Send	[1]	R/W	RTSn 0 – Force RTS output to a logic 1 (normal default condition) 1 – Force RTS output to a logic 0
Out[1]	[2]	R/W	OUTn [1]. This bit is used in the Loopback mode only. In the Loopback mode, this bit is used to write the state of the modem RIn interface signal via OUTn [1].
Out[2]	[3]	R/W	OUTn[2], INT enable. Used to control the modem DCD signal in the Loopback mode. 0 – Set OUTn[2] to HIGH. In the Loopback mode, sets OUTn[2] (DCDn) internally to a logic 1. 1 – Set OUTn[2] to LOW. In the Loopback mode, sets OUTn[2] (DCDn) internally to a logic 0.
Loop	[4]	R/W	Loopback. Enable the local Loopback mode (diagnostics). In this mode the transmitter output (ROUT) and the receiver input (RIN), CTSn, DSRn, DCDn, and RIn are disconnected from the UART's I/O pins. Internally the modem data and control pins are connected into a loopback data configuration. In this mode, the receiver and transmitter interrupts remain fully operational. The Modem Control Interrupts are also operational, but the interrupts' sources are switched to the lower four bits of the Modem Control. Interrupts continue to be controlled by the IER register. 0 – Disable Loopback mode (normal default condition) 1 – Enable local Loopback mode (diagnostics)
Flow Control Enable	[5]	R/W	AFE. This bit is the auto flow control enable. When this bit is set, the auto flow control is enabled. Refer to Table
Reserved	[31:6]	R	Returns "0"

Table 3-4.8a: Flow Control Configuration

MCR[5] (AFE)	MCR[1] (RTSn)	Flow Configuration
1	1	auto RTSn and CTSn enabled
1	0	auto CTSn only enabled
0	X	auto RTSn and CTSn disabled

4.3.3.9 Line Status Register

Register Address location: 0x40021014

Reset Value: 0x00

Table 3-4.9: Line Status Register

Name	Bit(s)	Type	Description
Data Ready	[0]	R/W	Receive data ready. 0 – no data in receive holding register or FIFO (normal default condition) 1 – data has been received and is saved in the receive holding register or FIFO
Overrun Error	[1]	R/W	Overrun error. 0 – No overrun error (normal default condition) 1 – Overrun error. A data overrun error occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case, the previous data in the shift register is overwritten. Note that under this condition, the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.
Parity Error	[2]	R/W	Parity error. 0 – No parity error (normal default condition) 1 – Parity error. The receive character does not have correct parity information and is suspect. In the FIFO mode, this error is associated with the character at the top of the FIFO.
Framing Error	[3]	R/W	Framing error. 0 – No framing error (normal default condition) 1 – Framing error. The receive character did not have a valid stop bit(s). In the FIFO mode, this error is associated with the character at the top of the FIFO.
Break Interrupt	[4]	R/W	Break interrupt. logic 0 – No break condition (normal default condition)

			logic 1 – Break Condition The receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO.
Transmitter Holding Register	[5]	R/W	THR empty. This bit is the Transmit Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to CPU when the THR interrupt enable is set. The THR bit is set to a logic 1 when a character is transferred from the transmit holding register into the transmitter shift register. The bit is reset to a logic 0 concurrently with the loading of the transmitter holding register by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.
Transmitter Empty	[6]	R/W	THR and TSR empty. This bit is the Transmit Empty indicator. This bit is set to a logic 1 whenever the transmit holding register and the transmit shift register are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode, this bit is set to logic 1 whenever the transmit FIFO and transmit shift register are both empty.
Error in Receiver FIFO.	[7]	R/W	FIFO data error. 0 – No error (normal default condition) 1 – FIFO Data Error At least one parity error, framing error or break indication is in the current FIFO data. This bit is cleared when LSR register is read.
Reserved	[31:8]	R	Returns “0”

4.3.3.10 Modem Status Register

Register Address location: 0x40021018

Reset Value: 0x00

Table 3-4.10: Modem Status Register

Name	Bit(s)	Type	Description
Delta Clear To Send	[0]	R/W	ΔCTSn logic 0 – no CTSn change (normal default condition) logic 1 – the CTSn input to the UART has changed state since the last time it was read. A modem Status Interrupt will be generated.
Delta Data Set Ready	[1]	R/W	ΔDSRn logic 0 – no DSRn change (normal default condition) logic 1 – the DSRn input to the UART has changed state

			since the last time it was read. A modem Status Interrupt will be generated.
Trailing Edge Ring Indicator	[2]	R/W	ΔRIn 0 – No RIn change (normal default condition) 1 – The RIn input to the UART has changed from a logic 0 to a logic 1. A modem Status Interrupt will be generated.
Delta Data Carrier Detect	[3]	R/W	ΔDCDn 0 – No DCDn change (normal default condition) 1 – The DCDn input to the UART has changed state since the last time it was read. A modem Status Interrupt will be generated.
Clear To Send	[4]	R/W	Clear To Send. CTS. CTSn functions as hardware flow control signal input if it is enabled via MCR[5]. Flow control (when enabled) allows starting and stopping the transmissions based on the external modem CTSn signal. A logic 1 at the CTSn pin will stop UART transmissions as soon as the current character has finished transmission. Normally, MSR[4] is the complement of the CTSn input. However, in the Loopback mode, this bit is equivalent to the RTSn bit in the MCR register.
Data Set Ready	[5]	R/W	Data Set Ready. DSR (active HIGH, logic 1). Normally, this bit is the complement of the DSRn input. In Loopback mode this bit is equivalent to the DTR bit in the MCR register.
Ring Indicator	[6]	R/W	Ring Indicator. RI (active HIGH, logic 1). Normally, this bit is the complement of the RIn input. In the Loopback mode, this bit is equivalent to the OUT [1] bit in the MCR register.
Data Carrier Detect	[7]	R/W	Data Carrier Detect. DCD (active HIGH, logic 1). Normally this bit is the complement of the DCDn input. In the Loopback mode this bit is equivalent to the OUT [2] bit in the MCR register.
Reserved	[31:8]	R	Returns “0”

5 Revision History

Date	Revision	Author	Description
17 Sep 2020	1.00	Randy O	Initial Release

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