Decimation Filter 3to1 FPGA IP

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1 Theory of Operation

This FIR Decimation Filter IP has a decimation factor of 3. For example, it can down sample 48KHz audio data to 16KHz. This IP module is currently meant to operate with the I2S Slave Rx IP module, but it can be used independently or with other IP modules, provided that the raw data is provided to this Decimation Filter in a similar fashion. Currently, the I2S Slave Rx module places raw audio data into a RAM block, which is then read from by this Filter module to perform the decimation. The down-sampled data, which is the output of this Filter module, is then written into a FIFO and DMA'd into system memory in the S3.

Previously, the I2S Slave Rx logic and the Decimation Filter logic were combined into one IP module. These two functions have now been separated into two separate IP modules. In order to help maintain compatibility with existing software, the register maps for both the I2S Slave Rx and the Decimation Filter have not been collapsed/condensed, and bitfields within registers have not been collapsed/condensed. Therefore, any registers/bitfields that are used by the I2S Slave Rx module have been marked as "reserved" in the register map for this IP module, and now only exist in the I2S Slave Rx IP module.

2 Features

- Supports 16-bit data width I2S data.
- Supports Sampling rate of 48KHz.
- Decimation 48Khz to 16Khz is supported for Left channel only.
- Supports DMA

3 Dependency

The C16 clock frequency should be set to 6Mhz (1024 * 6000) or higher. This is required so the Decimator can keep up with I2S receive data (assumed to be 48KHz, being received with an I2S bit clock rate of 3MHz).

4 I2S Slave Rx + Decimation Filter IP block diagram:

The following block diagram shows this Decimation Filter IP module in conjunction with the I2S Slave Rx module.

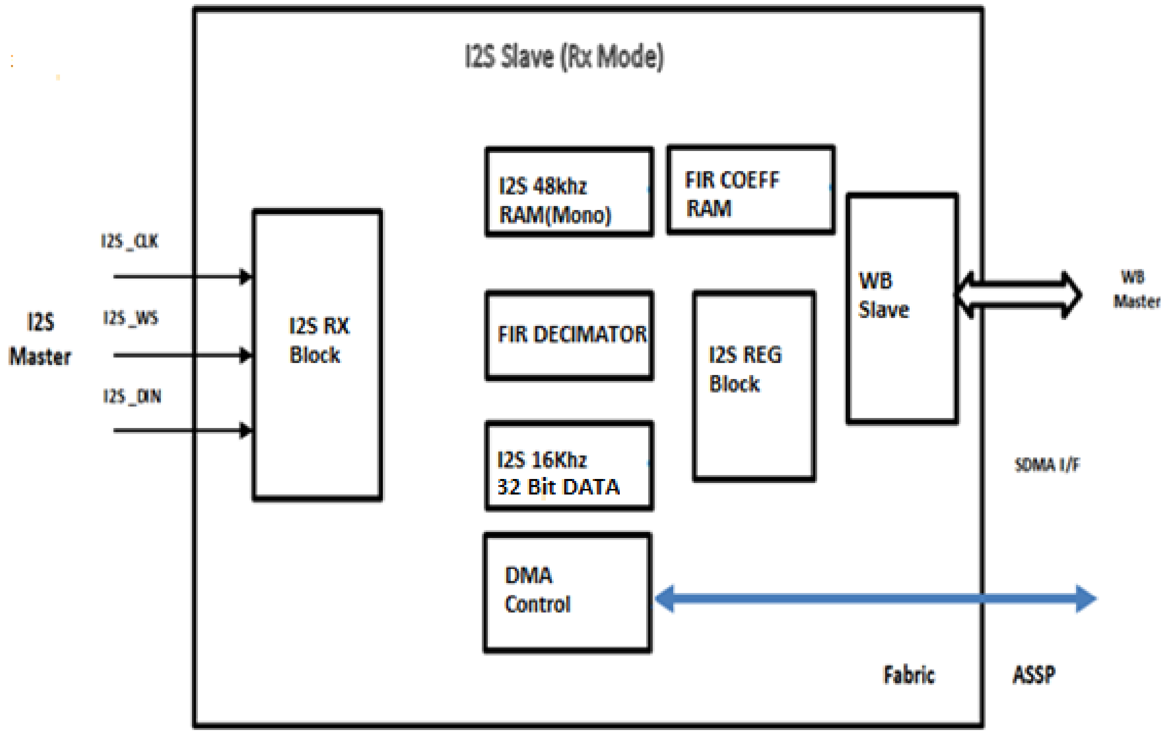

Figure 4-1: I2S Slave IP Block Diagram

- ## Block description

3.1.1 I2S Rx Block:

The audio data Mono is received serially from a data input line. The receiving is timed with respect to the serial clock (sclk) and the word select line (ws). The serial data is latched into the receiver on the leading edge of the serial clock signal.

3.1.2 RAM Block

The IP utilizes 2 RAM blocks for Storing I2S 48khz data and FIR Coefficients. Each of these RAM blocks are 512x16 in size.

3.1.2.1 I2S 48khz RAM(Mono)

The I2S data sampled at 48Khz is written to this block by the I2S Rx Block. This RAM is read accessible by the FIR filter only. This RAM block may be cleared via the Wishbone interface (writing any data to a RAM location will result in a write of all 0's to that RAM location).

The FIR decimation filter if enabled will read from the pre-decimation RAM and perform decimation.

3.1.2.2 FIR Coefficient RAM

This RAM stores the pre-calculated FIR coefficients. The FIR coefficients are calculated in matlab.

Following equation is used for calculating coefficients for 121 Tap FIR filter.

b1 = fir1(120, 0.90/3, kaiser(121, 6.3));

b2 = round(b1*32768);

The M4 should write the coefficient values in the FIR Coefficient RAM during the initialization phase. Since the RAM is 512x16 in size, only the lower 16 bits of each 32-bit write from the Wishbone interface will be written to the Coefficient RAM. The coefficients need not be modified thereafter.

3.1.3 I2S slave register block:

This block supports the I2S slave register and the DMA registers. Details provided in the Address Map specification section.

3.1.4 FIR Decimation block:

This block has 121 tap coefficient FIR filter with built-in decimator. The decimator decimates by a factor of 3. Input data which is sampled at 48khz is down sampled to 16khz. FIR decimation filter utilizes RAM as a delay element and operates at a rate of ~5Mhz by doing fast access per sample.

The coefficient RAM is initialized by host. The filter uses coefficient RAM for calculating the final decimated sample value.

When I2S clock stops and there are no I2S data writes to RAM, FIR decimator detects this condition and uses Zero data for calculating decimated sample values. After FIR decimator has pushed all zeroes in the virtual delay elements and I2S writes have stopped then FIR decimator stops its operation, decimation enable bit is cleared and an interrupt is generated.

When host receives decimation done interrupt it needs to clear the I2S 48khz RAM buffer by writing 0x0, 16-bit data to this RAM.

3.1.5 DMA control block:

This block generates the DMA Request to the SDMA block when there is 1 Word of DMA data is available in the decimation RAM. DMA complete is indicated by DMA done signal from Assp. Once the DMA done is received then DMA done interrupt is generated to the M4.

3.1.6 Wishbone Slave Interface:

This block is a communication bridge between M4 and fabric design.

Address Map Specification

3.2 Memory Map

The EOS 3B system maps the FPGA IP into the address range of 0x40020000 to 0x4003FFFF. This address range provides 128K bytes of address range for FPGA based IP. Each instantiation of this Decimation Filter IP module should be allocated a base address within the FPGA's address space. The register offsets described in this document are all relative to the Decimation Filter IP's base address that you have chosen for your design. The Decimation Filter module currently uses 8KB of address space, although this address space may not be fully utilized.

Table 5-1: Fabric IP Register Space

Register	Block	Space Allocated	Remarks
0x0000 – 0x0FFF	Decimation Filter		
0x1000 – 0x1FFF	FIR coefficient RAM		

3.3 Decimation Filter Register Address Table

The table below shows the expected allocation of the Decimation Filter Register address space.

Table 5-2: Decimation Filter Register Table

Register	Register Name	Reset Value	Description
0x0000	IER	0x0	I2S Enable Register
0x0004	*Reserved*	*0x0*	*Reserved*
0x0008	ISR	0x0	Interrupt Status Register
0x000C	IEN	0x0	Interrupt Enable Register
0x0010	DFSTS	0x0	Decimation FIFO Status Register
0x0014	DFDREG	0x0	Decimation Data Register 16 bit
0x0018	*Reserved*	*0x0*	*Reserved*
0x001C	DFRST	0x0	Decimation FIFO reset.
0x0020	DER	0x0	DMA Enable Register
0x0024	DSR	0x0	DMA Status Register
0x0028	DCNT	0x2	DMA Count Register
0x002C	*Reserved*	*0x0*	*Reserved*
0x0030	FDCR	0x0	FIR Decimation control.
0x0034	FDSR	0x0	FIR Decimator Status Register

Register	Register Name	Reset Value	Description
0x0038	*Reserved*	*0x0*	*Reserved*
0x003C–0x03FF	*Reserved*	*0x0*	*Reserved*
0x1000–0x1FFF	FCRAM	0x0	FIR decimator coefficient RAM.

3.4 I2S Slave Register Description:

3.4.1 Coeff RAM Access Control Register (0x0000)

Register Address location: 0x0000

Reset Value: 0x00

Table 5-3: Coeff RAM Access Control Register

Name	Bit(s)	Type	Description
Reserved	[31:4]	R	Returns 0
COERAMRD_AC	3	R/W	Setting this bit to 1 enables the read access to Coefficient Ram from Wb interface cutting off the FIR decimator read access. Added for initial Software debug. Needs to be set to 0 after reading the RAM for FIR decimation.
Reserved	*2:0*	*R*	*Reserved*

3.4.2 Reserved (0x0004)

Register Address location: 0x0004

Reset Value: 0x00

Table 5-4: Reserved Register

Name	Bit(s)	Type	Description
Reserved	*[31:0]*	*R*	*Returns 0*

3.4.3 Interrupt Status Register (0x0008)

Register Address location: 0x0008

Reset Value: 0x00

Table 5-5: Interrupt Status Register

Name	Bit(s)	Type	Description
Reserved	[31:3]	R	Returns 0
DES_CMPL	2	RO	Decimation Complete. FW needs to clear the interrupt, write 0 to clear
DES_DAT_AVL	1	RO	Data Available in the Decimation Rx FIFO. For each 16bit data availability an interrupt is generated.
DMA_DONE_INT	0	R/W	DMA complete interrupt FW needs to clear the interrupt, write 0 to clear

3.4.4 Interrupt Enable Register (0x000C)

Register Address location: 0x000C

Reset Value: 0x00

Table 5-6: Interrupt Enable Register

Name	Bit(s)	Type	Description
Reserved	[31:3]	R	Returns 0
DEC_D_AVL_INT_EN	2	R/W	Decimation data available. 0 – disable 1 – enable
DEC_DN_INT_EN	1	R/W	Decimation Done interrupt. 0 – disable 1 – enable
DMA_DONE_INT_EN	0	R/W	Dma done interrupt. 0 – disable 1 – enable

3.4.5 Decimation Rx FIFO Status Register (0x0010)

Register Address location: 0x0010

Reset Value: 0x00000000

Table 5-8: Decimation Rx Fifo Status register

Name	Bit(s)	Type	Description
DFSTS	[31:18]	R	Decimation fifo status register
DRxFIFOFUL	[17]	R	Decimation Rx FIFO Full.
DRxFIFOEMP	[16]	R	Decimation Rx FIFO empty.
DRxFIFOLVL	[15:0]	R	Decimation Rx FIFO level.

3.4.6 Decimation Rx FIFO Data Register (0x0014)

Register Address location: 0x0014

Reset Value: 0x00000000

Table 5-8: Decimation Rx Fifo Data register

Name	Bit(s)	Type	Description
DFDREG	[31:16]	R	Decimation Odd Data
	[15:0]	R	Decimation Even Data

3.4.7 Reserved (0x0018)

Register Address location: 0x0018

Reset Value: 0x00000000

Table 5-8: Reserved register

Name	Bit(s)	Type	Description
Reserved	*[31:0]*	*R*	*Reserved.*

3.4.8 Decimation Fifo Reset(0x001C)

Register Address location: 0x001C

Reset Value: 0x0

Table 5-12: Reserved

Name	Bit(s)	Type	Description
DFRST	[31:0]	W	Write 0x1 to reset the FIFO. This bit is auto clear.

3.4.9 DMA Enable Register (0x0020)

Register Address location: 0x0020

Reset Value: 0x0

Table 5-11: DMA Enable Register

Name	Bit(s)	Type	Description
Reserved	*[31:1]*	*R*	*Returns 0*
DMA_EN	0	R/W	0 - Disable 1 – Enable HW clears this bit when the DMA transfer is done

3.4.10 DMA Status Register (0x0024)

Register Address location: 0x0024

Reset Value: 0x0

Table 5-12: DMA Status Register

Name	Bit(s)	Type	Description
Reserved	*[31:1]*	*R*	*Returns 0*
DMA_REQ	0	R	Fabric IP generates the DMA Request to the SDMA block
DMA_ACTIVE	0	R	DMA Active signal from the SDMA block
DMA_DONE	0	R	1 - DMA is completed
DMA_Busy	0	R	0 – DMA not in progress 1 – DMA in progress

3.4.11 DMA Count Register (0x0028)

Register Address location: 0x0028

Reset Value: 0x4

Table 5-13: DMA Count Register

Name	Bit(s)	Type	Description
Reserved	*[31:9]*	*R*	*Returns 0*
DMA_CNT	[8:0]	R/W	DMA count register (in 16-bit word length) Reset value: 0x2 (Two 16 Bit Data) FW need to write the DMA count while setting up the SDMA register. This register gives the DMA count in 16 bit word.

3.4.12 Reserved (0x002C)

Register Address location: 0x002C

Reset Value: 0x0

Table 5-12: Reserved

Name	Bit(s)	Type	Description
Reserved	*[31:0]*	*R*	*Returns 0*

3.4.13 FIR Decimation Control Register (0x0030)

Register Address location: 0x0030

Reset Value: 0x0

Table 5-11: FIR decimation control Register

Name	Bit(s)	Type	Description
Reserved	[31:1]	R	Returns 0
FIR_DECI_INT_EN	1	W	0 - Disable 1 – Enable
FIR_DECI_EN	0	R/W	0 - Disable 1 – Enable Enable FIR decimation. Cleared by the Hardware automatically at the end of Decimation cycle.

3.4.14 Reserved (0x0034)

Register Address location: 0x0034

Reset Value: 0x0

Table 5-11: FIR decimation Status Register

Name	Bit(s)	Type	Description
Reserved	*[31:0]*	*R*	*Returns 0*

3.4.15 Reserved (0x0038)

Register Address location: 0x0038

Reset Value: 0x0

Table 5-12: Reserved

Name	Bit(s)	Type	Description
Reserved	*[31:0]*	*R*	*Reserved*

3.4.16 Reserved (0x003C-0x03FF)

Register Address location: 0x003C-0x03FF

Reset Value: 0x0

Table 5-12: Reserved

Name	Bit(s)	Type	Description
Reserved	*[31:0]*	*R*	*Reserved*

3.4.17 FIR COEFF RAM(0x1000-0x17FF)

Register Address location: 0x1000-0x17FF

Reset Value: 0x0

Table 5-12: FIR Coefficient RAM

Name	Bit(s)	Type	Description
Reserved	*[31:16]*	*R/W*	*Unused*
FIR coefficient Data	[15:0]	W	Lower 16 bits of the coefficient RAM.

4 Programming Sequence:

The following programming sequence should be performed by software when this Decimation Filter IP is used in conjunction with the I2S Slave Rx IP.

4.1.1 Decimation Data Read sequence

a. AP interrupts S3B (M4) through the SW interrupt register indicating I2S master is ready to send data.

b. M4 runs the ISR routine to set up the I2S slave to receive the Audio data

1. Power on the fabric block if it is in power down mode

2. Enable and setup the fabric clocks (C16 = 5Mhz and C21)

3. Set up the SDMA to DMA the data from the fabric FIR decimation Buffer Port to the M4 SRAM

    - Source address from the fabric DFDREG (0x1014).
    - DREQ will be generated for each 32 bit Decimation data available, the DMA count register(DCNT 0x1028) is set to default value of 0x1 which indicates availability of one 32 bit data. The register can be set to higher count values as well to do burst transfers of 32 bit data.

    - Destination address, M4SRAM location allocated for Audio buffer incremented on every 32-bit data received

    - SDMA channel dedicated for this I2S slave path is Channel 12

4. Enable the fabric interrupt in the NVIC

5. Enable the I2S DMA done fabric interrupt in the interrupt controller

- I2S DMA done interrupt done is tied on the fb_intr[2]

- Set up FB_INTR_TYPE, its level interrupt (0x40004888 = 0x0)

- Set up FB_INTR_POL, its high polarity (0x4000488C = 0x4)

- Set up FB_INTR_EN_M4, interrupt enable to M4 (0x40004894 = 0x4)

6. Set up the fabric register to receive the Decimated data

   - Set up the DMA count, write DMA_CNT (in 16- bit words) to DMA count register (0x1028). The count register is by default set to 2. Since DMA request is generated for two 16 bit data packed in 32 bit.

   - Clear the DMA done intr (if any) write 0 to bit[0] of the interrupt status register (0x1008)

   - Enable DMA done interrupt, bit[0] = 1 of the interrupt enable register (0x100C)

   - Enable the DMA, write 0x1 to 0x1020, HW clears this bit when the DMA transfer is done

     - Enable Write access to FIR I2S 48khz RAM. Write 0x1000 = 0x2
     - Clear the RAM. Write (0x0800-0x0FFF) =0x0. (This process of zero data initialization of the I2S 48khz RAM needs to be done after the decimation process is completed)
     - Initialize the FIR COEFF RAM memory(0x2000-0x2FFF)= 121 Tap pre-calculated coefficient data. After writing meaningful 121, 32 bit data(lower 16 bit valid), write 0s.

   - Enable the FIR decimator and interrupt:
     - Write 0x1030 = 0x3

   - Enable the FB I2S slave:
     - Write 0x1000 = 0x1(Here the wishbone write access to I2S RAM is also released so that I2S block can write data to this RAM).

c. Now I2S slave in the fabric is ready to receive the I2S data

d. Interrupt AP, indicating S3 device is ready to receive the I2S data and I2S master in the AP can start transmitting the Audio data

e. FB I2S Slave receives the I2S Audio data and stores in the FIR I2S 48khz RAM . FIR decimator reads this Data and uses coefficient RAM data to calculate the decimated Samples. When two 16 bit sample value are available then fabric generates DMA_REQ to the SDMA indicating SDMA to start the DMA transfer.

f. SDMA starts DMA transfer of audio data from the Decimation Rx FIFO data to M4 SRAM. Dreqs are generated based on the threshold set in DCNT(0x1028)

g. Once the DMA transfer is completed, fabric generates DMA done interrupt to M4 indicating that DMA transfer is complete and M4 can process the received data.

h. M4 runs the ISR routine to process the DMA done interrupt, M4 clears the DMA done interrupt by writing 0 to bit [0] of the interrupt status register (0x1008)

i. M4 sets up the next DMA transfer by configuring the SDMA engine

j. M4 enables the DMA by writing 0x1 to 0x1020

k. Fabric will generate the DMA_Req again when it has data in FIR decimation data reg.

l. The process repeats till the AP indicates to M4 to disable the I2S slave in the fabric.

m. At the end of Decimation (When no I2S data is available), Fabric generates FIR decimation Done interrupt. This bit is indicated in FIR decimation status register. After receiving this interrupt the Host needs to disable I2S enable & get write access to I2S 48khz RAM and initialize the RAM to zero. The write access bit after clearing needs to be set to 0.

n. The host can then re enable the entire flow by

    a. Write 0x1030 = 0x3.
    b. Write 0x1000 = 0x1 (Clear I2S 48khz RAM before each Decimation run).

5 Revision History

Date	Revision	Author	Description
25 Mar 2021	1.00	Randy O	Initial Release
17 Jun 2021	1.01	Randy O	Removed registers that were relocated to the I2S Rx module. The register map and bitfields within registers have not be collapsed/compacted, to help maintain compatibility with software.

6 Copyright and Trademark Information

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