QuickFeather FPGA – USB Serial Port
Register Map:

Offsets shown are for the FPGA base address, as seen by the M4 (I believe this to be 0x4002_0000).

Note: Registers may be accessed 8, 16 or 32 bits at a time. To avoid confusion, 16-bit accesses should be 16-bit aligned (offsets 0x0, 0x2, 0x4, 0x6, 0x8, etc. only), and 32-bit accesses should be 32-bit aligned (offsets 0x0, 0x4, 0x8, 0xC only).

The least-significant byte (LSB) is always on the "right", so a 32-bit register at offset 0x00 has bits [7:0] = offset 0x00, bits [15:8] = offset 0x01, etc.

Offset	Name	Bits	R/W	Default Val	Description
0x00	Device ID	[31:0]	R	0x0000_A5BD	Device ID.
0x04	Revision Number	[31:0]	R	0x0000_0200	Revision Number. 0x0000_0100: initial release. 0x0000_0200: Added support for multi-byte packets (up to 8 bytes) from device to host over USB (previously only 1 byte per packet). Added support for Clock Select (see register offset 0x0C).
0x08	Scratch Register	[15:0]	R/W	0x0000	Scratch Register. May be used to test out FPGA register accesses.
0x0A	Reserved	[15:0]	R	0x0000	Reserved, always 0.
0x0C	Clock Control	[0]	R/W	0	Bit 0: Clock select 0 = [defaut] Use raw eFPGA clock (the HSOSC must be set to 48MHz). 1 = Divide by 1.5 (the HSOSC must be set to 72MHz). This allows the HSOSC, and therefore the M4 clock, to be run at a faster rate for better performance, while keeping the USB clock at 48MHz. Bits 31 downto 1: reserved, always 0.
0x10	USB PID	[15:0]	R/W	0x6140	Bits [15:0]: USB ProductID (PID). Bits [31:16]: Reserved, always 0.
0x14 – 0x3C	Reserved	[31:0]	R	N/A	Reserved.
0x40	USB2M4 FIFO Flags	[3:0]	R	0x0	Pop flag: 0b0000 = empty 0b0001 = 1 entry in FIFO 0b0010 = at least 2 entries 0b0011 = at least 4 entries 0b0100 = at least 8 entries 0b0101 = at least 16 entries 0b0110 = at least 32 entries 0b1000 = less than 1/4 to 64 entries 0b1101 = 1/4 or more full 0b1110 = 1/2 or more full 0b1111 = full others = reserved
0x41 – 0x43	Reserved		R	0x0	Reserved, always 0.
0x44	USB2M4 FIFO Read Data	[7:0]	R	N/A	USB-to-M4 FIFO Read Data.
0x45 – 0x47	Reserved		R	0x0	Reserved, always 0.
0x80	M42USB FIFO Flags	[3:0]	R	0x1	Push flag: 0b0000 = full 0b0001 = empty 0b0010 = room for more than 1/2 0b0011 = room for more than 1/4 0b0100 = room for less than 1/4 to 64 0b1010 = room for 32 to 63 0b1011 = room for 16 to 31 0b1100 = room for 8 to 15 0b1101 = room for 4 to 7 0b1110 = room for at least 2

					0b1111 = room for at least 1 others = reserved
0x81 – 0x83	Reserved		R	0x0	Reserved, always 0.
0x84	M42USB FIFO Write Data	[7:0]	W	N/A	M4-to-USB FIFO Write Data.
0x85 – 0x87	Reserved		R	N/A	Reserved.
0x88 – 0xBC	Reserved	[31:0]	R	N/A	Reserved.
0xC0	USB2M4 FIFO Data Interrupt Enable	[0]	R/W	0x0	USB-to-M4 FIFO Data Interrupt Enable. 0 = disable interrupt to M4 when U2M FIFO data is available. 1 = enable interrupt to M4 when U2M FIFO data is available.
0xC1 – 0xC3	Reserved		R	0x0	Reserved, always 0.

Pin Out:

	Port Name	**Pin Number (PU64)**	**Alias Name**
SPI I/F:			
	spi_cs_o	11	IO_39
	spi_sck_o	20	IO_34
	spi_mosi_o	16	IO_38
USB:			
	usb_pu_cntrl_o	15	IO_37
	usbn_io	14	IO_41
	usbp_io	10	IO_42
	led_o	38	IO_18