AEC FPGA Project

Revision: 1.0

Date: 21 Jan 2021

QuickLogic Corporation

# Requirement:

# Pinout:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Sl. No.** | **Signal Name** | **PAD Number** | **Direction** | **Description** |
| FLL | | | | |
| 1 | I2S\_bitclk\_in |  | Input |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |

# FPGA Interrupts:

|  |  |  |
| --- | --- | --- |
| **Sl. No.** | **FPGA Interrupts to M4** | **Interrupt Description** |
| 1 | FB\_INTERRUPT\_0 | Local clock slow down |
| 2 | FB\_INTERRUPT\_1 | Local clock speed up |
| 3 | FB\_INTERRUPT\_2 | Reserved |
| 4 | FB\_INTERRUPT\_3 | Reserved |

# Address Map Specification

## Memory Map

The EOS 3B system maps the FPGA IP into the address range of 0x40020000 to 0x4003FFFF. This address range provides 128K bytes of address range for FPGA based IP. The following tables further define the registers within this range.

Table 1‑1: FPGA IP Register Space

|  |  |  |  |
| --- | --- | --- | --- |
| Register | Block | Space Allocated | Remarks |
| 0x40020000 – 0x400200FF | FPGA IP Registers | 256 bytes |  |
| 0x40020100 – 0x40020FFF | Reserved |  |  |
| 0x40021000 – 0x40021FFF | FLL\_I2S | 4096 bytes |  |
| 0x40022000 – 0x40022FFF | I2S RAM | 4096 bytes |  |
| 0x40023000 – 0x40023FFF | I2S Slave Registers | 4096 bytes |  |
| 0x40024000 – 0x40024FFF | FIR Coefficients | 4096 bytes |  |
| 0x40025000 – 0x4003FFFF | Reserved |  |  |
|  |  |  |  |

## Register Address Table

The following sections will outline the expected allocation of registers and describe their operations.

### FPGA Registers Address Table

Table 1‑2 shows the expected allocation of FPGA Registers address space.

Table 1‑2: FPGA IP Register Table

| Register | Block | Reset Value | Remarks |
| --- | --- | --- | --- |
| 0x40020000 | IP Device ID | 0xABCD0200 | Read only |
| 0x40020004 | IP Revision number | 0x0100 | Read only  Version |
| 0x40020008 – 0x400200FF | Not Used | 0x0 | Reserved. |

### FLL\_I2S Register Map

The FLL\_I2S module has a base address that starts at offset 0x1000 from the FPGA’s base address (0x40020000 + 0x1000). The register map for the FLL\_I2S Controller is described in a separate document, and can be found along with the RTL source code for the FLL\_I2S module (currently in QuickLogic’s s3-gateware repository on github, under ip\_modules).

### I2S RAM and I2S Slave Register Map

The I2S Slave module has a base address that starts at offset 0x2000 from the FPGA’s base address (0x40020000 + 0x2000). The I2S RAM starts at offset 0x2000 from the FPGA’s base address, and the I2S Slave registers start at offset 0x3000 from the FPGA’s base address. The register map for the I2S Slave Controller is described in a separate document, and can be found along with the RTL source code for the I2S Slave module (currently in QuickLogic’s s3-gateware repository on github, under ip\_modules).

### FIR Coefficients Register Map

The 3to1 Decimation (FIR) Filter module has a base address that starts at offset 0x4000 from the FPGA’s base address (0x40020000 + 0x4000). The register map for the Decimation Filter is described in a separate document, and can be found along with the RTL source code for the I2S Slave module (currently in QuickLogic’s s3-gateware repository on github, under ip\_modules).

# Revision History

|  |  |  |  |
| --- | --- | --- | --- |
| **Date** | **Revision** | **Author** | **Description** |
| 21 Jan 2021 | 1.00 | Randy O | Initial Release |
|  |  |  |  |
|  |  |  |  |

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