Contents

- Number Representation
- Logic Gates
- Combinational Circuits
- Sequential Circuits

Number Representation

- Binary (2)
- Octal (8)
- Decimal (10)
- Hexadecimal (16)
- Binary Coded Decimal (BCD)
- Gray Code
- Excess -3 Code

Any(2,8,16) to Decimal

Multiply by Radix

$$1358.246 = (1 \times 10^3) + (3 \times 10^2) + (5 \times 10^1) + (8 \times 10^0) + (2 \times 10^{-1}) + (4 \times 10^{-2}) + (6 \times 10^{-3})$$

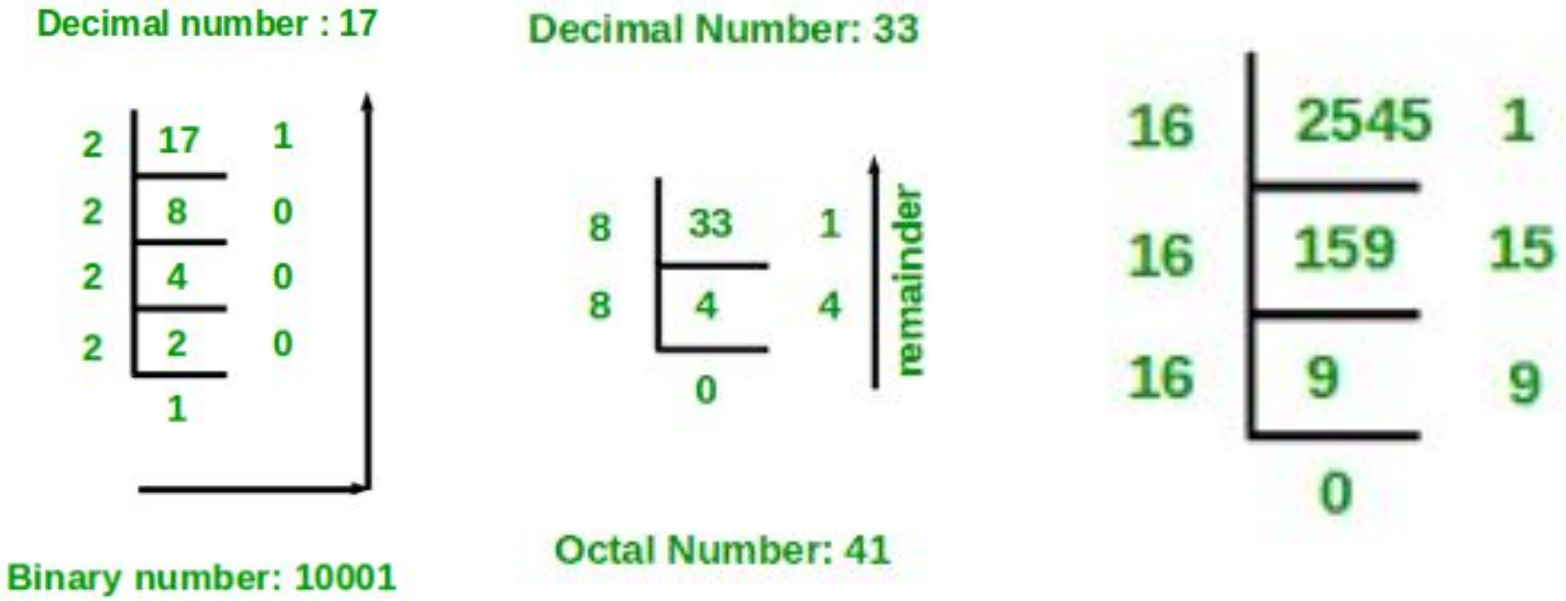
$$1101.011 = (1 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0) + (0 \times 2^{-1}) + (1 \times 2^{-2}) + (1 \times 2^{-3})$$

$$1457.236 = (1 \times 8^3) + (4 \times 8^2) + (5 \times 8^1) + (7 \times 8^0) + (2 \times 8^{-1}) + (3 \times 8^{-2}) + (6 \times 8^{-3})$$

$$1A05.2C4 = (1 \times 16^3) + (10 \times 16^2) + (0 \times 16^1) + (5 \times 16^0) + (2 \times 16^{-1}) + (12 \times 16^{-2}) + (4 \times 16^{-3})$$

Decimal to Other (2,8,16)

Divide by Radix



Other Conversion

Binary to

Octal	Substitution	$10111011001_2 = 10\ 111\ 011\ 001_2 = 2731_8$
Hexadecimal	Substitution	$10111011001_2 = 101\ 1101\ 1001_2 = 5D9_{16}$
Decimal	Summation	$10111011001_2 = 1 \cdot 1024 + 0 \cdot 512 + 1 \cdot 256 + 1 \cdot 128 + 1 \cdot 64 + 0 \cdot 32 + 1 \cdot 16 + 1 \cdot 8 + 0 \cdot 4 + 0 \cdot 2 + 1 \cdot 1 = 1497_{10}$

Octal to

Binary	Substitution	$1234_8 = 001\ 010\ 011\ 100_2$
Hexadecimal	Substitution	$1234_8 = 001\ 010\ 011\ 100_2 = 0010\ 1001\ 1100_2 = 29C_{16}$
Decimal	Summation	$1234_8 = 1 \cdot 512 + 2 \cdot 64 + 3 \cdot 8 + 4 \cdot 1 = 668_{10}$

Hexadecimal to

Binary	Substitution	$C0DE_{16} = 1100\ 0000\ 1101\ 1110_2$
Octal	Substitution	$C0DE_{16} = 1100\ 0000\ 1101\ 1110_2 = 1\ 100\ 000\ 011\ 011\ 110_2 = 140336_8$
Decimal	Summation	$C0DE_{16} = 12 \cdot 4096 + 0 \cdot 256 + 13 \cdot 16 + 14 \cdot 1 = 49374_{10}$

Binary Addition / Subtraction

c_{in} **or** b_{in}	x	y	c_{out}	s	b_{out}	d
0	0	0	0	0	0	0
0	0	1	0	1	1	1
0	1	0	0	1	0	1
0	1	1	1	0	0	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	0	0	0
1	1	1	1	1	1	1

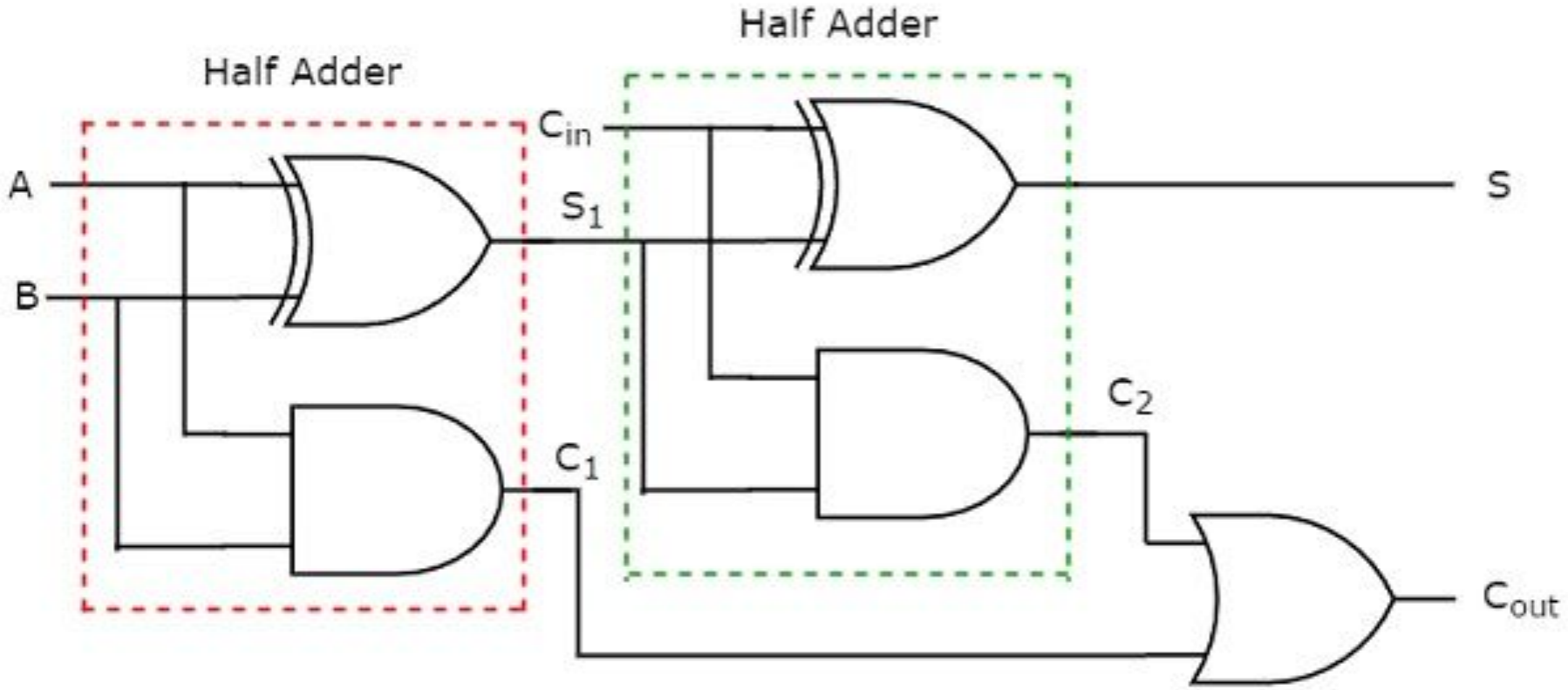
Logic Gates

- AND Gate
- OR Gate
- NOT Gate
- Ex-OR Gate
- Ex- NOR Gate
- **NAND Gate**
- **NOR Gate**

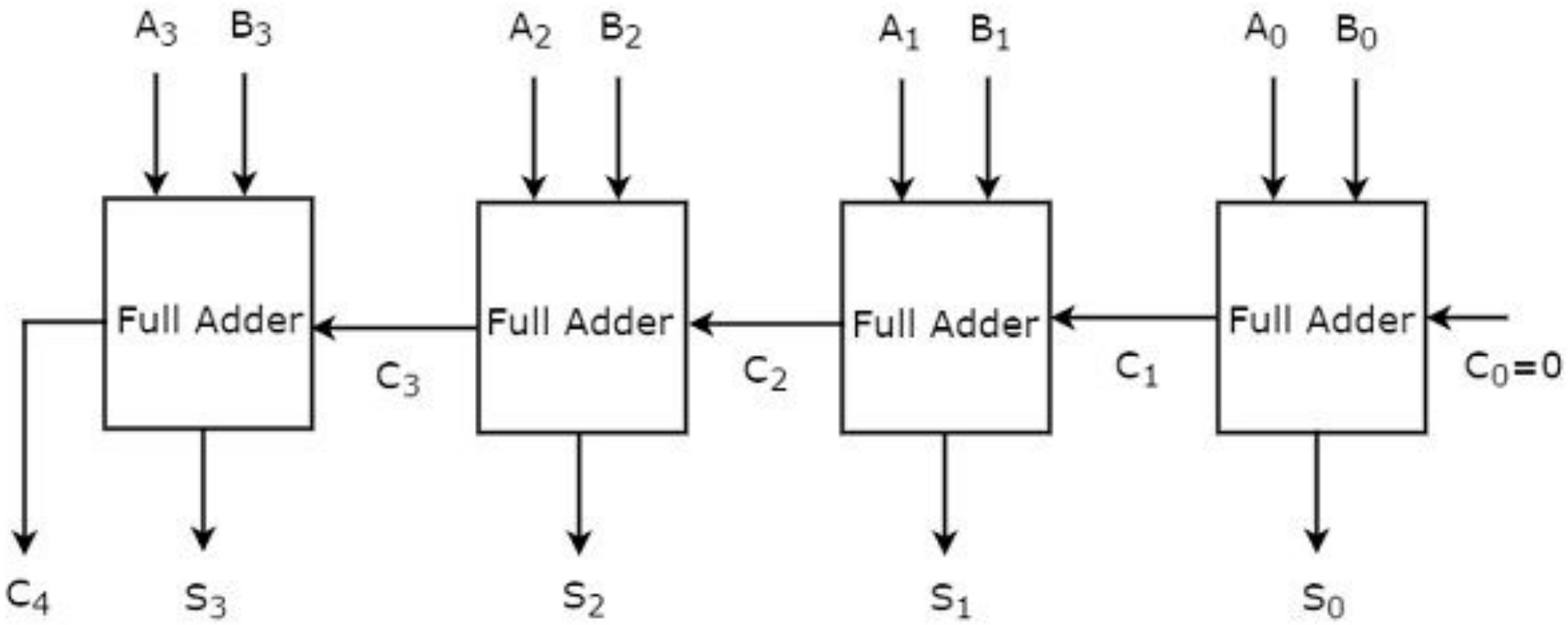
Combinational Circuits

- Adder
- Subtractor
- Multiplexer
- Demultiplexer
- Decoder
- Encoder

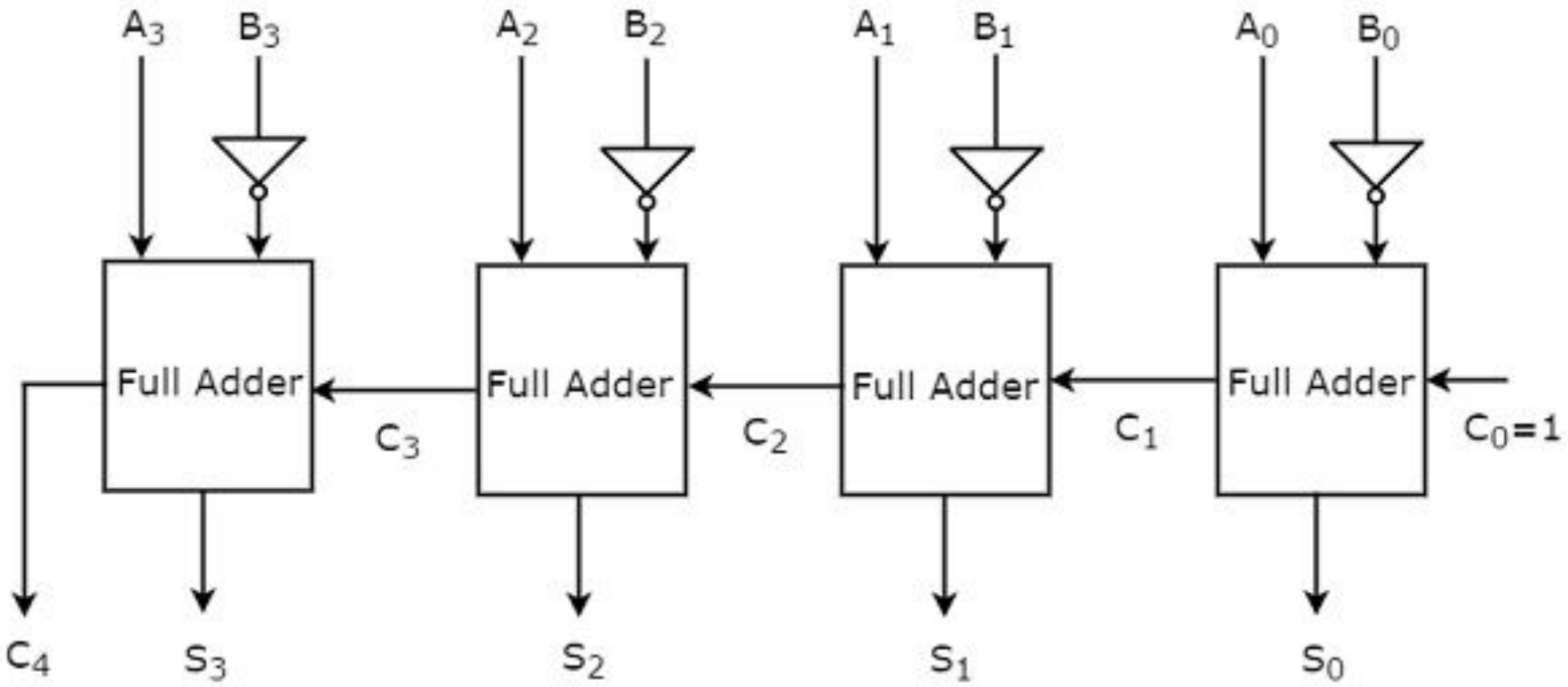
Full Adder



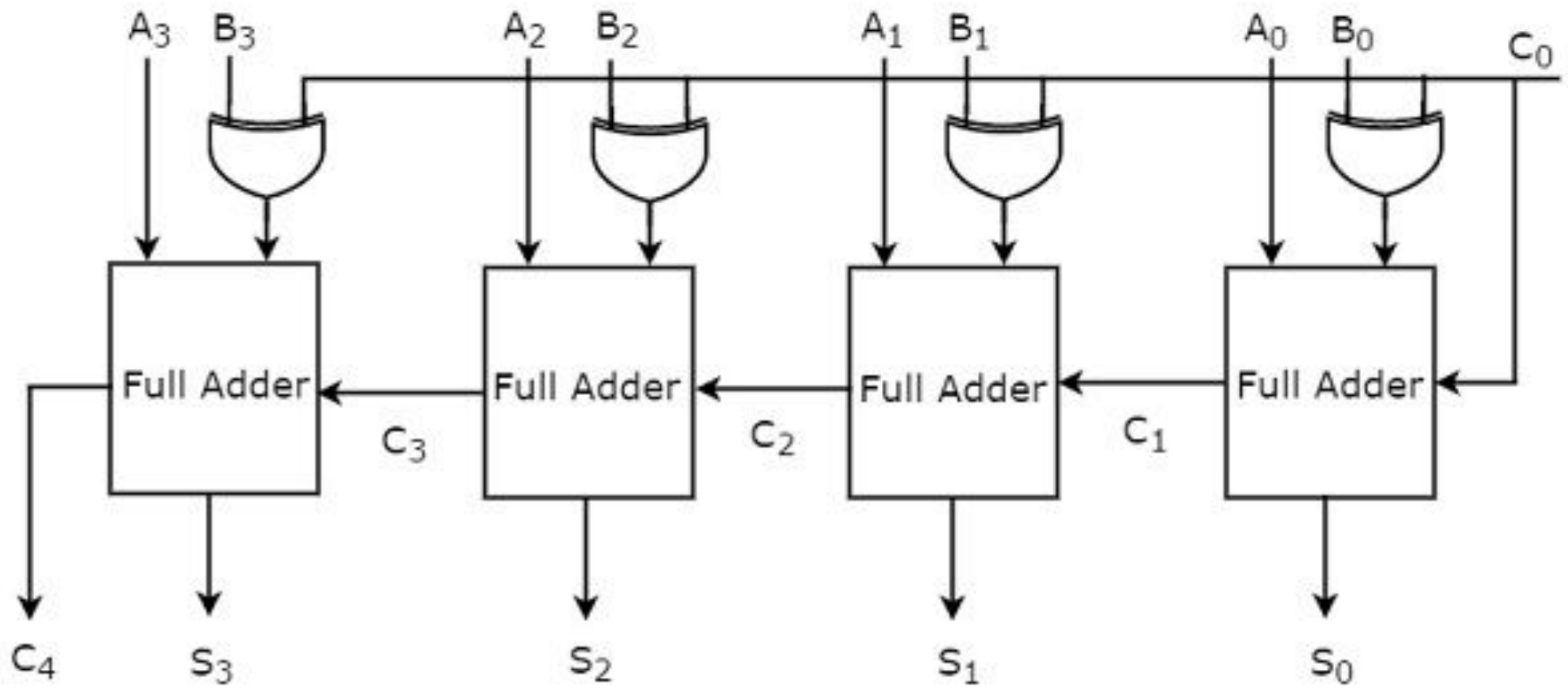
4 Bit Full Adder



Binary Subtractor



Adder and Subtractor



BCD Adder

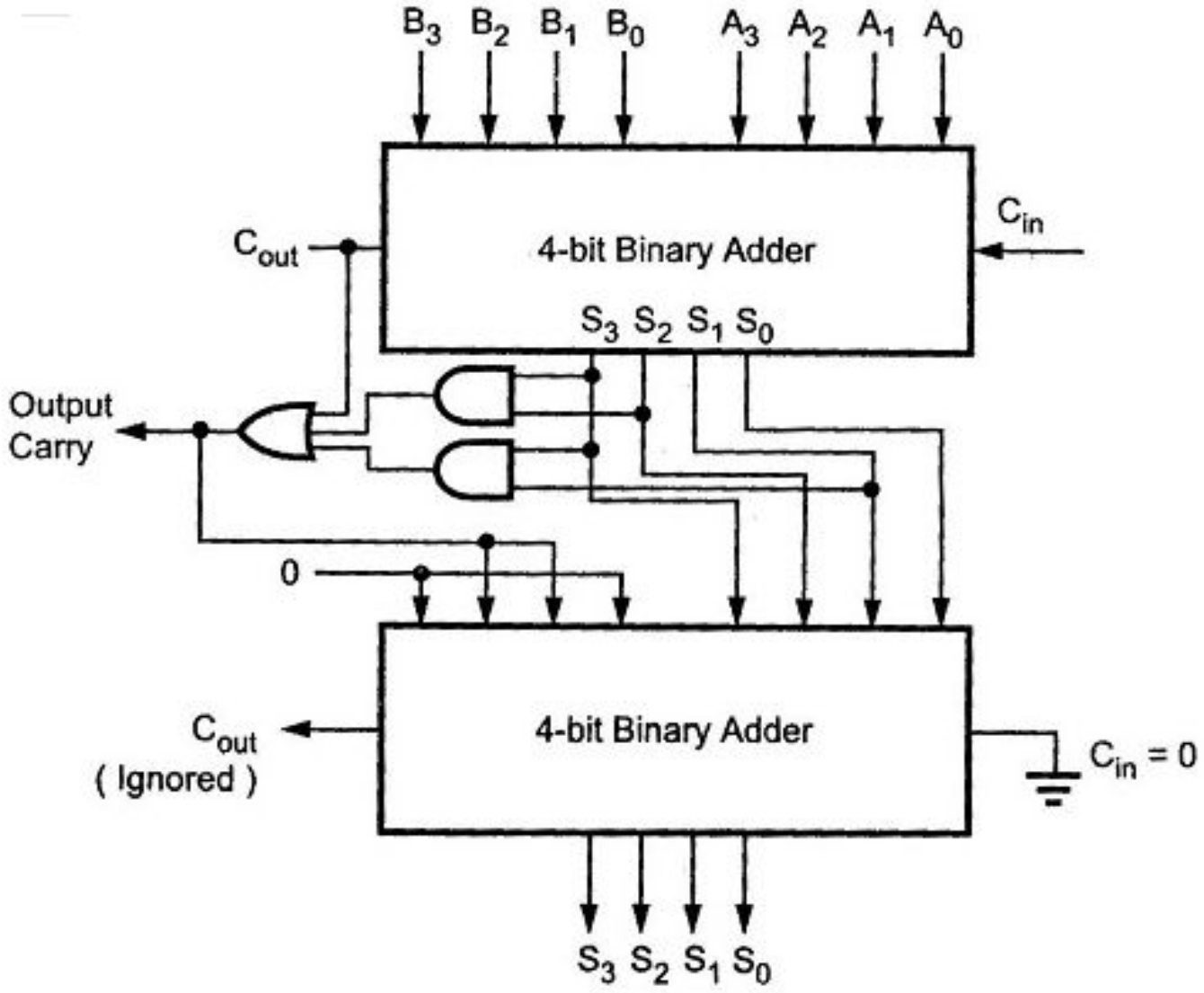
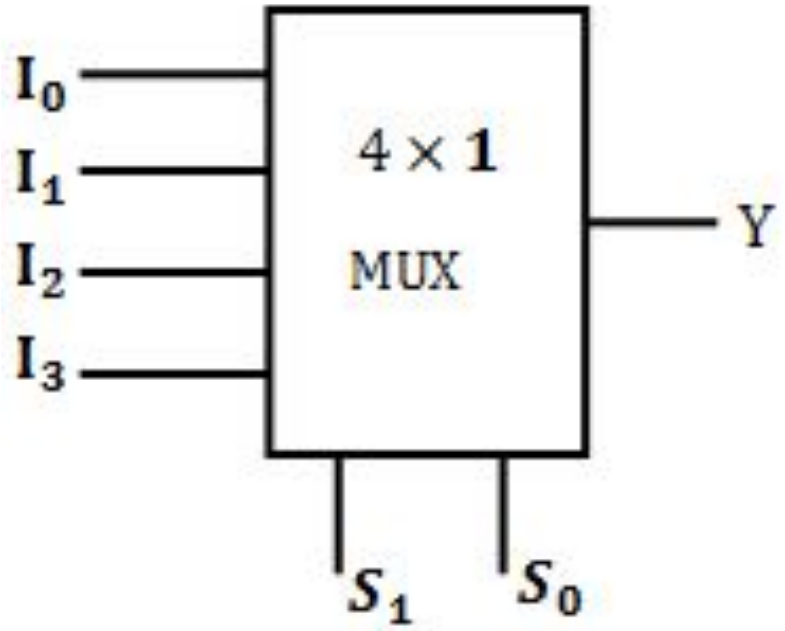


Fig.: Block diagram of BCD adder

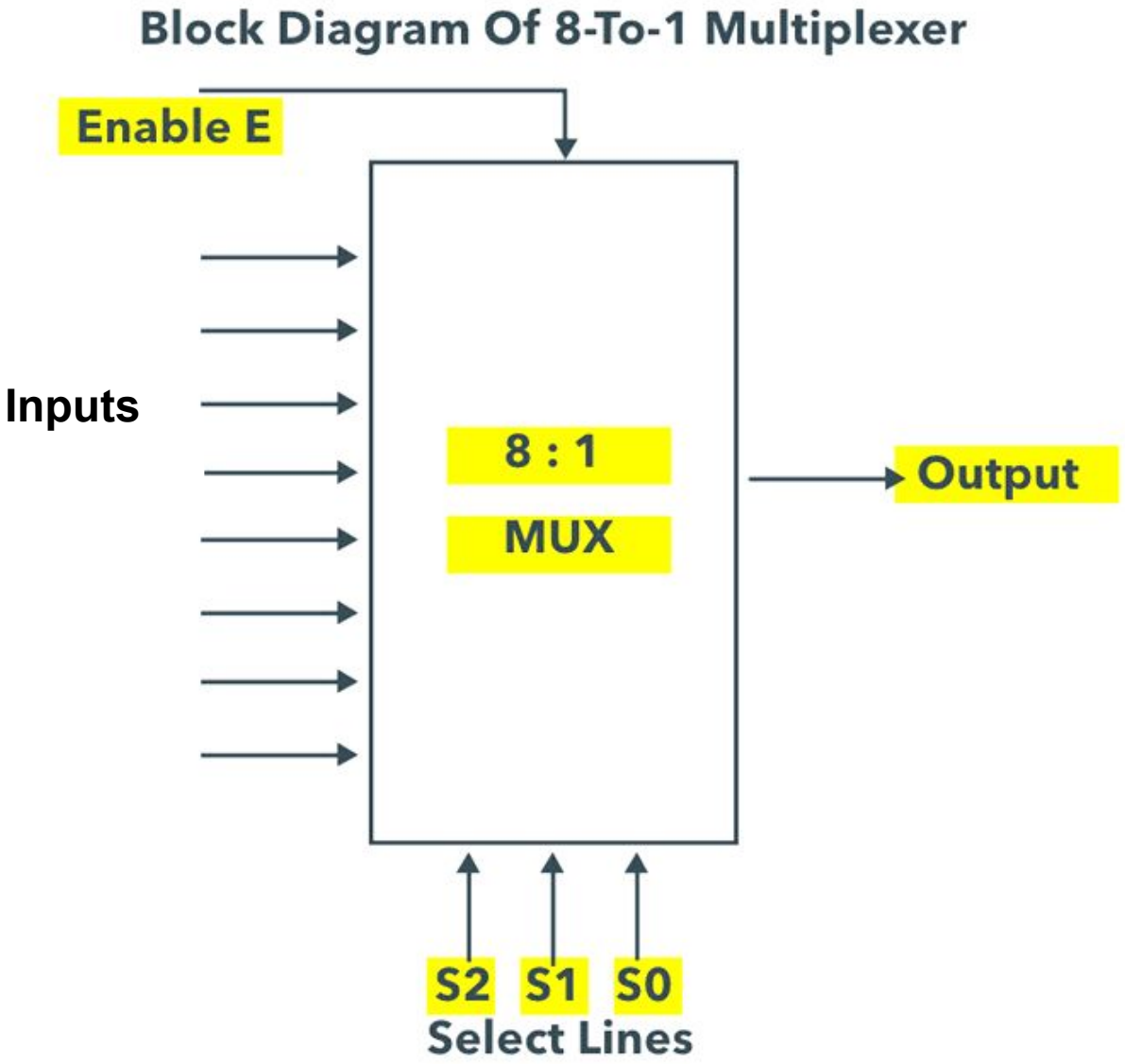
Multiplexer



Truth table

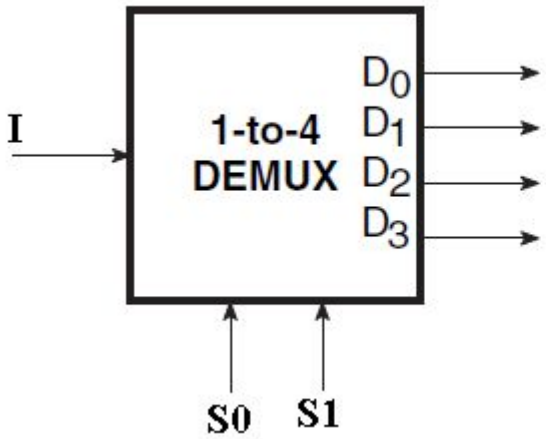
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Multiplexer



Input			Output
S2	S1	S0	Y
0	0	0	I0
0	0	1	I1
0	1	0	I2
0	1	1	I3
1	0	0	I4
1	0	1	I5
1	1	0	I6
1	1	1	I7

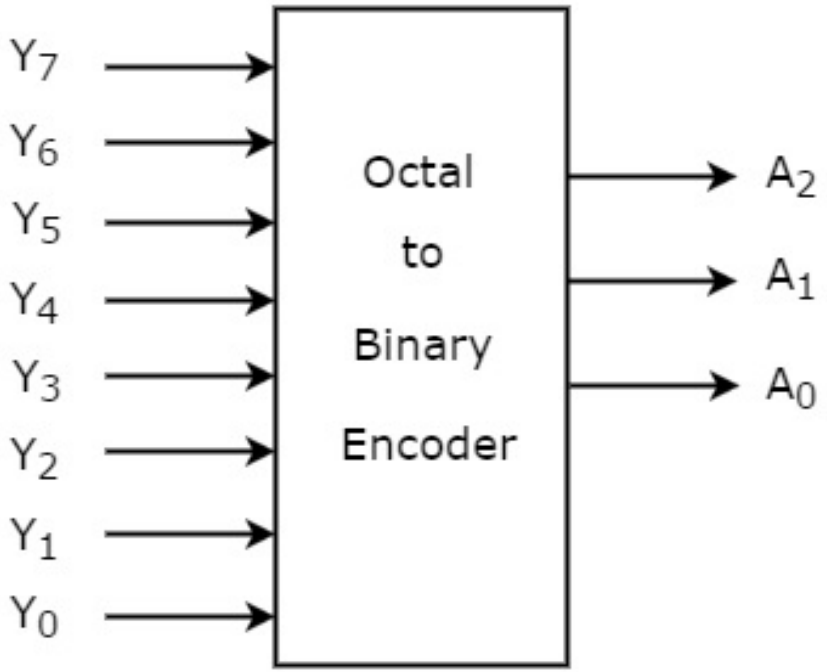
Demultiplexer



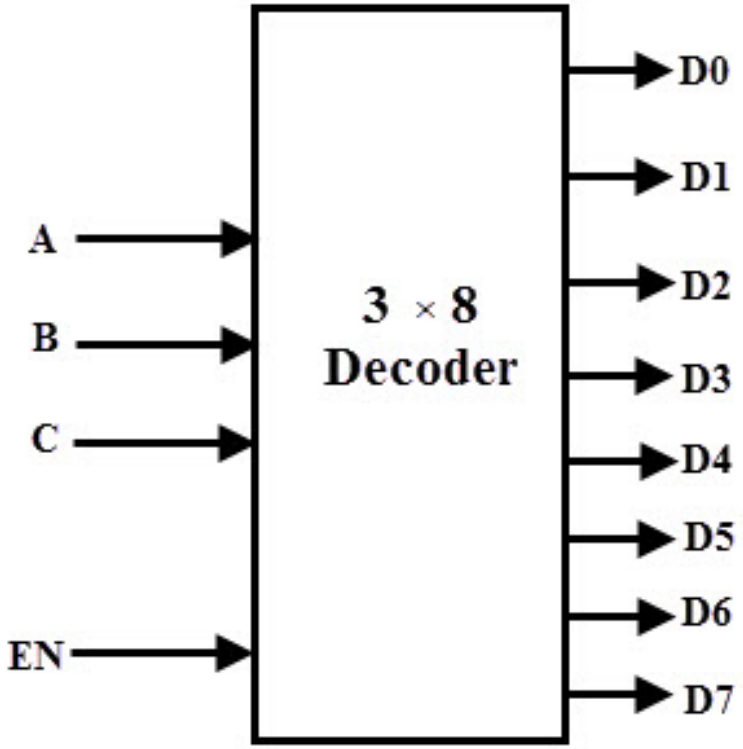
I	Select		O/P			
	S0	S1	D_0	D_1	D_2	D_3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

Encoder

8:3 Encoder

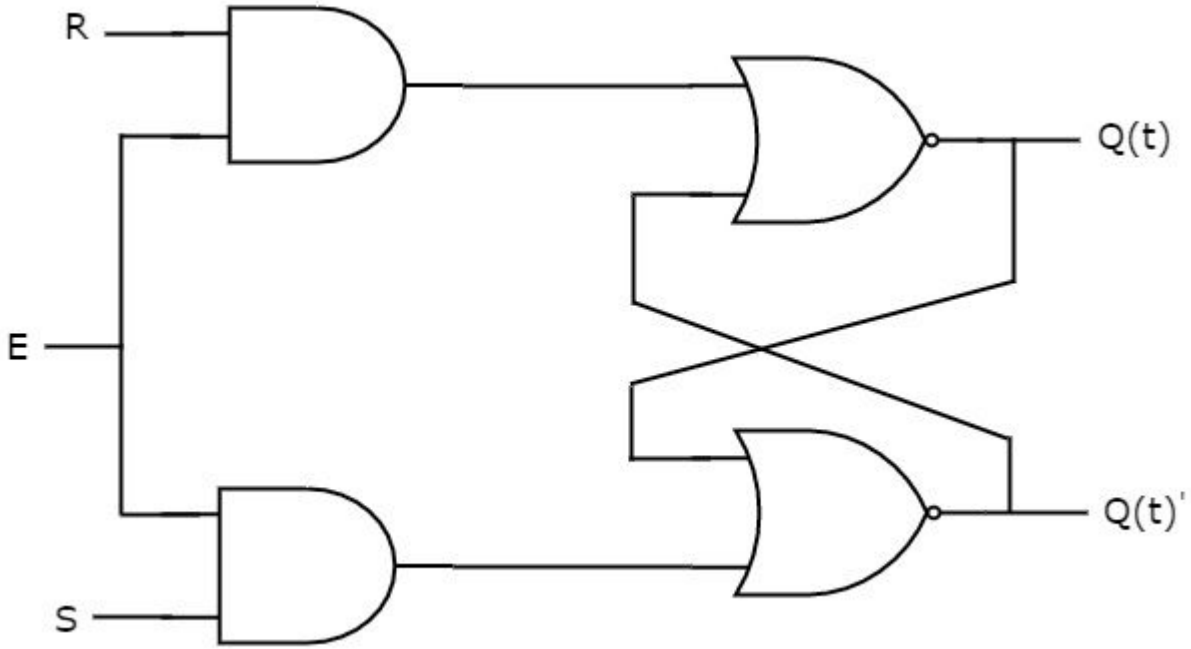


Decoder

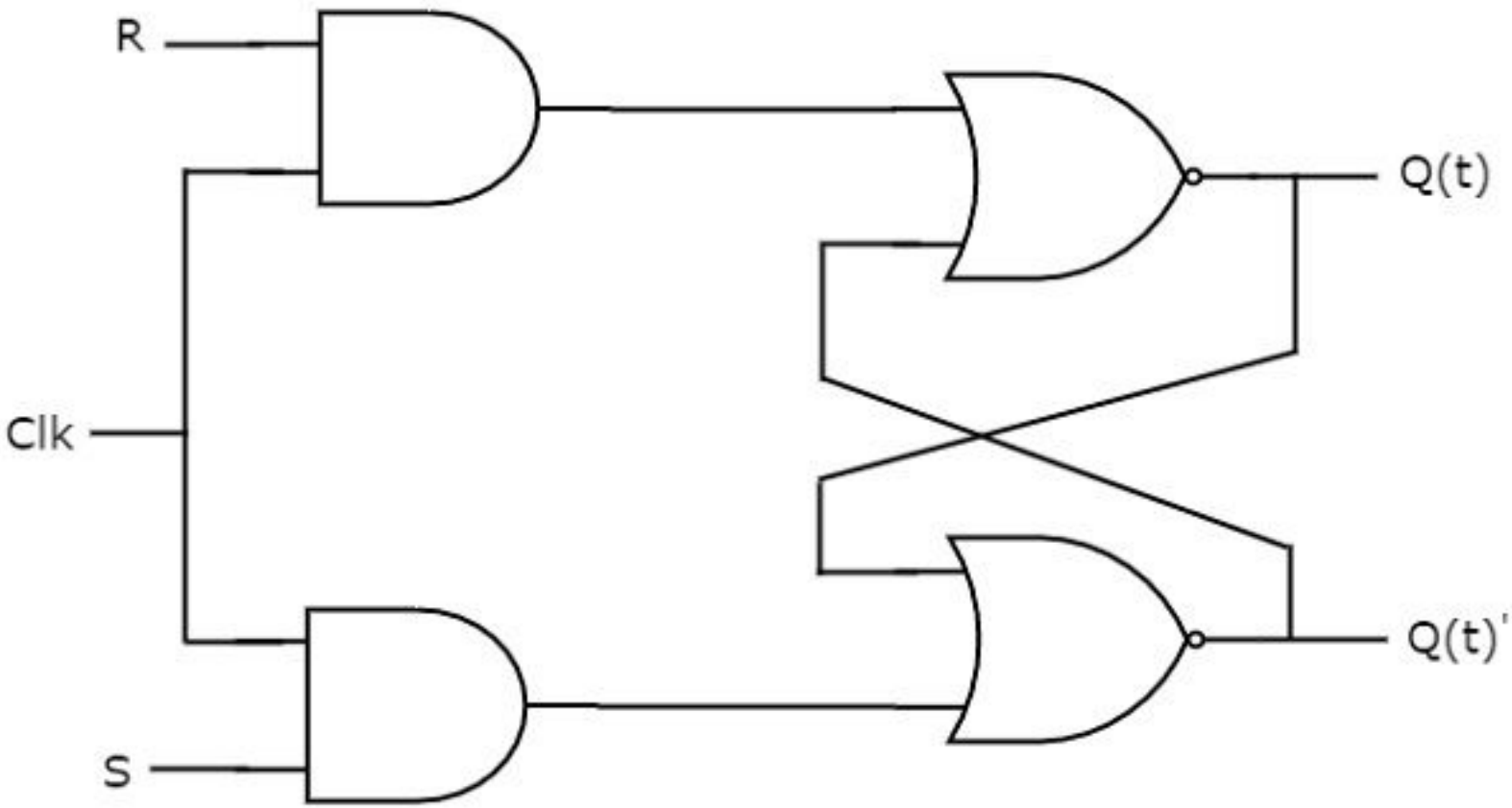


Latch and Flip Flop

- Latches operate with enable signal, which is level sensitive. Whereas, flip-flops are edge sensitive

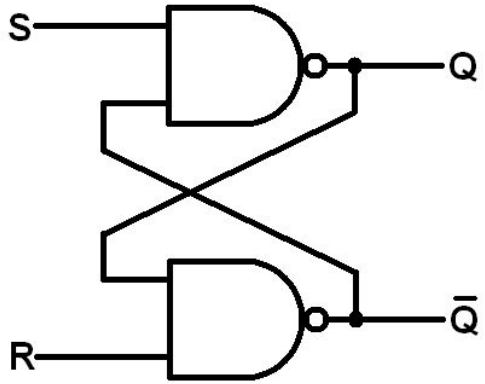


Latch and Flip Flop



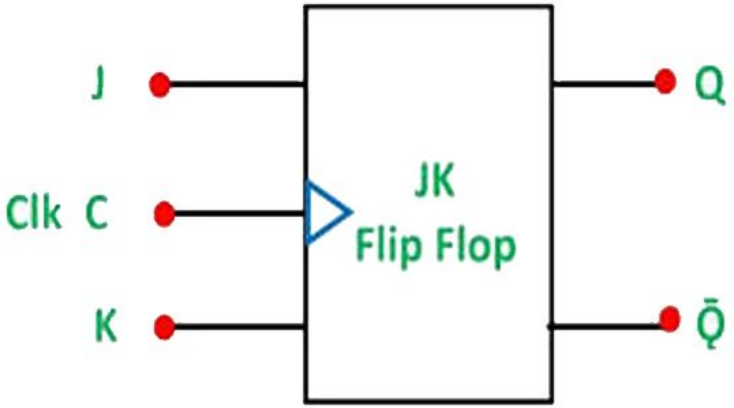
SR Flip Flop

SR Flip Flop

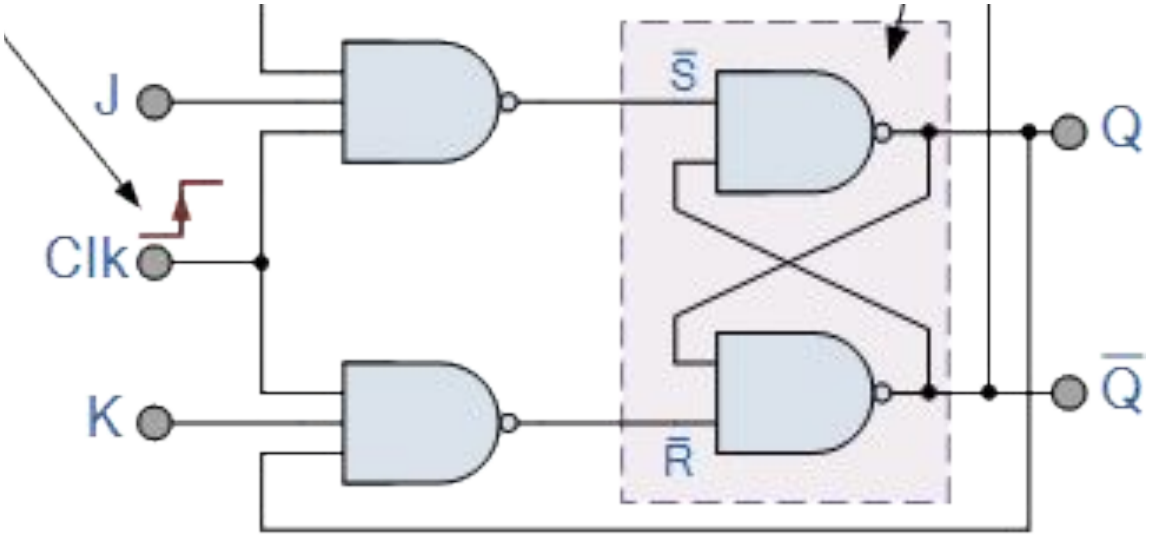


Sno	S	R	Q	Q'	State
1	1	0	1	0	Q is set to 1
2	1	1	1	0	No change
3	0	1	0	1	Q' is set to 1
4	1	1	0	1	No change
5	0	0	1	1	Invalid

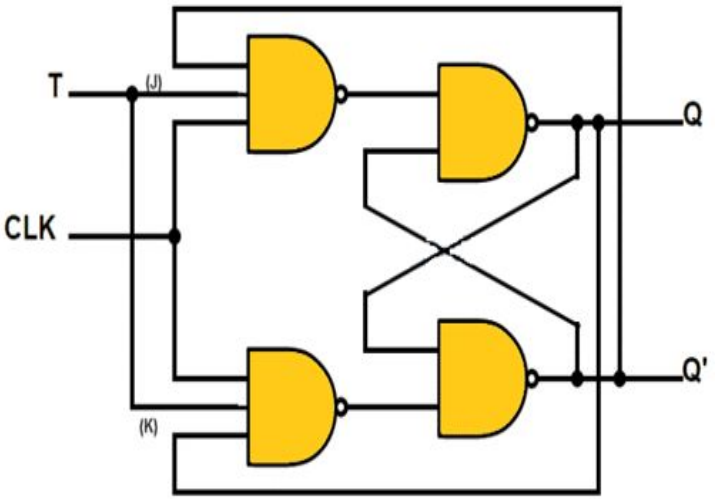
JK Flip Flop



Clk	J	K	Q	Q'	State
1	0	0	Q	Q'	No change in state
1	0	1	0	1	Resets Q to 0
1	1	0	1	0	Sets Q to 1
1	1	1	-	-	Toggles

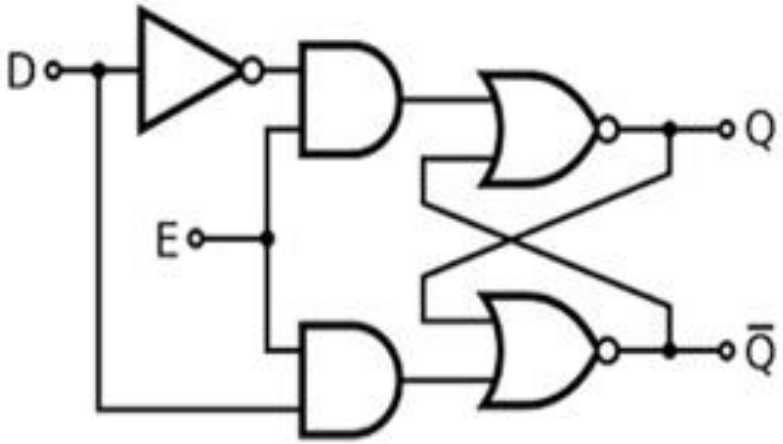


T Flip Flop



T	Q	Q'
0	0	0
1	0	1
0	1	0
1	1	0

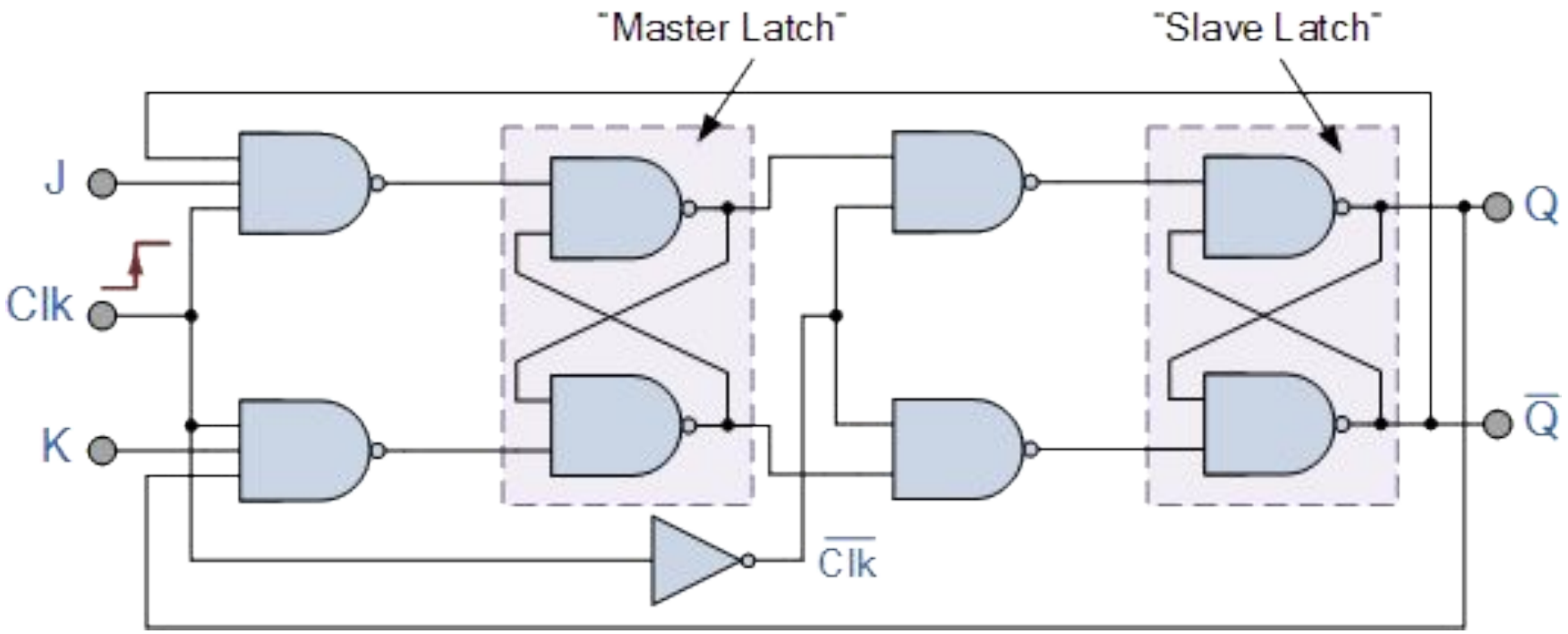
D Flip Flop



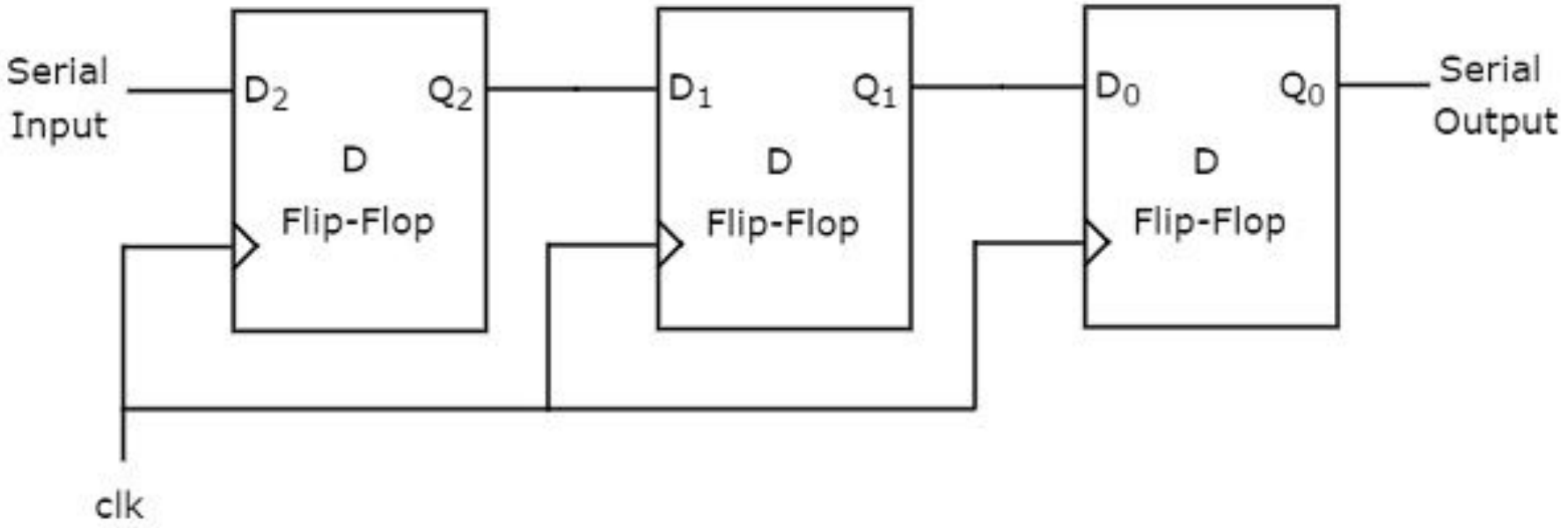
D	S	R	Q	State
	0	0	Previous State	No Change
0	0	1	0	Reset
1	1	0	1	Set
	1	1	?	Forbidden

SR & D Flip Flop TruthTable

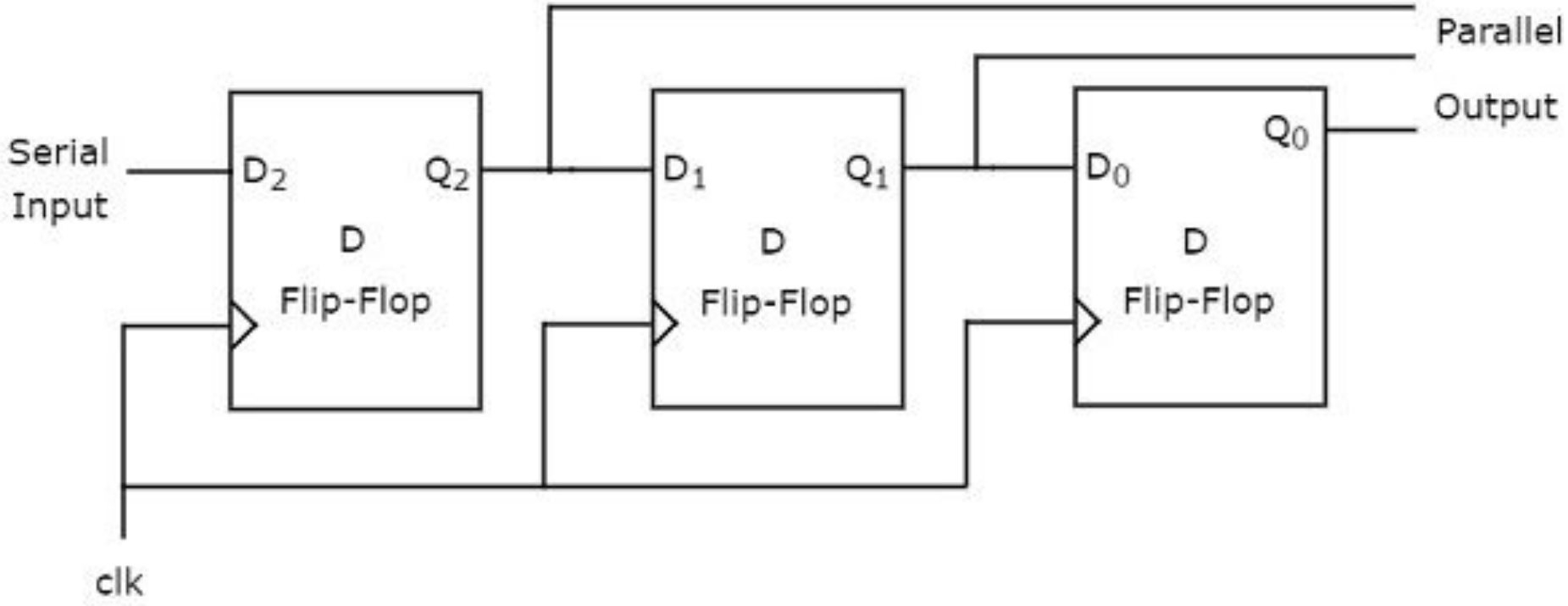
Master Slave Flip Flop



Registers


Serial
Input
D2
Q2
D
Flip-Flop
D1
Q1
D
Flip-Flop
D0
Q0
D
Flip-Flop
Serial
Output
clk

Registers


Parallel
Output
Serial
Input
D2
Q2
D
Flip-Flop
D1
Q1
D
Flip-Flop
D0
Q0
D
Flip-Flop
clk