Experiment No. **Date:**

Design of Multiplexers and Demultiplexers (Software)

Aim:

To design and verify Multiplexers (2-to-1, 4-to-1) and Demultiplexers (1-to-2, 1-to-4) using simulation.

Software required:

LTspice software

Theory:

MUX

A multiplexer is a combinational circuit that has 2^n data inputs, 'n' selection lines and a single output line. One of these data inputs will be connected to the output based on the values of the selection lines. Since there are 'n' selection lines, there will be 2^n possible combinations of zeros and ones. So, each combination will select only one data input. The multiplexer or MUX is also called a data selector.

1) 2x1 MUX

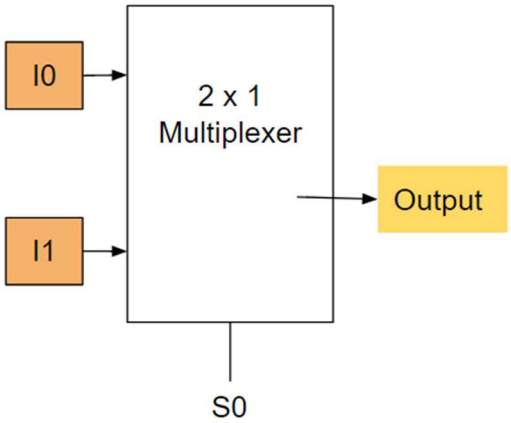


Fig.1 Block Diagram of 2x1 MUX

INPUT	OUTPUT
S0	Y
0	I0
1	I1

Table 1. Truth Table of 2x1 MUX

$$\mathbf{Y = \overline{S_0} I_0 + S_0 I_1}$$

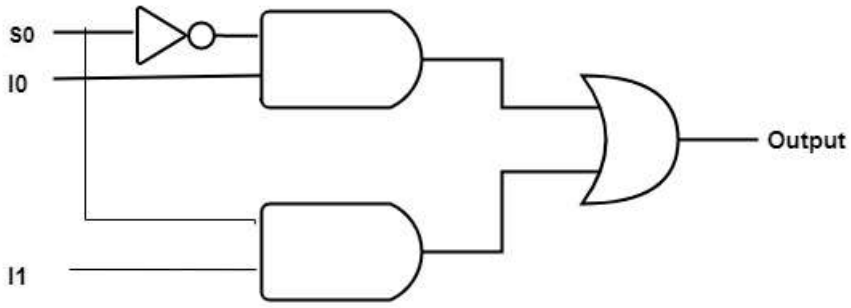


Fig.2 Logical circuit of 2x1 MUX

2) 4x1 MUX

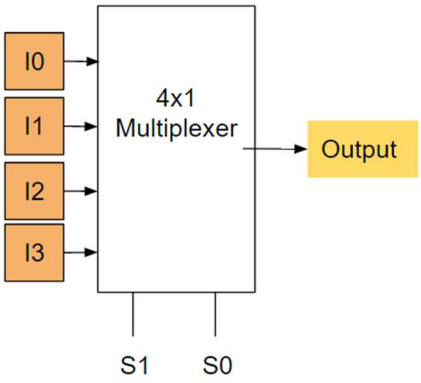


Fig.3 Block Diagram of 4x1 MUX

INPUT		OUTPUT
S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

Table 2. Truth Table of 4x1 MUX

$$\mathbf{Y = \overline{S_1}\ \overline{S_0}\ I_0 + \overline{S_1}\ S_0\ I_1 + S_1\ \overline{S_0}\ I_2 + S_1 S_0 I_3}$$

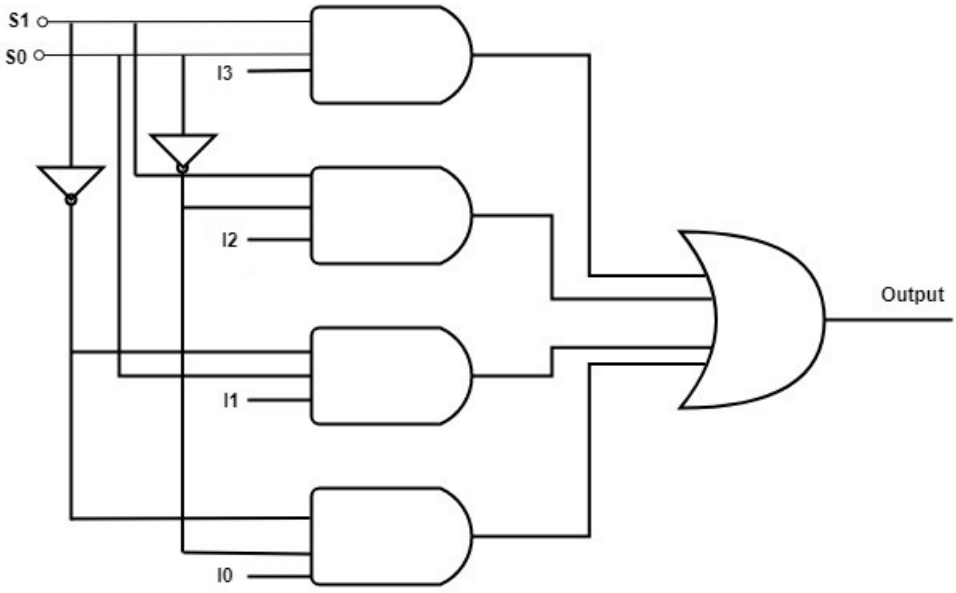
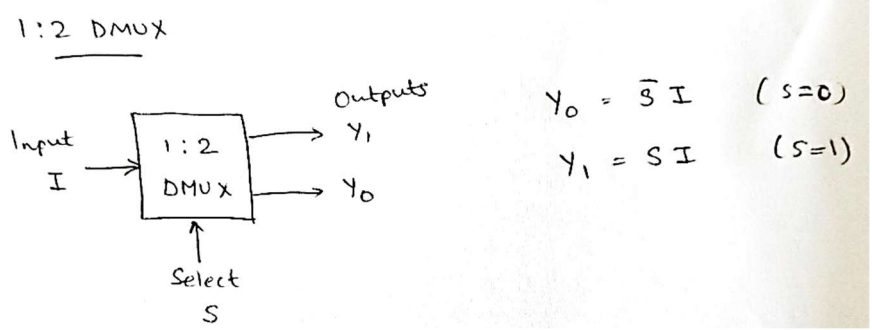


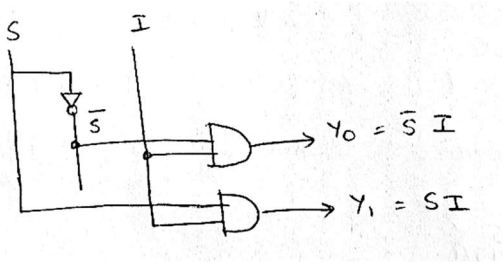
Fig.4 Logical circuit of 4x1 MUX

DMUX

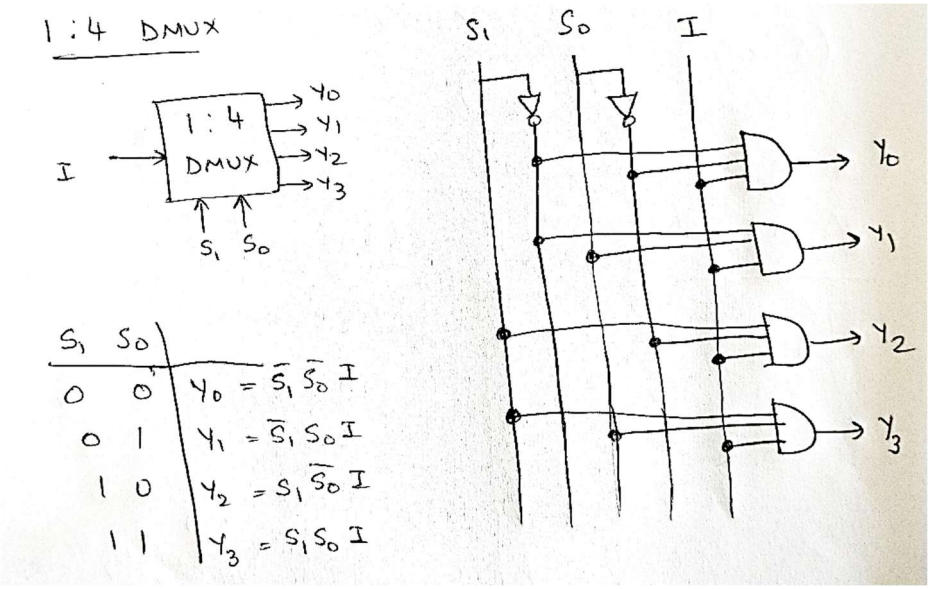
A demultiplexer, sometimes abbreviated dmux, is a circuit that has one input and more than one output. It is used when a circuit intends to send a signal to one of many devices.

3) 1:2 DMUX





4) 1:4 DMUX



Procedure:

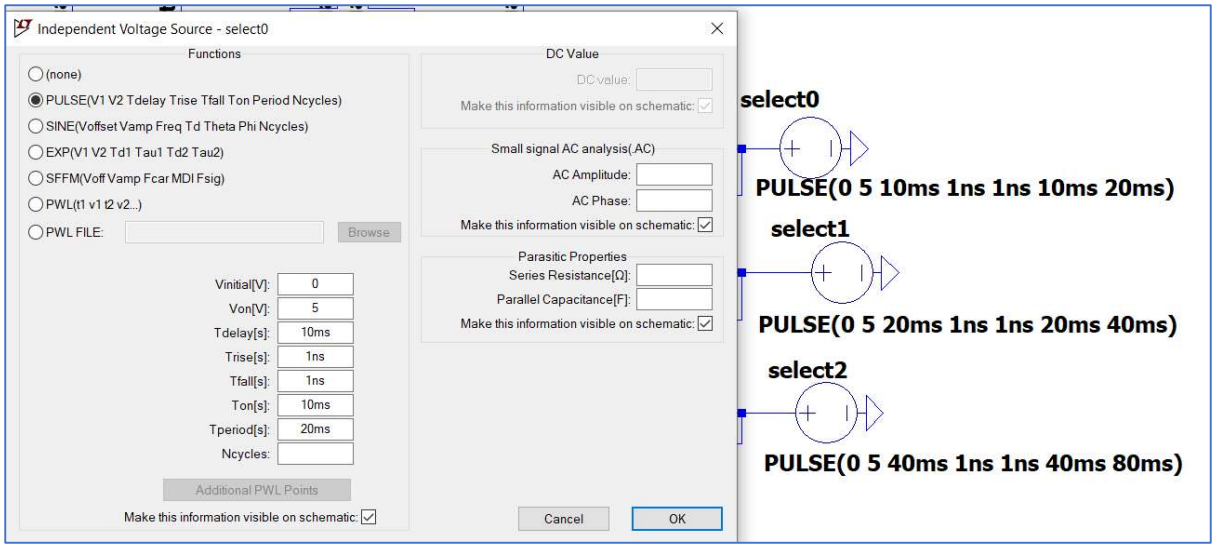
1. Launch LTSpice window.
2. Go to File and then New Schematic
3. Go to Edit and then components and choose the required components (AND, OR, Inverter) and draw the circuit diagram.
4. Set the values of the components as per the circuit diagram.

Inputs I0 – I4 (MUX) and input I (DMUX) : dc voltage source of 1V.

For select signals, Right click on the voltage sources and click Advanced option and then Select PULSE (Vinitial Von Tdelay Trise Tfall Ton Tperiod).

S0 = 0 5 10ms 1ns 1ns 10ms 20ms

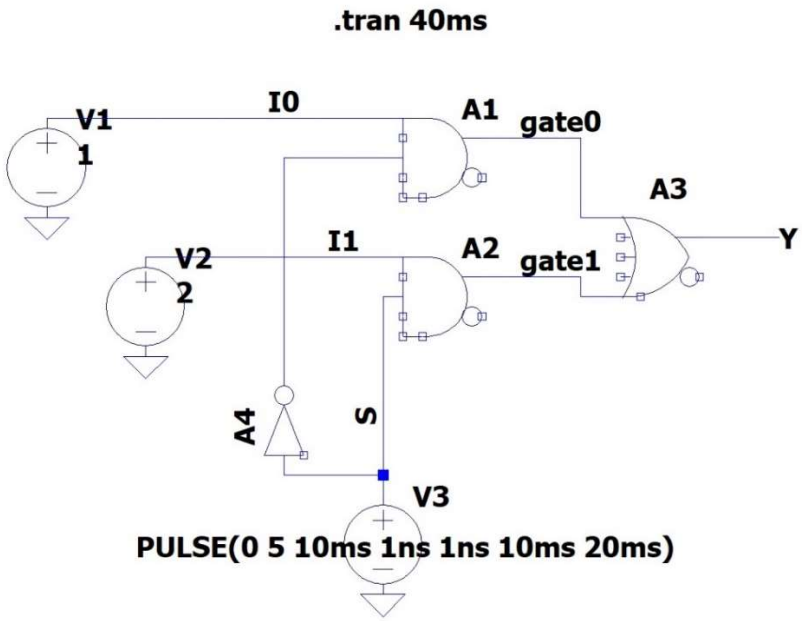
S1 = 0 5 20ms 1ns 1ns 20ms 40ms



5. Then go to simulate, edit simulation command and choose transient analysis of 40ms.
6. Then run the simulation.

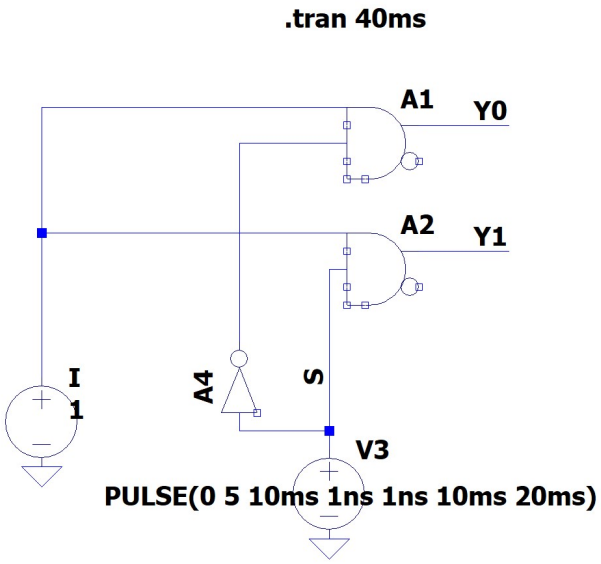
Simulation: *(Paste your simulation diagram)*

1) **LTspice diagram of 2:1 MUX**



2) **LTspice diagram of 4:1 MUX**

3) **LTspice diagram of 1:2 DMUX**

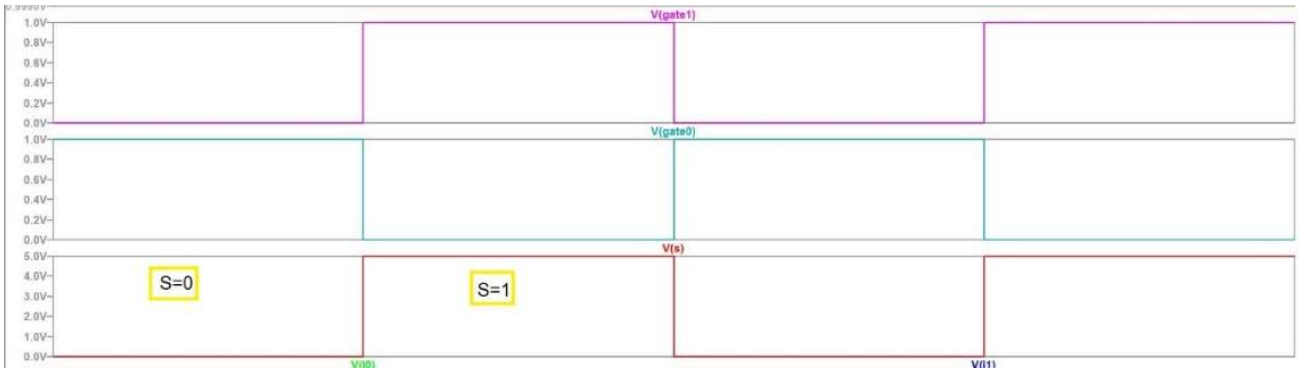


4) **LTspice diagram of 1:4 DMUX**

Simulations Results: (SELECT waveforms & AND gate output waveforms)

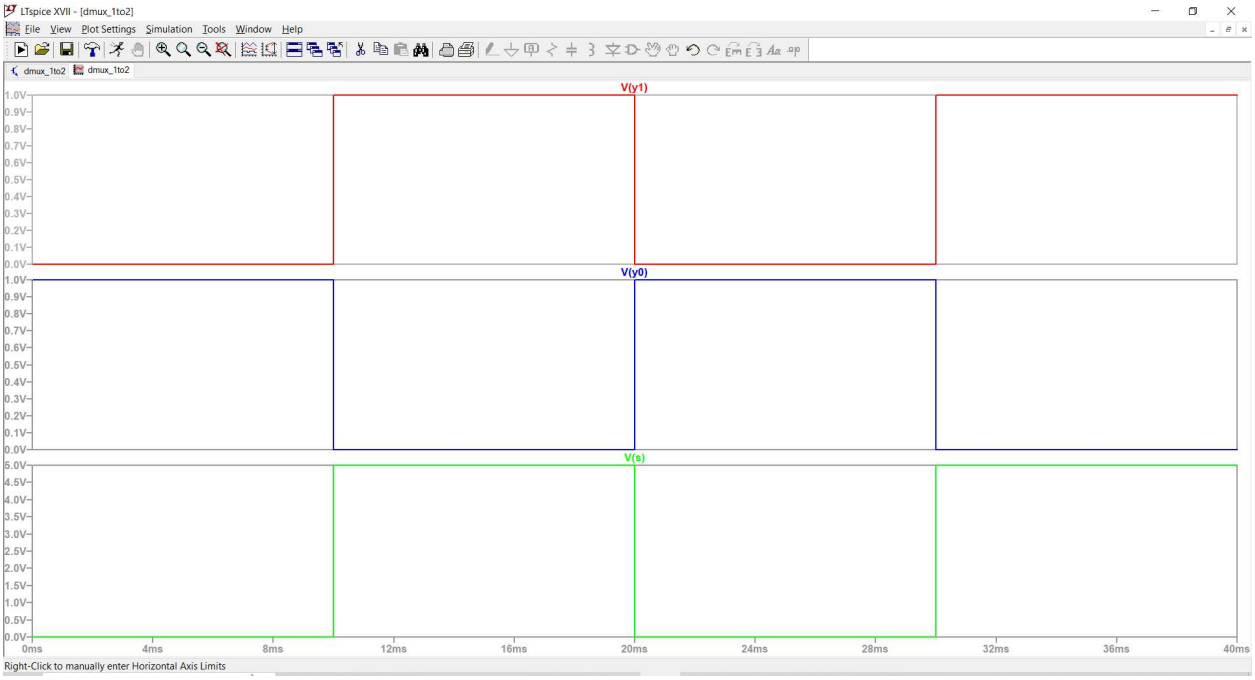
(Paste your simulation diagram for each case)

1) **2:1 MUX**



2) **4:1 MUX**

3) 1:2 DMUX



4) 1:4 DMUX

Result:

Thus, different types of Multiplexers (2-to-1, 4-to-1) and Demultiplexers (1-to-2, 1-to-4) were designed and verified using simulation.