Homework 3 Due: Nov 3rd, 2025

Please write legibly or type. Show your work to the extent possible.

1. (50 points) Answer the following questions based on the following table. All different datapaths support the following four instruction types with listed delay of each component. Assume no hazard is detected in the pipelined datapath. Please explain your answer.

Instruction class	Instruction fetch	Register read	ALU operation	Data access	Register write	Total time
Load word (`lw`)	200 ps	100 ps	200 ps	200 ps	100 ps	800 ps
Store word (`sw`)	200 ps	100 ps	200 ps	200 ps		700 ps
R-format (`add`, `sub`, `and`, `or`, `slt`)	200 ps	100 ps	200 ps		100 ps	600 ps
Branch (`beq`)	200 ps	100 ps	200 ps			500 ps

a) What should clock cycle time be for the single-cycle and pipelined datapaths? Please explain your answer.
b) What is the latency (defined as the delay from when the instruction enters the datapath until it finishes) of an R-format instruction in the single-cycle and pipelined datapaths?
c) What is the latency (defined as the delay from when the instruction enters the datapath until it finishes) of load word (lw) instruction in the single-cycle and pipelined datapaths?
d) What is the averaged throughput (defined as the number of instructions executed in 1 nanosecond in this case) of the single-cycle and pipelined datapaths? Assume the frequency of four different instruction types are the same.

2. (50 points) The following codes run on the five-stage pipelined datapath. For each piece of code, answer the following questions.

a) Without forwarding, insert the necessary number of 'nops' for the code to execute correctly.
b) With the forwarding unit available (only supports forwards MEM-> EX and WB->EX), show how the code will execute. Mention the data that's forwarded between the stages. Use 'nops' only when necessary.

```
Code 1:
sub t1, t2, t3
add t1, t4, t5
or t4, t2, t6

Code 2:
and t2, t5, t1
sub t3, t2, t0
nor t7, t1, t5

Code 3:
and t2, t5, t1
sub t3, t2, t0
nor t7, t2, t1

Code 4:
lw t1, 22(t0)
and t2, t1, t3

Code 5:
lw t1, 22(t0)
sub t6, t0, t2
xor t3, t1, t5
```