Homework 2 Due: Sep 26th , 2025

Please write legibly or type. Show your work to the extent possible.

1. **(40 points)** Assume we have a 64KB 8-way associative cache, with 32B blocks

a) What is the set number we are accessing for virtual address 0x08B56A?

b) What is the set number and the tag if the for virtual access in part a if cache is 2-way associative?

c) Repeat b for direct mapped cache.

d) What is the effect – between part a to part c – (i.e. when reducing associativity) on following metrics: miss rate, and hit time.

2. **(30 points)** Assume page table and a 64-bit processor with 4KB pages. The page table root is at address 0xFF2400, and each page table entry (PTE) is 8 bytes.

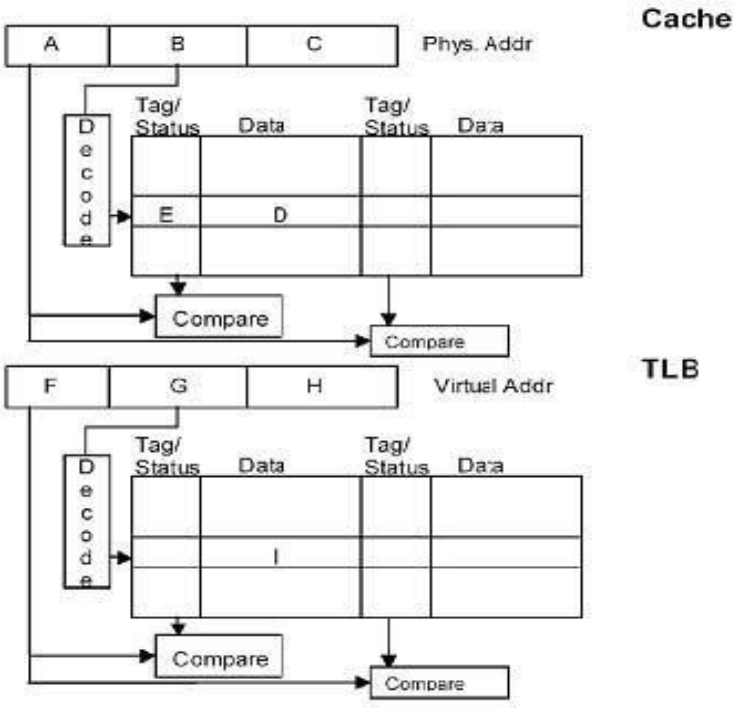
   a) what is the size of hypothetical linear page table

   b) If four-levels page table is used, what are the indices of the corresponding PGD, PUD, PMD and PTE when accessing 0x0542354C1508?

3. **(30 points)** Consider a memory system with the following parameters:

- Translation Lookaside Buffer has 512 entries and is 2-way set associative.
- 64Kbyte L1 Data Cache has 128 byte lines and is also 2-way set associative.
- Virtual addresses are 64-bits and physical addresses are 32 bits.
- 4KB page size

Below are diagrams of the cache and TLB. Please fill in the appropriate information (Name and size -in bits- of each field) in the table that follows the diagrams, assume 2 status bits :



L1 Cache		TLB	
A =	bits	F =	Bits
B =	bits	G =	Bits
C =	bits	H =	Bits
D =	bits	I =	Bits
E =	bits		