Q1 [15 Points]. In a UART communication system, the receiver is configured to oversample at 16x the baud rate, and the communication happens at a baud rate of 9600 bps. The UART transmits 8 data bits, 1 start bit, 1 stop bit, and no parity.

(Part 1) What is the minimum required sampling frequency of the UART receiver.

(Part 2) Calculate how much time it will take to transmit a single byte (including the start and stop bits).

(Part 3) Suppose the transmitting UART has a clock that is running 2% faster than the receiving UART. Given that the receiver oversamples each bit 16 times, how many incorrect samples could occur due to this clock mismatch over the course of 10 bits (1 start bit, 8 data bits, and 1 stop bit)? Would the receiver still be able to correctly sample the bits?

Q2 [25 Points]. A system requires UART communication at a baud rate of 115200 bps, and you need to configure the UART for 8 data bits, no parity, 1 stop bit, and SMCLK as the clock source. The SMCLK frequency is set to 4 MHz.

(Part 1) What would be the hexadecimal value of UCAxCTLW0, UCAxMCTLW, and UCAxBRW for this configuration if oversampling is disabled.

(Part 2) What would be the hexadecimal value of UCAxCTLW0, UCAxMCTLW, and UCAxBRW for this configuration if oversampling (with factor of 16x) is enabled.

Q3 [10 Points]. In an embedded system, the system clock (SMCLK) is running at 8 MHz, and the UART baud rate is determined by a clock divider stored in the UCAxBRW register. The oversampling mode can either be enabled or disabled. The UART supports a 16-bit divider, meaning the value of UCAxBRW can range from 0x0001 to 0xFFFF. The oversampling mode (if enabled) divides the effective clock frequency by 16 before applying the divider. In this system,

(Part 1) Calculate the maximum baud rate achievable when oversampling is disabled.

(Part 2) Calculate the minimum baud rate achievable when oversampling is enabled

Q4 [30 Points]. An embedded microcontroller is communicating with a sensor using UART (8 data bits, no parity, 1 stop bit). The microcontroller's UART is configured to transmit at a baud rate of 115200 bps, derived from its 16 MHz system clock. However, due to a manufacturing defect, the microcontroller's clock is actually running at 15.6 MHz. The sensor's UART operates at an accurate baud rate of 115200 bps.

(Part 1) Calculate the actual baud rate at which the microcontroller is transmitting data due to the defective clock.

(Part 2) Determine the percentage difference between the microcontroller's actual baud rate and the sensor's baud rate.

(Part 3) UART communication can tolerate up to a ±2% difference in baud rates between the transmitter and receiver for reliable communication. Given the calculated baud rate difference, will the microcontroller be able to communicate reliably with the sensor?

(Part 4) Considering the cumulative timing error, after how many bits will the timing error amount to half a bit period, potentially causing a framing error?

Q5 [20 Points]. You are designing an embedded system that communicates over an I2C bus at 400 kHz (Fast Mode). The microcontroller you are using has a peripheral clock frequency of 8 MHz for its I2C module.

The I2C peripheral requires you to configure the I2C clock speed by setting a prescaler and a divider to generate the desired clock frequency. The formula for calculating the I2C clock is given by:

$$f_{SCL} = \frac{f_{PCLK}}{2 \times (PRESCALER + 1) \times (DIVIDER + 1)}$$

Where f_{SCL} is the desired I2C clock frequency (in Hz), f_{PCLK} is the peripheral clock frequency (in Hz), PRESCALER is the value of the prescaler (0 to 15), and DIVIDER is the value of the divider (0 to 255).

(Part 1) Calculate the values of PRESCALER and DIVIDER to achieve an I2C clock frequency of 400 kHz. You are required to select the smallest possible values for both PRESCALER and DIVIDER.

(Part 2) What would the resulting actual I2C clock frequency be with your selected configuration, and how much error (%) does this configuration introduce compared to the desired 400 kHz frequency?

Homework Policies

(I) Homework 3 is due by 11:59PM on Thursday 10/17/2025. Late submissions will be penalized unless prior arrangements have been made with the instructor. The standard late penalty is a 10% deduction for each day late. Assignments more than one week late will not be accepted unless there's an exception (with prior communication with the instructor).

(II) All homework must be submitted electronically (PDF) via Webcourses. Ensure that your file is properly named (e.g., "Lastname_Firstname_EEL4742_HW3.pdf"). If you encounter technical issues during submission, you must notify the instructor before the due date by email.

(III) All submitted work must be your own. Plagiarism, including copying from other students, online sources, or using GPTs, is strictly prohibited. Any instances of plagiarism will result in a zero for the assignment.

(IV) If you believe there has been a grading error, you may request a regrade within one week of receiving your graded assignment.

(V) Remember to show your work for full credit. If you provide only the final answer, you willl earn partial credit.

(VI) For certain assignments, you may be required to attend a check-off meeting (in-person or online) with the instructor after submission. During this meeting, you will discuss your solution, explain your approach, and answer questions about your work. Failure to attend a required check-off meeting, or inability to explain your solution, may result in a reduction of your grade for that assignment.