Q1 [25 Points]. In an embedded system, you are configuring a UART module to communicate with a custom microcontroller. The assumptions are

- **System Clock**: 14 MHz
- **Desired Baud Rate**: 115200 baud
- **Acceptable Baud Rate Error Rate**: $\pm 2\%$
- **Available Oversampling Rates**: 16x, 8x, 4x, and no oversampling
- **Baud Rate Register Configuration**:
  - **Integer Baud Rate Register (IBRD)**: 12-bit integer part
  - **Fractional Baud Rate Register (FBRD)**: 4-bit fractional part
  - Rounding to the nearest integer for both IBRD and FBRD values will be used.

[Part A][6/25]: Based on the above assumptions, calculate the integer (IBRD) and fractional (FBRD) baud rate register values required to achieve a baud rate of 115200 with 16x oversampling.

[Part B][7/25]: Using the values from Part 1, calculate the actual baud rate generated and determine the resulting error percentage compared to the desired baud rate.

[Part C][12/25]: Based on the error rate, what oversampling ratio is the best configuration for this system?

Q2 [20 Points]. For the I2C protocol:

- The slave address is `0x2BA`.
- The internal register address is `0x1010`.
- The data to be read is `0xABCDEF`.

[Part A][12/20]: If the I2C is operating at the maximum frequency for fast mode plus, how long will it take for the master to read this data from the slave over the I2C channel?

[Part B][8/20]: Is the time calculated in Part A the minimum possible delay? If not, how could this delay be reduced without changing any protocol configurations?

Q3 [30 Points]. In a 6-bit SAR ADC with a capacitive network consisting of $C, \frac{C}{3}, \frac{C}{9}, \frac{C}{27}, \frac{C}{81}, \frac{C}{243}$, the reference voltage V_{ref} is 5V (range of voltage is 0 to 5V).

[Part A][17/30]: Given an input voltage $V_{\text{in}} = 3V$, determine the digital output of the ADC using the SAR approach, showing how each bit is set (0 or 1) during the SAR process.

[Part B][7/30]: After the conversion is complete, calculate the resolution of this 6-bit ADC in terms of voltage per step.

[Part C][6/30]: Based on the resolution calculated in Part B, is the voltage step size consistent (uniform increase) across all steps of the ADC conversion process? Explain your response with an example.

Q4 [25 Points]. In an SPI daisy chain configuration, three devices (Device A $\rightarrow$ Device B $\rightarrow$ Device C $\rightarrow$ Device A ...) are connected in series to a microcontroller. Each device has an 8-bit shift register, and the SPI operates at a clock speed of 1 MHz in Mode 0 (CKPL = 0, CKPH = 0). Initially, the registers in each device hold the following data:

- **Device A**: `0x3C`
- **Device B**: `0xA7`
- **Device C**: `0xE1`

The microcontroller starts sending a new 8-bit data frame of `0x5D` to Device A.

[Part A][10/25]: After 5 clock pulses, what would be the exact data in each device's register (the microcontroller, Device A, Device B, and Device C)?

[Part B][9/25]: After 11 clock pulses, what would be the exact data in each device's register (the microcontroller, Device A, Device B, and Device C)?

[Part C][6/25]: Calculate the total delay from when the microcontroller sends the first bit of `0x5D` until `0x5D` fully appears in Device C's register.