Embedded Systems: Homework #2

Yousef Alaa Awad

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1

Given: For Timer_A, answer the following questions.

A) Timer A is using a 100 KHz (100,000 Hz) clock signal. What is the timer's period (in seconds) if the continuous mode is used? Give the answer for all values of ID (Input Divider).

B) Timer A is using a 100 KHz (100,000 Hz) clock signal. We're aiming at a timer period of 0.1 seconds using the up mode. Find suitable values of TACCR0 and ID (Input Divider). *Give all the possible solutions.*

2

Given: For Timer_A, answer the following questions.

A) Timer A is using ACLK configured to a 32 KHz (32,768 Hz) crystal. What is the timer period if the continuous mode is used? Give the answer for all the values of ID (Input Divider).

B) Timer A is using an 5 MHz (5,000,000 Hz) clock signal. Can we configure the timer to (directly) generate a delay of 0.5 seconds? Show your analysis.

3

Given: For manual delay insertion using loops, answer the following questions.

A) How many bits is an integer (int) n the C language?

B) A programmer wrote a software delay loop that counts the variable (unsigned int counter) from 0 up to 45,000 to create a small delay. If the user wishes to double the delay, can they simply increase the upperbound to 90,000? If not, explain why?

C) If your answer to (Part B) is *No*, what alternative solution can be used for this specific scenario. *Give all the possible solutions.*

4

Given: Timer A is in up mode with a clock source of ACLK (32.768 kHz) and a clock divider of 8. The compare register (CCR0) is set to 500. Both TAIE and CCIE for CCR0 are enabled. TAIFG has a priority of 2, while the CCR0 (CCIFG) interrupt has a priority of 1. Answer the following questions.

A) Calculate how often the TAIFG and CCIFG interrupts will be triggered (actual time).

B) If both interrupts occur at the same time, which interrupt will be serviced first? Explain why.

C) If the clock divider is changed to 32 while keeping all other settings the same, how will the interrupt timing change? Recalculate the new interrupt period for TAIFG and CCIFG.

5

Given: Timer_A is in continuous mode with SMCLK (1 MHz) as the clock source and no clock division. The compare register CCR1 is set to 30,000, and both TAIE and CCIE are enabled. The CPU is put into low-power mode (LPM3). Answer the following questions.

A) Explain what will happen when TAR reaches CCR1 and then overflows.

B) If you want the CPU to wake up and handle both the CCR1 compare interrupt and the overflow interrupt, how would you modify the system configuration to achieve this?

C) Calculate how long the CPU will stay in low-power mode before it wakes up to handle the CCR1 interrupt if you reconfigure the system correctly.