**Q1 [20 Points]**. For I2C transfer protocol:

**(Part 1)** If the 3 most significant bits are reserved for special use, when should the I2C addressing be extended from 7-bit to 10-bit addressing?

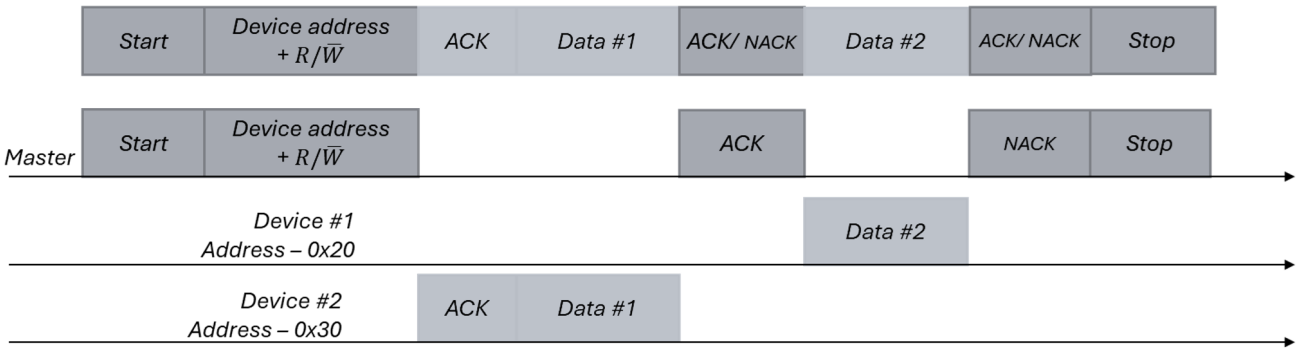
**(Part 2)** If 10-bit addressing is used, draw the timing diagram of the I2C data transfer when the master sends 2 bytes of data to a slave device.

**(Part 3)** Using the timing diagram from Part 2, and assuming the I2C protocol is operating in fast mode, calculate the duration of the data transfer in seconds.

**Q2 [20 Points]**. For the following I2C timing diagram,

**(Part 1)** What function does this timing diagram illustrate?

**(Part 2)** Are there any issues present in this timing diagram? If yes, what solutions could address them?




**Q3 [30 Points]**. A 12/10-bit Analog-to-Digital Converter (ADC) used for the temperature sensor with the range from 0° C to 100° C. The ADC has a reference voltage of 3.3V, and the sensor produces a linear output from 0V (0° C) to 3.3V (100° C).

**(Part 1)** Calculate the quantization step size for the 10-bit and 12-bit ADC.

**(Part 2)** Determine the maximum quantization error for both the 12-bit and 10-bit ADC configurations.

**(Part 3)** If the ADC is used to measure a temperature of 37℃, calculate the corresponding digital value from the ADC for both the 12-bit and 10-bit resolutions.

**(Part 4)** Given the digital values, calculate the actual voltage that the ADC would output back (after the conversion) for each resolution.

**Q4 [30 Points]**. You are given a 4-bit Successive Approximation Register (SAR) ADC that uses a capacitive model for conversion. The reference voltage ($V_{ref}$) is 3.3V, and the input voltage ($V_{in}$) is 2.0V.

The capactive model uses a non-ideal array of capacitors with the following values instead of perfect binary weighting:

- $C_3$ = 8C (Ideally should be 8C)
- $C_2$ = 3.5C (Ideally should be 4C)
- $C_1$ = 2.1C (Ideally should be 2C)
- $C_0$ = 1.4C (Ideally should be C)

**(Part 1)** Determine the digital output of the SAR-ADC after the conversion process, given that $V_{in}$ = 2.0V. List the decision for each bit (1 or 0) and the corresponding comparator voltage at each step.

**(Part 2)** Assuming that ideal capacitance values are in place, re-calculate the digital output of the SAR-ADC after the conversion process.

**(Part 3)** Compare the digital outputs obtained from Part 1 and Part 2. Calculate the error in terms of the difference in the resulting digital values between the non-ideal and ideal cases.

**Homework Policies**

(I) Homework 4 is due by 11:59PM on Sunday 11/02/2025. Late submissions WILL NOT BE ACCEPTED, as the solution will be released immediately after the deadline to aid in your preparation for Midterm 2.

(II) All homework must be submitted electronically (PDF) via Webcourses. Ensure that your file is properly named (e.g., "Lastname_Firstname_EEL4742_HW4.pdf"). If you encounter technical issues during submission, you must notify the instructor before the due date by email.

(III) All submitted work must be your own. Plagiarism, including copying from other students, online sources, or using GPTs, is strictly prohibited. Any instances of plagiarism will result in a zero for the assignment.

(IV) If you believe there has been a grading error, you may request a regrade within one week of receiving your graded assignment.

(V) For certain assignments, you may be required to attend a check-off meeting (in-person or online) with the instructor after submission. During this meeting, you will discuss your solution, explain your approach, and answer questions about your work. Failure to attend a required check-off meeting, or inability to explain your solution, may result in a reduction of your grade for that assignment.