A1

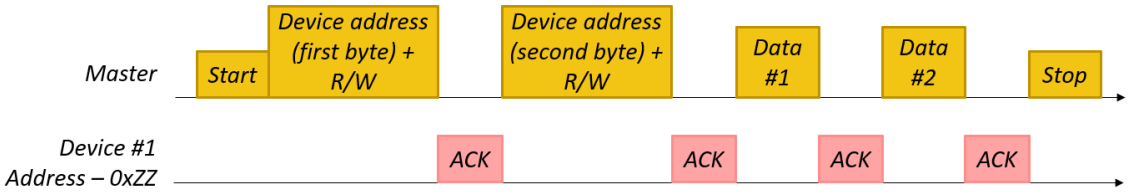
(Part a) When 3 most significant bits are reserved for special use (let say ”111”), then other 4 bits can be used for addressing. Meaning that:

$$\text{\# of devices to have unique addresses} = 2^4 = 16$$

IF the system requires to be connected to more than 16 devices, and IF the chip select or/and power-gating is not available, then addressing should be updated to 10 bits. With 10 bits for addressing, while 3 bits are reserved:

$$\text{\# of devices to have unique addresses} = 2^7 = 128 \text{ (Up to 128 devices can be supported.)}$$

(Part b) The following shows the timing diagram of sending two bytes of data when 10-bit addressing is used.



(Part c) When we are in fast mode, the frequency will be 400kHZ. For the timing diagram shown in (part b), the following are the total clock cycles required for this transmission:

- Start (from the master) = 1 clock cycle
- First address byte (from the master) = 8 clock cycles
- ACK (from the slave) = 1 clock cycle
- Second address byte (from the master) = 8 clock cycles
- ACK (from the slave) = 1 clock cycle
- First byte of the data (from the master) = 8 clock cycles
- ACK (from the slave) = 1 clock cycle
- Second byte of the data (from the master) = 8 clock cycles
- ACK (from the slave) = 1 clock cycle
- Stop (from the master) = 1 clock cycle

$$\text{\# of clock cycles for the whole transmission} = 38$$

$$\text{Time required for the transmission} = 38 \times \frac{1}{400kHz} = 95\mu s$$

A2

(Part a) The master starts communicating with device #2 located in physical address 0x30. The communication is a ”READ”, meaning that the master requested data from device #2. Device #2 sends the first data to the master, and the master returns ”ACK”, meaning that the master looks for more data from device #2. Then, after ”ACK”, this time device #1 starts to send data to the master. The master sends ”NACK” to ask for no more data and ”STOP” the communication.

(Part b) The issue with this diagram is that the data transfer can only happen between the master and one slave at a time. To resolve this, and in case the master needs to deal with device #1 as well, after reading from device #2, the master should send a NACK to signal that it has finished reading from that device. Following this, the master should initiate another start condition and send the address for device #1. Device #1 would then respond with an ACK and transmit data #2, to which the master would reply with a NACK.

A3

(Part a) To calculate the quantization step size, we need to divide the analog value range by the number of bits in digital version:

$$\text{quantization step size for 10-bit} = \frac{(3.3V - 0V)}{2^{10}} = 3.223mV$$

$$\text{quantization step size for 12-bit} = \frac{(3.3V - 0V)}{2^{12}} = 0.806mV$$

(Part b) To calculate the quantization error, we determine the maximum possible difference between an analog value and its corresponding digital representation. Since we have discrete steps, the analog value within one step will define the error.

For example, in a 10-bit ADC, the step size is $3.233mV$. So, from 0000000001 to 0000000010, the analog voltage will change from $3.233mV$ to $6.466mV$. This means that all analog values within this range are missed. The worst-case scenario is when the analog value lies in the middle of this range. So,

$$\text{quantization error for 10-bit} = \frac{(3.3V - 0V)}{2^{10} \times 2} = 1.611mV$$

$$\text{quantization error for 12-bit} = \frac{(3.3V - 0V)}{2^{12} \times 2} = 0.403mV$$

(Part c) We need first to convert the temperature to the voltage range (0:100 to 0:3.3). Then, we need to define each bit weight (from the MSb to LSb), and then by setting them 1/0, we should determine each bit of the digital value.

$$\frac{37}{100} \times 3.3 = 1.22V$$

Let's start with ADC-10: (The final digital value (DV): $a_9, a_8, a_7, ...a_2, a_1, a_0$)

$$a_9 = 1 \rightarrow \text{DV} = 0.5 \times 3.3 = 1.65V > 1.22V \quad (\text{we can't keep it. } a_9 \text{ should be 0.})$$

$$a_8 = 1 \rightarrow \text{DV} = 0.25 \times 3.3 = 0.825V < 1.22V \quad (\text{we should keep it. } a_8 \text{ should be 1.})$$

$$a_7 = 1 \rightarrow \text{DV} = 0.125 \times 3.3 = 0.4125V((+0.825V)) = 1.2375V > 1.22V \quad (\text{we can't keep it. } a_7 \text{ should be 0.})$$

$$a_6 = 1 \rightarrow \text{DV} = 0.0625 \times 3.3 = 0.20625V((+0.825V)) = 1.03125V < 1.22V \quad (\text{we should keep it. } a_6 \text{ should be 1.})$$

We should continue this flow to see the value of each a_i. The final DV for 10-bit is "01 0111 1010" (378).

Similarly, we can do the same for 12-bit ADC. The final DV for 12-bit is "0101 1110 1010" (1514).

(Part d) To calculate the actual voltage that the ADC would output back, we just require to multiply the DVs (part c) by the the quantization step size:

$$\text{For the 10-bit ADC} \quad \rightarrow 378 \times 3.223mV = 1.2182V$$

$$\text{For the 12-bit ADC} \quad \rightarrow 1514 \times 0.806mV = 1.2202V$$

A4

(Part a) For the total capacitance of the given circuit:

$$C_{\text{total}} = 8C + 3.5C + 2.1C + 1.4C = 15C$$

Then, we use the following to calculate the value of each bit of the digital value:

$$\text{For bit 3:} \rightarrow V_{\text{comp}} = \frac{8C \cdot 3.3V}{15C} = 1.76V \quad \text{Since } 2.0V > 1.76V \text{ bit 3 = 1.}$$

$$\text{For bit 2:} \rightarrow V_{\text{comp}} = 1.76V + \frac{3.5C \cdot 3.3V}{15C} = 2.51V \quad \text{Since } 2.0V < 2.51V \text{ bit 2 = 0.}$$

$$\text{For bit 1:} \rightarrow V_{\text{comp}} = 1.76V + \frac{2.1C \cdot 3.3V}{15C} = 2.22V \quad \text{Since } 2.0V < 2.22V \text{ bit 1 = 0.}$$

$$\text{For bit 1:} \rightarrow V_{\text{comp}} = 1.76V + \frac{1.4C \cdot 3.3V}{15C} = 2.068V \quad \text{Since } 2.0V < 2.068V \text{ bit 0 = 0.}$$

Non-Ideal Digital Output: 1000

(Part b) For the total capacitance of the given circuit (in the ideal scenario):

$$C_{\text{total}} = 8C + 4C + 2C + 1C = 15C$$

Then, we use the following to calculate the value of each bit of the digital value:

$$\text{For bit 3:} \quad \rightarrow \quad V_{\text{comp}} = \frac{8C \cdot 3.3V}{15C} = 1.76V \qquad \text{Since } \ 2.0V > 1.76V \ \text{ bit 3 = 1.}$$

$$\text{For bit 2:} \quad \rightarrow \quad V_{\text{comp}} = 1.76V + \frac{4C \cdot 3.3V}{15C} = 2.64V \qquad \text{Since } \ 2.0V < 2.64V \ \text{ bit 2 = 0.}$$

$$\text{For bit 1:} \quad \rightarrow \quad V_{\text{comp}} = 1.76V + \frac{2C \cdot 3.3V}{15C} = 2.20V \qquad \text{Since } \ 2.0V < 2.20V \ \text{ bit 1 = 0.}$$

$$\text{For bit 1:} \quad \rightarrow \quad V_{\text{comp}} = 1.76V + \frac{1C \cdot 3.3V}{15C} = 1.98V \qquad \text{Since } \ 2.0V > 2.068V \ \text{ bit 0 = 1.}$$

Ideal Digital Output: 1001

(Part c) While the non-ideal digital value is 1000 (part a), the ideal digital value is 1001 (part b), showing that the error is 1001 - 1000 = 0001 ($1 \times 3.3V/16 \approx 0.20625V$ error).