**Q1 [25 Points]**. The MSP430 has an 8-bit register `P1OUT`. Assume:

- `BIT0` = Red LED (active-high → ON if bit=1)
- `BIT7` = Green LED (active-low → ON if bit=0)

**[Part A][15/25]:** You want the **final state**: (i) Red LED ON; (ii) Green LED OFF; (iii) All other bits unchanged. For each candidate operation below, **fill in the table**: does it *always* achieve the target, *sometimes* (depends on previous value), or *never*? Briefly justify case x | x = (right most digit of your id) %5.

| **Expression** | **Always / Sometimes / Never** |
|---|---|
| (case 0) `P1OUT = P1OUT \| BIT0` | |
| (case 1) `P1OUT = P1OUT & ~BIT7` | |
| (case 2) `P1OUT = (P1OUT \| BIT0) & ~BIT7` | |
| (case 3) `P1OUT = (P1OUT & ~BIT7) \| BIT0` | |
| (case 4) `P1OUT = P1OUT ^ (BIT0 \| BIT7)` | |

**[Part B][10/25]:** Now let's assume we want to clear both `BIT1` and `BIT3` of `P1OUT` using the following code:

```
P1OUT = P1OUT & ~BIT1 | ~BIT3
```

Is it the correct code? If not, explain why and write the correct code? If so, explain why?

**Q2 [20 Points]**. The MSP430's Timer_A (16-bit) is clocked from **SMCLK = 1 MHz**. You configure it in **Up Mode** with CCR0 $= 49{,}999$.

- In Up Mode, Timer_A counts from 0 $\rightarrow$ CCR0, then resets to 0.
- The interrupt flag `CCIFG` is set each time CCR0 is reached.

**[Part A][10/20]:** What is the period (in ms) of the CCR0 interrupt? Show your calculation.

**[Part B][5/20]:** How many interrupts occur in exactly 1 second?

**[Part C][5/20]:** Suppose instead you want exactly a **10 Hz** interrupt rate from the same 1 MHz SMCLK, using Up Mode. What CCR0 value must you load?

**Q3 [25 Points]**. An MSP430 controls a small coffee machine using Timer_A interrupts. ACLK = 32.768 kHz, Timer_A is 16-bit in Up mode. The FSM has four states with the following descriptions:

- **IDLE**: waiting for button press
- **HEAT**: warm up heater — 20s
- **BREW**: pump water — 45s
- **DONE**: blink LED at 1 Hz for 5s, then return to IDLE

**[Part A][5/25]:** Draw the FSM with all states, transitions, and timing.
**[Part B][10/25]:** Using ACLK = 32.768 kHz, and assuming that divider can be 1, 4, 16, and 64, select a suitable timer configuration and CCR0 so that all state durations can be achieved (calculate the tick period and the number of ticks for each state).
**[Part C][10/25]:** In the **DONE** state, the LED must blink at 1 Hz (50% duty). Explain how you can achieve this with Timer_A.

**Q4 [30 Points]**. For 14-segment LCD provided in MSP430, answer the following questions:

**[Part A][10/30]:** The LCD is driven using the 32.768 KHz ACLK. The LCD is configured with a 4-mux, and the required segment frequency is 1 Hz. What should be the values of the divider (`LCDDIVx`) and pre-scaler (`LCDPREx`) settings?

**[Part B][20/30]:** Configure the MSP430 to display "your UCF ID most right 6 digits" on the LCD. Write the values that should be loaded into the LCDMx registers to represent the segments for these digits.

| LCDMEM | Port Pin | FR6989 Pin | LCD Pin | COM3 | COM2 | COM1 | COM0 | Port Pin | FR6989 Pin | LCD Pin | COM3 | COM2 | COM1 | COM0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **LCDM22** | P2.4 | S43 | | | | | | P2.5 | S42 | | | | | |
| **LCDM21** | P2.6 | S41 | | | | | | P2.7 | S40 | | | | | |
| **LCDM20** | P10.2 | S39 | 16 | A4H | A4J | A4K | A4P | P5.0 | S38 | 15 | A4Q | A4COL | A4N | A4DP |
| **LCDM19** | P5.1 | S37 | 14 | A4A | A4B | A4C | A4D | P5.2 | S36 | 13 | A4R | A4F | A4G | A4M |
| **LCDM18** | P5.3 | S35 | 34 | B5 | B3 | B1 | [] | P3.0 | S34 | | | | | |
| **LCDM17** | P3.1 | S33 | | | | | | P3.2 | S32 | | | | | |
| **LCDM16** | P6.7 | S31 | 20 | A5H | A5J | A5K | A5P | P7.5 | S30 | 19 | A5Q | DEG | A5N | A5DP |
| **LCDM15** | P7.6 | S29 | 18 | A5A | A5B | A5C | A5D | P10.1 | S28 | 17 | A5E | A5F | A5G | A5M |
| **LCDM14** | P7.7 | S27 | 33 | B6 | B4 | B2 | BATT | P3.3 | S26 | | | | | |
| **LCDM13** | P3.4 | S25 | | | | | | P3.5 | S24 | | | | | |
| **LCDM12** | P3.6 | S23 | | | | | | P3.7 | S22 | | | | | |
| **LCDM11** | P8.0 | S21 | 4 | A1H | A1J | A1K | A1P | P8.1 | S20 | 3 | A1Q | NEG | A1N | A1DP |
| **LCDM10** | P8.2 | S19 | 2 | A1A | A1B | A1C | A1D | P8.3 | S18 | 1 | A1E | A1F | A1G | A1M |
| **LCDM9** | P7.0 | S17 | 38 | A6H | A6J | A6K | A6P | P7.1 | S16 | 37 | A6Q | TX | A6N | RX |
| **LCDM8** | P7.2 | S15 | 36 | A6A | A6B | A6C | A6D | P7.3 | S14 | 35 | A6E | A6F | A6G | A6M |
| **LCDM7** | P7.4 | S13 | 8 | A2H | A2J | A2K | A2P | P5.4 | S12 | 7 | A2Q | A2COL | A2N | A2DP |
| **LCDM6** | P5.5 | S11 | 6 | A2A | A2B | A2C | A2D | P5.6 | S10 | 5 | A2E | A2F | A2G | A2M |
| **LCDM5** | P5.7 | S9 | 12 | A3H | A3J | A3K | A3P | P4.4 | S8 | 11 | A3Q | ANT | A3N | A3DP |
| **LCDM4** | P4.5 | S7 | 10 | A3A | A3B | A3C | A3D | P4.6 | S6 | 9 | A3R | A3F | A3G | A3M |
| **LCDM3** | P4.7 | S5 | | | | | | P10.0 | S4 | 32 | TMR | HRT | REC | ! |
| **LCDM2** | P4.0 | S3 | | | | | | P4.1 | S2 | | | | | |
| **LCDM1** | P1.4 | S1 | | | | | | P1.5 | S0 | | | | | |