Yousef Alaa Awad

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Education

University of Central Florida Orlando, FL
Bachelor of Science in Computer Engineering with Honors | GPA: 3.73 May 2027
Relevant Courses: HDL in Digital Systems Design, Adv. Computer Architecture, Verification of Digital Systems
Affilliations: IEEE-HKN (Zeta Chi Chapter), IEEE, ACM

Work Experience

FPGA/ASIC Intern Orlando, FL
Lockheed Martin – Missiles and Fire Control Feb 2026 – Present

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Embedded Software Engineering Intern Orlando, FL
Lockheed Martin – Missiles and Fire Control Apr 2025 – Feb 2026

- Designed a system-level Hardware-in-the-Loop (HIL) simulation environment in **C++**, enabling high-fidelity testing alongside integrating into already developed tools for 20+ engineers by implenting a CIGI v2 compliant image generator.
- Developed custom **C++** automation tools for Hardware-in-the-Loop (HIL) test environments, reducing manual data analysis efforts by 20% and further optimized CI/CD pipeline via **Bash** scripts to decrease software integration time by 10%.
- Engineered the migration of legacy **C++**/Qt tooling environments from Visual Studio to a **CMake** build system, slashing compilation times by 50% and establishing a modular architecture to improve future scalability of the program.

Projects

KnightCore – Full RISC-V SoC – 2025 AMD Hardware Competition – *Group Project* Apr 2025 – Aug 2025

- Architected a modular, reusable verification environment from scratch in Python (CocotB) to validate a custom 32-bit RISC-V SoC against the **RV32I** instruction set architecture (ISA).
- Developed a comprehensive test suite with directed tests for all ISA-defined instructions and constrained-random stimulus generation to stress the ALU and branch prediction logic, leading to the discovery and resolution of 5 critical RTL bugs.

2025 SouthEastCon Robotics Competition – Embedded Software Lead – *Group Project* Sep 2024 – Apr 2025

- Led software pipeline for 10+ team using **ROS2**, enabling low-latency control between modular hardware and decision nodes. Used Gazebo and **OpenCV** for validation, contributing to **1st place** in Design and **2nd** in Performance at competition.
- Developed embedded firmware on Teensy 4.1 for sensor fusion and actuator control with modular, **real-time C++** code. Optimized for high-frequency loops and low resource use, improving system responsiveness and performance.

CyndaQuil Compiler/Language – *Solo Project* Sep 2024 – Jan 2025

- Applied principles of language design by creating 'CyndaQuilLanguage,' a custom programming language. Implemented its compiler from scratch in **C++** and **C** (using **CMake**), engineering its parsing, semantic analysis, and assembly generation.
- Engineered low-level system components and optimized performance, integrating **Assembly** and **C** to enhance hardware-software interfacing, ensuring minimal latency and efficient computation for embedded systems.

Leadership

IEEE-HKN Zeta Chi
Vice President & Treasurer Apr 2025 – Present

- Leading the re-establishment of the dormant IEEE-HKN chapter, positioning the organization to achieve national 'Key Chapter' status by growing membership to 31 students and developing a new recruitment pipeline.
- Architecting the chapter's operational revival by engineering foundational processes for member induction and organizational scope, while simultaneously managing the financial and logistical strategies to double national conference delegation.

IEEE UCF
Treasurer Apr 2025 – Present

- Managing the IEEE UCF chapter's finances, developing and tracking over a $10,000+ budget across multiple projects and events, ensuring accurate allocation of resources and financial accountability.
- Facilitating over $6500 in sponsorship funding through effective communication with industry partners, directly supporting student project development and participation in competitions like the SouthEastCon Hardware Competition.

Technical Skills

Languages: Verilog, SystemVerilog, C++, Python, C, Rust, Bash, Assembly (x86, RISC-V, MIPS)
Hardware Verification: UVM Methodologies, Testbench Architecture, Functional Coverage, Constrained Randomization
Computer Architecture: RISC-V ISA, AXI/Memory-Mapped Interfaces, Pipelining, Caching, Memory Hierarchy
Hardware & EDA Tools: Xilinx Vivado, Synopsys VCS, Verilator
Systems & Scripting: Linux, Git, ROS/ROS2, Real-Time C++, CMake