Yousef Alaa Awad

(717)-601-9976 | yousefalaaawad@gmail.com | linkedin.com/in/yousefalaaawad | github.com/Quil180

EDUCATION

University of Central Florida — Orlando, FL
Bachelor of Science in Computer Engineering with Honors | GPA: 3.73 — Expected May 2027
Relevant Courses: Verification and Validation of Digital Systems, Computer Arch., and Computer Org.

EXPERIENCE

Embedded Systems Engineering Intern — Orlando, FL
Lockheed Martin Work Experience Program — Apr 2025 – Present
- Developed C++ tools to automate data analysis within the Hardware-in-the-Loop (HIL) testing environment, reducing manual processing time by 20% and improving the efficiency of test result validation work.
- Optimized existing C++ scripts within the CI/CD pipeline to accelerate build and test execution speed, resulting in a 10% reduction in overall integration time and enhanced software release frequency for system updates.

PROJECTS

Chikorita Filter – FPGA Vision Accelerator — Aug 2025 – Present
- Architecting a low-latency FPGA DSP pipeline in Verilog/VHDL for the 2026 IEEE SoutheastCon Competition, implementing parallel modules for real-time vision preprocessing, motor control, and IR communication.
- Developing and verifying the FPGA-to-CPU interface (AXI/Memory-Mapped) to stream sensor data for Kalman filter processing, enabling successful hardware/software sensor fusion.

KnightCore – Full RISC-V SoC – 2025 AMD Hardware Competition — Apr 2025 – Aug 2025
- Collaborated within a 5-member team to design and implement a complete System-on-Chip (SoC), featuring a custom 32-bit RISC-V CPU and full custom GPU, capable of vector math and memory management on the Red Pitaya 125-14 board.
- Developed a comprehensive verification environment using the CocotB framework, creating testbenches for all modules. Authored directed and randomized stress tests, and assertion-based checks to ensure correctness and ISA compliance.

Anqa 32-bit RISC-V Processor — Feb 2025 – Present
- Designed a 32-bit RISC-V CPU core, implementing key components like a parameterized adder (half/full/multi-bit) and instruction decoding logic for the RV32I base instruction set (arithmetic, logical, load/store, branch).
- Developed a Verilog implementation plan using Vivado, detailing the ALU, register file, single-cycle datapath design, and instruction pipeline stages, with comprehensive documentation for future development.

Fallout Style Pip-Boy — Oct 2024 – Apr 2025
- Developed a modular Rust application employing dynamic linking and Cargo workspaces for a scalable, plugin-based architecture, designed for enhanced code reusability and maintainability.
- Architected the system to effectively support dynamic loading of plugins, enabling flexible extension of functionality with minimal modification to the application's core components and overall structure.

CyndaQuil Compiler/Language — Sep 2024 – Jan 2025
- Designed and implemented 'CyndaQuilLanguage', a custom programming language, developing its compiler in C++ and C with Makefile and CMake, showcasing expertise in language design, parsing, and code generation for efficient execution.
- Engineered low-level system components and optimized performance, integrating Assembly and C to enhance hardware-software interfacing, ensuring minimal latency and efficient computation for embedded systems.

LEADERSHIP

IEEE UCF
Treasurer — Apr 2025 – Present
- Managed the IEEE UCF chapter's finances, developing and tracking over a $6000+ budget across multiple projects and events, ensuring accurate allocation of resources and financial accountability.
- Oversaw budget planning and resource allocation for technical project teams, including the South EastCon robotics team, providing guidance on financial feasibility, and ensuring projects received necessary funding for hardware, and software.

SouthEastCon Hardware/Robotics Competition Software Lead — Sep 2024 – Apr 2025
- Led software pipeline for 10+ team using ROS2, enabling low-latency control between modular hardware and decision nodes. Used Gazebo and OpenCV for validation, contributing to 1st place in Design and 2nd in Performance at competition.
- Developed embedded firmware on Teensy 4.1 for sensor fusion and actuator control with modular, real-time C++ code. Optimized for high-frequency loops and low resource use, improving system responsiveness and performance.

SKILLS

Computer Architecture: RISC-V ISA, FPGA Design, Pipelining, Caching, Memory Hierarchy
Embedded Systems: ROS/ROS2, ESP32, Teensy 4.1, Sensor Integration, Real-Time C++, Firmware Optimization
Hardware Design & Verification: Verilog, SystemVerilog, RTL Design, Testbenches, Timing Closure, FPGA Prototyping
Hardware Tools: Vivado, ModelSim, Verilator, Synthesis, Simulation, XDC/SDC Constraints
Programming Languages: C++, C, Rust, Bash, Assembly (x86, RISC-V, MIPS), Python