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Title of Submission: CMOS

Type of Submission: ☐ Program ☐ Project ☑ Report ☐ Paper ☐ Other (specify) _____

Date of Submission: 8/19/17

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[1]http://www.kvazer.com/datascheet_pdf/Transistor.pdf

Group Information

Full Name	Signature
Jayce Caylah Ching	
Gabriel De Jesus	

Course Information

Course Code & Section: CS 152B - B

Course Title: Computer Organization II

Course Instructor: Patricia Angela R. Abu

Ching, Jayce Caylah
De Jesus, Gabriel

I. Theoretical Background

This laboratory assignment focuses on CMOS, using MOSFETs in circuits - how they work and how to arrange them to produce various working circuits. CMOS means Complementary Metal Oxide Semi-conductor while MOSFET stands for Metal Oxide Semi-conductor Field Effect Transistor. The transistor is a device that can function as a signal amplifier or as a solid-state switch[1]. The transistors used in this assignment, the MOSFETs, are used as a switch, which could either connect the electric flow to the rest of the circuit or obstruct it. As the transistor is one of the most basic components in building a circuit, it is essential to understand its function and its role in a circuit.

II. Methodology

The circuits were made by examining corresponding truth tables with the required number of inputs. To determine which CLK was used for which input, the truth tables were consulted. For example, given the truth table below, CLK1 would be used to input B, and CLK2 would be used to input A.

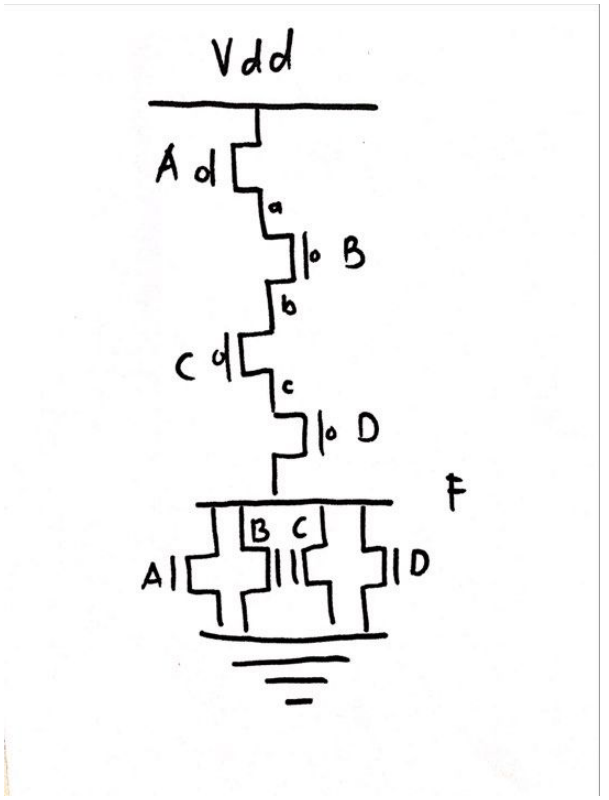
A	B
0	0
0	1
1	0
1	1

By checking which bit arrangements output 1 and 0, the inputs were then connected to vdd and ground respectively. Boolean algebra was used to simplify the equation and find the optimal setup for each input, while adhering to the required gate output.

III. Results

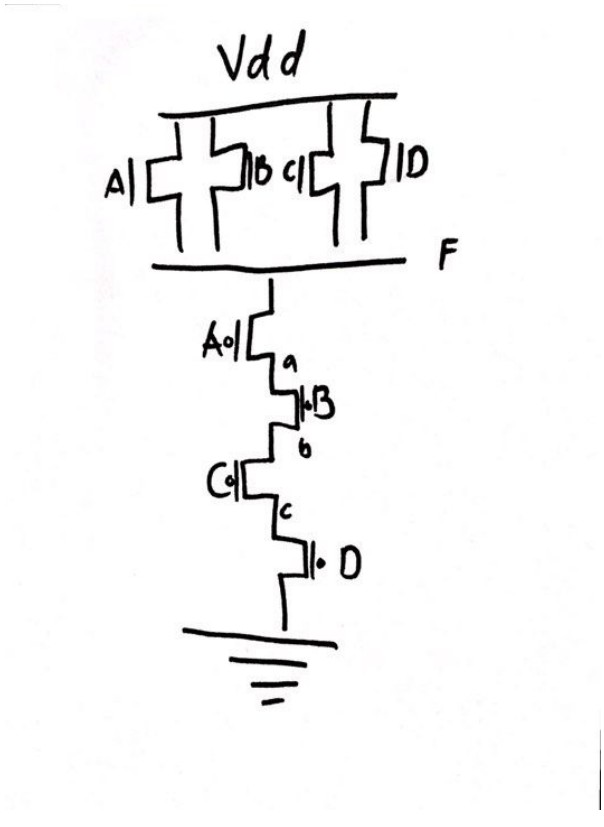
4 Input NOR Gate

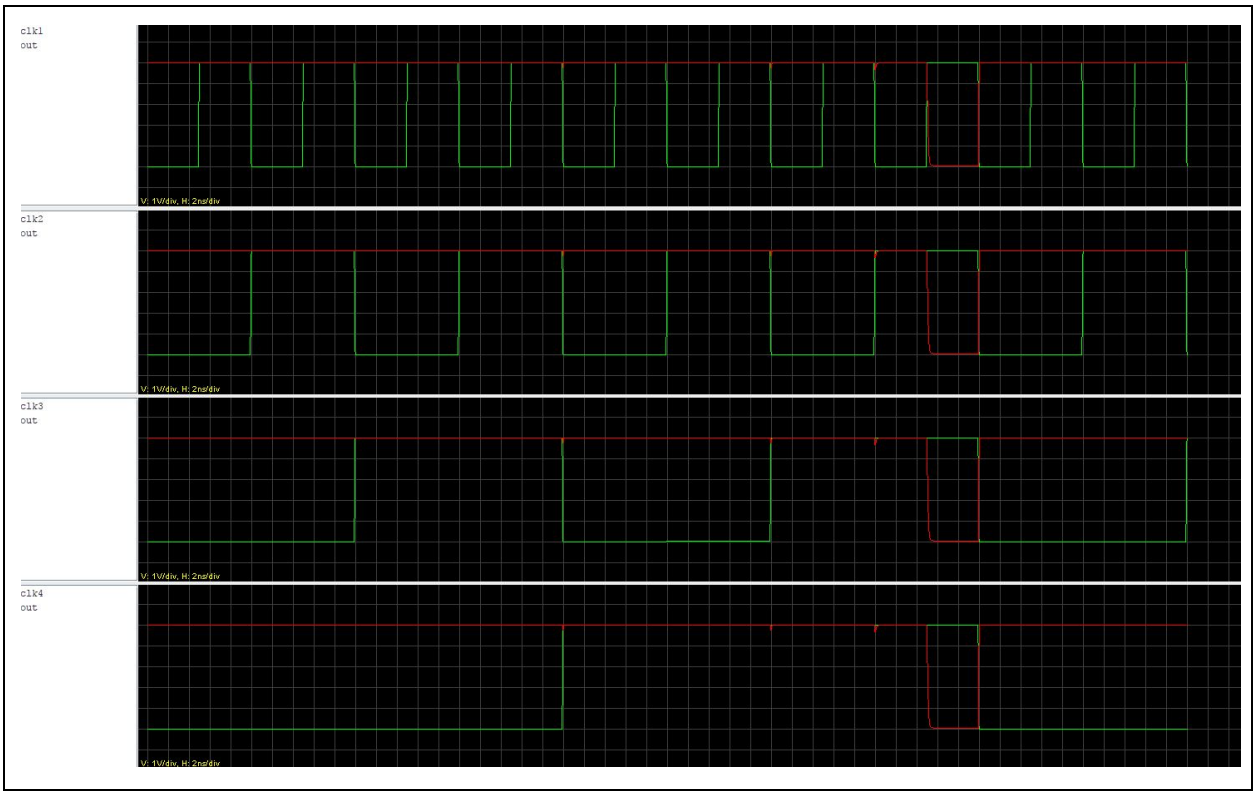
```
*Implementation for a 4 input NOR gate
*By Gabriel De Jesus & Jayce Caylah Ching, CS152B

.include "8clocks.jsim"
.include "nominal.jsim"

*Written in the format source gate drain

*CLK1 MOSFET [MP1, MN1]
MP1 vdd clk4 a vdd PENH W=1u L=1u
MN1 out clk4 0 0 NENH W=1u L=1u

*CLK2 MOSFET [MP2, MN2]
MP2 a clk3 b vdd PENH W=1u L=1u
MN2 out clk3 0 0 NENH W=1u L=1u

*CLK3 MOSFET [MP3, MN3]
MP3 b clk2 c vdd PENH W=1u L=1u
MN3 out clk2 0 0 NENH W=1u L=1u

*CLK4 MOSFET [MP4, MN4]
MP4 c clk1 out vdd PENH W=1u L=1u
MN4 out clk1 0 0 NENH W=1u L=1u

*Plot
.tran 100ns
.plot clk1 out
.plot clk2 out
.plot clk3 out
.plot clk4 out
```



4 Input NAND Gate

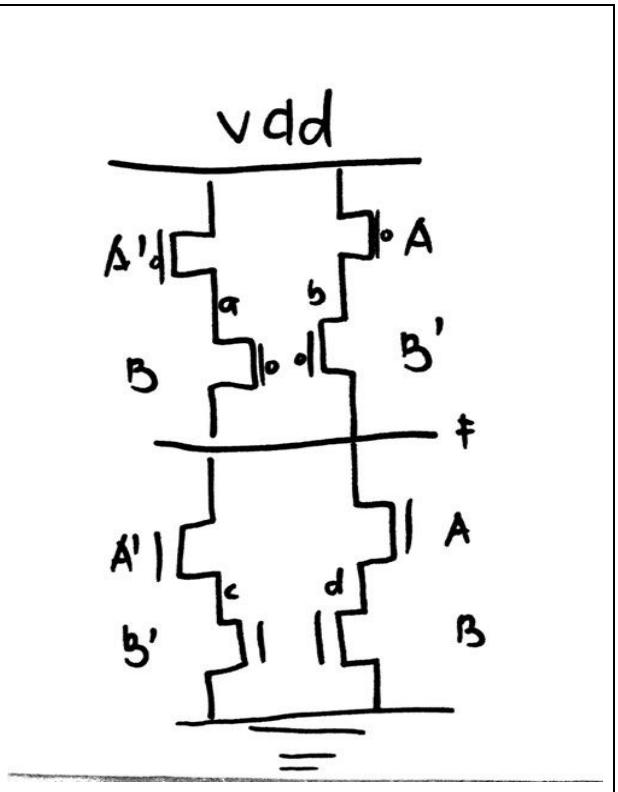
```
*Implementation for a 4 input NAND gate
*By Gabriel De Jesus & Jayce Caylah Ching, CS152B

.include "8clocks.jsim"
.include "nominal.jsim"

*CLK1 MOSFET [MP1, MN1]
MP1 vdd clk4 out vdd PENH W=1u L=1u
MN1 out clk4 a 0 NENH W=1u L=1u

*CLK2 MOSFET [MP2, MN2]
MP2 vdd clk3 out vdd PENH W=1u L=1u
MN2 a clk3 b 0 NENH W=1u L=1u

*CLK3 MOSFET [MP3, MN3]
MP3 vdd clk2 out vdd PENH W=1u L=1u
MN3 b clk2 c  0 NENH W=1u L=1u

*CLK4 MOSFET [MP4, MN4]
MP4 vdd clk1 out vdd PENH W=1u L=1u
MN4 c clk1 0 0 NENH W=1u L=1u

*Plot
.tran 100ns
.plot clk1 out
.plot clk2 out
.plot clk3 out
.plot clk4 out
```

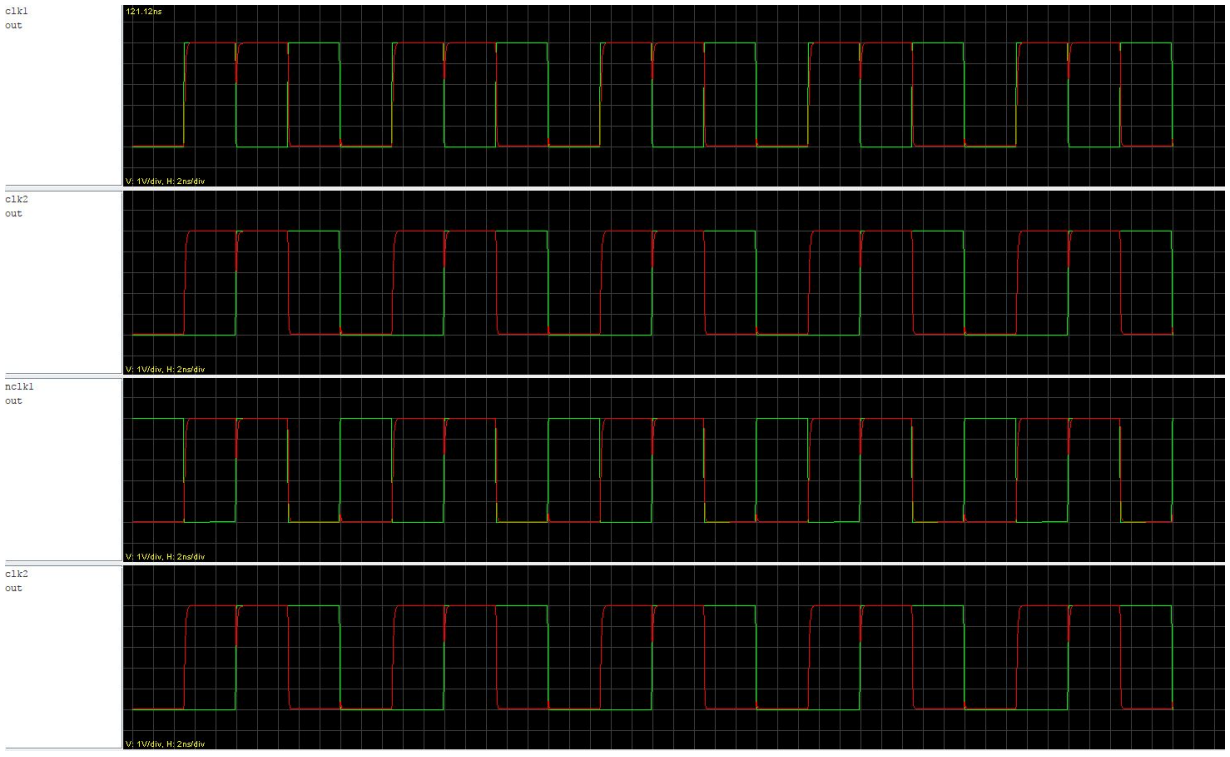



clk1
out
V: 1V/div, H: 2ns/div
clk2
out
V: 1V/div, H: 2ns/div
clk3
out
V: 1V/div, H: 2ns/div
clk4
out
V: 1V/div, H: 2ns/div

2 Input XOR

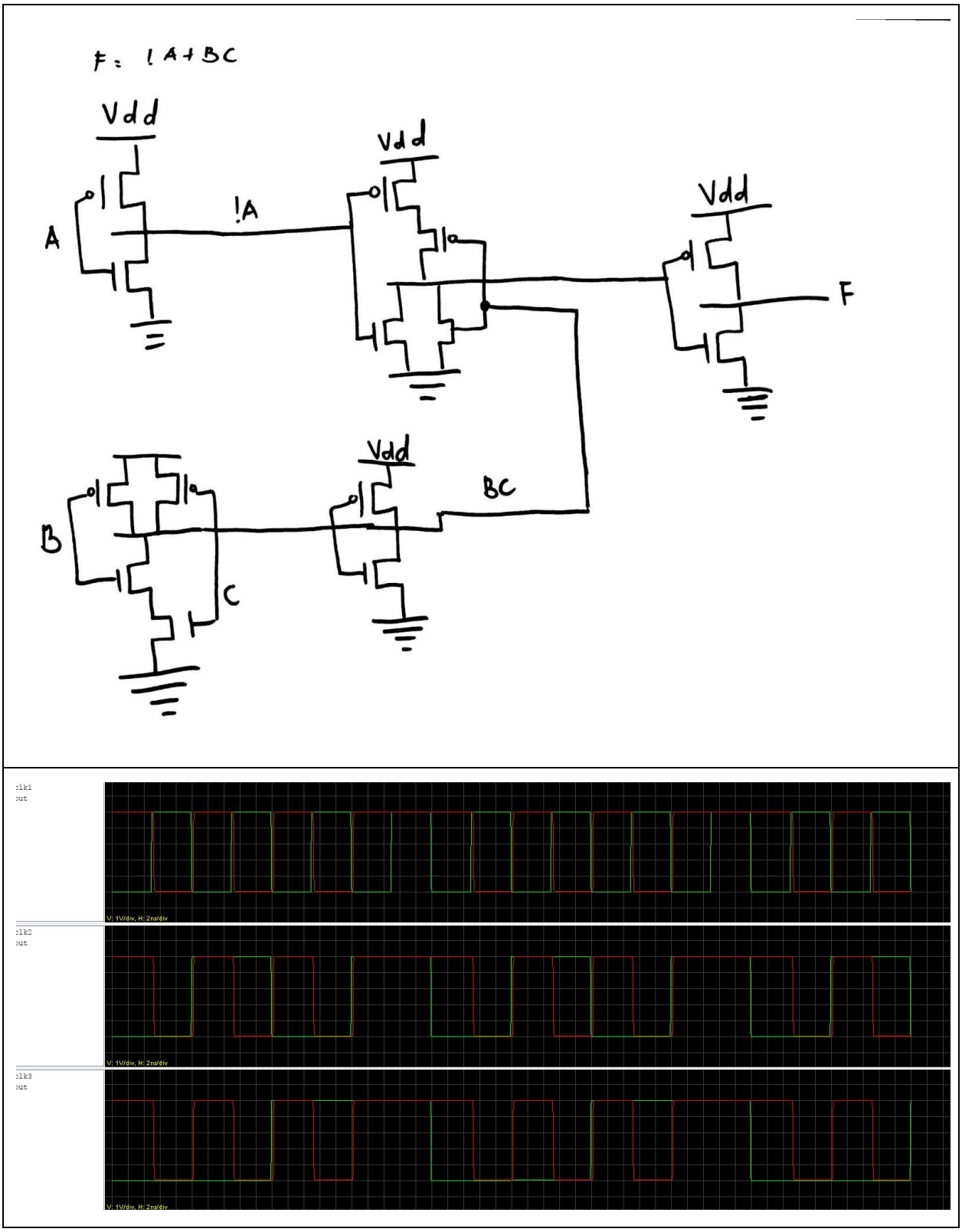
```
*Implementation for a 2 input XOR gate
*By Gabriel De Jesus & Jayce Caylah Ching, CS152B

.include "8clocks.jsim"
.include "nominal.jsim"

*CLK1 MOSFET [MP1, MN1]
MP1 vdd nclk2 a vdd PENH W=1u L=1u
MN1 out nclk2 c 0 NENH W=1u L=1u

*CLK2 MOSFET [MP2, MN2]
MP2 vdd clk2 b vdd PENH W=1u L=1u
MN2 out clk2 d 0 NENH W=1u L=1u

*NCLK1 MOSFET [MP3, MN3]
MP3 a clk1 out vdd PENH W=1u L=1u
MN3 d clk1 0 0 NENH W=1u L=1u

*clk2 MOSFET [MP4, MN4]
MP4 b nclk1 out vdd PENH W=1u L=1u
MN4 c nclk1 0 0 NENH W=1u L=1u

*Plot
.tran 100ns
.plot clk1 out
.plot clk2 out
.plot nclk1 out
.plot clk2 out
```





F = !A + BC

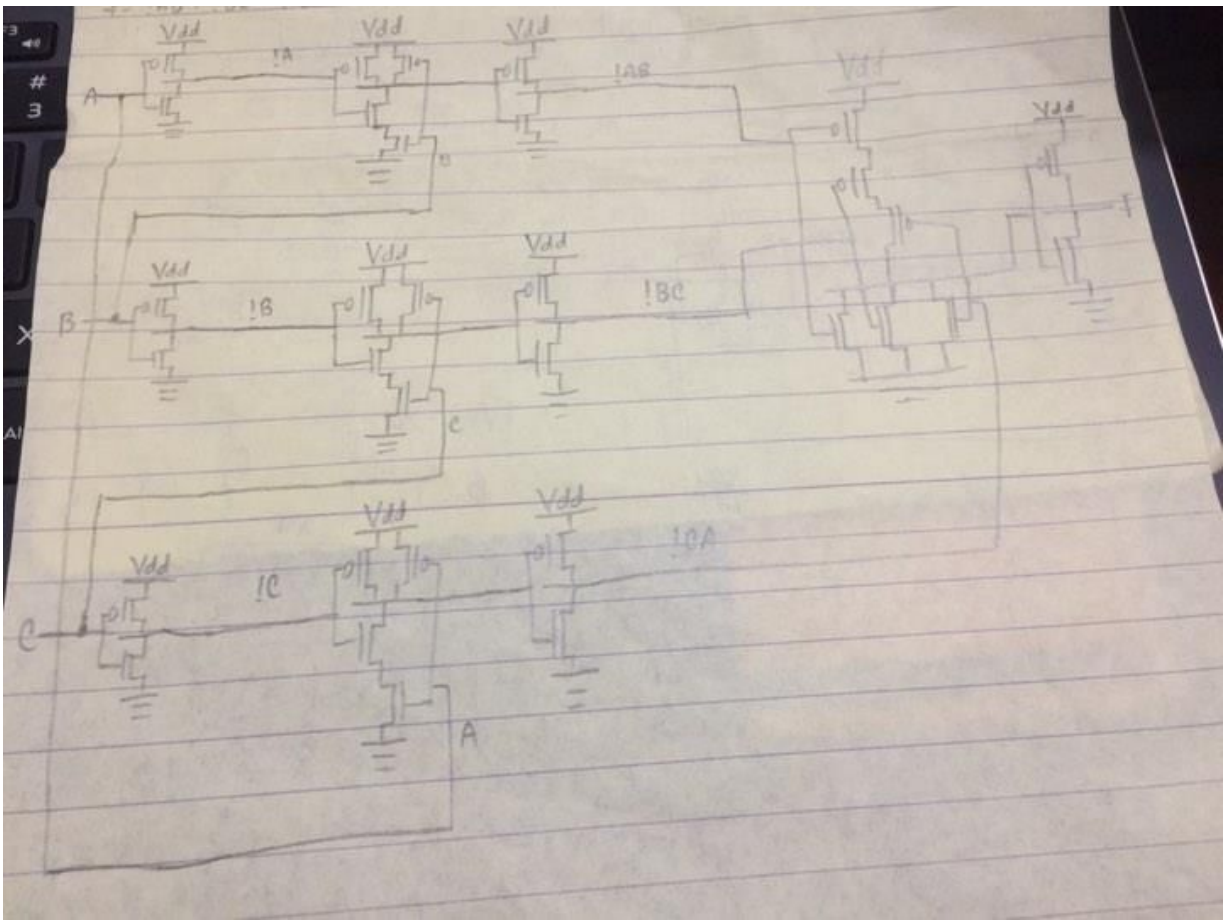
```
*Implementation for F = !A + BC
*By Gabriel De Jesus & Jayce Caylah Ching, CS152B

.include "8clocks.jsim"
.include "nominal.jsim"

*clk1 MOSFETs (clk1 INVERTER); a = !A
MP1 vdd clk1 a vdd PENH W=1u L=1u
MN1 a clk1 0 0 NENH W=1u L=1u

*clk2 NAND clk3 MOSFETs; b = B NAND C
MP2 vdd clk2 b vdd PENH W=1u L=1u
MN2 b clk2 i 0 NENH W=1u L=1u

MP3 vdd clk3 b vdd PENH W=1u L=1u
MN3 i clk3 0 0 NENH W=1u L=1u

*clk2 AND clk3 MOSFETs (INVERT NAND OUTPUT); c = BC
MP4 vdd b c vdd PENH W=1u L=1u
MN4 c b 0 0 NENH W=1u L=1u

*!A NOR BC MOSFETs; d = !A NOR BC
MP5 vdd a x vdd PENH W=1u L=1u
MN5 d a 0 0 NENH W=1u L=1u

MP6 x c d vdd PENH W=1u L=1u
MN6 d c 0 0 NENH W=1u L=1u

*!A + BC MOSFETs (INVERT !A NOR BC); out = !A + BC
MP7 vdd d out vdd PENH W=1u L=1u
MN7 out d 0 0 NENH W=1u L=1u

*PLOT
.tran 50ns
.plot clk1 out
.plot clk2 out
.plot clk3 out
```

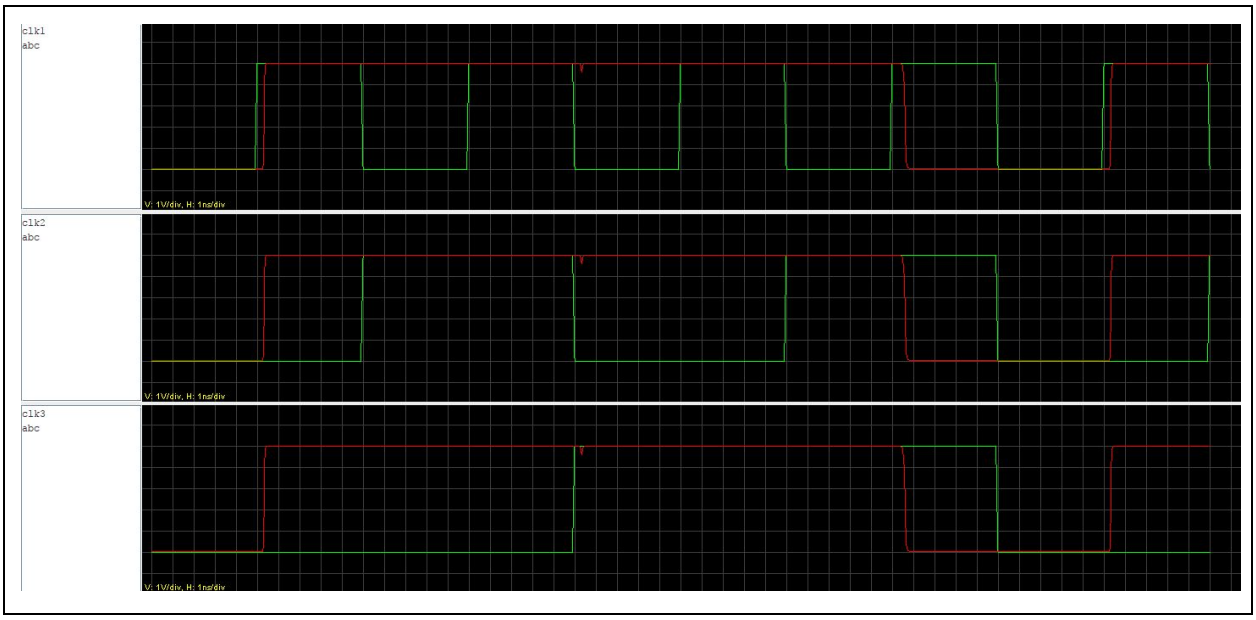


F = !AB + !BC + !CA

```
*Implementation for F = !AB + !BC + !CA
*By Gabriel De Jesus & Jayce Caylah Ching, CS152B

.include "8clocks.jsim"
.include "nominal.jsim"

*clk1 = A, clk2 = B, clk3 = C

*clk1 MOSFETs (clk1 INVERTER); na = !A
MP1 vdd clk1 na vdd PENH W=1u L=1u
MN1 na clk1 0 0 NENH W=1u L=1u

*clk2 MOSFETs (clk2 INVERTER); nb = !B
MP2 vdd clk2 nb vdd PENH W=1u L=1u
MN2 nb clk2 0 0 NENH W=1u L=1u

*clk3 MOSFETs (clk3 INVERTER); nc = !C
MP3 vdd clk3 nc vdd PENH W=1u L=1u
MN3 nc clk3 0 0 NENH W=1u L=1u

*!A NAND B MOSFETs (M4 = !A, M5 = B); nab = !A NAND B
MP4 vdd na nab vdd PENH W=1u L=1u
MN4 nab na i 0 NENH W=1u L=1u

MP5 vdd clk2 nab vdd PENH W=1u L=1u
MN5 i clk2 0 0 NENH W=1u L=1u

*!A AND B MOSFETs (INVERT NAND OUTPUT); ab = !AB
MP6 vdd nab ab vdd PENH W=1u L=1u
MN6 ab nab 0 0 NENH W=1u L=1u

*!B NAND C MOSFETs (M7 = !B, M8 = C); nbc = !B NAND C
MP7 vdd nb nbc vdd PENH W=1u L=1u
MN7 nbc nb i2 0 NENH W=1u L=1u

MP8 vdd clk3 nbc vdd PENH W=1u L=1u
MN8 i2 clk3 0 0 NENH W=1u L=1u

*!B AND C MOSFETs (INVERT NAND OUTPUT); bc = !BC
MP9 vdd nbc bc vdd PENH W=1u L=1u
MN9 bc nbc 0 0 NENH W=1u L=1u

*!C NAND A MOSFETs (M10 = !C, M11 = A); nca = !C NAND A
MP10 vdd nc nca vdd PENH W=1u L=1u
MN10 nca nc i3 0 NENH W=1u L=1u

MP11 vdd clk1 nca vdd PENH W=1u L=1u
MN11 i3 clk1 0 0 NENH W=1u L=1u

*!C AND A MOSFETs (INVERT NAND OUTPUT); ca = !CA
MP12 vdd nca ca vdd PENH W=1u L=1u
MN12 ca nca 0 0 NENH W=1u L=1u

*!AB NOR !BC NOR !CA (MP13 = !AB, MP14 = !BC, MP15 = !CA); nabc = !AB NOR !BC NOR !CA
MP13 vdd ab x vdd PENH W=1u L=1u
MN13 nabc ab 0 0 NENH W=1u L=1u

MP14 x bc y vdd PENH W=1u L=1u
MN14 nabc bc 0 0 NENH W=1u L=1u
```

```
MP15 y ca nabc vdd PENH W=1u L=1u
MN15 nabc ca 0 0 NENH W=1u L=1u

*!AB OR !BC OR !CA (INVERT NOR OUTPUT); abc = !AB + !BC + !CA
MP16 vdd nabc abc vdd PENH W=1u L=1u
MN16 abc nabc 0 0 NENH W=1u L=1u

.tran 50ns
.plot clk1 abc
.plot clk2 abc
.plot clk3 abc
```





IV. Conclusion

With this laboratory exercise designed to help the researchers get accustomed to working and implementing MOSFET circuits, the researchers have gained a better understanding on how MOSFETs work and how to use them. By having the researchers make 5 different CMOS circuits with various difficulty and usage of given 2-input NOR and NAND CMOS logic gates, the researchers were driven to analyze the circuits properly to be able to make a different circuit of their own with the desired output.