

Inspired by the MTM Turing Machine, the RNG outputs stepped CV that is semi-random but semi-looping. With each clock pulse, the sequence is advanced and the next value in the loop is played. But, there is a chance for that value to be replaced with a new random value first, resulting in musical but always-evolving sequences. While the left side of the module controls the CV output, the right side controls a trigger output. Each step, a trigger will be played on one of two channels based on the primary output.

Chance

Adjusts the probability values in the loop being mutated before they are played. At full CCW, the sequence is locked. At full CW, every value is random.

Spread

Attenuates the range of primary CV output. Does not change the sequence itself; attenuation is only applied on the output.

Polarity

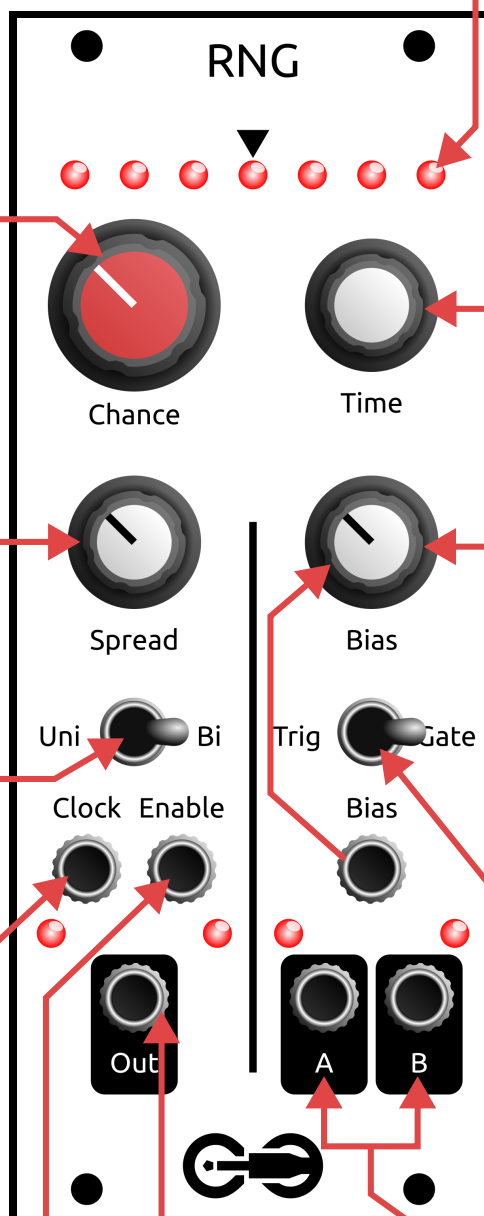
Switches output between unipolar (0v to 5v) and bipolar (-10v to 10v).

Clock Input

Every trigger on this input shifts the loop forward one step and sends a new value to all three outputs

Mutation Enabled Gate

Normalised HIGH. When pulled LOW, the sequence is locked. LED shows when mutation is enabled



Primary Output

Outputs the main semi-looping, semi-random stepped CV value. Updates on each clock pulse

LEDs

LEDs show a section of the current sequence. Lit LEDs indicate a value above the bias threshold. The center LED is the currently active value.

Time

Changes the length of the loop from 1 to 32. LEDs briefly indicate the new length in binary. Normally adjusts in powers of 2; hold down the encoder to step by 1. Negative lengths (indicated by left-most LED) will cause the sequence to alternate direction.

Bias

Sets the cutoff point for the gate/trigger output. On each step, if the output value is above the cutoff it will trigger output A. Otherwise, B.

Trig/Gate Switch

In trigger mode, A or B will output a trigger at each step. In gate mode, A or B will stay high (maybe for multiple steps) until the other would be triggered.

Trig/Gate outputs

Either A or B will output a trigger or gate based on the main output and bias.