Tutorial D — Altera DE0-CV Board

Section I: Overview

In the lab, we will take the circuit that you wrote up in Verilog, and program it onto a development board to test it. We will be using the Altera DE0-CV development board, which is shown in Figure 1. This board contains a large number of components, which interact with a *field-programmable gate array* (FPGA). While it is a bit more complicated, you can think of it as a chip that contains thousands of logic gates, each of which we can program to perform our Boolean functions.

When a circuit is written in Verilog, this is translated by Quartus to determine how it should set up each of these gates. Each of the gates on the FPGA is then configured so that they each run in parallel, just as if we had taken some chips and wired them together ourselves. If there is a mistake in our program, we can simply update the Verilog file and then reprogram the FPGA to implement the updated circuit.

The DE0-CV components we will be using in this lab are:

- Cyclone V 5CEBA4F23C7N FPGA
- Seven-segment displays
- Toggle switches
- Push-button switches
- LED indicators

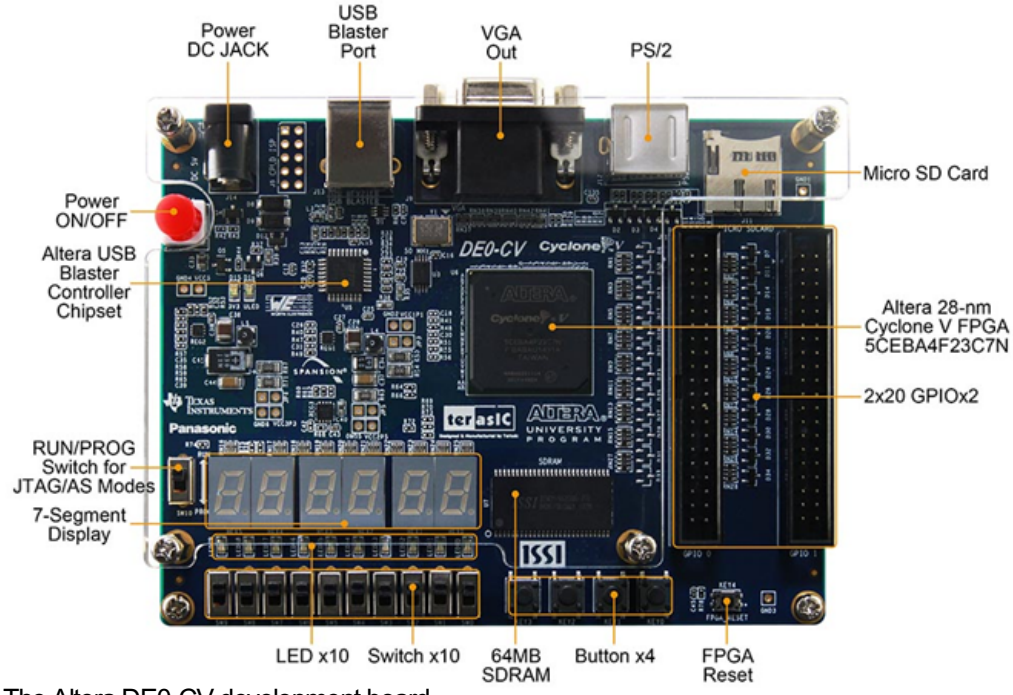

Figure 1. The Altera DE0-CV development board.

Section II: DE0-CV Inputs

A. Push-Button Switches

The five push-button switches on the DE0-CV board are identified by the names **KEY0** to **KEY3,** and **RESET_N**. Each push-button is connected to a fixed pin on the Cyclone V FPGA. Each push-button is active low, so pressing a push-button sends a logic "0" to the FPGA, while not pressing it sends a logic "1." The four push-button pinouts are shown in Table A.

PUSH-BUTTON	PIN
KEY0	PIN_U7
KEY1	PIN_W9
KEY2	PIN_M7
KEY3	PIN_M6
RESET_N	PIN_P22

Table A. DE0-CV pin assignments for the push-button switches.

B. Slide Switches

The 10 slide switches (toggle switches) on the DE0-CV board are labeled, from right to left, **SW0** to **SW9**. Each toggle switch is connected to a fixed pin on the Cyclone V FPGA. In the *DOWN* position, a toggle switch outputs a low signal, and in the *UP* position, a toggle switch outputs a high signal. The pinouts of toggle switches are shown in Table B.

SWITCH	PIN
SW0	PIN_U13
SW1	PIN_V13
SW2	PIN_T13
SW3	PIN_T12
SW4	PIN_AA15
SW5	PIN_AB15
SW6	PIN_AA14
SW7	PIN_AA13
SW8	PIN_AB13
SW9	PIN_AB12

Table B. DE0-CV pin assignments for the toggle switches.

C. Clocks

The 50 MHz oscillator on the DE0-CV board is buffered 4 times. Each buffer is connected to a fixed pin on the Cyclone V FPGA, and provides the clock for a bank of I/O pins. Table C shows the pinout for these clocks.

SIGNAL	PIN
CLOCK_50	PIN_M9
CLOCK2_50	PIN_H13
CLOCK3_50	PIN_E10
CLOCK4_50	PIN_V15

Table C. DE0-CV pin assignments for the clock signals.

Section III: DE0-CV Outputs

A. LEDs

The 10 red LEDs on the DE0-CV board are named **LEDR0** to **LEDR9**. Each LED is connected to a fixed pin on the Cyclone V FPGA. The LEDs are active high, so asserting a high signal to it turns the LED on, and asserting a low signal turns it off. Table D shows the pinouts of LEDs.

LED	PIN
LEDR0	PIN_AA2
LEDR1	PIN_AA1
LEDR2	PIN_W2
LEDR3	PIN_Y3
LEDR4	PIN_N2
LEDR5	PIN_N1
LEDR6	PIN_U2
LEDR7	PIN_U1
LEDR8	PIN_L2
LEDR9	PIN_L1

Table D. DE0-CV pin assignments for the LEDs.

B. Seven-Segment Displays

The 6 seven-segment displays on the DE0-CV board are named, from right to left, **HEX0** to **HEX5**. Each segment of the display is connected to fixed pins on the Cyclone V FPGA. Each segment is active low, so applying a logic "0" to a segment causes it to turn on. Segments are numbered as shown in Figure 2.

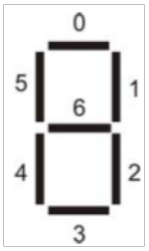

Figure 2. Pinout of seven-segment display.

The pin assignments for each segment are given in Table E. **HEX5** is the most significant digit, while **HEX0** is the least significant digit. We will typically provide you with a driver file that will translate binary numbers into seven segment outputs.

DISPLAY	SEGMENT	PIN
HEX0	0	PIN_U21
HEX0	1	PIN_V21
HEX0	2	PIN_W22
HEX0	3	PIN_W21
HEX0	4	PIN_Y22
HEX0	5	PIN_Y21
HEX0	6	PIN_AA22
HEX1	0	PIN_AA20
HEX1	1	PIN_AB20
HEX1	2	PIN_AA19
HEX1	3	PIN_AA18
HEX1	4	PIN_AB18
HEX1	5	PIN_AA17
HEX1	6	PIN_U22
HEX2	0	PIN_Y19
HEX2	1	PIN_AB17
HEX2	2	PIN_AA10
HEX2	3	PIN_Y14
HEX2	4	PIN_V14
HEX2	5	PIN_AB22
HEX2	6	PIN_AB21

DISPLAY	SEGMENT	PIN
HEX3	0	PIN_Y16
HEX3	1	PIN_W16
HEX3	2	PIN_Y17
HEX3	3	PIN_V16
HEX3	4	PIN_U17
HEX3	5	PIN_V18
HEX3	6	PIN_V19
HEX4	0	PIN_U20
HEX4	1	PIN_Y20
HEX4	2	PIN_V20
HEX4	3	PIN_U16
HEX4	4	PIN_U15
HEX4	5	PIN_Y15
HEX4	6	PIN_P9
HEX5	0	PIN_N9
HEX5	1	PIN_M8
HEX5	2	PIN_T14
HEX5	3	PIN_P14
HEX5	4	PIN_C1
HEX5	5	PIN_C2
HEX5	6	PIN_W19

Table E. DE0-CV pin assignments for the seven-segment displays.