Radio Frequency Circuit Design. W. Alan Davis, Krishna Agarwal

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CHAPTER TWELVE

Phase Lock Loops

12.1 INTRODUCTION

Phase lock loops (PLL) are not a recent invention. Their use became widespread with the availability of high-quality integrated circuit operational amplifiers (op-amps) in the 1960s. This versatile circuit has found applications across the frequency spectrum in consumer, commercial, deep space, and military projects. Tracking *Voyager* through the solar system and tuning a car radio are made to order uses for a PLL. To understand a PLL, a good working knowledge of RF techniques, oscillator design, closed loop control theory, analog circuit design, and digital circuit design is required. A comprehension of each of the components and its place in the system is essential. Fortunately not all of this knowledge is required at once. The books listed at the end of this chapter can each provide an in-depth insight into areas beyond the present scope [1–5]. This discussion will begin with the basic concepts and rapidly expand these ideas into practical considerations.

12.2 PLL DESIGN BACKGROUND

Discussion of the PLL draws heavily on many other areas of analysis, which includes an understanding of the principles of closed loop control theory. From control theory comes the concept of negative feedback to tailor the performance of closed loop systems. Response time, transient performances, bandwidth, damping ratio, and phase margin are used to describe PLL operation. The type and order of a closed loop system define the complexity and response to a stimulus.

In most PLL's, at least two of the components, the voltage-controlled oscillator (VCO) and phase detector, are high-frequency components. There may also be amplifiers, mixers, frequency multipliers, and other oscillators. To use these items, a familiarity with RF design practices and terminology is important.

Frequency multiplication may require digital integrated circuits (ICs) within the PLL. These ICs require digital control words to set the desired frequency.

Many integrated circuits are presently available that combine many of the PLL functions on a single chip. Most of the interface control is digital.

Analog circuit design is perhaps the most demanding of the circuit areas within a PLL. Op-amps are used in many of the filtering circuits used within a loop. Inverting and noninverting circuits are required for loop filters and search circuits. Integrators, dc amplifiers, Schmitt triggers, and offset circuits are used to set the loop operation. Resistor/capacitor circuits provide phase shift for stability. The oscillator is an intrinsic part of a PLL, and its design in itself is a specialized and technically challenging area.

12.3 PLL APPLICATIONS

A phase lock loop is a frequency domain device that can be used to multiply, divide, or filter different frequencies. Consider a space probe rapidly moving away from the earth. To recover data from the probe, the transmitter frequency must be known. The signal is very weak because of the distance, and the low signal-to-noise ratio requires a very small receiver filter bandwidth to recover the data. However, because of the relative motion, there is a significant and changing Doppler shift to the transmit frequency. The system requires a filter that may be only a few Hertz wide operating at a varying frequency that is centered at several GHz.

An electronic phase lock loop is one form of a closed loop system. The cruise control is another. A switching power supply, a camera's light meter, a radio's automatic gain control, the temperature control in a building, a car's emission system controls, and a Touch-Tone dialing system are examples of closed loop systems. A broadcast receiver changes frequency with a button push or electronically. Each time the station is accurately centered with no manual adjustment required. Physically these PLLs are all very different working at different jobs and in different environments. However, they all must follow the same rules, and the loops must all be stable.

A clear understanding of the concept of feedback control is illustrated by an everyday situation of the simple action of controlling the speed of a car. If the desired speed is 60 mph, then this becomes the reference. Any deviation from this speed is an error. The accelerator pedal is the control element. On level terrain, a constant pressure on the pedal will maintain constant speed. As the car goes up a hill, it will slow down. The difference between the actual speed and the reference value generates an error. This error generates a command to push the accelerator pedal. Pushing the pedal will increase the speed, but there will continue to be a slight error. As the car crests the hill and starts down, the speed will increase. Releasing pedal pressure will slow the acceleration, but an error will remain until a steady state condition is again reached. For this example, the driver's brain is the feedback path. The driver controls the sense of the feedback by knowing when to push and when to release the pedal. By his reaction time, he controls how close to the reference he maintains the car's speed. He may

decide to rapidly change the correction to tightly match the desired speed, or he may choose to compensate slowly so his speed averages out to the correct value. His actions coupled with the car's controls form a system closely analogous to a phase lock loop. Replace the human with an electrical circuit that senses the speed error, include another circuit that tempers the response time, and couple it to the accelerator controls. This is the typical cruise control system. The elements of understanding the operation of a phase lock loop are all available here. The next step is to apply the concepts of this example to the classical elements that make up a PLL.

12.4 PLL BASICS

A PLL is a closed loop system used for frequency control. Several building blocks are common to most PLL designs:

1. The phase detector
2. The loop filter
3. The voltage-controlled oscillator

Figure 12.1 illustrates the connection of these blocks to make a complete phase lock loop. The phase detector has two inputs and one output. This block can be realized by a specialized mixer described in Chapter 11 where the IF port passband goes down to dc. If the two input signals are very close in frequency, then the output will contain a term at twice the input frequency and a term that is almost zero frequency. The loop error signal in the PLL is the near-zero term. This signal contains everything that is needed to control the VCO. This error signal goes to the loop filter for amplification and frequency limiting. The loop filter may be as simple as a capacitor and a resistor, or it can be one or more operational amplifiers with many resistors and capacitors. The loop filter is generally a simple circuit that requires an in depth analysis. It is the "glue" that holds all the other parts together and makes the PLL work the way it is supposed to work. The VCO is the control element of this loop. The input is a control voltage from the loop filter, while the output is the required frequency.

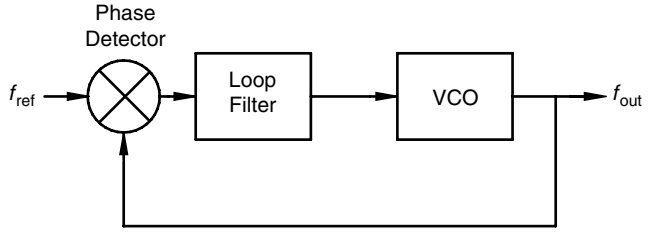


FIGURE 12.1 Basic phase lock loop.

Frequency is the time rate of change of phase, so phase is the time integral of frequency. Consequently, if the frequency of the VCO is proportional to the tuning voltage, the output phase is proportional to the integral of tuning voltage. The output frequency can range from a few Hertz to many GHz. The VCO output becomes the second input to the phase detector.

When the loop is first turned on, the VCO frequency is not controlled. The loop filter output voltage can be anywhere between the high and low limits set by the power supply. However, the phase detector produces an error voltage that is the difference between the VCO frequency and the reference frequency. Like the cruise control example, this signal tells the loop filter whether the VCO is going too fast or too slow relative to the reference frequency. The loop filter is "smart enough" to know what to do. If the error signal indicates that the VCO frequency is less than the reference, the loop filter adjusts the control voltage to raise the VCO frequency. If the VCO frequency is too high, the loop filter changes the voltage and lowers the VCO frequency. The loop filter design sets how fast this happens. Some loops may be designed for a fast bumpy ride, while others may require a slow smooth ride. When the loop filter has done its job, the VCO frequency will exactly match the reference frequency, and the two inputs will have a constant phase difference. This match in frequency and constant phase difference will be maintained even if the reference frequency changes. With each change, the PLL again goes through the settling out process. If the reference is noisy, the PLL is in a continual state of change, working hard to follow the input. If a PLL were nothing more than a box with the same frequency in and out, it would not be much of an invention. Happily there is a lot more to it than that. Before preceding any farther, the basic idea of the frequency control by a closed loop operation must be clarified.

12.5 LOOP DESIGN PRINCIPLES

There are many design rules that go into a successful, stable closed loop design, but many of these details are beyond the scope of his text. However, this discussion will lead to an understanding of how the loop works and how to select parts to customize its operation. From the overall system point of view, the PLL designer must know the overall requirements and be able to translate these requirements into the PLL parameters for the design.

With a PLL, the important top-level parameters are the input and output frequency, the response time, the loop bandwidth and the loop damping ratio. The top-level view concentrates on these system level values. The detailed aspects of the phase detector and VCO must be considered. These are usually high-frequency parts requiring high-frequency design techniques. The design of the loop filter requires an understanding of analog design techniques. Figure 12.2 illustrates the PLL block diagram, which includes a frequency divider in the feedback path. Both frequencies coming into the phase detector must be the locked together at the same frequency. This will force the output frequency,

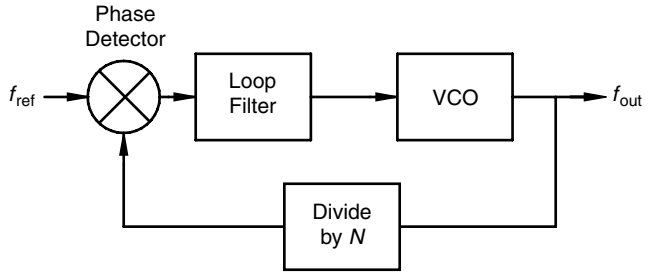


FIGURE 12.2 Phase lock loop with a frequency divider.

f_{out}, to be N times the reference frequency, f_{ref}. Familiarity with digital circuit design is required to complete the design. A PLL design is not just a system design nor an RF design nor an analog design, but it is a combination of all these areas. The actual design process can be summarized by three principles.

1. *Know each component.* The components of a PLL, the VCO, phase detector, loop filter, and frequency divider must be thoroughly understood and tested as stand-alone individual components. Testing of the actual parts must show that they each meet the design goals. These tests may extend far beyond the information on the manufacturer's data sheet.
2. *Test the components together.* The individual components must work correctly when connected together in an open loop configuration. The loop filter must put out enough voltage to drive the VCO. The VCO must have enough output to drive the frequency divider. The phase detector output must be large enough for the loop filter to use. An open loop analysis must show the correct phase margin and bandwidth for stability. These issues are resolved with an open loop analysis.
3. *Compare the closed loop configuration to the design goals.* A closed loop analysis should show that the final connection matches the system level design goals. Both test measurement techniques and analysis can be applied for PLL design verification.

12.6 PLL COMPONENTS

The basic building blocks, except in exotic applications, are those shown in Fig. 12.2. This section describes in greater depth each of these functions.

12.6.1 Phase Detectors

Phase detectors come in many configurations. These include those with logic level inputs, passive and active analog versions, and sampling versions used for high-frequency multiplication. In addition there are phase detectors with automatic

frequency search features to aid in initial frequency acquisition. In its simplest form, a phase detector is a frequency mixer. As described in Chapter 11, when two signals come into the mixer, the output consists primarily in the sum and difference frequencies. The sum frequency is filtered out by the loop filter. The difference frequency, historically called the *beat note*, is typically a few kHz or less in a PLL. If the two input frequencies are exactly the same, the phase detector output is the phase difference between the two inputs. This loop error signal is filtered and used to control the VCO frequency. The two input signals can be represented by sine waves:

$$V_1 = V_a \sin(\omega_1 t + \phi_1) \tag{12.1}$$

$$V_2 = V_b \sin(\omega_2 t + \phi_2) \tag{12.2}$$

The difference frequency term is the error voltage given as

$$V_e = K_m \cdot V_1 \cdot V_2 = \frac{K_m V_a V_b}{2} \cos[(\omega_1 - \omega_2)t + (\phi_1 - \phi_2)] \tag{12.3}$$

where K_m is a constant describing the conversion loss of the mixer. Equation (12.3) gives the time-varying cosine waveform at the beat note frequency. When the two frequencies are identical, the output voltage is a function of the phase difference, $\Delta\phi = \phi_1 - \phi_2$:

$$V_e = \frac{K_m V_a V_b}{2} \cos(\Delta\phi) \tag{12.4}$$

This is maximum when $\Delta\phi = 0^\circ$, a minimum when $\Delta\phi = 180^\circ$, and zero when $\Delta\phi = 90^\circ$ or 270° (Fig. 12.3).

When modeling a PLL in the frequency domain, the phase detector can be modeled as

$$K_{pd} \frac{a}{a + s} \tag{12.5}$$

which at low frequencies is simply the slope of the voltage with relation to the phase curve. The units for K_{pd} is volts/rad:

$$K_{pd} = \frac{dV_e}{d\Delta\phi} = -\frac{K_m V_a V_b}{2} \sin(\Delta\phi) \tag{12.6}$$

Thus $K_{pd} = 0$ when $\Delta\phi = 0^\circ$ or 180° and a maximum absolute value at $\Delta\phi = 90^\circ$ or 270°.

12.6.2 Voltage-Controlled Oscillator

The voltage-controlled oscillator is the control element for a PLL in which the output frequency changes monotonically with the tuning voltage. A linear

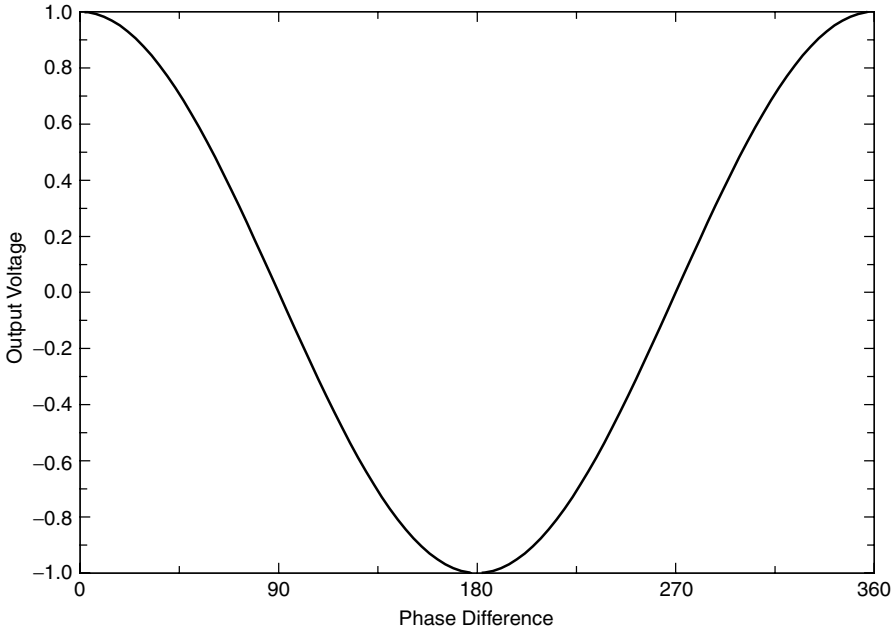


FIGURE 12.3 Phase detector voltage output as function of phase difference.

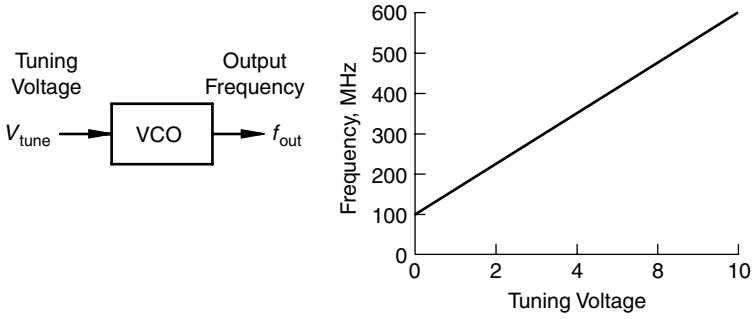


FIGURE 12.4 Voltage-controlled oscillator tuning.

frequency versus tuning voltage is an adequate model for understanding its operation (Fig. 12.4):

$$\omega_{\text{out}} = K_{\text{vco}} \cdot V_{\text{tune}} + \omega_0 \tag{12.7}$$

In a PLL the ideal VCO output phase may be expressed as

$$\phi(t) = \omega_0 t + \int_0^t K_{\text{vco}} V_{\text{tune}} dt + \phi_0 \tag{12.8}$$

where ω_0 is the free-running VCO frequency when the tuning voltage is zero and K_{vco} is the tuning rate with the dimension of rad/s-volt.

The error voltage from the phase detector first steers the frequency of the VCO to exactly match the reference frequency, and then holds it there with a constant phase difference. It is modeled as having a low-frequency gain K_{vco} and one or more poles of the following form:

$$\frac{K_{vco}}{s(s+a)} \tag{12.9}$$

12.6.3 Loop Filters

A loop filter is a low-frequency circuit that filters the phase detector error voltage with which it controls the VCO frequency. While it can be active or passive, it is usually analog and very simple. In extreme cases it might be an entire microprocessor. This discussion will be limited to analog loop filters, such as the representative topologies shown in Fig. 12.5. Figure 12.5*a* shows an op-amp integrator with nearly infinite dc gain. This is the loop filter often associated with the type 2 PLL. The order and type of a PLL is defined in Section 12.9. Figure 12.5*b* shows an op-amp loop filter with a finite gain and is associated with a type 1 PLL. Figure 12.5*c* is a passive filter used with a phase detector whose output is current rather than voltage. This type of detector is frequently found in synthesizer ICs and is associated with a type 2 PLL. While the loop filter is a simple circuit, its characteristic is important in determining the final

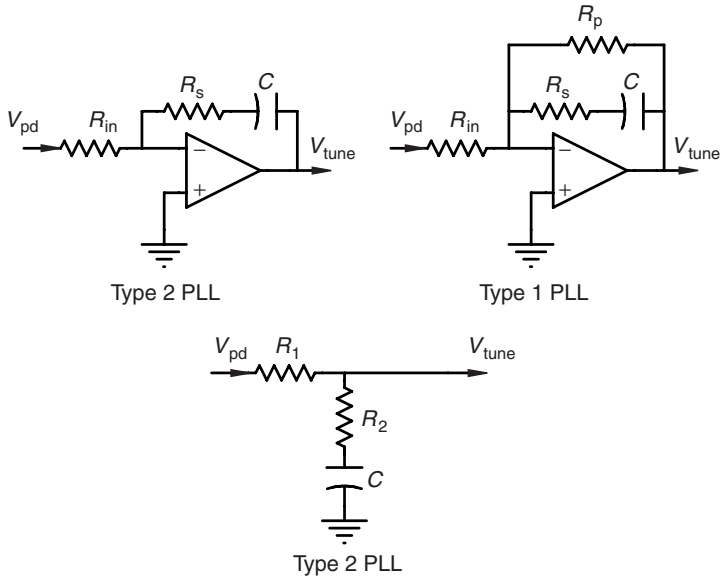


FIGURE 12.5 Loop filter used in a (*a*) type-2 PLL, (*b*) type-1 PLL, and (*c*) type-2 PLL.

closed loop operation. The wrong design will make the loop unstable causing oscillation or so slow that it is unusable. The loop filters shown in Fig. 12.5 are modeled by

$$F(s) = \frac{s + a}{s^n(s + b)(s + c)} \tag{12.10}$$

where a is a zero and b and c are poles.

12.6.4 Frequency Dividers

When the output frequency must be a multiple of the input frequency, frequency dividers may be included in a PLL. Most dividers are a digital circuit, although analog techniques dating from 1939 are available for very high frequency devision. With the availability of complete synthesizers on a single IC, fewer standalone divider circuits are on the market. Most dividers have a division ratio equal to a binary number or switchable from a binary to a binary +1 (e.g., divide by 64 or 65). The upper limit on the input frequency is about 3 GHz, although only a few ICs will go that high. Divide by four circuits has been demonstrated with inputs above 14 GHz, but this is a very specialized device not required by most PLLs. For a linear analysis when the loop bandwidth is much less than the reference frequency, dividers are modeled as a gain element with a value $= 1/N$.

12.7 LINEAR ANALYSIS OF THE PLL [1]†

From the perspective of the time domain, the control voltage for the VCO is

$$V_{\text{tune}}(t) = V_{\text{tune}-0}(t) + \int_0^t v_e(t) f(t - \mu) d\mu \tag{12.11}$$

where $f(t)$ is the impulse response of the filter. Now the Laplace transform of $f(t)$ is

$$F(s) = \int_0^\infty f(t) e^{-st} dt, \qquad t > 0 \tag{12.12}$$

and the inverse transform can be obtained in principle by the contour integral shown below:

$$f(t) = \frac{1}{2\pi i} \int_{-\infty}^{\infty} F(s) e^{st} ds, \qquad \Re s > 0 \tag{12.13}$$

† This material is based on A. J. Viterbi, *Principles of Coherent Communication*, 1966, by permission of the McGraw-Hill Company.

Then the VCO frequency is

$$\frac{d\phi_2(t)}{dt} = \omega_0 + \frac{K_m V_a V_b}{2} \int_0^t f(t-\mu)\cos\Delta\phi(\mu) \tag{12.14}$$

where $\Delta\phi(t) = \phi_1(t) - \phi_2(t)$. Consequently, a the general equation describing the phase error is

$$\frac{d\Delta\phi}{dt} \triangleq \frac{d\phi_1}{dt} - \omega_0 - \frac{K_m V_a V_b}{2} \int_0^t f(t-\mu)\cos\Delta\phi(\mu)d\mu \tag{12.15}$$

For a given input phase ϕ_1, the solution of this equation describes the exact operation of the PLL. However, to avoid carrying along ω_0, a new phase variable may be defined:

$$\psi_1(t) \triangleq \phi_1(t) - \omega_0 t \tag{12.16}$$

$$\psi_2(t) \triangleq \phi_2(t) - \omega_0 t \tag{12.17}$$

The equation for the phase error is now given without ω_0:

$$\frac{d\Delta\phi}{dt} = \frac{d\psi_1}{dt} - \frac{K_m V_a V_b}{2} \int_0^t f(t-\mu)\cos\Delta\phi(\mu)d\mu \tag{12.18}$$

This suggests an alternate representation for the phase lock loop shown in Fig. 12.6. In this representation the multiplier is replaced by a subtracter and a cosinusoidal nonlinearity, while the VCO is replaced by an integrator.

When the phase error $\Delta\phi$ deviates from 90° by a small amount, $\cos(\Delta\phi + 90°) \approx \Delta\phi$. Then Eq. (12.18) becomes

$$\frac{d\psi_1}{dt} = \frac{d\Delta\phi}{dt} + K\int_0^t f(t-\mu)\Delta\phi(\mu)d\mu \tag{12.19}$$

where

$$K = \frac{K_m V_a V_b}{2} \tag{12.20}$$

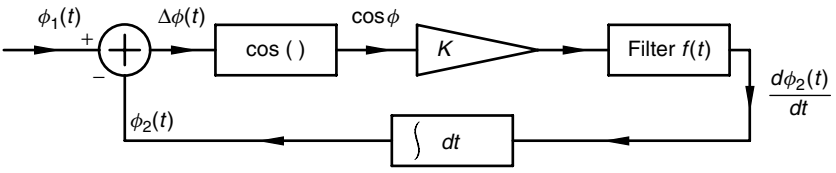


FIGURE 12.6 Time domain nonlinear phase lock loop.

If the Laplace transform of $\psi_1(t)$ is represented by $\tilde{\psi}(s)$ and the Laplace transform of $\Delta\phi(t)$ is represented by $\Delta\tilde{\phi}(s)$, then the Laplace transform of Eq. (12.19) is

$$s\Delta\tilde{\phi}(s) + KF(s)\Delta\tilde{\phi}(s) = s\tilde{\psi}_1(s) \tag{12.21}$$

This linear frequency domain equation for the PLL can be represented as shown in Fig. 12.7.

The solution for the phase error gives

$$\Delta\tilde{\phi}(s) = \frac{\tilde{\psi}_1(s)}{1 + KF(s)/s} \tag{12.22}$$

so that the phase shift at the output of the PLL is

$$\begin{aligned} \tilde{\psi}_2(s) &= \tilde{\psi}_1(s) - \Delta\tilde{\phi}(s) \\ \frac{\tilde{\psi}_2(s)}{\tilde{\psi}_1(s)} &\triangleq P(s) = \frac{G(s)}{1 + G(s)} \end{aligned} \tag{12.23}$$

where $G(s) = V_a V_b K_m/2F(s)/s$. The phase error can in turn be written in terms of this transfer function:

$$\Delta\tilde{\phi}(s) = \tilde{\psi}_1(s) - \tilde{\psi}_2(s) = [1 - P(s)]\tilde{\psi}_1(s) \tag{12.24}$$

If, for example, the phase of the incoming signal is $\phi_1(t) = \omega t + \phi_0$ and the PLL has no filter, $F(s) = 1$. Readjusting the phase reference as was done in Eqs. (12.16) and (12.17) gives

$$\psi_1 = \phi_1 - \omega_0 t \tag{12.25}$$

$$= (\omega - \omega_0)t + \phi_0 \tag{12.26}$$

In the frequency domain this becomes

$$\tilde{\psi}_1(s) = \frac{\omega - \omega_0}{s^2} + \frac{\phi_0}{s} \tag{12.27}$$

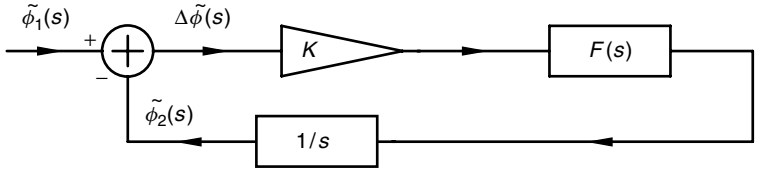


FIGURE 12.7 Frequency domain linear phase lock loop.

The phase error is found from Eq. (12.22):

$$\Delta\tilde{\phi}(s) = \frac{1}{K/s}\left[\frac{\omega - \omega_0}{s^2} + \frac{\phi_0}{s}\right] \tag{12.28}$$

The inverse transform in this case is straightforward and gives the phase error in the time domain:

$$\Delta\phi(t) = \frac{\omega - \omega_0}{K}(1 - e^{-Kt}) + \phi_0 e^{-Kt} \tag{12.29}$$

The steady state phase error is found by allowing $t \to \infty$:

$$\Delta\phi(t = \infty) = \frac{\omega - \omega_0}{K} \tag{12.30}$$

Clearly, the phase will change when the incoming frequency changes, so that phase lock is not achieved.

The insertion of a low-pass filter into the PLL will produce lock. An active filter such as that shown in Fig. 12.8 is recognized as basically a noninverting amplifier. The inverting amplifier has right half-plane poles and is therefore unstable. For the noninverting case the voltage gain can be found by writing node equations at the input nodes of the operational amplifier:

$$F(s) = \frac{V_o}{V_i} = 1 + \frac{R_2 + 1/sC}{R_1} = \left(1 + \frac{R_2}{R_1}\right) + \frac{1}{sCR_1} \tag{12.31}$$

The phase transfer factor is found from Eq. (12.23):

$$P(s) = \frac{\tilde{\psi}_2(s)}{\tilde{\psi}_1(s)} = \frac{K[(1 + R_2/R_1)R_1Cs + 1]}{s^2CR_1 + CR_1K(1 + R_2/R_1)s + K} \tag{12.32}$$

Thus, using Eq. (12.24), the phase error is easily obtained:

$$\Delta\tilde{\phi}(s) = [1 - P(s)]\psi_1(s) \tag{12.33}$$

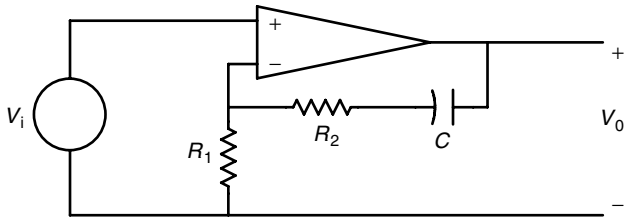


FIGURE 12.8 Possible active low-pass filter for the PLL.

$$\Delta\tilde{\phi}(s) = \frac{(\omega - \omega_0)CR_1 + \phi_0 CR_1 s}{s^2 CR_1 + CR_1 K(1 + R_2/R_1)s + K} \tag{12.34}$$

Rather than find the inverse transform this time, the final value theorem may be used to find the steady state phase error:

$$\lim_{t\to\infty} \Delta\phi(t) = \lim_{s\to 0} s\Delta\tilde{\phi}(s) = 0 \tag{12.35}$$

In this case the phase error is independent of frequency and in the steady state is zero.

12.8 LOCKING A PHASE LOCK LOOP

The previous sections examined each of the elements in a PLL. As an example of how these parts go together, consider a simple loop with no frequency divider. Also assume that initially the loop is not locked and that the reference frequency is 100 MHz. A VCO tuning voltage of 5 volts is required to make the VCO frequency be 100 MHz. The phase detector can produce a cosine wave beat note of 1 volt peak to peak.

To simplify the design, a type 1 loop filter will be used. This is an inverting op-amp circuit with a gain of 100 at low frequency and a gain of 0.1 at high frequency (Fig. 12.9). With the loop unlocked, the VCO frequency could be anywhere within its operating limits. Assume that it is operating at 101 MHz, so that there is a 1 MHz beat note at the phase detector output when the reference frequency is first applied. This beat note frequency is high enough to only be amplified with a gain of 0.1 by the loop filter. The VCO tuning voltage will be modulated by the phase detector output of 0.1 volt peak to peak, but this voltage will not cause any significant change in the VCO frequency.

With the VCO frequency too far away from the reference frequency, there is not enough gain in the loop to bring the loop into lock. However, if the VCO

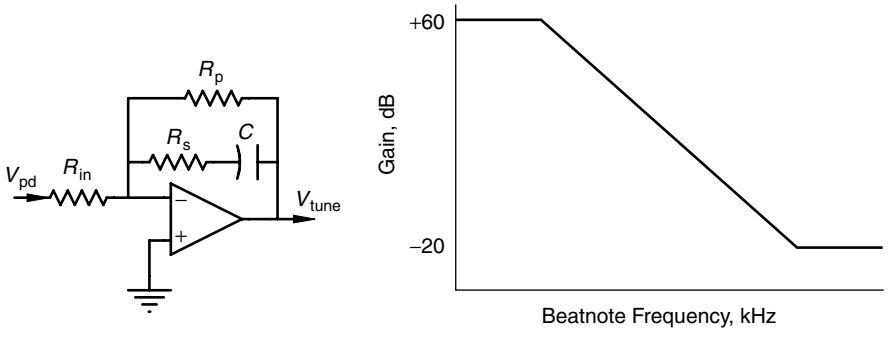


FIGURE 12.9 (*a*) Type 1 loop filter and (*b*) its frequency response.

frequency is 100.1 MHz when the reference frequency was applied, the beat note frequency would be 100 kHz. That is well within the high-gain frequency range of the loop filter for this design. The amplified beat note voltage modulates the VCO frequency. As the VCO frequency swings closer to the reference frequency, the beat note frequency gets even lower, it enters an even higher-gain region of the loop filter. This action accelerates the VCO frequency change until it crosses the reference frequency. At this point the beat note frequency is zero. The PLL has been designed as a stable closed loop system, and the VCO is at the same frequency as the reference. The transient phase detector output voltage and the VCO tuning voltage are shown in Figs. 12.10 and 12.11, respectively. The input voltage to the VCO is 5 volts when the PLL is at frequency lock. Since the loop filter has a dc inverting gain of 100, the voltage at the phase detector output is

$$V_e = \frac{4}{-100} = -50 \text{ mV} \tag{12.36}$$

The maximum voltage it could reach is 1.0 volt, so from Eq. (12.4) the phase difference is $\Delta\phi = \arccos(V_e/0.5 \cdot 1.0) = 95.7^\circ$. The loop filter will keep the VCO at 100 MHz and maintain a 95.7° phase difference between the two phase detector inputs.

An oscillator accumulates 360° of phase rotation in each cycle. If the frequency increases it will accumulate more phase rotation in a given period of time. If the VCO tries to drift higher in frequency, it will quickly accumulate more phase rotation. The phase detector output voltage will go up, and the loop filter will amplify this change, which will lower the VCO control voltage. The VCO output

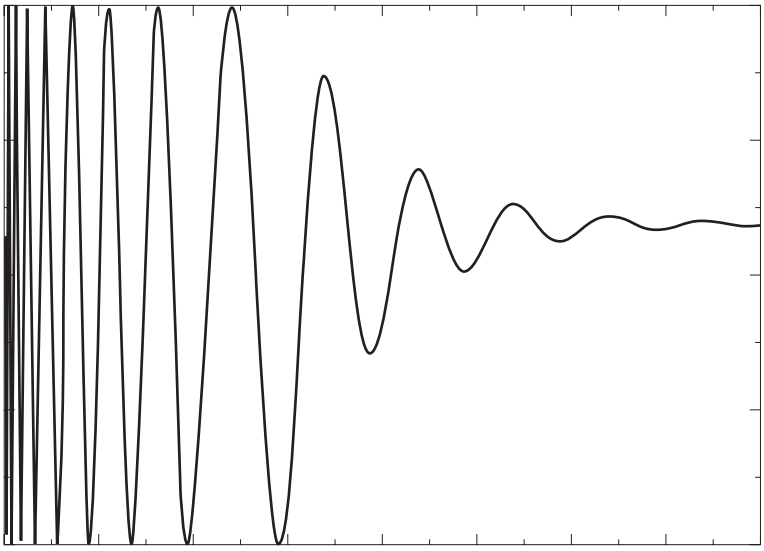


FIGURE 12.10 Phase detector voltage as the PLL pulls into lock.

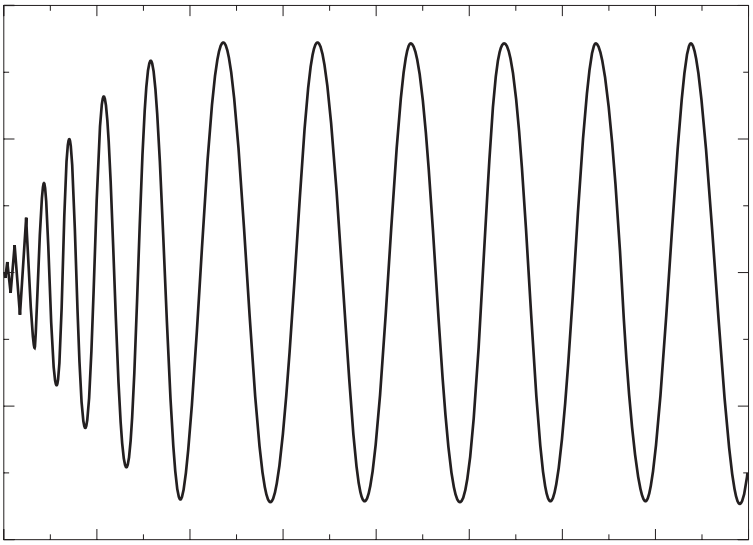


FIGURE 12.11 VCO tuning voltage as PLL pulls into lock.

frequency will drop and return to 100 MHz. The situation is similar for the VCO trying to move lower in frequency. This is the effect of the negative feedback within the loop. The battle for control goes on continuously. Small changes in the VCO due to temperature, noise, or even gravity cause small frequency changes. The PLL will not tolerate errors due to frequency or phase changes. When an error voltage develops at the phase detector output, the loop filter will amplify it, and the VCO frequency and phase will return to the correct value. The corrective action of the loop will make whatever adjustments are required to hold the phase and frequency constant.

It is important to understand that the initial beat note frequency must be well within the loop filter's bandwidth to achieve lock without frequency aiding. In any loop the first event is to bring the VCO frequency in line with the reference frequency. Once the circuit is in lock, a steady state phase relationship that satisfies the loop feedback and dc requirements is found and that will hold its lock frequency.

12.9 LOOP TYPES

The PLL is a closed loop system controlled by negative feedback. The closed loop gain P(s) is described by

$$H(s) = \frac{G(s)}{1 + G(s)/N} \tag{12.37}$$

where $G(s)$ is the open loop or forward gain, and $G(s)/N$ is called the *loop gain*. For this discussion, the forward gain G(s) is the product of the phase detector gain, the loop filter gain, and the VCO gain. The frequency divide ratio is N.

The number of pure integrators (or number of poles at the frequency origin) in the denominator of Eq. (12.37) determines the type of the system. This can be produced by an op-amp integrator with near-infinite dc gain. Obviously this cannot be produced with a passive filter where the maximum gain is 1. A VCO is a pure phase integrator that will contribute one pole to the type determination. Therefore a PLL will be at least type 1. A loop filter with a finite dc gain will not increase the type number. A loop filter with an integrator will increase the type to 2.

The order of the PLL is the degree of the denominator polynomial of Eq. (12.37). The loop filter op-amp has at least two significant breakpoints: one at a frequency between 1 and 100 kHz and a second above 10 MHz. The VCO has frequency roll-offs in its modulation performance. A low-pass filter may be included in the phase detector output to further reduce the unwanted high frequencies.

In the previous example using a type 1 loop, the only pure integrator is the VCO, so there is only one pole at dc. The loop filter has a dc inverting gain of 100. If the VCO gain is 1 MHz/volt and the reference frequency is changed to 103 MHz, the VCO tuning voltage will now be 8 volts. With a gain of -100, the phase detector voltage must be $V_e = 8/(-100) = -80$ mV.

This represents an angular difference of $\Delta\phi = \arccos(V_e/0.5 \cdot 1.0) = 99.7^\circ$ in contrast to 95.7° found earlier when the reference frequency was 100 MHz. The phase difference between the VCO and reference frequency was 95.7 degrees. If the reference frequency continues to change, the VCO frequency will change to match it, which in turn will change the phase detector output voltage. As the reference frequency changes in a type 1 loop, the phase difference changes. This is an important characteristic that is sometimes desirable and other times unacceptable.

If the dc gain of the loop filter is increased to 1000, the phase detector output voltage for a 100 MHz lock is only -5 mV. For phase lock at 103 MHz, the phase detector output voltage is -8 mV. These values represent phase differences, $\Delta\phi$, of 90.57° and 90.92°, respectively. If the dc gain is further increased, the change of $\Delta\phi$ with frequency will further decrease. If the gain is increased to the limit, the dc feedback resistor, R_p, will approach an open circuit, and the loop filter dc gain will increase to infinity. The loop filter in Fig. 12.5*b* is transformed to that shown in Fig. 12.5*a*.

This loop filter is now a pure integrator. The total number of integrators for the PLL with this loop filter is two: one for the VCO and one for the loop filter. This loop filter used in a PLL creates a type-2 loop. Among the features of this loop is the constant phase shift between the VCO and reference frequency that is maintained with a change in frequency.

Type-1 and type-2 loops constitute the majority of applications. Type-3 and higher loops are required to solve frequency change problems in unusual

situations. For example, a ground-launched missile must track an orbiting satellite during its own launch and orbital insertion. During the launch phase, the rocket is consuming fuel and thus reducing its mass. With a constant force, its acceleration will be increasing at an increasing rate. As the satellite comes overhead its transmit frequency is shifted due to the relative motion with the rocket. This shift is constantly changing at an increasing rate. Then the booster separates from the rocket, and the force goes to zero during coast. To track the satellite frequency with no phase error requires a PLL type of at least four. Most high-type loops are used to solve complicated motional problems. This discussion will not cover the design details of loops of a type higher than two.

12.10 NEGATIVE FEEDBACK IN A PLL

A frequency change that generates a change in the phase of a stable negative feedback loop generates a correction for the phase error. In the previous example the type 1 loop filter was described as having a dc inverting gain of 100. The VCO requires 5 volts to produce a 100 MHz output. An open loop connection of the PLL components will demonstrate what is called the "sense" of the loop. For open loop testing the VCO is connected to a manually adjustable power supply. With the power supply set at 5 volts, there will be a low-frequency beat note observed at the phase detector output. If the voltage is changed to either 4 or 6 volts, the beat note will be 1 MHz. With a mixer as the loop phase detector, the beat note will be a cosine wave at the difference frequency, 1 MHz. The frequency of the VCO cannot be determined from looking at the beat note. The beat note shows the frequency difference between the two signals, but it does not tell which signal is the higher or lower frequency. A complete description of the difference frequency between the VCO and reference requires both a direction and a magnitude. With the loop out of lock, this type of phase detector can only determine magnitude, $|\Delta\phi|$. The VCO frequency must be forced close enough to the reference frequency for the beat note to be inside the loop bandwidth for a PLL with this type of phase detector to pull into phase lock.

In the previous example the VCO frequency increased as the tuning voltage increased. Many VCOs have the opposite characteristic; that is, the frequency decreases with increased tuning voltage. This difference does not change the stability or operation of the closed loop if a mixer is used as the phase detector. If the loop locked up at 90° difference between the two inputs with the positive slope VCO, it will lock up at 270° with the negative slope VCO. The phase detector output in either case will be correct to speed up or slow down the VCO to match the reference input frequency and phase.

Most synthesizer ICs and PLLs using frequency dividers or logic ICs have a different type of phase detector. Using flip-flops to count the input edges, these phase detectors produce an error voltage that has not only a magnitude but also a sense of the direction between the two inputs. The output is a series of voltage or current pulses. The loop filter averages these pulses to form the control voltage

for the VCO. A pulse duty cycle above 50% indicates that the VCO frequency is higher than the reference frequency, and a duty cycle of less than 50% indicates that the VCO frequency is lower. If the VCO is running faster than the reference frequency, the control voltage will force it toward the correct value. If the VCO is running too low, the error voltage will drive the frequency higher. This type of phase detector can drive a PLL into lock even when the VCO and reference frequencies are a great distance apart, far outside the loop bandwidth. The typical IC synthesizer will have a pin available to reverse the sense of the error voltage to accommodate VCOs of either positive or negative tuning slope.

12.11 PLL DESIGN EQUATIONS

A phase lock loop design requires the basic understanding of the locking mechanism as previously discussed. However, the values for the loop filter and other components must be carefully selected to assemble a stable loop. These values can be both analyzed and synthesized using basic closed loop equations and linear algebra.

The normal phase lock loop model includes a phase detector, a loop filter, a VCO and a frequency divider connected as shown in Fig. 12.12. Each block is described by a gain value that may be a constant or a function of frequency. The frequency response of the closed loop is typically displayed as a Bode plot with a minimum frequency of 1 Hz and a maximum frequency between 10 kHz and 10 MHz. This describes the filtering bandwidth and in turn the transient response of the PLL to the input voltage spectrum, V_{in}.

12.11.1 Inverting Loop Filter

The analysis proceeds by writing the voltage equations at points V_{e} and V_{o}. Combining these equations produces the well-known equation for closed loop gain of a system with negative feedback. When K_{pd} is the phase detector gain, $F(s)$, is the noninverting loop filter function, and K_{vco}/s is the VCO gain, the

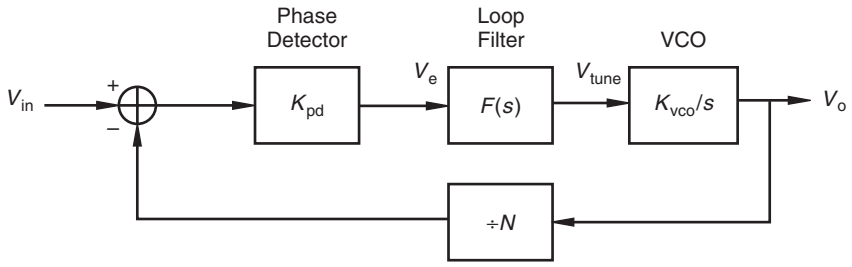


FIGURE 12.12 Frequency domain closed loop model for a PLL.

error voltage is easily found:

$$V_e = \left(V_{in} - \frac{V_o}{N}\right) K_{pd} \tag{12.38}$$

$$V_o = \left(V_{in} - \frac{V_o}{N}\right) \cdot \left(K_{pd} F(s) \frac{K_{vco}}{s}\right) \tag{12.39}$$

This is solved for the voltage transfer function:

$$H(s) \triangleq \frac{V_o}{V_{in}} = \frac{K_{pd} F(s) K_{vco}/s}{1 + \{[K_{pd} F(s) K_{vco}/s]/N\}}$$

$$= \frac{G(s)}{1 + G(s)/N} \tag{12.40}$$

A similar analysis for a PLL with an inverting loop filter gives a similar equation except for a sign reversal. Positive feedback is used at the summer block since the sign reversal has already occurred in the inverting amplifier:

$$H(s) = \frac{G(s)}{1 - G(s)/N} \tag{12.41}$$

In either case, when the gain, $G(s)$, is large, $|H(s)| \approx N$.

These equations for closed loop gain can now be used to determine the loop filter values required for a desired bandwidth and damping ratio. The procedure initially assumes a second-order type-1 loop, since that is most frequently used. A type 2 loop can then be easily derived. The transfer function for the filter in Fig. 12.5*b* is

$$F(s) = -\frac{R_p \| [R_s + (1/Cs)]}{R_{in}}$$

$$= -\frac{(R_p R_s / R_{in}) sC + (R_p / R_{in})}{(R_p + R_s) sC + 1} \tag{12.42}$$

The open loop gain is

$$G(s) = \frac{F(s) K_{pd} K_{vco}}{s} \tag{12.43}$$

For a type 1 PLL, $R_p \to \infty$ and

$$F(s) = -\frac{R_s sC + 1}{R_{in} sC} \tag{12.44}$$

When Eqs. (12.43) and (12.44) are substituted into the expression for the gain of the closed loop PLL, Eq. (12.41), the result is clearly of second order in

the denominator:

$$H(s) = -\frac{[K_{pd}K_{vco}(R_p + sCR_s)R_p/R_{in}]/C(R_p + R_s)}{s^2 + s[1/C(R_p + R_s) + (K_{pd}K_{vco}/NR_{in})(R_pR_s/R_p + R_s)] + [K_{pd}K_{vco}R_p/NR_{in}C(R_p + R_s)]} \tag{12.45}$$

The denominator can be converted to the familiar form used in control theory, $s^2 + 2\zeta\omega_n s + \omega_n^2$ where ζ is the damping factor and ω_n is the natural frequency of the system. In this case,

$$\omega_n = \sqrt{\frac{K_{pd}K_{vco}R_p}{NR_{in}C(R_p + R_s)}} \tag{12.46}$$

$$\zeta = \frac{(1/C) + (K_{pd}K_{vco}R_pR_s/NR_{in})}{2\omega_n(R_p + R_s)} \tag{12.47}$$

For the type-2 PLL when $R_p \to \infty$,

$$\omega_n = \sqrt{\frac{K_{pd}K_{vco}}{NCR_{in}}} \tag{12.48}$$

and

$$\zeta = \frac{K_{pd}K_{vco}R_s}{NR_{in}2\omega_n} \tag{12.49}$$

The design specification for a PLL is typically given in terms of a damping ratio and natural frequency. The design task is to determine circuit values that will meet these specifications. For ease of writing, define

$$K_t \triangleq \frac{K_{pd}K_{vco}}{N} \tag{12.50}$$

Furthermore, the filter response at dc is

$$F_{dc} = -\frac{R_p}{R_{in}} \tag{12.51}$$

Thus Eq. (12.46) can be rearranged to give

$$R_p + R_s = -\frac{K_tF_{dc}}{C\omega_n^2} \tag{12.52}$$

and this substituted into Eq. (12.47) to give

$$R_p + R_s = -\frac{K_tF_{dc}}{C\omega_n^2} = \frac{1}{2C\omega_n\zeta} - \frac{K_tF_{dc}R_s}{2\omega_n\zeta} \tag{12.53}$$

Using Eq. (12.52) to replace R_s above,

$$-\frac{K_t F_{dc}}{C\omega_n^2} = \frac{1}{2C\omega_n\zeta} - \frac{K_t F_{dc}}{2\omega_n\zeta}\left(\frac{-F_{dc}K_t}{C\omega_n^2} - R_p\right) \tag{12.54}$$

If, in addition to the damping ratio and the natural frequency, values for C and the dc gain are chosen, then the required resistance values can be found as summarized below. Solution of Eq. (12.54) gives the value for R_p.

$$\begin{aligned} R_p &= \frac{1}{K_{pd}K_{vco}C}\left[\frac{2\zeta K_{pd}K_{vco}}{\omega_n} + \frac{K_{pd}K_{vco}F_{dc}}{N\omega_n^2} - \frac{N}{F_{dc}}\right] \\ &= \frac{1}{K_t C}\left[\frac{2\zeta K_t}{\omega_n} + \frac{K_t F_{dc}}{N\omega_n^2} - \frac{1}{F_{dc}}\right] \end{aligned} \tag{12.55}$$

$$\begin{aligned} R_s &= -\frac{K_{pd}K_{vco}F_{dc}}{NC\omega_n^2} - R_p \\ &= -\frac{K_t F_{dc}}{C\omega_n^2} - R_p \end{aligned} \tag{12.56}$$

$$R_{in} = -\frac{R_p}{F_{dc}} \tag{12.57}$$

The type 2 PLL equations are found by allowing $R_p \to \infty$.

Figure 12.13 illustrates the expected PLL bandwidth verses frequency for several values of damping ratio. These results are calculated for a second-order loop with a natural frequency of 1 Hz. The results can be easily scaled for loops requiring higher natural frequencies. When $\zeta < 1$, the PLL is under damped and peaking occurs. The response of such a loop to a disturbance will be a damped oscillation that finally converges to the final answer. When $\zeta > 1$, the PLL is overdamped. The -3 dB gain frequency for a damping of 1.0 is 2.4 Hz. If a -3 dB frequency of 50 kHz were required with a damping of 1.0, then a natural frequency of 20.833 kHz would be chosen. The requirements of the PLL design and the available parts will determine the best choice for the natural frequency and damping ratio.

A second-order loop can be built either as type 1 or type 2 with either an inverting or noninverting loop filter. The actual loop order may be several orders higher than 2 when all the extraneous poles are considered. A good design procedure initially ignores these poles and assumes ideal VCOs, phase detectors, op-amps, and so on, with which it determines a set of loop filter values based on the second-order model. Subsequently nonideal parts can then be added to the model and the analysis refined as more values become available. Computer modeling is encouraged for this process.

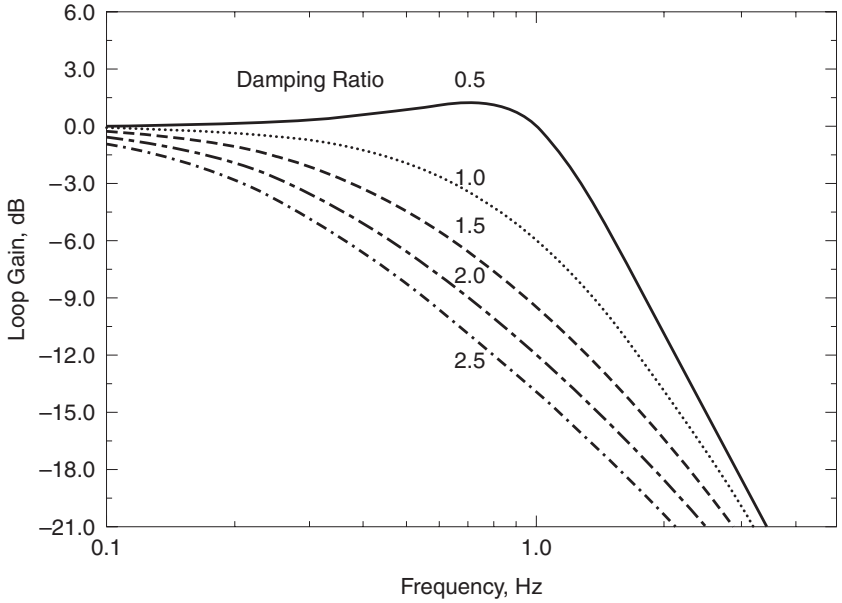


FIGURE 12.13 PLL response with natural frequency of 1 Hz and various damping ratios.

12.11.2 Noninverting Loop Filter

Design equations can be developed for a noninverting loop filter like that shown in Fig. 12.5. The filter transfer function is

$$F(s) = 1 + \frac{R_p \| [R_s + (1/sC)]}{R_{in}}$$
$$= \frac{1 + (R_p/R_{in}) + sC[(R_p R_s/R_{in}) + R_p + R_s]}{1 + sC(R_p + R_s)} \tag{12.58}$$

The closed loop gain is found by substituting Eq. (12.58) into Eq. (12.37) while making use of Eq. (12.50):

$$H(s) = \frac{NK_t\{1 + (R_p/R_s) + sC[(R_p R_s/R_{in}) + R_p + R_s]\}}{s[1 + sC(R_p + R_s)] + \{1 + (R_p/R_{in}) + sC[1 + (R_p R_s/R_{in}) + R_p + R_s]\}K_t} \tag{12.59}$$

$$= \frac{[NK_t/C(R_p + R_s)]\{1 + (R_p/R_s) + sC[(R_p R_s/R_{in}) + R_p + R_s]\}}{s^2 + s\{[1/C(R_p + R_s)] + [R_p R_s K_t/(R_p + R_s)R_{in}] + K_t\} + [(R_{in} + R_p/(R_p + R_s)]K_t/C)} \tag{12.60}$$

From this the loop natural frequency and damping ratio can be identified:

$$\omega_n = \sqrt{\frac{(R_{in} + R_p)K_t}{(R_p + R_s)R_{in}C}} \tag{12.61}$$

$$\zeta = \frac{R_{in} + CR_pR_sK_t + R_{in}(R_p + R_s)CK_t}{2\omega_n C(R_p + R_s)R_{in}} \tag{12.62}$$

The typical synthesis procedure is to design a PLL with a given natural frequency and damping ratio using a specified capacitance, C. Solving Eq. (12.61) for $R_p + R_s$ and substituting this into Eq. (12.62) gives an equation in terms of one unknown, R_p. First, from Eq. (12.61),

$$R_s = \frac{K_t(R_p + R_{in})}{R_{in}C\omega_n^2} - R_p \tag{12.63}$$

then substitution gives

$$\frac{K_t(R_p + R_{in})}{R_{in}C\omega_n^2} = \frac{1}{2\zeta\omega_n CR_{in}}\left[R_{in} + CR_pK_t\left(\frac{K_t(R_{in} + R_s)}{R_{in}C\omega_n^2} - R_p\right) + CK_tR_{in}\frac{K_t(R_{in} + R_p)}{R_{in}C\omega_n^2}\right] \tag{12.64}$$

This has one unknown, R_p, that can be solved by the quadratic formula as follows:

$$0 = R_p^2(K_t^2 - CK_tR_{in}\omega_n^2) + R_p2K_tR_{in}(K_t\zeta - \omega_n) + R_{in}^2(\omega_n^2 + K_t^2 - 2\zeta K_t\omega_n) \tag{12.65}$$

So, if

$$a = K_t^2 - CK_tR_{in}\omega_n^2 \tag{12.66}$$

$$b = 2K_tR_{in}(K_t\zeta - \omega_n) \tag{12.67}$$

$$c = R_{in}^2(\omega_n^2 + K_t^2 - 2\zeta K_t\omega_n) \tag{12.68}$$

then

$$R_p = \frac{-b + \sqrt{b^2 - 4ac}}{2a} \tag{12.69}$$

Again, the value of R_{in} is associated with the voltage gain of the noninverting loop filter:

$$R_{in} = \frac{R_p}{F_{dc} - 1} \tag{12.70}$$

The value for R_s is obtained from Eq. (12.63).

The type 2 PLL parameters with the noninverting loop filter can be found by letting $R_p \to \infty$. Thus the design equations for a given natural frequency, damping ratio, and capacitance are

$$\omega_n^2 = \frac{K_t}{R_{in}C} \tag{12.71}$$

or

$$R_{in} = \frac{K_t}{C\omega_n^2} \tag{12.72}$$

and the damping ratio is

$$2\omega_n\zeta = 0 + \frac{R_s K_t}{R_{in}} + K_t \tag{12.73}$$

or

$$R_s = R_{in}\frac{2\omega_n\zeta - K_t}{K_t} \tag{12.74}$$

The value for K_t is given by Eq. (12.50).

12.12 PLL OSCILLATORS

A phase lock loop will have a least two oscillators associated with it: the reference oscillator and the voltage controlled oscillator. The reference is typically a fixed frequency, but in some applications it may change over a wide frequency range. In any event, the VCO must be able to follow it.

The types of oscillators used depend on the design requirements and the frequency range. Low-frequency oscillators use a resistor capacitor combination to set the frequency. A larger charging current in the capacitor results in a higher-oscillation frequency. These oscillators can be used from a few hertz to several megahertz. They can sweep a wide frequency range, but the output is usually noisy and drifts rapidly with temperature. This oscillator is frequently found in simple PLL ICs.

An LC oscillator's frequency is set by a combination of inductors and capacitors in a resonant circuit. This oscillator is useful from about 100 kHz to somewhat above 5 GHz. A high Q network will produce a very clean output with a small tuning range. Frequency control of a voltage-controlled version can be built either by varying a dc voltage in the circuit or, more commonly, by adding a voltage-controlled capacitor, called a *varactor diode*, to the resonant network. A varactor is a low-loss reverse-biased diode whose depletion capacitance has been optimized for large change with changes in bias. Reverse-biased voltages range from about 2 volts to 28 volts. Capacitance values range from fractions of a pF to 500 pF.

Oscillator design at any frequency is a specialized area. The design or purchase of either the reference oscillator or the VCO is an activity that should be completed before the PLL design is attempted. Available power supply voltages will determine the tuning voltage available for the VCO. Simulations can determine an approximate tuning rate for the VCO, from which an appropriate oscillator type can be picked from the various available types and manufacturer's data sheets. The characteristics of both oscillators should be well defined.

12.13 PHASE DETECTOR TYPES

Previous sections have introduced both the mixer and flip-flop-based phase detectors. These are the two main configurations that are widely used, although there are many specialized variations of each type. A sampling phase detector is a third type that is frequently used in RF and microwave applications. A careful study of the design requirements will usually point to the correct choice.

12.13.1 Mixer Phase Detectors

Mixers with a dc coupled output make an excellent phase detector. At high frequencies, a mixer may be either active (with transistors) or passive (with diodes). The diode versions provide better dc stability and are generally preferred. The diode mixer is the best choice for low-noise designs or when the PLL reference input is a low-level signal buried in noise. When the PLL is locked and running closed loop, both frequencies will be exactly the same. The two inputs are applied to the RF and local oscillator (LO) ports of the mixer, and the beat note output comes from the intermediate frequency (IF) port. The IF port is loaded with a total resistance of 50 to 1000 Ω. Blocking capacitors are used to ac couple the signals into the two input ports, but the IF output port must not be ac coupled. A mixer must be chosen that is appropriate for the frequency range and power level of the inputs. The beat note output is typically 100 mV to 1 volt peak to peak, depending on the mixer type and application. The mixer type phase detector is the best choice when the input signal is pulsed or noncontinuous. The ability of this type of detector to resolve an angular difference is limited to $\pm 90^\circ$. It has no ability to determine which input is the higher frequency. Thus it is not capable of frequency discrimination.

12.13.2 Sampling Phase Detectors

Sampling phase detectors (SPD) can be used in a phase lock loop to produce an output frequency that is an integer multiple of the reference frequency. This mixer relies on a device to generate a comb of frequencies at multiples of the reference. The VCO then mixes with the correct spectral line to produce an error signal. A SPD is used in a phase lock loop where the output frequency is an integer multiple of the input frequency. If $f_{\text{out}} = N \cdot f_{\text{in}} + \Delta f$, the SPD output

is a cosine wave of frequency Δf. If f_{out} is exactly N times f_{in}, the SPD output is a dc level proportional to the phase difference between its two inputs. The input frequency, f_{in}, is typically between 50 and 200 MHz at a power level of +20 dBm or higher, and f_{out} can be at any harmonic of f_{in} up to 18 GHz. The low-frequency high-power input signal produces a comb of spectral lines inside the SPD where lines up to the 150th multiple are useful.

A sampling phase detector is one of the best choices for a very high frequency PLL where excellent phase noise is a requirement. However, an external circuit is usually required to bring the VCO into lock range. Additionally provisions must be made to ensure that the VCO will be locked to the correct multiple of f_{in}.

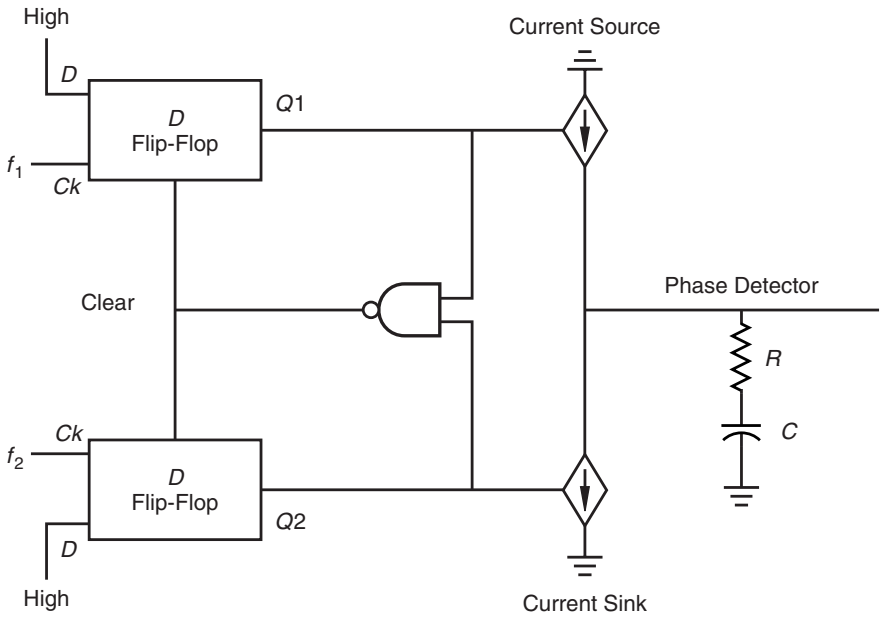
12.13.3 Flip-Flop Phase Detector with Frequency Acquisition Aiding

All of the other phase detectors previously discussed have a major drawback. They produce an output equal to the difference between the two input frequencies, either a cosine wave or a triangle wave. However, this output does not have information about whether the VCO is too high in frequency or too low. A PLL using these phase detectors must also include a sweep or search circuit to initially bring the VCO close enough to lock. This can involve a substantial amount of circuitry. The phase detector circuit shown in Fig. 12.14*a* uses positive edge triggered *D* type flip-flops to overcome this problem. The *D* inputs are connected to a logic 1. Figure 12.14*b* illustrates the timing sequence. The signal, f_1 positive edge arrives first causing $Q1$ to clock high. Later positive edge of f_2 causes $Q2$ to clock high. Two 1's at the NAND gate's input cause its output to go low and clear both $Q1$ and $Q2$. The output at $Q2$ is a pulse whose duty cycle represents the time delay between f_1 and f_2. The pulse at $Q2$ is very short, being the sum of the propagation times through the flip-flops and gates. Of course, if f_2 arrives before f_1, then the output pictures are reversed.

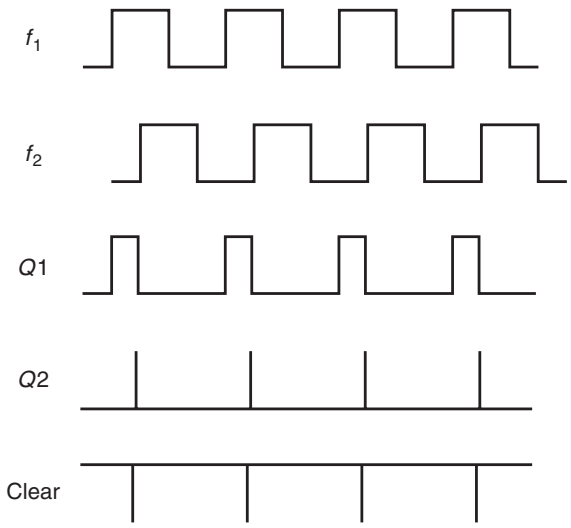
The outputs, $Q1$ and $Q2$, turn on the current sources. These current sources either source or sink current to the capacitor which ramps up or down the phase detector output voltage. The action of this circuit is identical to the op-amp integrator. So the phase detector has added another integrator to the PLL. A PLL using this circuit will be at least a type 2 loop.

The advantage to this circuit is the self-searching capability. If f_1 is higher than f_2, the output voltage will go to the positive voltage limit. If f_1 is lower than f_2, the output voltage will go to the negative voltage limit. If f_1 equals f_2, the output voltage will be proportional to the phase difference. Thus this circuit can sense which input frequency is higher. The output voltage can then be used to drive the VCO in the correct direction to bring the loop into lock. Once the two frequencies are the same, this circuit becomes a phase detector and drives the VCO for no phase error.

This phase detector circuit is used in many present-day frequency synthesizer ICs, where its built-in search capability makes it ideal for a variety of applications. However, there are at least two drawbacks to this circuit that force limits on its usage. The largest problem is the short pulse on one of the flip-flop



(*a*)



(*b*)

FIGURE 12.14 (*a*) Phase detector using a *D* flip-flop and (*b*) the timing chart.

outputs. With high-speed logic, this pulse is only a few nanoseconds long. If f_1 and f_2 are high in frequency, this may be a significant part of their period. This pulse dead time due to propagation delays results in a nonlinear phase detector transfer curve. In older versions there were flat spots with zero gain and regions where the gain reversed its slope. The pulse also contributes heavily to the output noise, and it can easily add 20 dB of noise to the PLL output even in the most modern devices. The second problem is that the searching capability can become confused if there is any interruption in either f_1 or f_2. This circuit should be used in applications where very low phase noise is not required and the inputs are continuous. For this phase detector the gain is $K_{\text{pd}} = 1/4\pi$.

12.13.4 Exclusive OR Phase Detector

An exclusive OR gate works as a frequency doubler and phase detector. Figure 12.15 illustrates a typical connection for the phase detector. For correct operation, both inputs f_1 and f_2 must be at the same frequency, and both must have 50% duty cycles. The XOR output will be a logic level waveform at twice the input frequency. The duty cycle of the output depends on the phase difference between the two inputs. Phase shifts of 90° or 270° produce a 50% output. The RC low-pass filter produces a dc value proportional to the duty cycle. For a 90° or a 270° phase difference, the filter output is one-half the difference between the logic high- and logic low-output voltages.

The XOR gate is the functional equivalent of the balanced mixer. This circuit is useful for PLL applications requiring a high-frequency VCO to be divided down and locked to a low-frequency logic level frequency reference. This phase detector is suitable for low-phase noise applications, but it frequently requires an external search circuit to initially achieve lock. The gain, K_{pd}, of this phase detector is $1/\pi$ volts/rad.

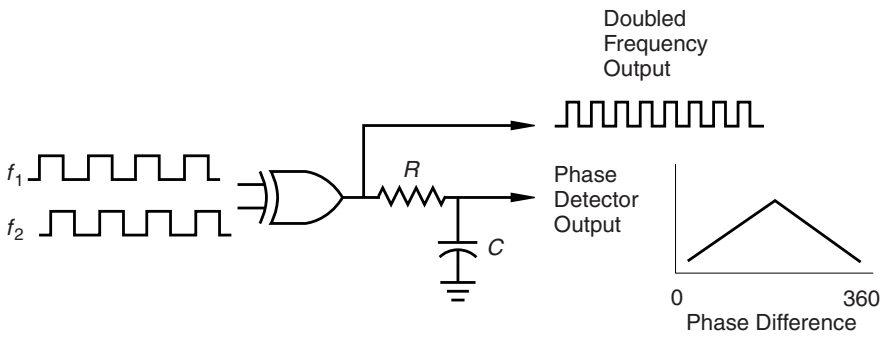


FIGURE 12.15 Exclusive OR phase detector.

12.14 DESIGN EXAMPLES

Example 1. The phase lock loop design shown in Fig. 12.16 requires an output frequency of 1600 MHz and the reference oscillator is 100 MHz. The design approach chosen is to use an inverting type-2 loop filter with a frequency divider and a mixer phase detector. The VCO chosen shows a typical tuning slope of 1 MHz/volt. Measurements of the phase detector output show a cosine wave that is 100 mV peak to peak. A 3 dB bandwidth of 100 kHz is required with a damping ratio of 1.

a. Using a 100 pF capacitor, find the remaining loop filter values.
b. Using a 10 kΩ R_{in}, find the remaining loop filter values.

Solution 1. From the graph in Fig. 12.13, the 3 dB frequency for a damping ratio of 1 is at 2.45 Hz. The type 2 circuit for this example is shown in Fig. 12.16. If 100 kHz 3 dB frequency is required, the natural frequency is found from scaling the graph. Thus $f_n = 100\ \text{kHz}/2.45 = 41\ \text{kHz}$. The output frequency is 16 times the input frequency, so $N = 16$. The value for K_{vco} is specified at 1 MHz/volt. The phase detector output is a cosine wave. If the loop locks at 90° or 270°, the phase detector output voltage is zero. For a positive R_{in}, the slope is the first derivative evaluated at 270°, so $K_{pd} = 50$ mV/rad.

For part a, use the equations derived earlier with C set at 100 pF. Then $K_t = [(1 \cdot 50)/16] \cdot 2\pi \cdot 10^3$, and from Eq. (12.48), $R_{in} = 2.96$ kΩ. Finally Eq. (12.49) gives $R_s = 77.6$ kΩ.

For part b, $R_{in} = 10$ kΩ. With R_{in} set, $C = 29.6$ pF and $R_s = 262.4$ kΩ.

Example 2. The synthesizer design shown in Fig. 12.17 requires an output frequency from 900 to 920 MHz. The output frequency can be changed in 1 kHz steps by changing the divide ratio. Design a PLL using a synthesizer IC and an external VCO. The synthesizer IC data sheet lists the current mode phase detector output as 5 mA/rad. The VCO data sheet lists the tuning rate at 10 MHz/volt.

Solution 2. The output frequency must be an integer multiple of the reference frequency, so the reference frequency is 1 kHz. The circuit diagram is shown

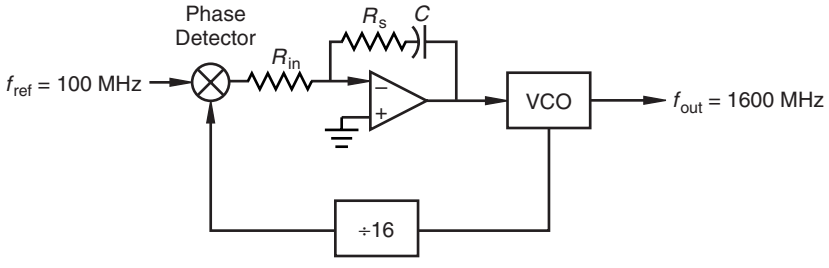


FIGURE 12.16 PLL for Example 1.

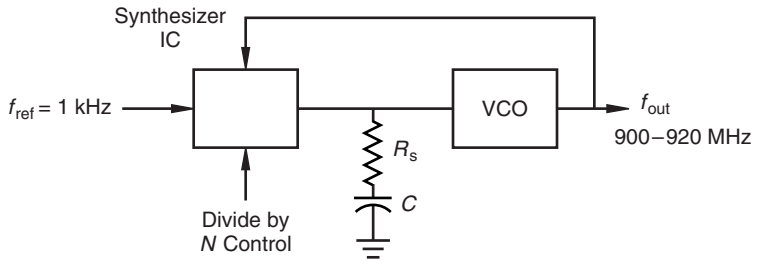


FIGURE 12.17 Synthesizer design for Example 2.

in Fig. 12.17. The divide ratio must change from 900 MHz/1 kHz or $9 \cdot 10^5$ to 920 MHz/1 kHz or $9.2 \cdot 10^5$. The midpoint value, $9.1 \cdot 10^5$, can be used for the design. A damping ratio of 1 is chosen for a rapid settling time when the divide ratio changes. The loop filter must attenuate the pulses from the phase detector output running at 1 kHz. Figure 12.13 shows that 14 dB of attenuation can be expected at 10 times the natural frequency. With a slope of -20 dB/decade, 34 dB attenuation can be expected at 100 times the natural frequency. Choosing $f_n = 10$ Hz will work with a 1 kHz reference frequency. Here the value of K_t is in dimensions of V/A:

$$K_t = \frac{K_{vco}K_{pd}}{N} \cdot \frac{\text{MHz}}{\text{volt}} \cdot \frac{\text{mA}}{\text{Hz}} \cdot \frac{2\pi \text{ rad}}{\text{Hz}}$$

Evaluation of this gives $K_t = 0.345$ A/V. To find R_s and C, K_t must be multiplied by R_{in}. This will cancel the R_{in} in Eqs. (12.46) and (12.47). Thus from the design equations $R_s = 364\ \Omega$ and $C = 87.45\ \mu$F.

Example 3. A frequency synthesizer contains a phase lock loop circuit. Inspection shows that the loop filter is to be a type 1 noninverting configuration. The data sheets for the phase detector show that the output waveform has a slope of 100 mV/rad. The VCO nominal output frequency is 3 GHz with a tuning rate of 100 MHz/volt. The reference is a 100 MHz crystal oscillator. If $R_{in} = 620\ \Omega$, $R_s = 150\ \Omega$, $R_p = 56$ kΩ, and $C = 1$ nF, what is the expected 3 dB bandwidth and damping ratio for this PLL?

Solution 3. With a 3 GHz output and a 100 MHz reference, the frequency divide ratio N must be 30. Also $K_t = 2.094 \cdot 10^6$. Substituting the given circuit values into the analysis equations show that $f_n = 293.7$ kHz and the damping ratio $\zeta = 0.709$. The curve for $\zeta = 0.709$ is not shown in Fig. 12.13, but a value can be found by interpolation. The 3 dB frequency for $\zeta = 0.5$ is 1.8 Hz. The 3 dB frequency for $\zeta = 1$ is 2.45 Hz. A linear approximation for 0.709 is 2.07 Hz. The 3 dB frequency for this PLL is approximately $2.07 \cdot f_n = 608$ kHz.

PROBLEMS

12.1 A phase lock loop can be described in the frequency domain in terms of the input and output phase angles shown in Fig. 12.7. The input phase is $\tilde{\phi}_1(s) = a + b/s^2$. The filter transfer function is

$$F(s) = \frac{1 + sCR_2}{1 + sC(R_1 + R_2)}$$

(a) What is the steady state phase error?

(b) What is the steady state phase error if the capacitance $C = \infty$?

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