Appendix B: Device Biasing

The initial small-signal bias state of the oscillator sustaining stage is generally less critical than with amplifiers because the steady-state operating voltage and current are largely a function of nonlinear conditions. Nevertheless, oscillator devices are normally initially biased in the linear region. This appendix reviews biasing techniques for bipolar, JFET, MOSFET, and dual-gate MOSFET devices.

B.1 Biasing Bipolar Transistors

With the appropriate use of coupling and bypass reactors, any of the following bias networks may be used for common-emitter (CE), common-base (CB), or common-collector (CC) device topologies. However, proper selection of the bias network minimizes the number of required coupling or bypass reactors.

B.1.1 Bipolar Model for Biasing

A simplified model for biasing a bipolar transistor is shown in Fig. B.1. The collector current is primarily the device forward beta, β, times the base current I_b. The reverse-biased collector-base junction leakage current, I_{cbo}, is generally less than a microamp and for our purpose it is assumed 0. The resulting error is small except at very low collector current or high operating temperature.

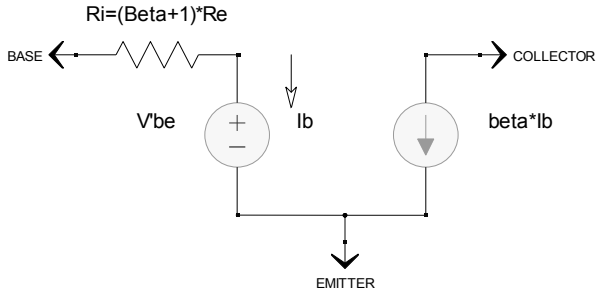

Figure B.1 Simplified bipolar transistor model for bias network design.

A significant factor in bias design is variation in β between devices, which is often 3:1 or more. For example, a typical β specification is 50 minimum and 150 maximum. β is the collector current to base current ratio.

Secondary influences on bias stability are temperature variations in the intrinsic forward base-emitter voltage drop, V'_{be}, and temperature variation in β. The intrinsic forward biased base-emitter junction potential for silicon is approximately 0.79 at 27°C with a negative temperature coefficient.

$$V'_{be}(T) = V'_{be(27^oC)} - 0.002\left(T - 27^oC\right) \qquad (268)$$

β increases with temperature and is approximated by

$$\beta(T) = \beta_{(27^oC)}\left(1 + 0.005\left(T - 27^oC\right)\right) \qquad (269)$$

The increase in β and drop in V_{be} with an increase in temperature can lead to thermal runaway in bipolar transistors. If the external resistance in the collector to emitter path is low, an increase in the collector current does not reduce the voltage across the transistor active region adequately and the transistor dissipation increases. This may further increase the current and lead to runaway. This was more of an issue with power devices and earlier germanium transistors.

The base current drive required to sustain the collector current is

$$I_b = \frac{I_c}{\beta} \qquad (270)$$

Since

$$I_e = I_c + I_b \qquad (271)$$

then

$$I_e = \frac{\beta}{\beta + 1} I_c \qquad (272)$$

It is sometimes convenient to use

$$\alpha = \frac{\beta}{\beta + 1} \qquad (273)$$

where α is the collector current to emitter current ratio.

Base current flowing in R_i increases the terminal base-emitter voltage drop. Therefore, the terminal base-emitter voltage, V_{be}, is

$$V_{be} = V'_{be} + R_i I_b \qquad (274)$$

where

$$R_i = (\beta + 1) r_e \tag{275}$$

and r_e is the intrinsic emitter-base diode resistance. It is approximately

$$r_e = \frac{kT(^oK)}{qI_e} = \frac{8.62 \times 10^{-5} \left(273.15 + T(^oC)\right)}{I_e} \tag{276}$$

At 27°C

$$r_e = \frac{26 \times 10^{-3}}{I_e} \tag{277}$$

The base emitter terminal voltage is approximated with a temperature-dependant V'_{be} and a temperature-independent r_e. Then,

$$V_{be}(T) \cong V'_{be}(T) + 0.026 = 0.817 @ 27^oC \tag{278}$$

It is interesting to note that with the simplified bias model used in this appendix, V_{be} is independent of the collector current and β. This greatly simplifies the following equations for bias networks.

B.1.2 Common Emitter Bias Networks

Fig. B.2 shows six different bipolar transistor bias networks that use a single-supply voltage. They are an expansion of networks described in Richter [1]. These six topologies are particularly well suited for CE device topologies. The bias network classifications in Fig. B.2 are Bias 1 through Bias 6. In the following formula for resistor values, V_{be} is calculated using Eq. 278, or if temperature can be ignored, V_{be} is fixed at 0.817. In the following sections, formulas are given for finding the bias network resistor values. Nominal β and temperature are used. Then the formula given for the collector current is used to assess the effect of β and temperature variation.

B.1.2.1 Bias 1 Simple

Consider first the Bias 1 network. The designer selects the desired device collector current, I_c, and the collector-emitter voltage, V_{ce}. Then

$$R_{c1} = \frac{(V_{cc} - V_{ce})}{I_c} \tag{279}$$

The designer typically either controls R_c by selecting V_{cc} or accepts R_c based on the required V_{cc}. Then

$$R_{b1} = \frac{\beta (V_{cc} - V_{be})}{I_c} \tag{280}$$

For example, using a nominal β of 80, a desired V_{ce} of 2 volts, I_c of 5 mA and V_{cc} of 2.7 volts, then V_{be} is 0.817 volts, R_{c1} is 140 ohms, and R_{b2} is 30.1K ohms.

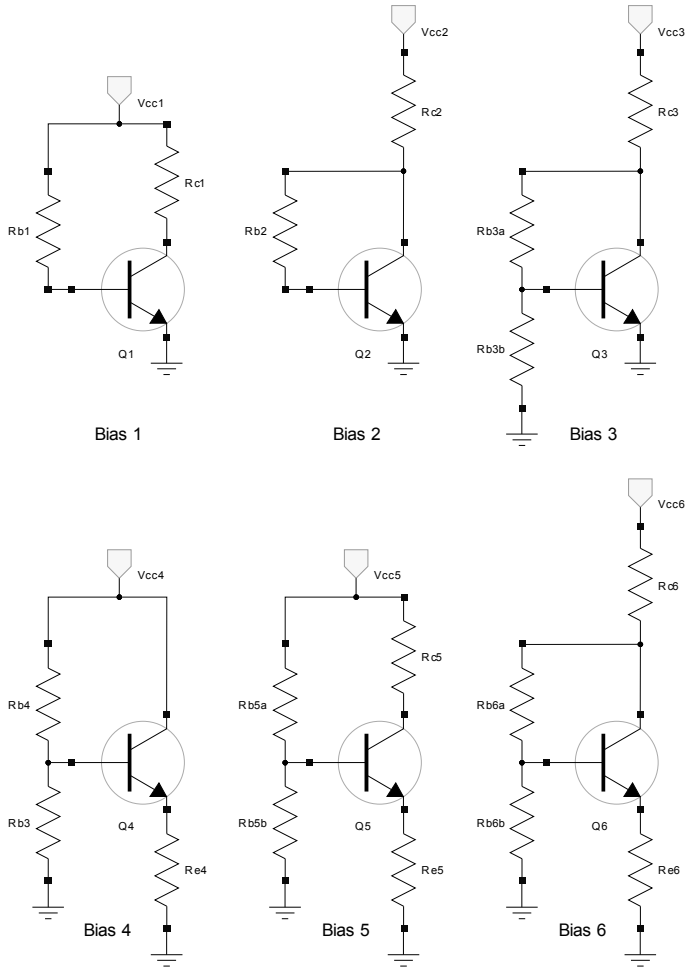

Figure B.2 Bipolar transistor one-battery bias networks for CE topologies.

The stability of the bias network is assessed by considering the collector current as a function of β and temperature. Using the temperature-dependant Eq. 278, then

$$I_{c1} \cong \frac{\beta(V_{cc} - V_{be})}{R_{b1}} \qquad (281)$$

The collector currents with β of 50, 80, and 150 are 3.12, 5, and 9.38 mA, respectively. These -36.4 and +87.6% bias shifts are the result of a nearly direct relationship between β and the collector current with type 1 biasing. The collector currents with a nominal β of 80 and temperatures of 0, 27, and 50°C are 4.20, 5, and 5.71 mA, respectively. Bias shift with temperature is moderate. However, the high sensitivity of the collector current to β suggests the use of a more stable bias network.

B.1.2.2 Bias 2 Simple FB

The Bias 2 network requires only two resistors and feedback insures that the device is biased in the active region at any β and temperature. The base bias is derived from the collector voltage. If the collector current increases, the collector voltage drops, reducing the base drive and thereby reducing the collector current. The bias resistor values are

$$R_{c2} = \frac{\beta(V_{cc} - V_{ce})}{(\beta + 1)I_c} \qquad (282)$$

$$R_{b2} = \frac{\beta(V_{ce} - V_{be})}{I_c} \qquad (283)$$

The collector current is

$$I_{c2} \cong \frac{\beta(V_{cc} - V_{be})}{R_{b2} + (\beta + 1)R_{c2}} \qquad (284)$$

Using a desired V_{ce} of 2 volts, I_c of 5 mA, and V_{cc} of 2.7 volts, the collector currents with β of 50, 80 and 150 are 3.61, 5, and 7.13 mA, respectively. These -27.8 and +42.6% bias shifts are significantly less than with the Bias 1 network. The collector currents at 0 and 50°C are 4.46 and 5.52 mA, a smaller shift than with Bias 1 networks. The Bias 2 network stability is generally adequate for oscillator design. Stability with β and temperature is improved with a larger voltage drop across R_{c2}.

B.1.2.3 Bias 3 Divided FB

The Bias 3 network adds a base bias resistor to the Bias 2 network. The current flowing in the base-bias resistors is a degree of freedom available to the designer. Increasing this current improves the bias stability with β. In the following equations for the bias resistor values, the current in R_{b3a} is set at 10% of I_c. The current in R_{b3a} must be greater than I_b at the minimum device β.

$$R_{c3} = \frac{V_{cc} - V_{ce}}{1.1 I_c} \tag{285}$$

$$R_{b3a} = \frac{V_{ce} - V_{be}}{0.1 I_c} \tag{286}$$

$$R_{b3b} = \frac{V_{be}}{I_c (0.1 - 1/\beta)} \tag{287}$$

The collector current is then

$$I_{c3} \cong \frac{\beta}{R_{c3}(\beta + 1) + R_{b3a}} \left(V_{cc} - V_{be} - \frac{V_{be}}{R_{b3b}} (R_{c3} + R_{b3a}) \right) \tag{288}$$

Using a desired V_{ce} of 2 volts, I_c of 5 mA, and V_{cc} of 2.7 volts, the collector currents with β of 50, 80, and 150 are 4.47, 5, and 5.51 mA, respectively. The collector currents at 0 and 50°C are 4.08 and 5.80 mA. This is a greater temperature shift than with the Bias 1 and 2 networks, but adequate for oscillator design. As seen later, the Bias 6 network resolves the temperature stability issue.

One of the advantages of the Bias 3 and Bias 6 networks is that the resistors serve the dual purpose of biasing and RF feedback, as illustrated in Section 1.5.7. This works best with relatively low supply voltage. At higher V_{cc}, the current in the resistors becomes excessive.

B.1.2.4 Bias 4 Emitter FB

The Bias 4 network is often used with common-collector Colpitts oscillators. It is also used with common-emitter sustaining stages with an inductive choke between the supply and the collector. The designer selects the current in R_{b4a}. In the following equations it is set at 10% of the collector current. The resistor values are then

$$V_e = V_{cc} - V_{ce} \tag{289}$$

$$R_{e4} = \frac{\alpha (V_{cc} - V_{ce})}{I_c} \tag{290}$$

$$R_{b4a} = \frac{V_{ce} - V_{be}}{0.1 I_c} \tag{291}$$

$$R_{b4b} = \frac{\frac{R_{e4}}{\alpha} + \frac{V_{be}}{I_c}}{(0.1 - 1/\beta)} \tag{292}$$

The collector current is

$$I_{c4} = \frac{\dfrac{V_{cc}}{1 + R_{b4a}/R_{b4b}} - V_{be}}{\dfrac{R_{e4}}{\alpha} + \dfrac{R_{b4a}}{\beta\left(1 + R_{b4a}/R_{b4b}\right)}} \qquad (293)$$

Using a desired V_{ce} of 2 volts, I_c of 5 mA, and V_{cc} of 2.7 volts, the collector currents with β of 50, 80, and 150 are 4.66, 5, and 5.30 mA, respectively. The collector currents at 0 and 50°C are 4.57 and 5.36 mA. The stability with β and temperature is good. However, Bias 4 through 6 may require capacitor bypass of the emitter resistance. If so, inductance in this path is critical at high frequency, so this emitter resistance is a disadvantage.

B.1.2.5 Bias 5 One-Battery Network

The classic Bias 5 network is often referred to as the one-battery bias network. The designer has two degrees of freedom; the voltage across R_{e4} and the current in R_{b4a}. Setting the voltage across R_{e4} at 10% of V_{cc} and I_{Rb4a} at 10% of the collector current the resistor values are

$$R_{e5} = \frac{0.1\alpha V_{cc}}{I_c} \qquad (294)$$

$$R_{c5} = \frac{V_{cc} - V_{ce} - 0.1V_{cc}}{I_c} \qquad (295)$$

$$R_{b5a} = \frac{V_{cc} - V_{be} - 0.1V_{cc}}{0.1I_c} \qquad (296)$$

$$R_{b5b} = \frac{0.1V_{cc} + V_{be}}{(0.1 - 1/\beta)I_c} \qquad (297)$$

The collector current is

$$I_{c5} = \alpha\left(\frac{\dfrac{V_{cc} - V_{be}}{R_{b5a}} - \dfrac{V_{be}}{R_{b5b}}}{(1-\alpha) + \dfrac{R_{e5}}{R_{p5}}}\right) \qquad (298)$$

where

$$R_{p5} = \frac{R_{b5a}R_{b5b}}{R_{b5a} + R_{b5b}} \qquad (299)$$

Using a desired V_e of 0.27 volts, V_{ce} of 2 volts, I_c of 5 mA, and V_{cc} of 2.7 volts, the collector currents with β of 50, 80, and 150 are 4.34, 5, and

5.67 mA, respectively. The collector currents at 0 and 50°C are 4.08 and 5.80 mA. The stability with β is fair and the stability with temperature is poor. A higher V_{cc} with a resulting increase in R_{e5} improves the stability of the Bias 5 network significantly.

B.1.2.6 Bias 6 Dual FB

The Bias 6 network uses both emitter and collector-base feedback to stabilize the collector current. The designer has two degrees of freedom; the voltage across R_{e6} and the current in R_{b6a}. Setting R_{e4} at 10% of V_{cc} and I_{Rb4a} at 10% of the collector current the resistor values are given below. Alternatively, the values of R_{b6a}, R_{b6b} and R_{e6} are chosen to set the gain and input and output impedances as described in Section 1.5.7, thus reducing the number of resistors and capacitors. As with the Bias 3 network, this is only practical with low V_{cc}.

$$V_e = 0.1V_{cc} \tag{300}$$

$$V_c = V_{ce} + V_e \tag{301}$$

$$R_{c6} = \frac{V_{cc} - V_c}{1.1I_c} \tag{302}$$

$$R_{e6} = \frac{\alpha V_e}{I_c} \tag{303}$$

$$R_{b6a} = \frac{V_c - (V_{be} + V_e)}{0.1I_c} \tag{304}$$

$$R_{b6b} = \frac{(V_{be} + V_e)}{I_c(0.1 - 1/\beta)} \tag{305}$$

The collector current is then

$$I_{c6} = \frac{V_{cc} - V_{be}(R_{b6a}/R_{b6b} + 1 + R_{c6}/R_{b6b})}{\frac{R_{b6a}}{\beta} + \frac{R_{e6} + R_{c6}}{\alpha} + \frac{R_{e6}(R_{b6a} + R_{c6})}{\alpha R_{b6b}}} \tag{306}$$

Using a desired V_e of 0.27 volts, V_{ce} of 2 volts, I_c of 5 mA, and V_{cc} of 2.7 volts, the collector currents with β of 50, 80, and 150 are 4.59, 5, and 5.37 mA, respectively. The collector currents at 0 and 50°C are 4.40 and 5.51 mA. The stability with β and temperature is good.

B.1.3 Bias 7 Network with Base Diode

The Bias 7 network shown in Fig. B.3 is used for near class-B biasing. Because of the voltage drop in R_i (see Fig. B.1), the base terminal voltage of the transistor is usually higher than the voltage drop of a diode. Therefore, R_{b7} must be rather small to forward bias $Q7$. A more moderate value of R_{b7}, for example 10K ohm, biases $Q7$ just below the active region. A variation of the Bias 7 network uses a stack of multiple diodes at the base and a small resistor in series with the emitter. In this case

$$I_c = \frac{V_{stack} - V_{be}}{\alpha R_e} \qquad (307)$$

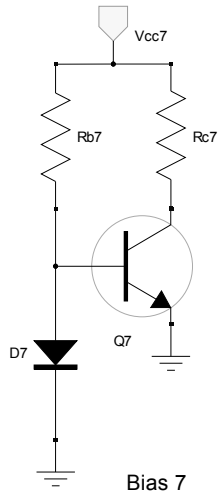

Figure B.3 Bias 7 network with base diode.

B.1.4 Bias 8 Network with Zener

The Bias 8 network utilizes a zener diode in series with a base resistor to provide base drive, as shown in Fig. B.4. The zener is a PN junction specifically designed to be operated in reverse bias. Zener diode operation is influenced by two modes; zener breakdown and avalanche breakdown. Silicon zener diodes up to about 4 volts exhibit a negative temperature coefficient similar to a forward biased diode. At approximately 5.6 volts the temperature coefficient is 2mV/°C, thus cancelling the temperature coefficient of the transistor. Higher-voltage zeners have an increasingly positive temperature coefficient.

V_{ce} must exceed the zener voltage plus V_{be}. Therefore, this network is not suitable for low supply voltage. The resistor values are

$$R_{c8} = \frac{\alpha(V_{cc} - V_{ce})}{I_c} \tag{308}$$

$$R_{b8} = \frac{\beta(V_{ce} - V_{be} - V_z)}{I_c} \tag{309}$$

Then the collector current is

$$I_c = \frac{V_{cc} - V_{be} - V_z}{\frac{R_{b8}}{\beta} + \frac{R_{c8}}{\alpha}} \tag{310}$$

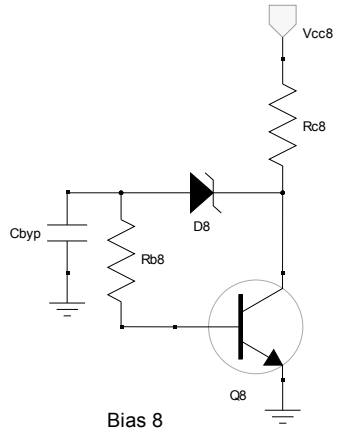

Figure B.4 Bias 8 network with zener diode.

Using a desired V_{ce} of 2 volts, I_c of 5 mA, and V_{cc} of 2.7 volts, the collector currents with β of 50, 80, and 150 are 3.63, 5, and 7.07 mA, respectively. The stability with beta is poor but acceptable for oscillators. The stability with temperature is excellent with proper selection of the zener.

B.1.5 Bias 9 Active Network

The Bias 9 network shown in Fig. B.5 utilizes a PNP sense transistor to control the collector current of the active transistor. The collector current of Q_9 flowing in R_{d9} develops a voltage drop. If the collector current in the active transistor increases, the voltage drop in R_{d9} increases and reduces the sense transistor V_{be} and the base drive to the active transistor. Therefore, the active transistor base drive is determined directly by the collector current. This significantly reduces the sensitivity of collector current to the device β.

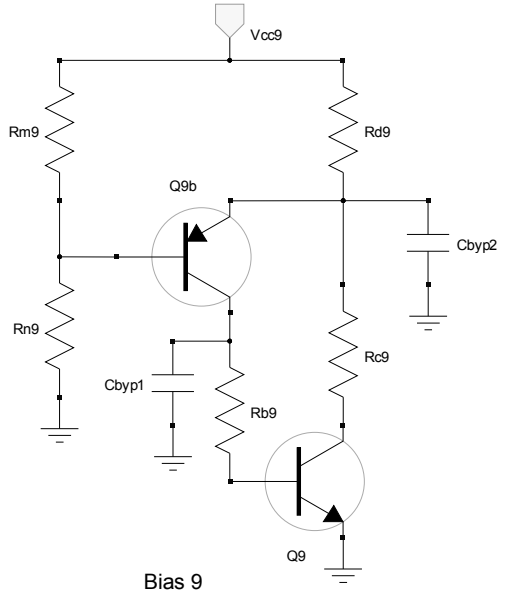

Figure B.5 Bias 9 network with active control of the base drive.

The base current in the sense transistor is approximately $1/\beta^2$ so it is ignored in the following equations. V_e is defined as the voltage at the emitter of the sense transistor. To improve temperature stability, V_e is generally set at least twice V_{be} below V_{cc}. Setting the current in R_{m9} at 10% of I_c, and setting both β and V_{be} of both transistors equal, the resistor values are

$$R_{d9} = \frac{\alpha(V_{cc} - V_e)}{I_c} \tag{311}$$

$$R_{m9} = \frac{V_{cc} - V_e + V_{be}}{0.1 I_c} \tag{312}$$

$$R_{n9} = \frac{V_e - V_{be}}{0.1 I_c} \tag{313}$$

Resistors R_{c9} and R_{b9} do not directly influence the collector current but their values are limited.

$$0 < R_{c9} < \frac{V_e}{I_c} \tag{314}$$

$$0 < R_{b9} < \frac{\beta(V_e - V_{be})}{I_c} \tag{315}$$

Resistor R_{c9} may be set at 0 by using an inductive choke, it may be set at 50 ohms, or it may be set high to avoid shunting signal. However, a resistor reduces V_{ce} of the active transistor.

$$V_{ce} = V_e - I_c R_{c9} \tag{316}$$

Resistor R_{b9} is set high enough to avoid shunting signal at the base of the active transistor. The collector current of the active transistor is

$$I_c = \frac{\alpha\left(V_{cc}\left(1 - \frac{R_{m9}}{R_{m9} + R_{n9}}\right) - V_{be}\right)}{R_{d9}} \tag{317}$$

Using a desired V_{ce} of 2 volts, I_c of 5 mA, and V_{cc} of 2.7 volts, the collector currents with β of 50, 80, and 150 are 4.96, 5, and 5.03 mA, respectively. The collector currents at 0 and 50°C are 4.61 and 5.34 mA. The stability with β is nearly perfect. The stability with temperature is good and improves with a larger voltage drop across R_{d9}. This degree of bias network complexity is justified only if a highly stable oscillator output amplitude is required.

B.1.6 Bias 10 Dual Supply

If both positive and negative supplies are available, the Bias 10 network shown in Fig. B.6 is economic and stable. It is well suited for common-base topologies. Using the absolute values for the voltages of V_{ee} and V_{be}, the value of the emitter resistor is

$$R_{e10} = \frac{\alpha(V_{ee} - V_{be})}{I_c} \tag{318}$$

where both V_{ee} and V_{be} are negative. The value of R_{c9} is confined by the range

$$0 < R_{c10} << \frac{V_{cc}}{I_c} \tag{319}$$

Smaller values of R_{c9} provide higher V_{ce}, which is desirable.

$$V_{ce} = V_{cc} - I_c R_{c10} + V_{be} \tag{320}$$

However, because the collector impedance of the CB stage is high, an inductive choke may be required at the collector for small V_{cc} to avoid shunting the signal with small values of R_{c10}.

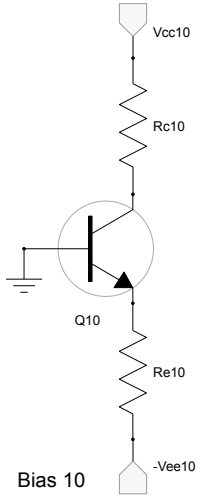

Figure B.6 Bias 10 network with dual supplies.

The collector current is

$$I_c = \frac{\alpha(V_{ee} - V_{be})}{R_{e10}} \qquad (321)$$

Using a desired V_{ee} of -2.7 volts, I_c of 5 mA, and V_{cc} of 2.7 volts, the collector currents with β of 50, 80, and 150 are 4.96, 5, and 5.03 mA, respectively. The collector currents at 0 and 50°C are 4.84 and 5.13 mA. The stability with β is outstanding and with temperature is excellent. The excellent temperature stability is because V_{ee} is several times V_{be}. Bias 10 network is the obvious choice for CB topologies when both positive and negative supplies are available.

B.1.7 Bias 11 Common Collector Network

The Bias 11 network depicted in Fig. B.7 is a variation of the Bias 4 network with the supply and ground nodes exchanged. An NPN device is used with a negative supply or a PNP device with a positive supply. The resistor values and collector current are identical to the Bias 4 network.

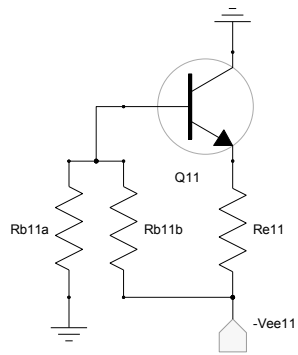

Figure B.7 Bias 11 network for common-collector topologies and a negative supply for NPN transistors.

A variation on the Bias 11 network omits resistor R_{b11b}. V_e is commonly near 50% of V_{ee}. Choosing V_e and I_e, then

$$R_{e11} = \frac{V_{ee} - V_e}{I_e} \qquad (322)$$

where the right-side variables are all negative. Then

$$R_{b11a} = \frac{\beta(V_e + 0.817)}{I_e} \qquad (323)$$

B.1.8 Bipolar Bias Network Summary

The collector currents with variation of β and temperature for each bias network are repeated in Table B.1. The bias stability performance of the networks is a function of design choices. These examples used a supply voltage of 2.7 volts and emitter resistor drops as low as 0.27 volts. These low values accentuate the effects of β and temperature changes.

Table B.1 Comparison of the stability of I_c for the 11 bipolar bias networks. The nominal current is 5 mA at beta=80 and T=27°C

Type	Name	Beta=50	=150	T=0°C	=50°C
1	Simple	3.12	9.38	4.20	5.71
2	Simple FB	3.62	7.10	4.42	5.48
3	Divided FB	4.47	5.51	4.08	5.80
4	Emitter FB	4.66	5.30	4.57	5.36
5	One Battery	4.34	5.67	4.08	5.80
6	Dual FB	4.59	5.37	4.40	5.51
8	Zener	3.63	7.07	N/A	N/A
9	Active	4.96	5.03	4.61	5.34
10	Dual supply	4.96	5.03	4.84	5.13

Because bias stability is not critical for most oscillator applications, any of the networks of type 3 and higher are adequate. The choice of bias network type is driven by minimization of the number of required resistors, chokes, and bypass capacitors.

B.1.9 Saturated Output Power and Biasing

When designing high-power amplifiers, whether for use as amplifiers or oscillators, the type of biasing is important. Higher-power compression levels are achieved by using a constant base voltage source rather than a current source [2]. In other words, at DC, the source impedance of the bias network should be low. Many bias schemes use high resistor values at the base for biasing to avoid shunting the signal. This is perfectly acceptable when high output power and efficiency are not critical. However, the highest output power and efficiency are achieved by using a low impedance voltage source to bias the base and then using a choke to deliver this voltage so as not to shunt the signal.

B.2 FET Bias Networks

Junction field-effect transistors (JFETs) are voltage-controlled current sources. Material between the source and drain terminals is doped with an abundance of positive charge carriers in the P-type JFET or of negative charge carriers in the N-type JFET. The gate terminal is reverse-biased but the field potential effectively changes the width of the source-drain channel and controls the current. The reverse-biased input gate is high resistance and little current flows into the gate.

Metal oxide silicon FET (MOSFET) devices have an insulating oxide layer between the gate and channel, further increasing the input resistance. MOSFETs typically have a lower transconductance. Today, the “metal” material is generally replaced by a polysilicon layer. VMOS devices are MOSFETs with a “V” shaped gate, allowing greater current in the source to drain channel. GaAs MESFETs, or GASFETs, are also related [3, 4]. In the FET, the drain current, I_d, is controlled by the gate to source voltage, V_{gs}.

$$I_d = I_{dss}\left(1-\frac{V_{gs}}{V_P}\right)^2 \qquad (324)$$

for

$$0 < V_{gs} < V_P \qquad (325)$$

where I_{dss} is the drain saturation current and V_P is the pinch-off voltage. The I_{dss} specification for the *2N5484* is 1 to 5 mA and for the *J309* is 12 to

30 mA [5]. A wide variation in I_{dss} is typical for FETs. The V_P specification for the *2N5484* is -0.3 to -3 volts and for the *J309* is -1 to -4 volts.

B.2.1 Bias 15 Simple FET Network

Fig. B.8 depicts three different FET bias networks. N-type FETs that utilize a positive drain supply voltage are shown. The supply voltage polarities are reversed for P-type FETs.

The Bias 15 network illustrates the simplest form of biasing for the FET. Resistor R_{g15} holds the gate near 0 volts. Since the DC current flowing in the gate is essentially nil, a large value such as 100K ohm is used for R_{g15} to avoid shunting signal. Alternatively, an inductive choke may be used. With a V_{gs}, of 0 volts, I_d, is equal to I_{dss}. The drain resistor is

$$R_d = \frac{V_{dd} - V_d}{I_{dss}} \qquad (326)$$

where V_d is the desired V_{ds} of the FET. I_{dss} has a small negative temperature coefficient so thermal runaway is not an issue.

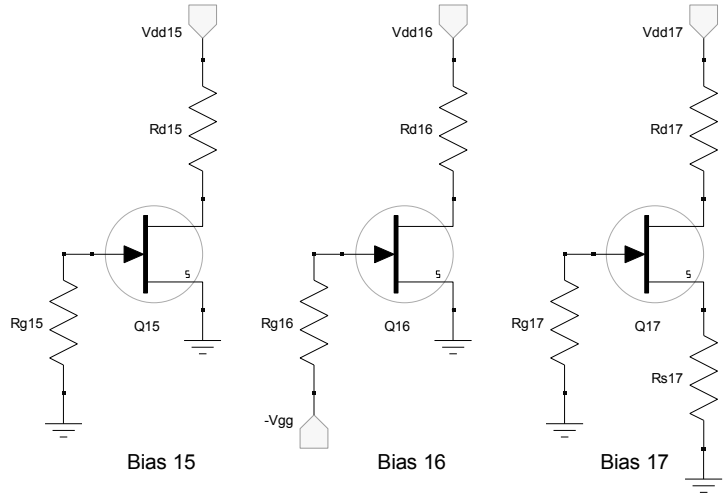

Figure B.8 Bias configurations for N-type FETs.

B.2.2 Bias 16 Gate Voltage

The Bias 16 network utilizes a fixed negative bias voltage at the gate. Again R_{g16} may be either a choke or high value of resistance. Because V_s is zero, V_{gg} equals V_{gs} and from Eq. 139, the gate voltage is

$$V_{gg} = V_P\left(1-\sqrt{\frac{I_d}{I_{dss}}}\right) \qquad (327)$$

For example, with I_{dss} of 17.2 mA and V_P of -1.72 volts, for a desired I_d of 5 mA, V_{gg}=-0.795 volts. The drain resistor is

$$R_{d16} = \frac{V_{dd} - V_d}{I_d} \qquad (328)$$

The drain current as a function of I_{dss} and V_P is then given by Eq. 324. The Bias 16 network provides a method of biasing the FET drain current at a value lower than I_{dss}. However, it does not stabilize the drain current against the high device to device variation of I_{dss}. It also requires a negative supply. A more practical solution is the next FET bias network.

B.2.3 Bias 17 Source FB

The Bias 17 network shown in Fig. B.8 provides a method for stabilizing the drain current and setting it at a specific value below I_{dss}. Drain current flowing in the source resistor biases the source at a positive voltage relative to the gate effectively reverse-biasing the gate. The required value of source resistance is

$$R_{s17} = -\frac{V_P}{I_d}\left(1-\sqrt{\frac{I_d}{I_{dss}}}\right) \qquad (329)$$

For a desired drain to source voltage, V_{ds}, the drain resistor is

$$R_{d17} = \frac{V_{dd} - V_{ds} - R_{s17} I_d}{I_d} \qquad (330)$$

The drain current is then

$$I_d = \frac{\left(\frac{2R_{s17}}{V_P} - \frac{1}{I_{dss}}\right) - \sqrt{\left(\frac{2R_{s17}}{V_P} - \frac{1}{I_{dss}}\right)^2 - 4\frac{R_{s17}^2}{V_P^2}}}{2R_{s17}^2 / V_P^2} \qquad (331)$$

Consider a desired V_{dd} of 5 volts, V_{ds} 0f 3 volts, and I_d of 8 mA. Using I_{dss} of 17.2 mA and V_P of -1.72, then R_{s17} is 68.37 and R_{d17} is 181.63. Using standard values of 68 and 180 ohms and device I_{dss} values of 12, 17.2, and 30, the drain currents are 6.57, 8.02, and 10.40 mA, respectively. Using these standard values and a nominal I_{dss} of 17.2 mA, the drain current with device pinch-off voltages of -1, -1.72, and -4 volts, the drain currents are 6.01, 8.02, and 11.25 mA, respectively. If capacitor bypass of the source

resistance is required, inductance in this path is critical at high frequency, so this source resistance is a disadvantage.

B.2.4 Bias 18 Dual-Gate FET

Dual-gate FETs are popular as amplifiers through the VHF frequency range and as mixers with the RF signal applied to gate 1 and the LO signal applied to gate 2. Dual-gate FETs also offer a convenient method of applying AGC to control the loop gain without limiting, thus linearizing an oscillator [6]. The Bias 18 network for dual-gate FETs is shown in Fig. B.9.

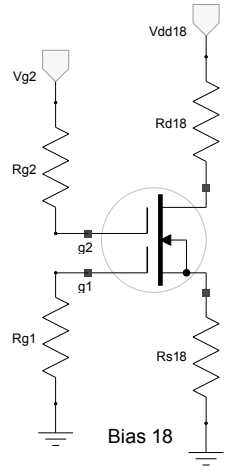

Figure B.9 Bias network for a dual-gate N-channel FET.

Figure B.10 shows drain current curves versus the gate 1 to source voltage for an MRF966 N-channel, dual-gate, depletion-mode GaAsFET. The drain-source voltage is 5 volts and the gate 2-to-source voltage is a running parameter.

Consider the case with a gate 2-to-source voltage of 0 volts. The drain current data from the graph agrees reasonably well with Eq. 324 with an I_{dss} of 48.5 mA and V_P of -5.3 volts. The specification I_{dss} is 30 mA minimum, 50 mA typical and 80 mA maximum. The specification gate 1-to-source V_P is -2.0 volts minimum and -4.5 volts maximum.

The Bias 15 network can be used to operate the dual-gate FET at I_d equal to I_{dss}. Gate 2 is also set at 0 volts to operate at full gain, or AGC is implemented by applying a gate 2 control voltage of 0 to -3 volts.

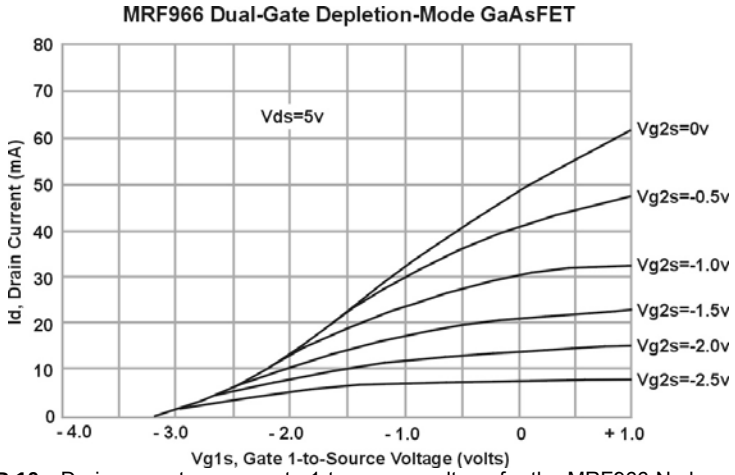

Figure B.10 Drain current versus gate 1-to-source voltage for the MRF966 N-channel, dual-date, depletion-mode GaAsFET with a drain-source voltage of 5 volts and gate 2-to-source running parameter.

Alternatively, the Bias 17 network can be used to operate I_d at less than I_{dss} and stabilize the operating point against variation in I_{dss}. For example, to operate at an I_d of 25 mA, a gate 1-to-source voltage of -1.4 volts is required. This gate bias is achieved using

$$R_{s18} = \frac{-V_{g1s}}{I_d} = \frac{1.4}{0.025} = 56 ohms \qquad (332)$$

The drain resistor is then given by Eq. 330. If necessary, the source resistance is bypassed and a choke is placed in series with the drain resistor.

B.3 Bias 19 MMIC Gain Block

As indicated in Chapter 1, MMIC gain blocks available from a variety of manufacturers make good oscillator sustaining stages. These device typically include internal bias networks and power only need be applied to the output via a choke or supply dropping resistor. A typical configuration is shown in Fig. B.11.

The MMIC operates at a specific voltage, V_c, and current, I_c. When the supply voltage equals the MMIC operating voltage, R_{c19} is replaced with an inductive choke and the device sinks the specified current. The choke may be a large value to avoid shunting the output signal or it may be a smaller value to act as a lead network to remove some high-frequency phase lag of the MMIC.

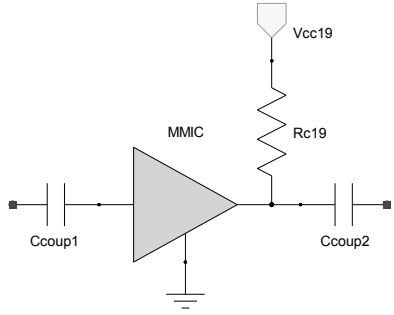

Figure B.11 Bias network for MMIC gain block with internal biasing.

If the supply voltage exceeds the operating voltage of the MMIC then the dropping resistor is

$$R_{c19} = \frac{V_{cc19} - V_c}{I_c} \qquad (333)$$

If R_{c19} is less than approximately 3X Z_o then a choke is placed in series with the resistor.

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