Quiz **02/03/24**

Bangladesh University of Engineering and Technology
Department of Computer Science and Engineering
CSE 206 - Digital Logic Design Sessional

Total Marks: 70 **Duration: 60 minutes**

Student Name: **Student ID:**

(For Examiner's Use Only)

1	2	3	4	5	6	7	8

Instructions

1. There are 5 Multiple Choice Questions and 5 True/False questions and 6 short questions in the script. Make sure all the questions are printed clearly before you start writing.

2. You should answer the all of the questions.

True/False Questions. Write T (for True) or F (for False) beside each of the question. [5]

1. a) The master latch of a positive edge-triggered master-slave D flip flop is active only during level 1 of the clock.

b) Once an up/down counter begins its count sequence, it cannot be reversed.

c) You cannot use Priority Encoder as a normal encoder.

d) You will need at least two 8x1 multiplexer and two 2x1 multiplexer to build a 16x1 multiplexer.

e) The product-of-sums (POS) is basically the OR-ing of AND-ed terms.

Multiple Choice Questions. Mark (√) beside the answer which suits best. **[5]**

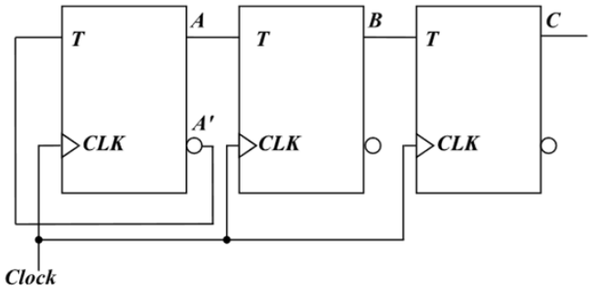
2. a) You have the following chips: 7404, 7408, 7432, 74138. What are the minimum chips required to solve: $\sum (8,11,13,15)$?

   i. 1x74138, 1x7408 ii. 1x74138, 1x7432
   iii. 2x74138, 1x7408 iv. 2x74138, 1x7432

   b) A MOD M and a MOD N up-counter when cascaded together results in a MOD _____ counter.

   i. M+N ii. M-N
   iii. M/N iv. M*N

   c) Assuming that the current state of the circuit (ABC) is 000, what will be the state of the circuit after 3 clock cycles?



   i. 111 ii. 101
   iii. 001 iv. 000

   d) If the number of n selected input lines is equal to 2^m then it requires _____ select lines.

   i. 2 ii. n
   iii. m iv. 2^n

   e) How many gates would be required to implement the following Boolean expression after simplification?

$$XY + X(X + Z) + Y(X + Z)$$

   i. 1 ii. 2
   iii. 3 iv. 4

Short Questions

3. Suppose you only have some 2 to 4 decoders and some 4 to 2 priority encoders with priority $0 < 1 < 2 < 3$. Now, you need a priority encoder with priority $3 < 2 < 1 < 0$. How would you implement this? **[10]**

4. Suppose you have two 2-bit numbers A and B and an additional input bit C. When C is 0, you have to output the bitwise XOR of A and B. When C is 1, you have to output the bitwise XNOR of A and B. Design a combinatorial circuit using only half subtractors. You can assume to have access to VCC and GND. **[10]**

5. Design an asynchronous MOD - 6 up/down counter using positive edge-triggered J-K flip-flops. The counter should have two modes of operation: down-counting when the mode bit M is set to 1, and up-counting when M is set to 0. **[10]**

6. Simplify the function into the minimal SOP form using K-Map. **[10]**

$$\sum(0,1,2,4,5,14,15) + d(6,7,8,9)$$

7 A sequential circuit has two T flip-flops A and B, and an input x. The circuit can be described by the following input equations: **[10]**

$$T_A = Bx,$$
$$T_B = A'x$$

Derive the next state equations $A_{(t+1)}$ and $B_{(t+1)}$. Also, draw the state diagram of this circuit.

8. Desing NAND, NOR, XOR and XNOR Gates using minimum numbers of 2x1 multiplexers only. **[10]**