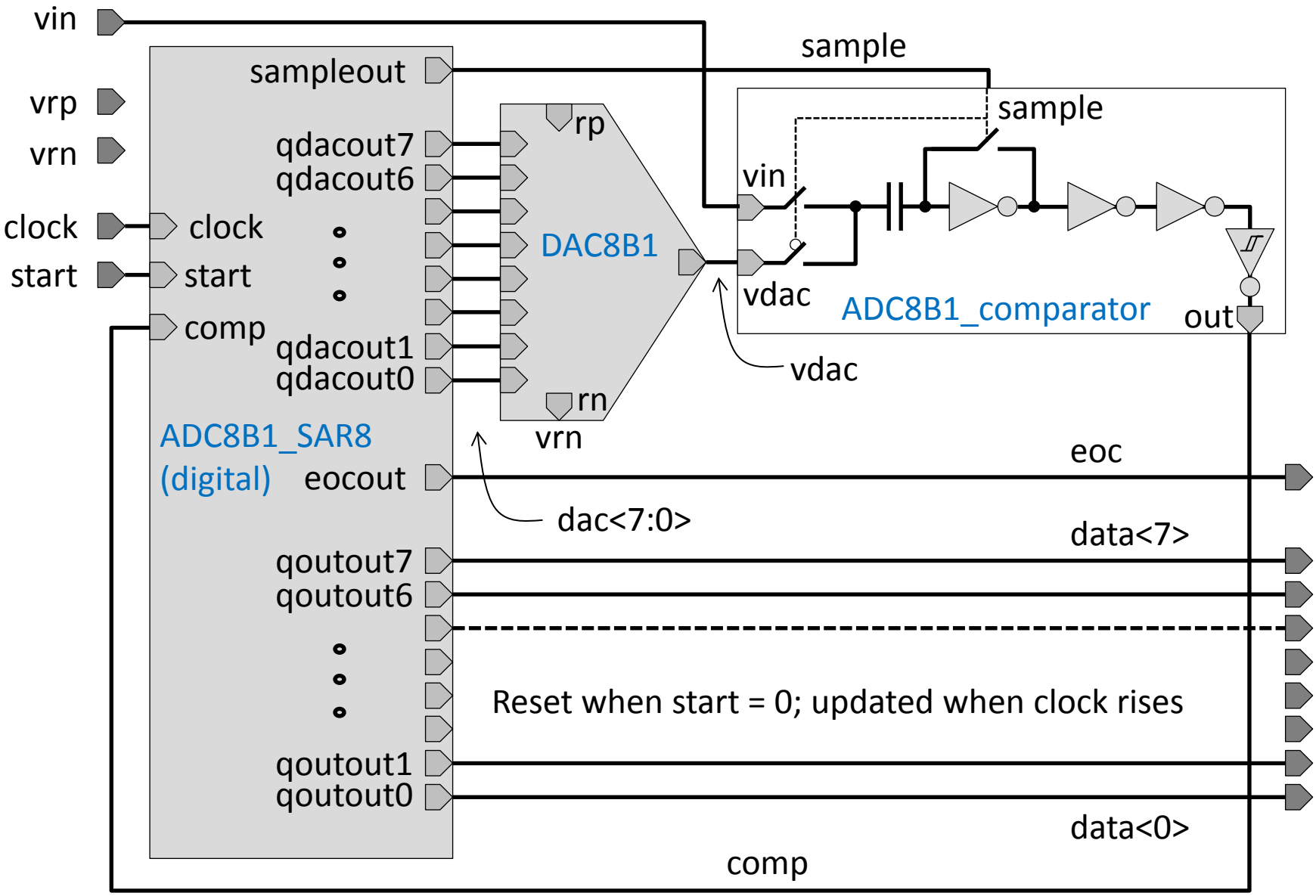
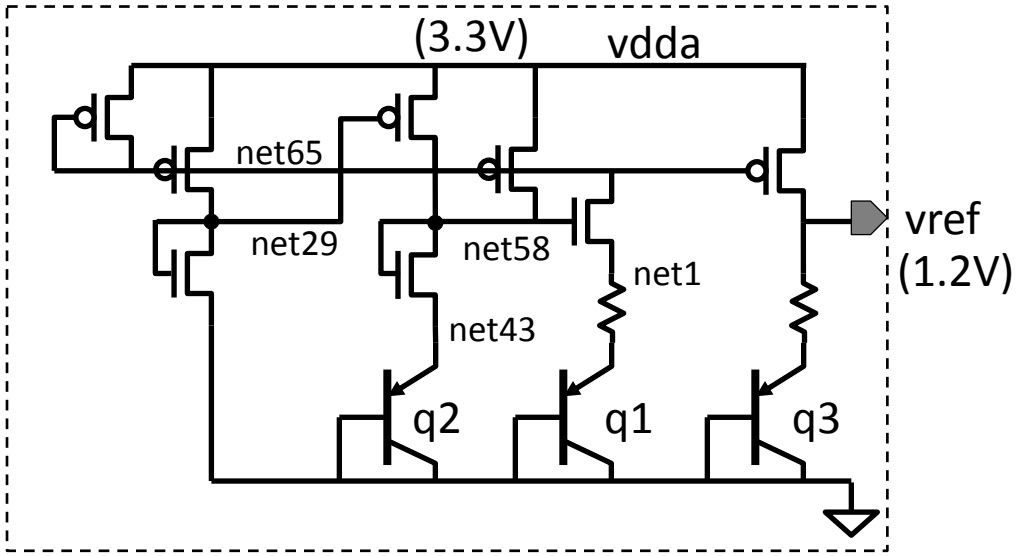
Schematics of the non-digital benchmark circuits

(listed in alphabetical order)

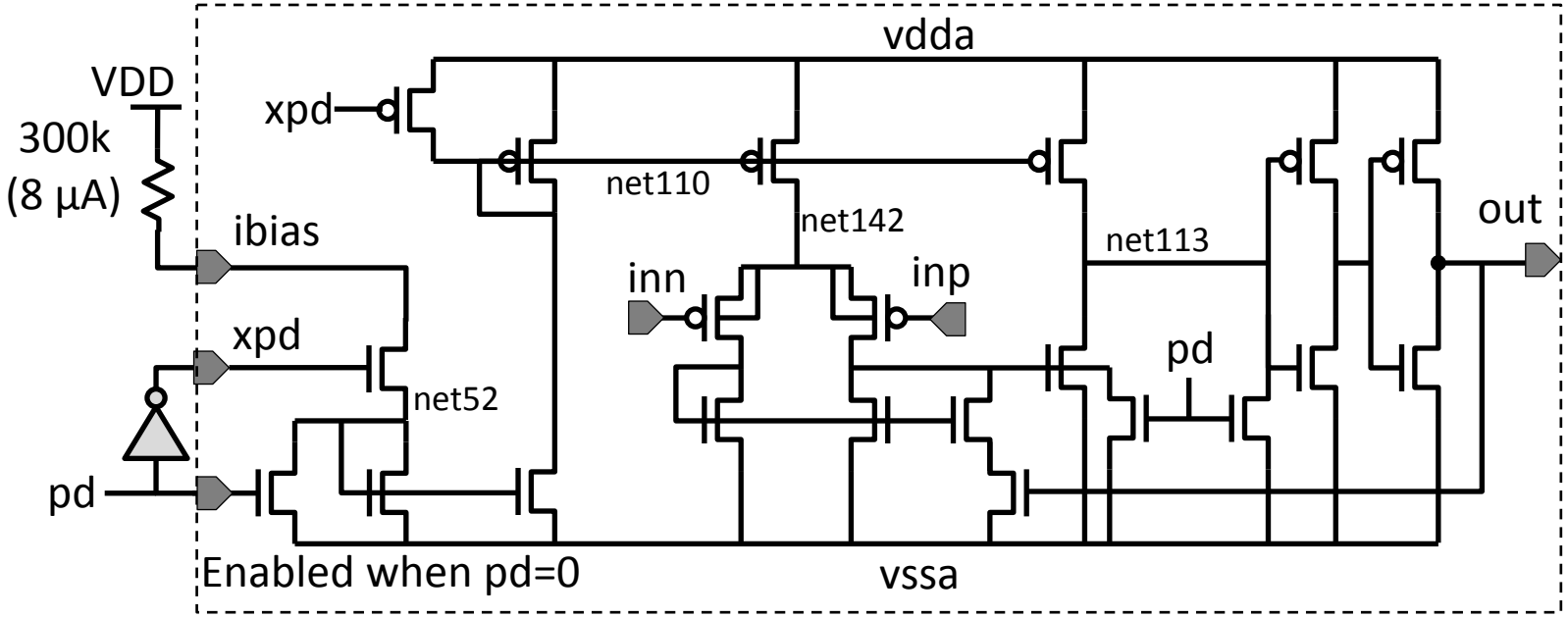
ADC8B1

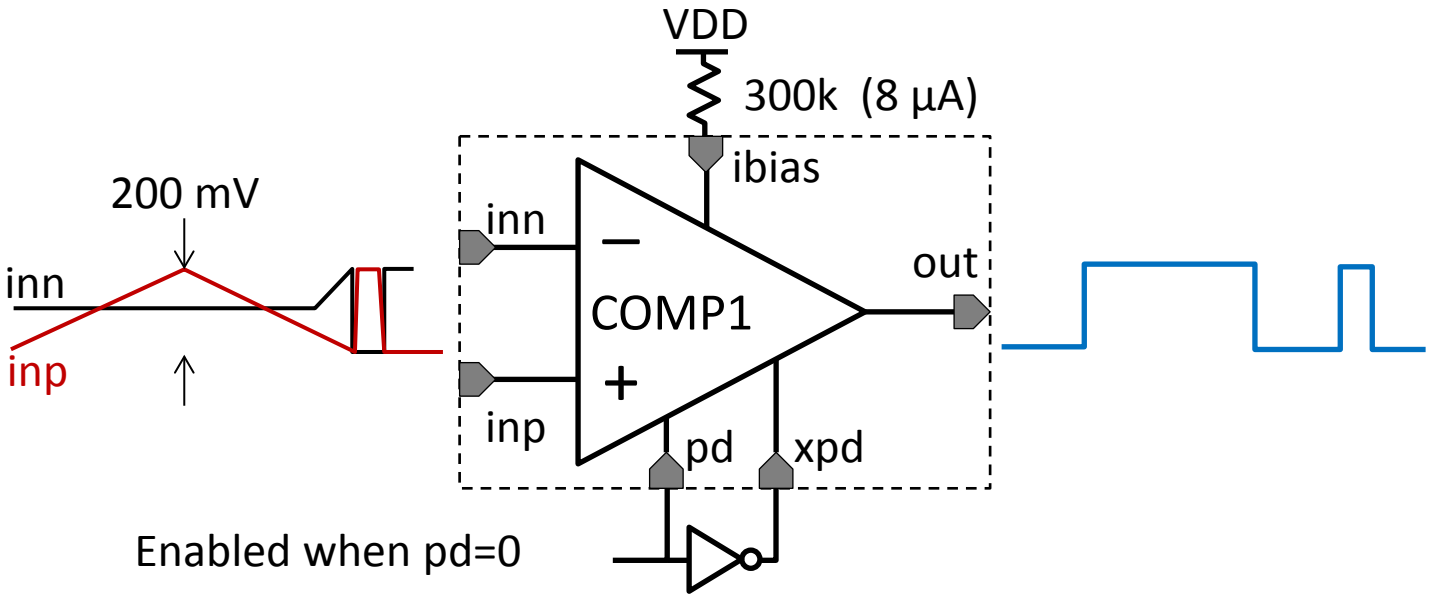

vin
vrp
vrn
clock
start
comp
sampleout
qdacout7
qdacout6
qdacout1
qdacout0
clock
start
ADC8B1_SAR8
(digital)
eocout
qoutout7
qoutout6
qoutout1
qoutout0
rp
rn
vrn
DAC8B1
sample
sample
vin
vdac
ADC8B1_comparator
out
vdac
dac<7:0>
eoc
data<7>
Reset when start = 0; updated when clock rises
data<0>
comp

BANDGAP1



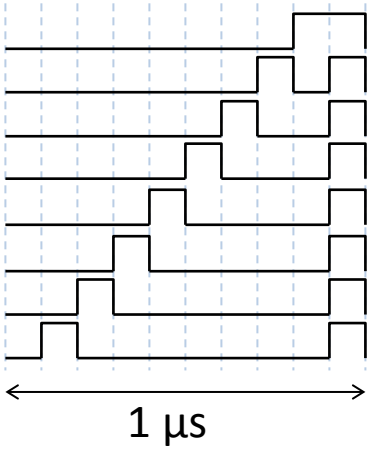
COMP1

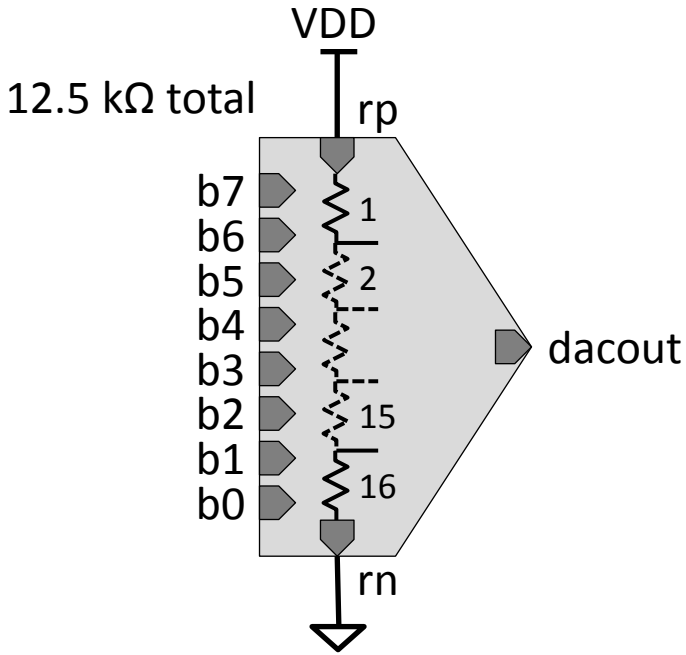

vdda
VDD
300k
(8 µA)
xpd
net110
net142
net113
out
ibias
inn
inp
xpd
pd
net52
pd
Enabled when pd=0
vssa


VDD
300k (8 µA)
ibias
200 mV
inn
inp
inn
COMP1
out
inp
pd
xpd
Enabled when pd=0

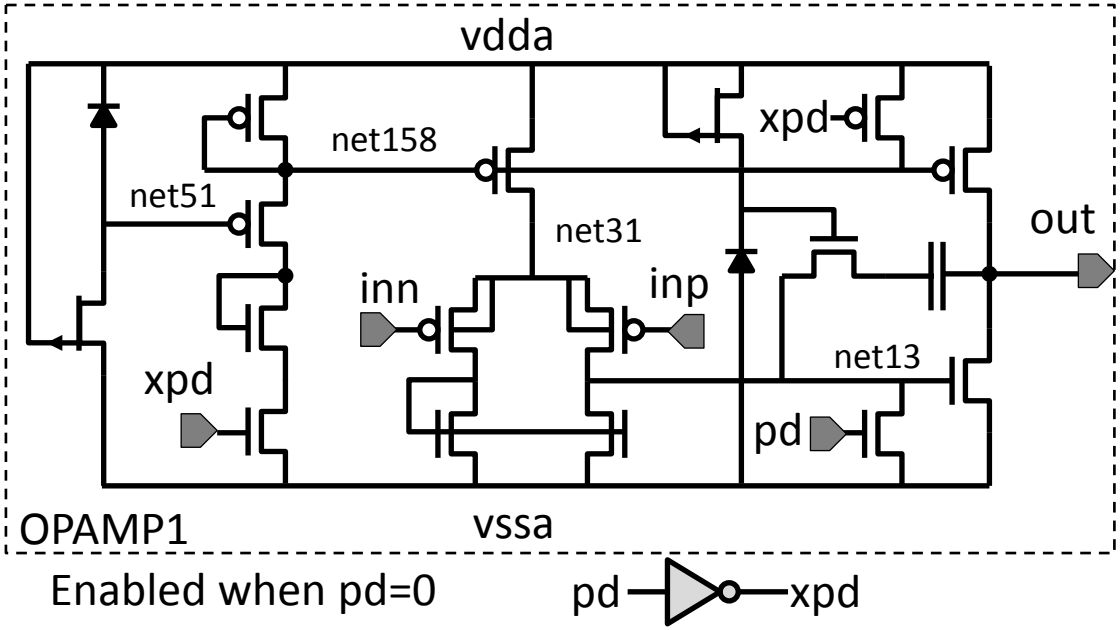
DAC8B1

Waveforms

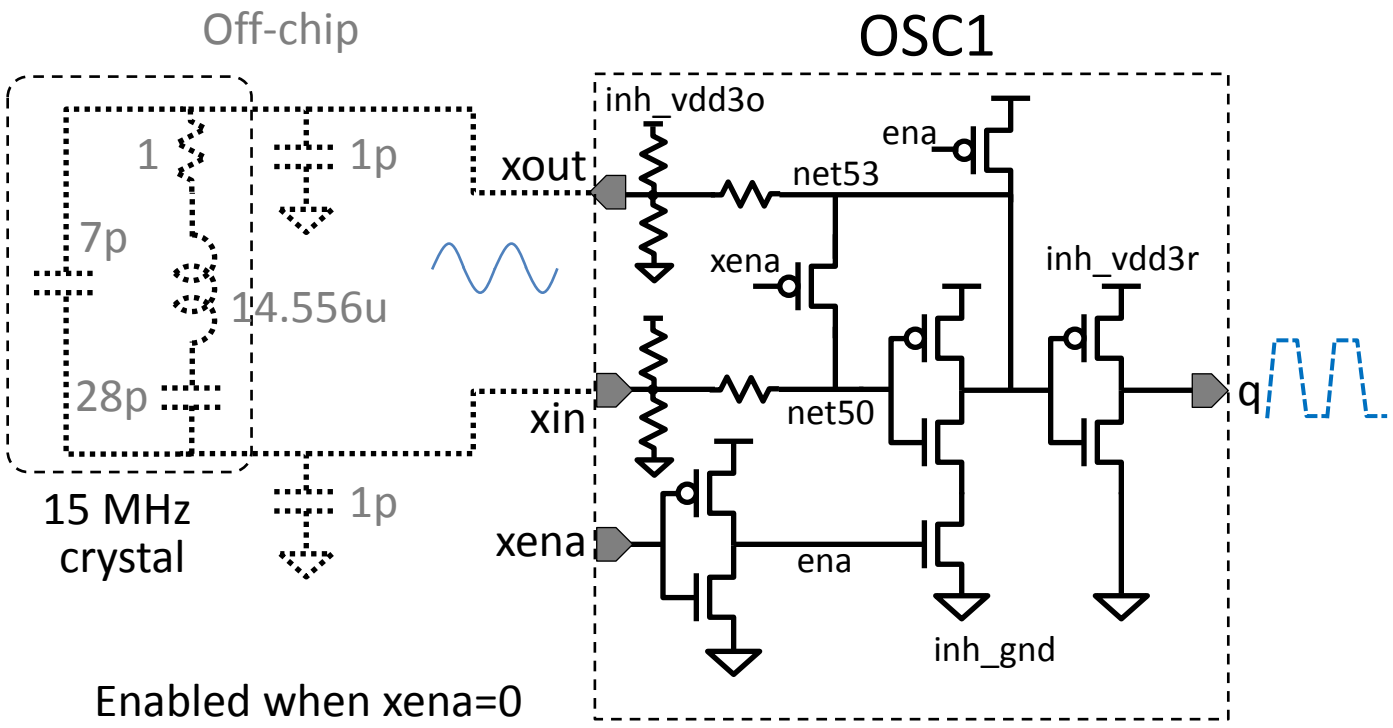




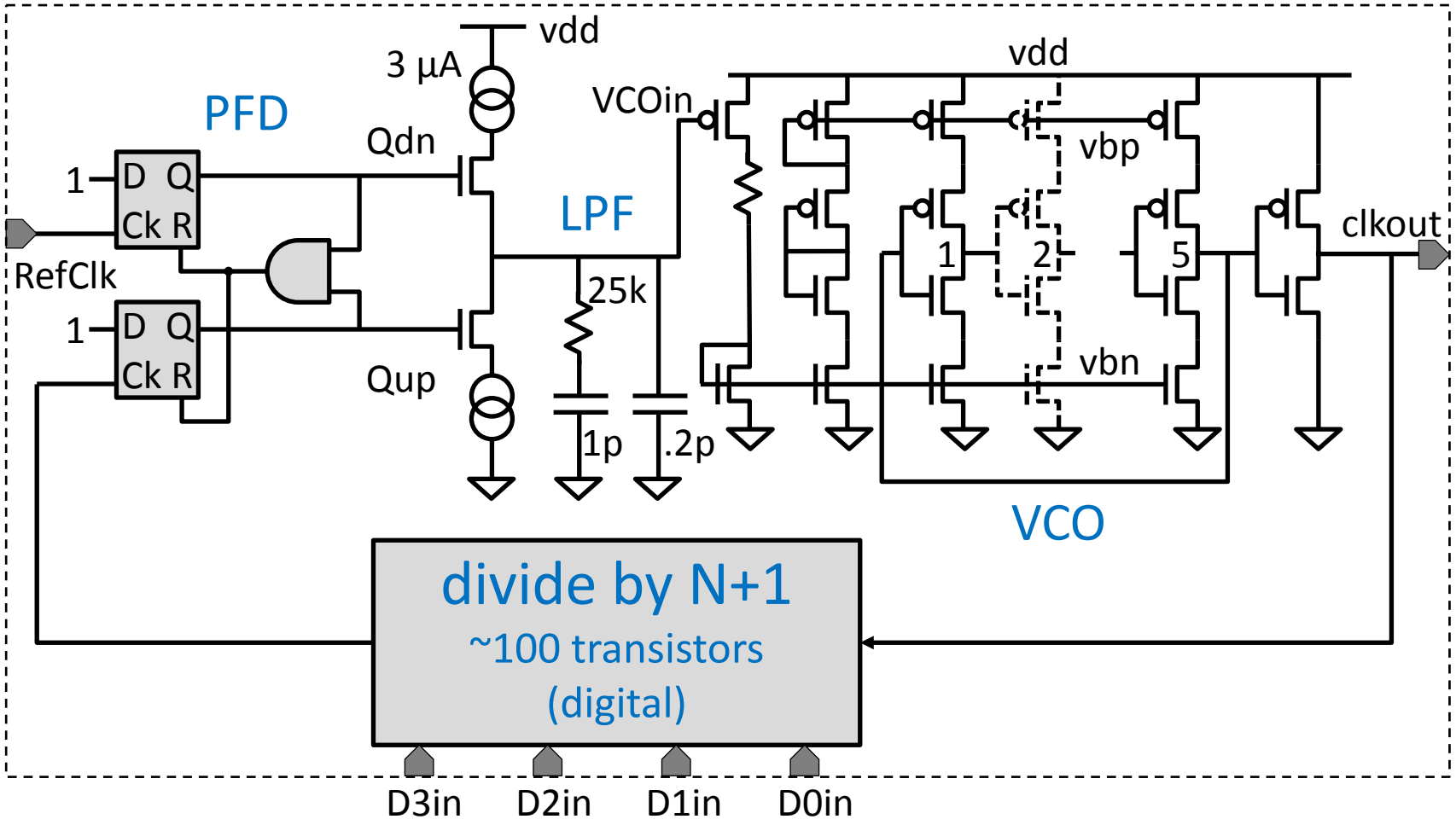
OPAMP1


vdda
net158
xpd
net51
net31
out
inn
inp
net13
xpd
pd
OPAMP1
vssa
Enabled when pd=0
pd
xpd

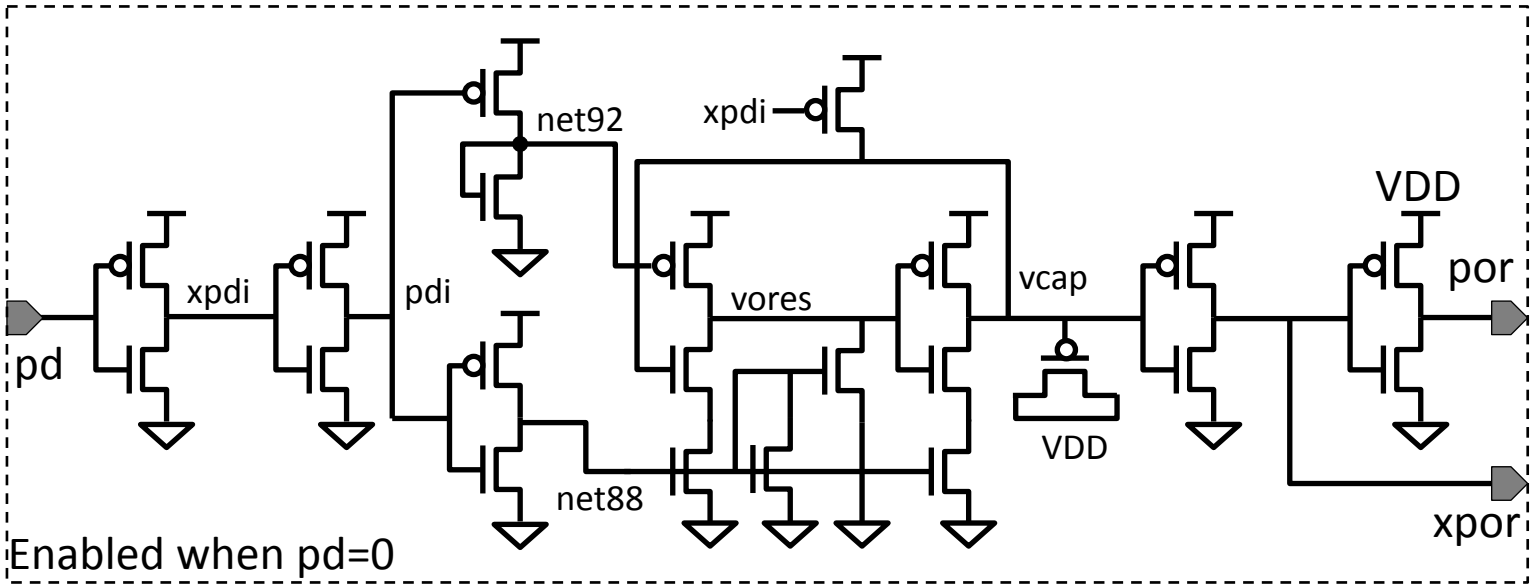
OSC1

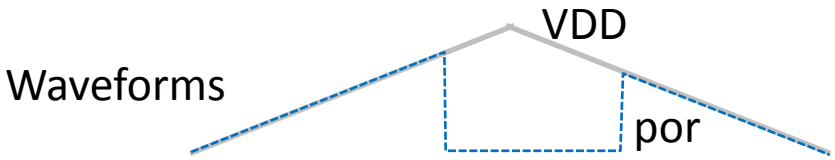

Off-chip
OSC1
1
1p
7p
14.556u
28p
1p
15 MHz
crystal
xout
xin
xena
inh_vdd3o
ena
net53
xena
inh_vdd3r
net50
q
ena
inh_gnd
Enabled when xena=0

PLL1

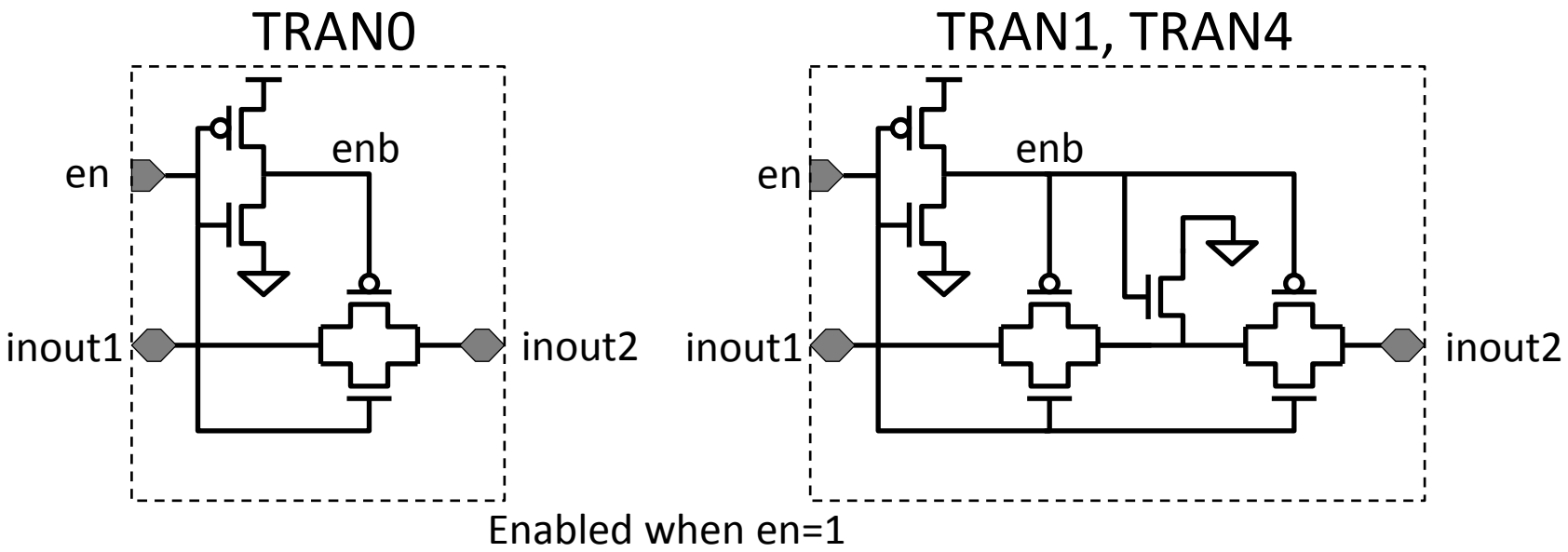

vdd
3 µA
PFD
Qdn
VCOin
vdd
vbp
1
D Q
Ck R
LPF
clkout
RefClk
1
2
5
1
D Q
Ck R
25k
Qup
vbn
1p
.2p
VCO
divide by N+1
~100 transistors
(digital)
D3in
D2in
D1in
D0in

POR1


net92
xpdi
VDD
xpdi
pdi
vores
vcap
por
pd
VDD
net88
xpor
Enabled when pd=0

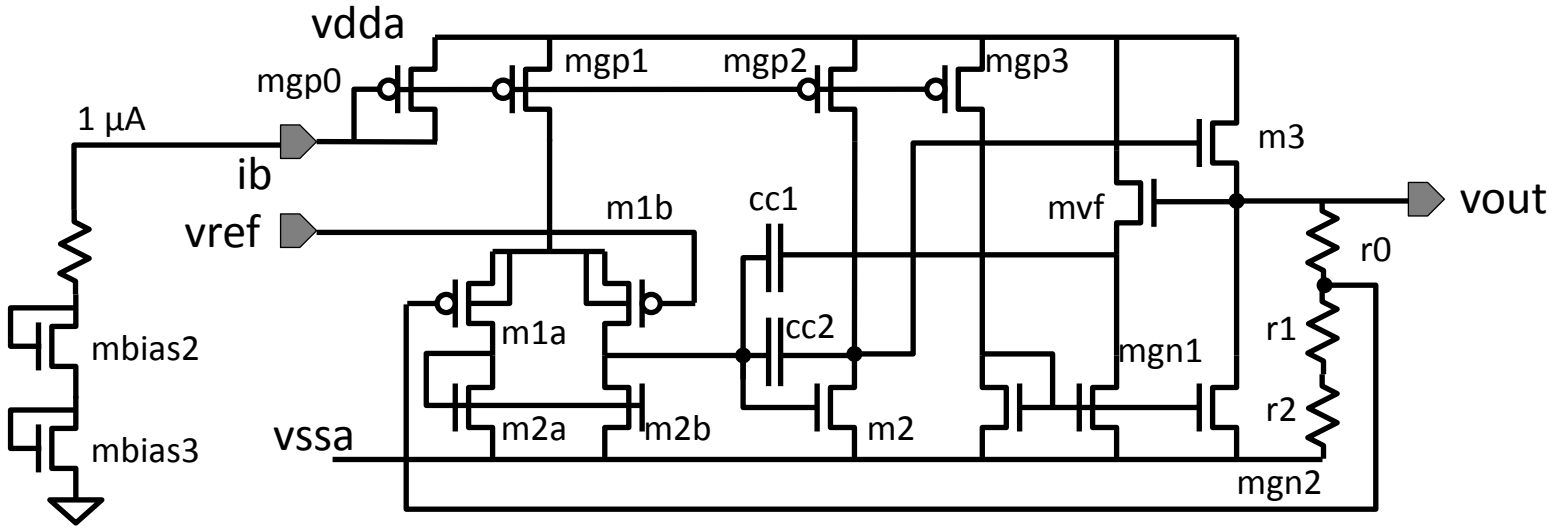

VDD
Waveforms
por

TRAN



Enabled when en=1

VREG1



1.8V voltage regulator (Vout = 3/2 x Vref)