Raghav Gupta

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EDUCATION

UNIVERSITY OF CALIFORNIA, BERKELEY | BS in Electrical Engineering and Computer Science
Expected May 2023 | GPA: 3.96/4.0
EECS Outstanding TA Award | Edward Frank Kraft Award

Relevant Coursework:
Computer Architecture and Engineering • Advanced Topics in Computer Systems • Introduction to Digital Design and Integrated Circuits • 22nm SoC for IoT • Great Ideas in Computer Architecture • Operating Systems and System Programming • Introduction to Robotics • Quantum Mechanics • Efficient Algorithms and Intractable Problems • Signals and Systems • Designing Information Devices and Systems I, II • Discrete Mathematics and Probability Theory • Teaching Techniques for Computer Science • Social Implications of Computer Technology

WORK/RESEARCH EXPERIENCE

ADEPT/SLICE LAB AT UC BERKELEY | Undergraduate Student Researcher
Jan 2021 – Present | Berkeley, CA | Website

FireMarshal
- A software workload management tool for reliable and reproducible RISC-V based full-stack hardware development and research
- Automates workload generation, development, and evaluation on FireSim, QEMU, and Spike.
- Implemented running multi-node workloads concurrently in QEMU
- Implemented a network interface using Virtual Distributed Ethernet for multi-node workloads emulated in QEMU

FirePerf
- An FPGA-accelerated full-system hardware/software performance profiling utility built on top of FireSim
- Provides high-fidelity out-of-band introspection with call stack reconstruction and automatic performance counter insertion
- Working on extending FirePerf to support userspace profiling

RPC Accelerator for a Hyperscale SoC
- Working on initial design space exploration to accelerate remote procedure calls as part of a datacenter SoC for a leading cloud provider

NVIDIA | Power Architect Intern
May 2022 – Aug 2022 | Santa Clara, CA

CPU Power Modeling for Gaming Workloads
- Developed a strategy for application-specific CPU power modeling on production silicon
- Targeted characteristics of gaming workloads and isolated static and dynamic power costs
- Automated data collection, processing, visualization, modeling and summary statistics

TEACHING EXPERIENCE

EECS 151/251A - INTRODUCTION TO DIGITAL DESIGN AND INTEGRATED CIRCUITS | Teaching Assistant
Aug 2022 – Present | Berkeley, CA | Website
- Teaching 1 weekly office hour and 1 weekly lab section using Xilinx PYNQ FPGAs for Berkeley's upper division VLSI course catered towards undergraduates and graduates
- Helping students learn hardware design methods and principles using Verilog, VCS, and waveforms as they implement FSMs, audio synthesis circuits, UART modules and FIFOs on FPGAs
- Supporting students in applying architectural and microarchitectural concepts to design a 3+ stage pipelined RISC-V datapath with L1 data cache, UART/MMIO and optimize it for timing

- Designed a memory controller lab with specification and testbenches as an introduction to working with synchronous memories

EECS16A - DESIGNING INFORMATION DEVICES AND SYSTEMS I | Lab Teaching Assistant and Head Lab Content/Development

Jun 2020 – May 2022 | Berkeley, CA | Website

- Taught a weekly lab section of 50+ engineering undergraduates for Berkeley's introductory EECS course for 5 semesters
- Assisted students in building a single pixel camera, resistive and capacitive touchscreens, and an acoustic positioning system
- Trained lab staff and managed lab content for 1000+ students, revamped existing labs, developed new labs and managed the shift to online labs while achieving the requisite learning goals.

CS61C - GREAT IDEAS IN COMPUTER ARCHITECTURE | Teaching Assistant

Jun 2021 – Aug 2021 | Berkeley, CA | Website

- Taught 2 discussion sections and 1 office hour weekly for Berkeley's introductory computer architecture and systems course
- Developed content and infrastructure for projects on C programming and Logisim datapath design
- Helped design labs on Logisim datapath design, pipelining, and caches

PROJECTS

BEARLY ML: SOC FOR MACHINE LEARNING | EE290C

Jan 2022 – May 2022

- Designed, verified, and taped-out a RISC-V SoC with ML/DSP accelerators in Intel 16 technology using the Chipyard environment
- Member of team developing a sparse-dense matrix multiplication accelerator using the Rocket Custom Coprocessor (RoCC) interface
- Tightly-coupled with a 5 stage, in-order Rocket core with 16KB L1D$, 4KB L1I$
- Wrote Chisel RTL, performed verification in functional simulation with unit-testing and integration testing with bare-metal C tests, and resolved floor-planning Design Rule Violations
- Maximum frequency: 500 MHz, Achievable Throughput: 2.6 GOPS

RISC-V CORE ON FPGA | EECS151

Oct 2021 – Dec 2021

- Designed a 3-stage RISC-V core with UART/MMIO, polyphonic audio synthesizer and BHT-based branch predictor in Verilog.
- Won class-wide Apple design contest for performance at a frequency of 70 MHz with a CPI of 1.16 on the matrix multiplication kernel.

BRANCH PREDICTOR | Lab Project for CS152

Mar 2021 – Apr 2021

- Designed and analyzed an 8192-entry tournament predictor using a Gshare predictor, a bimodal predictor, and an arbiter.
- Implemented using the C++ branch predictor framework in the BOOM out-of-order core
- Performed >25% better than baseline bimodal predictor.

PINTOS | Projects for CS162

Jan 2022 – May 2022

- Implemented the following features in an x86-based educational OS running as a VM in QEMU/Bochs with extensive debugging in GDB
- Supported user program execution with syscall argument passing, process control syscalls (halt, exec, wait, exit), basic file operation syscalls, and a floating point unit
- Implemented multithreading with an efficient sleep timer, strict priority scheduler with priority donation, and a simplified version of the user-level pthread library and user-level synchronization
- Implemented a Unix FFS-like filesystem with buffer cache, extensible files and support for subdirectories and relative paths

CS61CPU | Project for CS61C

Nov 2020

- Designed a 2-stage pipelined RISC-V Datapath in Logisim.
- Optimized control logic by simplifying boolean expressions for each signal.
- Won class-wide Apple design contest for minimal transistor use.