

Raghav Gupta

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EXPERIENCE

FIREMARSHAL | UNDERGRADUATE RESEARCH AT ADEPT LAB

Jan 2021– Present

- A software workload management tool for RISC-V based full-stack hardware development and research that automates workload generation, development, and evaluation.
- Implementing a network interface using Virtual Distributed Ethernet for multi-node workloads emulated using QEMU.

EECS16A - DESIGNING INFORMATION DEVICES AND SYSTEMS

I | LAB TEACHING ASSISTANT AND HEAD LAB CONTENT/DEVELOPMENT

Jun 2020 – Present | eecs16a.org

- Teach a weekly lab section of 50+ engineering undergraduates for Berkeley's introductory EECS course.
- Connect lecture knowledge with real-world applications, clear concepts and bugs as students build a single pixel camera, resistive and capacitive touchscreens, and an acoustic positioning system.
- Manage lab content for 1000+ students, revamp existing labs, develop new labs and shift to online labs while achieving the requisite learning goals.
- Train TAs and lab assistants, write, debug, and proctor midterms and finals.

CS61C - GREAT IDEAS IN COMPUTER ARCHITECTURE |

TEACHING ASSISTANT

Jun 2021 – Aug 2021 | cs61c.org

- Taught 2 discussion sections and 1 office hour weekly.
- Developed content and infrastructure for projects on C programming and Logisim datapath design.
- Helped design labs on Logisim datapath design, pipelining, and caches.

PROJECTS

BRANCH PREDICTOR | CS152

- Designed and analyzed an 8192-entry tournament predictor using a Gshare predictor, a bimodal predictor, and an arbiter in C++.
- Performed >25% better than baseline bimodal predictor.

CS61CPU | CS61C

- Designed a 2-stage pipelined RISC-V Datapath in Logisim.
- Optimized control logic by simplifying boolean expressions for each signal.
- Won class-wide Apple design contest for minimal transistor use.

HARDWARE PREFETCHER | CS152

- Designed a strided hardware prefetcher using C++/SystemVerilog DPI that showed >5% improvement on the Transpose kernel.
- Identified repeating patterns and accounted for timing of prefetch.

SIXT33N | EECS16B

- Made a dual motor voice controlled robot (while studying remotely).
- Implemented a mic board, frequency filters, closed-loop feedback control and k-means classification with PCA.

CS61CLASSIFY | CS61C

- Performed neural network forward propagation in RISC-V Assembly using ReLU, ArgMax, matrix multiplication, and file operations.

EDUCATION

UNIVERSITY OF CALIFORNIA, BERKELEY

BACHELOR OF SCIENCE IN
ELECTRICAL ENGINEERING AND
COMPUTER SCIENCE

Expected May 2023 | 3.97 / 4.0

Edward Frank Kraft Award

EECS Outstanding TA Award

COURSEWORK

CS152: Computer Architecture and Engineering • EECS151: Introduction to Digital Design and Integrated Circuits (in progress) • CS61C: Great Ideas in Computer Architecture • EE120: Signals and Systems • EECS16 A/B: Designing Information Devices and Systems I, II • CS70: Discrete Mathematics and Probability Theory

SKILLS

Python • C/C++ • Git • Verilog • AWS • Linux • RISC-V • SIMD • Parallel Programming • QEMU • Java • OOP • JavaScript • Matlab • VisualBasic • SQL • Computer Vision • Arduino • LaTeX • CircuitTikz • SolidWorks • Rapid Prototyping

CERTIFICATES

Machine Learning by Stanford University (Coursera)

ORGANIZATIONS

ETA KAPPA NU (EECS HONOR SOCIETY)

DeCal Assistant Officer - Responsible for facilitating "Going Down the EECS Stack", a course that explores the EECS major.

CURIOSITY

Co-founder - Raised funds for COVID-19 and flood relief by tutoring high school students and SAT aspirants.