# Raghav Gupta

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Website | GitHub | LinkedIn

## EDUCATION

### UNIVERSITY OF CALIFORNIA, BERKELEY

**PhD in Computer Science**
Aug 2023 - Present
Advisor: Prof. Borivoje Nikolic

**Coursework:**
Architectures and Systems for Warehouse-Scale Computers (A)

**BS in Electrical Engineering and Computer Science**
Aug 2019 - May 2023 | GPA: 3.95/4.0
High Honors | Dean's List

**Coursework:**
Computer Architecture and Engineering (A) • Operating Systems and System Programming (A) • Introduction to Digital Design and Integrated Circuits (A+) • 22nm SoC for IoT (A) • Advanced Topics in Computer Systems (A-) • Programming Languages and Compilers (A)

## RESEARCH INTERESTS

**COMPUTER ARCHITECTURE**
Hyperscale Architecture and Systems
Hardware Design Methodology

## TEACHING EXPERIENCE

CS152/252A - Computer Architecture and Engineering • EE290C - 22nm SoC for IoT • EECS 151/251A - Introduction to Digital Design and Integrated Circuits • CS61C - Great Ideas in Computer Architecture • EECS16A - Designing Information Devices and Systems I

## SKILLS

Python • C/C++ • Git • Linux/Bash • Verilog • Chisel • Go • RISC-V • CUDA • Java • Vivado • Docker • Kubernetes • ROS

## AWARDS

EECS Oustanding TA Award (2020-21)
CS61C Project - RISCV CPU in Logisim - Apple Design Award (Fall 2020)
EECS151 Project - RISCV Core on FPGA - Apple Design Award (Fall 2021)
Edward Frank Kraft Award (Fall 2019)
Times of India - Spark Scholarship (2018)

## RESEARCH EXPERIENCE

### SLICE LAB AT UC BERKELEY | Student Researcher

Jan 2021 – Present | Berkeley, CA | Website

**Hybrid Simulation/Emulation**
Collaboration with AMD/Xilinx | Sep 2024 - Present

- Building a hybrid simulation/emulation platform atop FireSim to enable design verification and early DSE
- Initial prototype allows system bus modules to be simulated in C++ while the rest of the SoC is emulated on an FPGA
- Initial results show O(10 MHz) simulation frequency when running Linux+Coremark and snooping on SoC memory requests in software

**Multi-level Simulation**
Oct 2023 - Apr 2024

- Helped build a multi-level simulator trading off speed and fidelity in a hierarchy of simulators for DSE on large workloads
- Used program analysis to identify critical portions of an execution trace to execute at high fidelity
- Investigated warm-up strategies to approximate cache state

**Extending FirePerf to Userspace**
Original Paper | Poster | Userspace Paper

- FirePerf is an FPGA-accelerated full-system hardware/software performance profiling utility that provides high-fidelity out-of-band introspection with call stack reconstruction and Flame Graph generation
- Extended FirePerf to support userspace profiling by instrumenting the Rocket Chip trace port, obtaining DWARF + hex information, constructing a user binary search space and matching traces to it

## WORK EXPERIENCE

### AMD/XILINX | Research and Advanced Development Intern

Jun 2024 – Dec 2024 | San Jose, CA

**Hybrid Simulation/Emulation**

- Implemented and evaluated two strategies to build a fast and flexible hybrid simulation/emulation platform
- Ported an internal co-simulation framework and an open-source emulation framework to an internal emulation machine

### NVIDIA | Power Architect Intern

May 2022 – Aug 2022 | Santa Clara, CA

**CPU Power Modeling for Gaming Workloads**

- Developed a strategy for application-specific CPU power modeling on production silicon
- Targeted characteristics of gaming workloads and isolated static and dynamic power costs

## PUBLICATIONS/PRESENTATIONS

- Whangbo, Joonho, et al. **"FireAxe: Partitioned FPGA-Accelerated Simulation of Large-Scale RTL Designs,"** ISCA 2024.
- Chi, Yufeng, Franklin Huang, **Raghav Gupta,** Ella Schwarz, Jennifer Zhou, Reza Sajadiany, Animesh Agrawal, et al. **"A Heterogeneous RISC-V SoC for ML Applications in Intel 16 Technology."** Poster presented at HotChips 2023, Stanford, CA.