Raghav Gupta

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GitHub | LinkedIn

EXPERIENCE

FIREMARSHAL | Undergraduate Research at ADEPT Lab
Jan 2021– Present

- A software workload management tool that automates workload generation, development, and evaluation.
- Used for RISC-V based full-stack hardware development and research
- Implementing a network interface using Virtual Distributed Ethernet for multi-node workloads emulated using QEMU.

EECS16A - DESIGNING INFORMATION DEVICES AND SYSTEMS I | Lab Teaching Assistant and Head Lab Development
Jun 2020 – Present | **eecs16a.org**

- Manage labs for 1000+ students by revamping current lab projects, developing new ones, training TAs and lab assistants, writing and proctoring exams
- Connect lecture knowledge with real-world applications, clear concepts and bugs as students build a single pixel camera, resistive and capacitive touchscreens, and an acoustic positioning system.

CS61C - GREAT IDEAS IN COMPUTER ARCHITECTURE | Teaching Assistant
Jun 2021 – Aug 2021 | **cs61c.org**

- Developed content and infrastructure for projects on C programming and Logisim datapath design.
- Helped design labs on Logisim datapath design, pipelining, and caches.

PROJECTS

RISC-V CORE ON FPGA | EECS151

- Designed a 3-stage RISC-V core with UART, polyphonic audio synthesizer and BHT-based branch predictor in Verilog.
- Won class-wide Apple design contest for performance at a frequency of 70 MHz with a CPI of 1.16 on the matrix multiplication kernel.

BRANCH PREDICTOR | CS152

- Designed and analyzed an 8192-entry tournament predictor using a Gshare predictor, a bimodal predictor, and an arbiter in C++.
- Performed >25% better than baseline bimodal predictor.

CS61CPU | CS61C

- Designed a 2-stage pipelined RISC-V Datapath in Logisim. Optimized control logic by simplifying boolean expressions for each signal.
- Won class-wide Apple design contest for minimal transistor use.

HARDWARE PREFETCHER | CS152

- Designed a strided hardware prefetcher using C++/SystemVerilog DPI that showed >5% improvement on the transpose kernel.
- Identified repeating patterns and accounted for timing of prefetch.

SIXT33N | EECS16B

- Made a dual motor voice controlled robot (while studying remotely).
- Implemented a mic board, frequency filters, closed-loop feedback control and k-means classification with PCA .

CS61CLASSIFY | CS61C

- Performed neural network forward propagation in RISC-V Assembly using ReLU, ArgMax, matrix multiplication, and file operations.

EDUCATION

UNIVERSITY OF CALIFORNIA, BERKELEY
Bachelor of Science in Electrical Engineering and Computer Science
Expected May 2023 | 3.95 / 4.0

COURSEWORK

CS152: Computer Architecture and Engineering • EE290C: 22nm SoC for IoT (in progress) • EECS151: Introduction to Digital Design and Integrated Circuits • CS61C: Great Ideas in Computer Architecture • CS162: Operating Systems and Systems Programming (in progress) • EE120: Signals and Systems • EECS16 A/B: Designing Information Devices and Systems I, II • CS70: Discrete Mathematics and Probability Theory

SKILLS

Python • C/C++ • Git • Verilog • Java • AWS • Linux • RISC-V • SIMD • Parallel Programming • Vivado • QEMU

ACHIEVEMENTS

Edward Frank Kraft Award
EECS Outstanding TA Award

CERTIFICATES

Machine Learning by Stanford University (Coursera)

ORGANIZATIONS

ETA KAPPA NU (EECS HONOR SOCIETY)
DeCal Assistant Officer
Responsible for facilitating "Going Down the EECS Stack", a course that explores the EECS major.