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Local-Station Calibration for Dummies!
The Missing Manual

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Abstract

The SD local station performs a collection of online calibration algorithms to set the gains of the PMTs to the nominal levels and make assignments of various trigger thresholds in correct physical units.

These local-station calibration procedures are implemented in the station DAQ software. During the transition from UB to UUB electronics, this software was ported from the OS-9 operating system of the UB running on a PowerPC processor to the Petalinux operating system of the UUB running on an ARM processor. The main architecture of the calibration procedures has remained almost unchanged. However, there is a lack of detailed documentation for both the UB and UUB.

This note aims to describe the calibration processes of the local station, trying, where possible, to highlight the differences between UB and UUB. HV settings, histogram filling, and the procedures for estimation of calibration parameters are also described.

Contents

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1 Introduction

The calibration procedures of the local station were developed to relate the response of the three PMTs to the most probable response produced by a vertical, through-going muon passing through the central axis of the tank, i.e. the response of a vertical-equivalen muon (VEM). At the time there is a severe lack of documentation regarding calibration in upgraded stations. This note aims to describe how the calibration is done, at the level of hardware as well as software. In this note, we will use the symbols and definitions as laid out in in Table 1.

The traces collected in the FPGA shower memory of the UUB are packaged by the DAQ and then sent to CDAS. The traces are shipped in raw form (ADC counts or in adc units), so they need a calibration procedure to ensure subsequent analysis can be performed independent from the local station.

2 Vertical vs omni-directional muons

The signal due to the Cherenkov light developing at the local station is measured in units of the signal produced by a vertical and central through-going muon, which is termed as vertical-equivalent muon (VEM). During the shower reconstruction procedure, the signals recorded in the local stations are converted from ADC counts (adc) to units of VEM, and the shower characteristics, i.e. total energy and direction of arrival, are determined.

Atmospheric muons passing through the detector are used as a reference to obtain the value of 1 VEM in ADC counts. However, the configuration of the station does not allow the selection of vertical through-going muons, so that the charge and pulse-height distributions of the signals from omnidirectional atmospheric muons are used. In a reference tank, only vertical muons were selected using a hodoscope, and Q_{VEM} and I_{VEM} were estimated to be the best measure of the

Table 1: The table shows the nomenclature used in this GAP.

Symbol	Definition
Q_{VEM}	VEM charge measured in a reference tank by selecting vertical through-going muons
Q_{rate}	charge estimated with an online, rate-based procedure at the local station
Q_{histo}	charge estimated offline with the histogram produced online
I_{VEM}	VEM peak measured in a reference tank by selecting vertical through-going muons
I_{rate}	peak estimated with an online, rate-based procedure at the local station
I_{histo}	peak estimated offline with histogram produced online

Table 2: Ratios of measured charge and peak for omnidirectional muons to their vertical-centered counterparts defining VEM, respectively.

q	Q_{VEM}/q
Q_{rate}	1.045
Q_{histo}	1.01

i	I_{VEM}/i
I_{rate}	1
I_{histo}	0.87

charge and peak of the signal of a vertical muon. These values cannot be calculated in a station in its normal working state, so it was necessary to measure the ratio between the quantities defined above and the quantities evaluated in the local station. The local station can estimate the quantities related to Q_{VEM} and I_{VEM} in two different ways: through calibration histograms and through a rate-based method. For clarity purposes, it is important to underline that there is no histogram fit procedure in the DAQ, so the histograms are reworked offline to estimate the parameters.

An example calibration histogram is shown in Fig. (Alex-pics), particularly the charge histogram on the right and pulse heights histogram on the left. The distributions have two characteristic peaks; the first peak is caused by a convolution of low-energy particle signals and noise, while the second peak is due to omnidirectional through-going muons.

The charge distribution is used to define the value Q_{histo} by estimating the position of the second peak. The estimation of this value is not done directly online, in fact, the histogram is sent to CDAS and then in the offline reconstruction of the event it is evaluated and used to convert the traces from ADC counts (adc) to VEM units.

The distribution of pulse heights also has the shape seen in the charge distribution due to the same physical mechanism caused by atmospheric muons. The estimation of the position of the second peak I_{histo} in this distribution would provides the common threshold in ADC counts to set the various trigger types defined for the surface detector. However, this value is not used practically in the DAQ software to set the thresholds, the estimate I_{rate} of it is used, and this operation is performed in a different process than the one that calculates the histograms. However, the histogram of the pulse heights is also sent to CDAS and the I_{histo} value extrapolated offline is used in subsequent analyses to discriminate muon signals from the main signal.

The DAQ also uses a method based on a reference rate to calculate the values of Q_{rate} and I_{rate}; these values are another estimate of Q_{VEM} and I_{VEM} and are in a different relation to them than the values obtained with the histograms. The various relations between all the quantities defined above are described in the **??**.

In this note, first, the structure of the memory buffers and the relation to the various triggers defined in the FPGA firmware will be described. Next, we will describe a higher level in the DAQ software where histograms calculation and estimation of I_{rate} and Q_{rate} are performed. ?...

3 Local station

To fully understand the calibration procedure, it is necessary to explore the hardware and software structure involved in this process. We will first cover that of the UB (Section 3.1) and then the UUB (Section 3.2).

Unless otherwise specified, descriptions apply to both UB and UUB. Differences are explicitly addressed.

The local station is comprised of the operating system on top of which a DAQ is running. The DAQ is conceptually split into the software (i.e. collection of Unix processes) and firmware (i.e. programming of the PLD or FPGA).

3.1 UB electronics

The electronics of the local station is called a Unified Board because it consists of a single board that includes the analogue front end and the hardware required for data acquisition and trigger generation.

The front end must receive the signals from the three PMTs (Photonis XP1805/D1). Due to their proximity to water, they operate with a positive anode voltage, with the photocathode at ground.

The high voltage is supplied locally by a module integrated into the PMT base and is proportional to a DC control voltage supplied by the slow control system. The signal to the last dynode is amplified and inverted by the PMT base electronics to provide a signal with 32 times the anode charge gain. No signal modeling is performed on the PMT base.

Analog signals from PMT are filtered and fed to a semi-flash ADC running at 40 MHz with 10 bit of accuracy (AD9203). The negative ADC inputs are polarized to −50 mV to bring the input pedestal on scale. The digitized signals are stored in circular buffers, and each time the electronics establishes that a trigger condition is met, a block of 768 time bins (1/40 MHz = 25 ns per bin) is acquired. If the higher trigger levels allow it, the data will be sent to the Central Data Acquisition System (CDAS) for subsequent analysis. There are six such time slots (2 per PMT) whose amplitude is measured in ADC counts (adc). Since they are 10 bit accurate and the converter range is between 0 V and 2 V, we have that 1 adc is about 1.95 mV ($2\,\mathrm{V}/2^{10}$).

A LED flasher is used to remotely test the photomultiplier linearity, incorporating two LEDs that can be pulsed independently or simultaneously and with variable amplitude.

The electronics has also a GPS receiver (Motorola OEM Oncore UT+) with the corresponding antenna mounted at the top of the tank for event timing and communications synchronization.

The station controller consists of an IBM PowerPC 403 GCX-80 MHz, with a 32 MB DRAM bank to store data and executable code, and a 2 MB Flash EPROM for bootstrapping and storing OS9 operating system.

In the UB, the trigger logic is implemented by two Altera programmable logic devices (PLDs) and an IDT static RAM chip.

The PLD firmware is written in Altera AHDL and is compiled using Altera's Quartus compiler.

The PLD code is divided between the two PLDs. PLD A receives only the high-gain ADC signals, which are the only ones used in the trigger, and stores them in its internal memory buffer. PLD B receives both high-gain and low-gain ADC signals. It stores the low-gain ADC signals in its internal memory buffer and uses the high-gain signals for trigger generation. Any shower triggers generated by one of the PLDs are passed to the other, so that both PLDs see exactly the same set of triggers. A more accurate description of memory buffers will be given in Section 3.3.

3.2 UUB electronics

The ADCs at the front-end of the UUB are fed with signals coming from the small PMT (SPMT), the large PMTs (LPMTs) detecting Cherenkov light from the WCD, and the PMT collecting light from the SSD. Sampling frequency? The five signals are divided into five high-gain and five low-gain signals, respectively. They are obtained by using two amplifiers in parallel with different

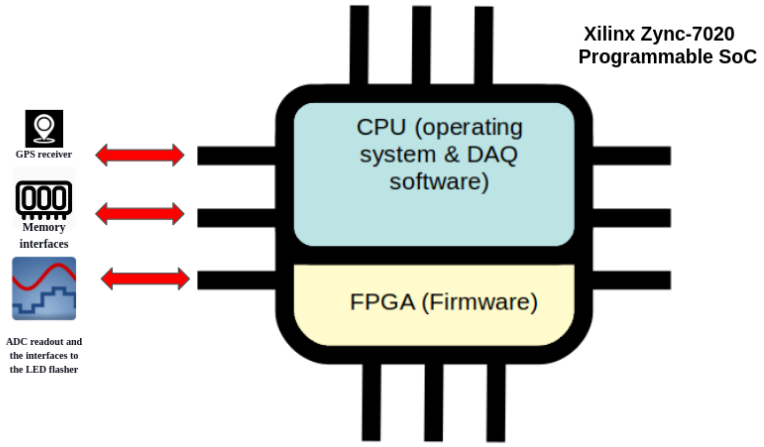

Figure 1: Schematic representation of the station system: SoC = FPGA + CPU. TODO: no red box, icons only, shorter names: ADC, memory, GPS, SoC

gains; the signals of the LPMTs are divided with a gain ratio of 32 while the signal of the SSD PMT is divided to reach a gain ratio of 128, allowing for it a dynamic range of 20 000 MIP (minimum-ionizing particle). What is the dynamic range for WCD?

The VEM signal is used to calibrate the high-gain channels of the WCD; the procedure is carried out by the DAQ software and has been mainly inherited from the one carried out with the old electronics. In addition, each WCD is equipped with two LEDs used for monitoring and linearity tests.

The management of slow control is performed by the MSP430 microcontroller. It controls the high voltage monitoring of the PMT, the supervision of the various supply voltages and the reset functionality. In addition, the micro-controller also provides a USB interface, which is very useful if you need to perform tests on the UUB. The 90 variables collected by the slow-control software are acquired by the DAQ software and sent to the Auger monitoring database.

A very important component of the UUB is the Xilinx Zync-7020 Programmable SoC (System on Chip), which forms an embedded system between an Artix-7 FPGA and associated Cortex A9 Dual 333 MHz ARM co-processor. Types of available memory... More hardware parts? Which GPS module? A schematic representation of the SoC of UUB is presented in Fig. 1.

The firmware of the UUB FPGA is written in IEEE standard synthesizable Verilog. Xilinx Vivado [**?**] is used as a development environment in which standard modules, such as access to different memories and other interfaces, can be found.

The logic functions encoded in the firmware include ADC reading, trigger generation, and interfaces with the LED flasher, GPS receiver, and memories.

The Xilinx PetaLinux operating system [**?**] runs on the ARM processor. The data acquisition software (DAQ) installed on Petalinux implements high-level functions such as data management and communication with the radio transmitter.

3.3 Triggering and buffering

- single-bin trigger (SB),
- time-over-threshold trigger (ToT),
- time-over-threshold trigger deconvolved (ToTd) trigger,
- multiplicity of positive steps (MoPS) trigger.

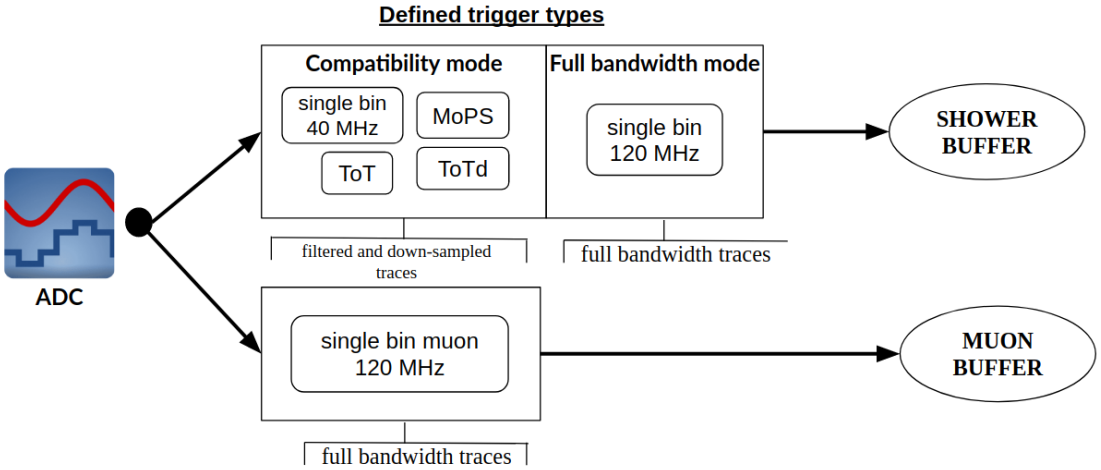

Figure 2: The structure of the memory buffers. The memory of the FPGA is divided into two channels, one used for event acquisition and the other for the calculation of calibration histograms, on each of these two channels different types of triggers are defined.

The larger conceptual structure of the firmware was mostly ported from the UB to UUB. We will describe this structure here, addressing differences between the UB and UUB where they exist. It must be specified that for historical reasons we respectively refer to the component of the UB and UUB that manages the logical properties of the station as the PLD and FPGA, and the programming of these two is generically referred to as *firmware*.

The firmware performs the readout of the ADC channels. There are six (ten) channels for the UB (UUB). The firmware has two acquisition modes, one used for buffering of so-called "shower" events and one used for buffering so-called "muon" events that are used to build calibration histograms. *Shower events* are events which satisfy a T1-level trigger. *Muon events* are events which satisfy a muon SB threshold trigger running on the three WCD PMTs. The memory related to shower events is dubbed as the *shower memory*, while muon events are stored in the *muon memory*. Both of these memories consist of two (four) buffers for UB (UUB). A schematic representation of the various triggers that initiate filling of the shower and muon memories is shown in Fig. 2.

It is important to say that only the high-gain ADC traces are fed to the trigger module for analysis. Low-gain traces do not participate in the trigger but are transmitted to CDAS with the other event data.

To reproduce UB triggers in the UUB as best possible, the full-bandwidth ADC trace t_i of a WCD PMT is first digitally filtered with a n_{fir}th-order finite-impulse response (FIR) filter (discrete convolution) so that the filtered trace f_i is expressed as a weighted sum of the previous values of the trace,

$$f_i = \frac{1}{B} \sum_{j=0}^{n_{\text{fir}}} b_j \, t_{i-j} \tag{1}$$

where the weights b_i are symmetric around the middle,

$$b_i = \{5, 0, 12, 22, 0, -61, -96, 0, 256, 551, 681, 551, 256, 0, -96, -61, 0, 22, 12, 0, 5\} \tag{2}$$

and thus $n_{\text{fir}} = 20$. While B should normally be set to $B = \sum_i b_i = 2059$, the integer division with this specific value of B is for performance reasons instead simplified into an 11-bit right shift, i.e. effectively dividing with $B = 2^{11} = 2048$. The filtered trace f_i is downsampled from 120 MHz to 40 MHz into the final decimated-filtered trace d_i by keeping every third ADC sample, $d_i = f_{3i+p}$, where a fixed phase $p \in \{0, 1, 2\}$ is randomly selected at the initialization of the FPGA.

These triggers are referred to as *compatibility triggers* in the UUB and are only used to fill the shower memory. They are the:

- single-bin trigger (SB),
- time-over-threshold trigger (ToT),
- time-over-threshold trigger deconvolved (ToTd) trigger,
- multiplicity of positive steps (MoPS) trigger.

To consider the introduction of SSD, a trigger similar to the SB trigger but with the introduction of the high-gain signal of SSD dubbed "full-bandwidth single-bin trigger" (FBW SB trigger) has also been implemented. This trigger has a similar structure as the compatibility SB trigger with the difference that it is defined on FBW traces. In addition, this trigger is similar in operation to muon trigger but with a separate hardware dedicated.

Currently, compatibility triggers are used on upgraded tanks in the field to acquire the event with the SSD in slave mode.

The FBW SB trigger is used to calculate the event rate used to set the high voltage of the SSD. While for the high voltage setting in PMTs, the event rate calculation is aided by scaler registers of the FPGA that automatically count events once trigger options are set. In UB only the scalers were used in the absence of the SSD, which have a largely unchanged structure in the FPGA of UUB.

In the definition of histograms the muon trigger is used. In this situation, the SSD is acquired in slave mode and the acquisition takes place when at least one of the three PMTs in the tank meets the trigger conditions.

In the online rate estimation of the Q_{VEM} and I_{VEM}, the SB trigger is used to calculate the value of I_{rate} and Q_{rate} in the DAQ. Here too the structure has remained almost unchanged in the transition from UB to UUB, in particular in the latter the filtered and downsampled tracks and the compatibility SB are used.

3.4 Data acquisition

Data acquisition of the two channels is performed in parallel by two processes in the DAQ:

- `muonfill` (fills buffers with the muon information),
- `FeShwrRead` (short for "front-end shower read").

These are the two processes that interact directly with the FPGA to acquire data from the memory buffers. The definition and filling of histograms is done by `muonfill` and its sub-processes, while `FeShwrRead` is used to acquire physics events.

Add explicit statement that what's sent to monitoring comes from the last 61 s, not five minute average!

When a T1 trigger occurs, the traces[1] are written into one of the four buffers. A signal is sent from the trigger module to the *time tagging module*, which determines the timestamp of the end of the traces. The trigger module tells the time tagging module which of the four buffers is filled and if there is at least one empty buffer available for other events or if all four buffers are full. The time tagging module also measures a "dead time," which corresponds to the time period during which all buffers were full and triggering was inhibited.

The trigger module also communicates with the CPU. If one of the four buffers is filled and the CPU is not reading any buffers, an interrupt is sent to the CPU that initiates the read performed by the `FeShwrRead` process.

The acquired data is transferred to a buffer in the shared memory called *fastbuffer* where traces and timing information are saved and accessible to all DAQ processes.

[1] The six traces of the three WCD PMTs in UB and the ten traces in the UUB.

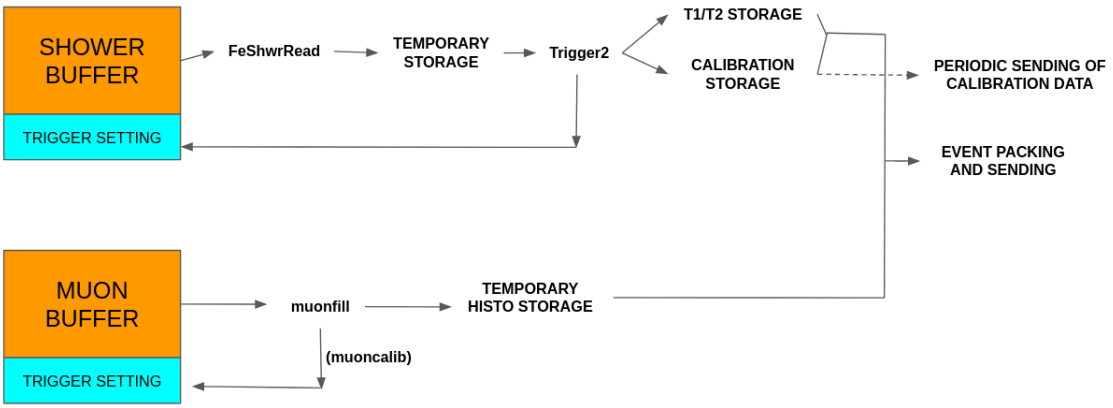

Figure 3: Schematic flow of the calibration data. Sent to CDAS at regular intervals (monitoring) or upon a T3 request for event data. All storage (in color x) is shared between the processes. TODO: remove "SENT TO CDAS", add T1 and T2 buffers filled by Trigger2, change "TEMPORARY BUFFER" to "TEMPORARY STORAGE", change "CALIBRATION BUFFER" to "CALIBRATION STORAGE", change "TEMPORARY HISTO BUFFER" to "TEMPORARY HISTOGRAM STORAGE", change evtsvt to CalMonSvr.

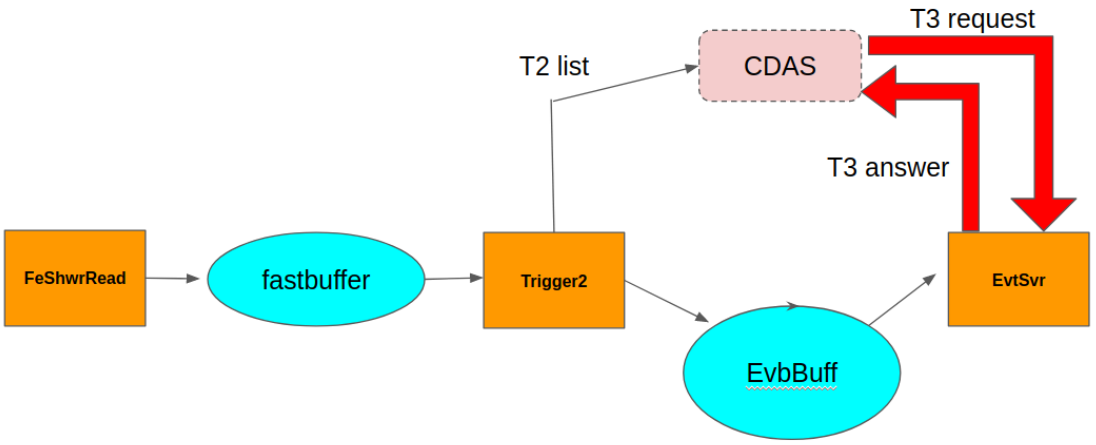

Figure 4: Foo

The events in the fastbuffer are processed by `Trigger2`, which makes a copy of them into the so-called T1 list (EvbBuff of 3000 events), and uses the data to calculate I_{rate} and Q_{rate}, and to generate a list of the T2 events. The microseconds of the T2 events are sent to CDAS in the T2 messages, which CDAS aggregates in 1 s windows to determine whether T3 criteria have been met. When a T3 criterion is met, CDAS emits a T3 request. Upon receiving this request, the `evtsvr` process in the local station scans the T1 list for events inside the requested microsecond time window[2]. sends to CDAS the calibration information and histograms with the other event data. In addition, it is important to note that calibration values are sent to CDAS periodically every 61s even if there are no T3 requests. A schematic representation of this process is in figure 4.

In parallel with the acquisition of `FeShwrRead` the calculation of histograms takes place. In the

[2]Window is zero for T2 events while T1-only events are searched for with a tolerance of 30 μs.

case of muon memory, an interrupt is released when one of the four buffers is full. The process is complementary to that described for shower memory. A substantial difference between these two memories is that a buffer in muon memory contains many muon events. The histograms are computed by a `muonfill` sub-process called `muoncalib` and are placed in a buffer waiting to be sent to CDAS by `evtsvr`.

4 Calibration procedures

4.1 Setting the high voltage

For the UB, a target of 50 ADC counts for the I_{VEM} was chosen as this results in the desired dynamic range of the acquisition system. The hump of omnidirectional muons lies at $I_{\mathrm{VEM}}/0.87 \approx 60$ ADC. In the rate spectrum, the omnidirectional muons may be observed as a small hump atop the all particle spectrum. The HV setting is adjusted until the omnidirectional muon hump in the rate spectrum lies at ~60 ADC for the UB. Given the rate spectrum, this corresponds to a rate of ~100 Hz at a threshold of ~150 ADC above baseline.

For the UUB the target for I_{VEM} is 150 ADC, the 100 Hz threshold is 500 ADC.

As soon as a tank is turned on, the first part of the calibration is started which consists of matching the gains of the PMTs to obtain a uniform response of the detector. For this purpose the spectrum of atmospheric muons at low energies is used as a tool for common reference since it is quite uniform throughout the array.

PMT matching is based on the fact that the trigger rate as a function of increasing threshold decreases monotonically.

The fundamental concept that is used in the matching process is that changing the gain of the PMTs stretches and scales the spectrum of the trigger frequency. Therefore, we can define a required single rate at a given threshold, and adjust the high voltage of each PMT to match that rate.

In the UB, the 100 Hz target was chosen for the calibration method as the optimal working point for the hardware and software at the time. The software function that handled the PMT matching in UB was `GoCalib`, which was with minor changes reintroduced in the UUB with exactly the same reference rates.

The rate calculation is done individually on all PMTs (in UUB also including the SSD). For the WCD PMTs, the scaler registers of the FPGA are used to count the triggers. However, since an FPGA scaler register was not implemented for the SSD, the software is counting the number of FBW single-bin triggers instead. A threshold of 500 ADC (150 ADC for UB) counts was chosen for the PMTs, and 50 ADC counts for the SSD (to be corrected).

Essentially, the `GoCalib` algorithm is performing these procedures:

1. The baseline of each PMT is determined as an average of values of a randomly triggered high-gain trace.
2. The HVs for WCD and SSD PMTs are simultaneously set to their initial values, and a HV step is set to a value that would generate a change in the gain of about 30%.
3. The trigger rate in all PMTs is estimated on a 2 s interval.
4. If the rate with the positive step is too high or the rate with the negative step is too low, the sign of the step is reversed and the step is divided by 3. This is repeated until the desired rate is reached.
5. A final rate check is performed 10 times by calculating the rates on 4 s intervals. If this check fails, the whole process is repeated starting at the second procedure of this algorithm.

The algorithm makes sure that the HVs of the PMTs are not set to values exceeding 1600 V (1200 V) for the WCD (SSD) and are not set to voltages below 98 V (73 V).

What has to happen to run GoCalib again? What are the tolerances?

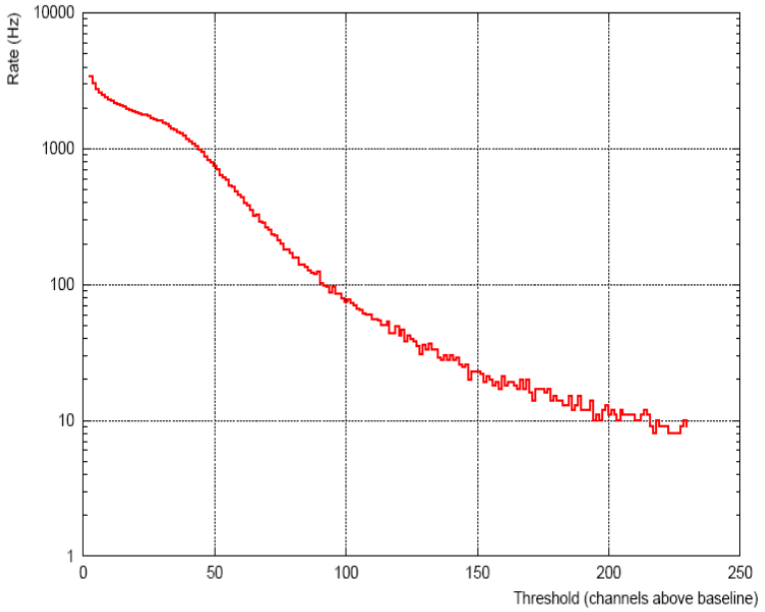

Figure 5: Trigger rate as a function of threshold for three-fold coincidence of the 3 PMTs. Around 50 ADC counts an inflection point due to through-going muons can be seen.

Table 3: The conversion factors between I_{rate} and the 70 Hz, SB T1, ToT, and SB T2 thresholds are given as functions of the number of working PMTs.

working PMTs	k_{70}	k_1	k_{ToT}	k_2
3	2.5	1.75	0.2	3.2
2	2.6	2.00	0.2	3.6
1	3.3	2.85	0.2	5.0

4.2 Rate-based estimation

All physics triggers are defined in terms of I_{VEM}. The approximation to I_{VEM} obtained here will be denoted with I_{rate}. With the current estimate of $I^{(i)}_{\text{rate}}$ for each PMT i, a procedure that sustains a 70 Hz trigger rate for SB (FBW???) triggers with a threshold of $t^{(i)}_{70} = b^{(i)} + k_{70}\, I^{(i)}_{\text{rate}}$ is performed. This is done for each PMT individually with corresponding values of baselines $b^{(i)}$. The conversion factor k_{70} depends on the number of working PMTs (see Table 3).

These estimates $I^{(i)}_{\text{rate}}$ are then used for a 3-fold SB trigger T1 where PMT thresholds are set to $t^{(i)}_{100} = b^{(i)} + k_1\, I^{(i)}_{\text{rate}}$. The rate of this 3-fold trigger should be very close to 100 Hz. If the number of working PMTs is not 3, the multiplicity of the T1 trigger is changed accordingly and a different conversion factor k_1 is used (see Table 3).

The target rate of 70 Hz and 100 Hz were chosen considering the optimal operation ranges of the electronics. The respective conversion factors k_{70} and k_1 were measured for different numbers of operating PMTs given these choices of rates [**?**].

Essentially the algorithm that continuously estimates $I^{(i)}_{\text{rate}}$ performs the following. Upon startup, $I^{(i)}_{\text{rate}}$ is estimated from the scaler rate after which the following steps are repeatedly performed indefinitely:

1. The T70 threshold is set to $t^{(i)}_{70} = k_1\, I^{(i)}_{\text{rate}}$ for a 3-fold coincidence of the PMTs;

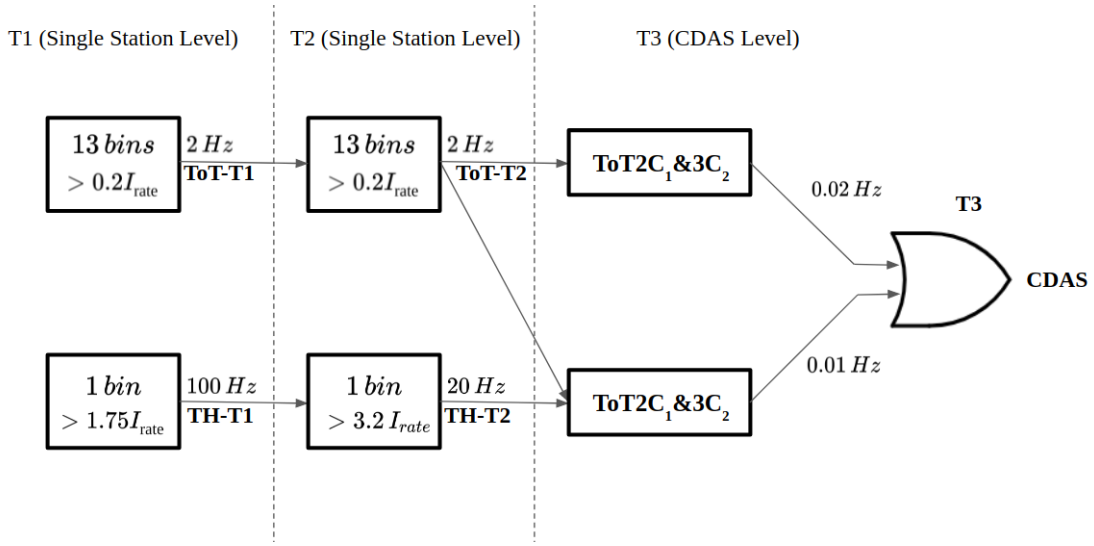

Figure 6: Schematic representation of the physics triggers. Taken from Ref. [2]. TODO: remake graphics with inkscape and our nomenclature.

2. The T70 rate is calculated from 61 s of data by counting how many T70 events for each PMT passed the threshold t_{70}.

3. If the rate for a given PMT i is greater than 70 Hz, the estimate $I^{(i)}_{\text{rate}}$ is increased, or vice versa;

4. The T1 rate, which is nominally 100 Hz, is calculated and sent to CDAS for monitoring.

In this way, even if initial estimates of $I^{(i)}_{\text{rate}}$ are far from $I^{(i)}_{\text{VEM}}$, they will converge.

The first level (T1) triggers (Fig. 6) are defined by the local station and their thresholds are determined and set by the `Trigger2` process. The T1-level triggers are the Single-Bin (SB) and Time-over-Threshold (ToT) triggers. The former is sometimes also called the T1-threshold (TH) trigger [2]. The ToT trigger has a threshold of $t^{(i)}_{\text{ToT}} = b^{(i)} + k_{\text{ToT}}\, I^{(i)}_{\text{rate}}$ and is directly promoted to the T2 level, whereas for a SB T1 trigger to be promoted, the signal must pass the higher SB T2 threshold $t^{(i)}_2 = b^{(i)} + k_2\, I^{(i)}_{\text{rate}}$.

The `Trigger2` process also produces the list of T2 events that are sent to CDAS each second. While the nominal T1 rate is 100 Hz, the rate of T2 triggers is nominally 20 Hz. More details can be found in Ref. [3].

The `Trigger2` process also computes an estimate of Q_{VEM} called Q_{rate}. This estimate is the average of integrated signals for a subset of T1 events, where the peak of the traces lies between t_1 and $t_1 + \Delta$ where $\Delta = 1$ (50) adc for UB (UUB). The integral is determined by the PLD (FPGA) as a sum over 20 (100) bins of the UB (UUB) traces, staring from the first bin that crossed the t_1 threshold, and the averaging of these values are done in the `Trigger2` subroutine defined in `xbtrig`. This value of Q_{rate} is sent to CDAS with the event data and is usually referred to as *online charge*.

4.3 Histogram-based estimation

For an independent offline check of I_{rate} and Q_{rate}, histograms of the peak, charge, baseline, and shape for events satisfying the muon trigger are filled by the `muonfill` process in time blocks of 61 s. A dedicated *muon trigger* initiates the writing of traces T of all PMTs with lengths $n_T = 20$ (69) bins for the UB (UUB) into the muon buffer. This muon trigger is issued when for at least one of the WCD-only PMTs, the SB trigger condition is satisfied where the thresholds are $t^{(i)}_{\mu} = b^{(i)}_{\text{soft}} + 30$ adc

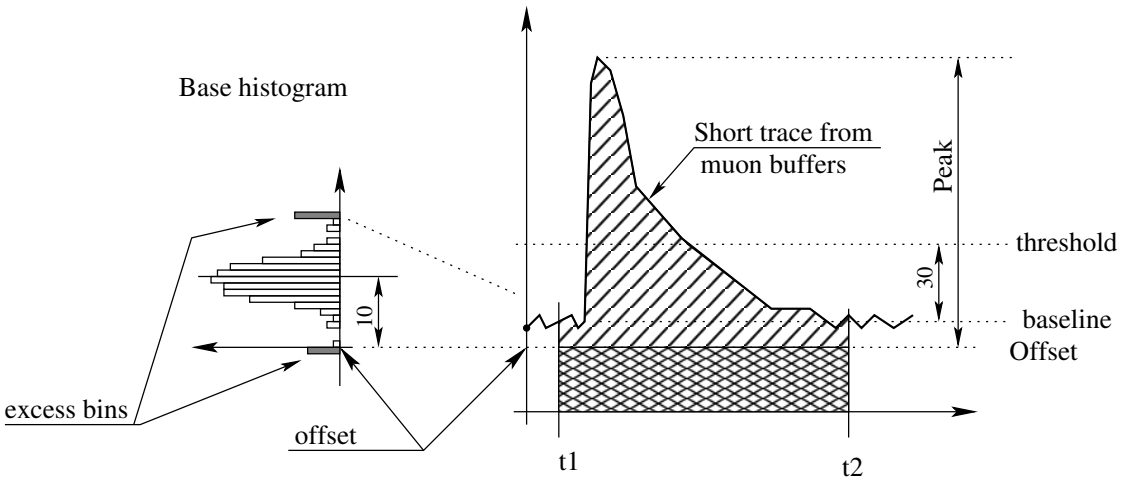

Figure 7: Traces saved by the muon trigger. Note that the specific values shown in the plot are valid UB only.

values and where the baselines $b_{\text{soft}}^{(i)}$ are estimated as an average of the first bins of the gathered traces in the previous 61 s block. For each muon trigger, traces for all PMTs are read out. This includes the SSD PMT, if present, even though it does not participate in the trigger. The muon memory is organized in three buffers that are filled and processed in a circular manner. A muon trigger results in the storage of the following information: timestamp, trigger bits, and $n_T = 20$ (69) bins[3] of the trace, where trigger latch bin is the 2nd (20th) for UB (UUB). When a muon buffer fills up to ?? (115) entries, an interrupt is issued for the `muonfill` process to read it out, but only if the CPU is not servicing any other interrupts. Acquisition continues by filling the next buffer in the ring.

An example of a trace from the muon memory is shown in Fig. 7. Among other things, the figure also shows the position of the threshold for the muon trigger, which is $b_{\text{soft}} + 30$ adc.

The following description of how histograms are generated by the DAQ refers for UUB only to calibration versions greater than 262.

The "peak" p of a trace T is defined as the maximum ADC value, where the an offset O has been subtracted, i.e.

$$p = \max_i (T_i - O). \tag{3}$$

In the UB, the value p is directly histogrammed in the *peak histogram* h^{peak} for all the traces in the current 61 s block. For the UUB, p/d is histogrammed instead, where $d = 4$ for WCD and $d = 2$ for SSD. The histogram h^{peak} is set up with bin widths equal to 1 for $p < 1500$ (100) ??? and otherwise equal to 3 (4) for UB (UUB). The offset O for the current 61 s block is set relative to the baseline estimate of the previous 61 s block, i.e. $O = b_{\text{soft}} - 10$ ($-$??) for UB (UUB). Therefore, during an offline analysis of the peak histogram the obtained mode (a.k.a. VEM-peak) of the distribution has to be corrected by $b - O$, where b is a better estimate of the baseline (usually obtained from the baseline histogram discussed below) for this particular 61 s block.

The "charge" q of a trace T is the integral of the portion of the trace where the offset O is subtracted from each bin,

$$q = \sum_{i=t_1}^{t_2} (T_i - O), \tag{4}$$

where for the UB WCD the values of parameters are $t_1 = 0$ and $t_2 = 19$, and for UUB the corresponding values are $t_1 = 0$ (10) and $t_2 = 49$ (29) for WCD (SSD) PMTs. The value q is histogrammed in the *charge histogram* h^{charge} for all the traces in the current 61 s block. The bin

[3] For UB running with calibration version 13 number of bins was $n_T = 19$.

widths of the histogram are equal to 1 (8) for $q < 400$ and otherwise equal to 4 (32) for UB (UUB). When analyzing the charge histogram in an offline procedure, note that the mode of the distribution (a.k.a. VEM-charge) has to be corrected by $(t_2 - t_1 + 1)(b - O)$, where, again, b is a better estimate of the baseline for this 61 s block.

The *shape histogram* h^{shape} is simply filled with all N_{61} traces T^j in a 61 s block stacked so that individual bins of the shape histogram are

$$h_i^{\text{shape}} = \sum_j^{N_{61}} T_i^j - O, \tag{5}$$

where T_i^j is the ith bin of trace j.

The *baseline histogram* h^{base} is filled with the suitably shifted first entry of each muon trace, i.e. with values $T_0^j - O$.

As many SSD traces do not have signals[4], the SSD trace T^j is only considered for histogramming when its maximum lies between the time bins 15 and 21. is this meant generally for all histograms? What happens at the initialization?

4.4 Dynode-to-anode and high-gain-to-low-gain ratio

In the UB, the anode channel of each PMT is fed into one input (low-gain), while the signal from the last dynode is amplified on the PMT base before being fed into a second input (high-gain). The ratio between the effective gains of these two inputs is called the dynode-to-anode ratio (D/A). This value is calculated online by the DAQ software using a fit procedure that is described in Ref. [4]. The calculation is performed in the same subroutine of `Trigger2` that performs the rate-based estimation of VEM.

The signals used come from the shower memory of the PLD of UB. A selection is made of the unsaturated signals that have exceeded a threshold of 500 adc counts.

The method consists in parameterizing the anode as a piecewise function,

$$f_{\text{A}}(x) = \frac{1}{R}((1-\epsilon) f_{\text{D}}(x) + \epsilon\, f_{\text{D}}(x+1)), \tag{6}$$

where R is the D/A ratio, ϵ is the fractional bin offset of the dynode, and $f_{\text{D}}(x)$ is a piecewise-defined dynode. Both dynode and anode are functions of bin x.

For the sake of simplicity, the function can be rewritten by decoupling the variables,

$$f_{\text{A}} = \bar{R}\, f_{\text{D}}(x) + C_f\, f_{\text{D}}(x+1), \text{ where } \bar{R} = \frac{1}{R} - C_f \text{ and } C_f = \frac{\epsilon}{R}. \tag{7}$$

The fit procedure implemented in the DAQ code of UB uses the OLS method to calculate $\bar{R}$ and C_f. Thus the D/A ratio given as R in Eq. (7) can be calculated from $\bar{R}$ via Eq. (7).

An example of the distribution of values coming from this fit for a subsample of UB-equipped stations is in **??**.

The currently used amplified dynode signal, however, is too noisy for the increased dynamic range in UUB. Therefore in UUB the high- and low-gain signals are both derived from the anode signal using two amplifiers in parallel with different gains (figure). For this reason, in UUB it is more correct to call the effective gain ratio between the two channels as a high-gain-to-low-gain ratio (HG/LG). The method used to calculate this value in UUB is not very different from UB. In fact, it is determined in the same subroutine of `Trigger2` with an OLS fit procedure.

The signals used come from the shower memory of the FPGA of UUB. A selection is made of the unsaturated signals that have exceeded a threshold of 1900 adc counts. The integration

[4] This is due, in part, to the larger area of the WCD. A particle inducing a signal in the WCD is not guaranteed to have passed through the SSD.

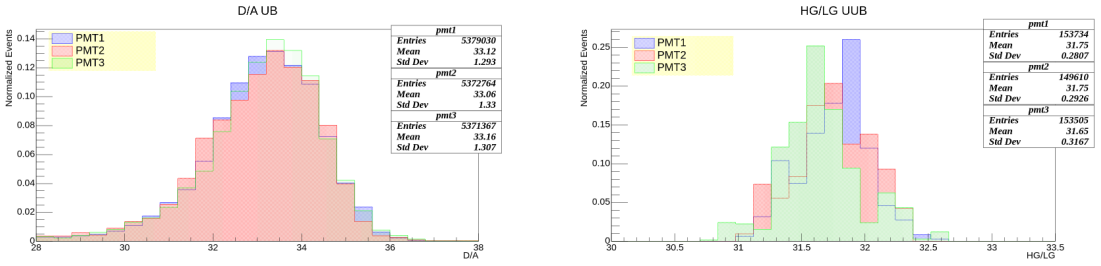

Figure 8: Title.

window is 70 bins (560 ns) and starts from the 650th bin, which is the trigger latch bin of a FBW trace.

The function with which the high gain is parameterized is

$$f_{\mathrm{H}}(x) = R\, f_{\mathrm{D}}(x) + b, \tag{8}$$

where R is HG/LG ratio and b is the bin offset.

Fitting this function directly results in a large correlation between the values of R and b. To avoid this problem, the calculation is done in two steps. First the average of high gain and low gain in the 70 bins window is calculated,

$$\bar{f}_{\mathrm{H}} = \frac{1}{70}\sum_{x=650}^{720} f_{\mathrm{H}}(x) \quad \text{and} \quad \bar{f}_{\mathrm{L}} = \frac{1}{70}\sum_{x=650}^{720} f_{\mathrm{L}}(x) \tag{9}$$

The OLS method is then applied to this function,

$$\tilde{f}_{\mathrm{H}}(x) = R\,\tilde{f}_{\mathrm{L}}(x) + b \quad \text{where } \tilde{f}_{\mathrm{H}}(x) = f_{\mathrm{H}}(x) - \bar{f}_{\mathrm{H}} \text{ and } \tilde{f}_{\mathrm{L}}(x) = f_{\mathrm{L}}(x) - \bar{f}_{\mathrm{L}}. \tag{10}$$

The distribution of high-gain-to-low-gain (HG/LG) ratios calculated by this method is shown in **??**. Clearly, the distribution has a smaller spread than that of UB since UUB does not suffer from the noise problems that the PMTs base caused in the dynode.

5 Event building

add schematics of event building

5.1 Packaging and sending from LS

5.2 CDAS event builder

unpacking of data, making of `sd_*.root` files.

5.3 Merging

In CC Lyon. making of `sdm_*.root` files.

5.4 Monitoring

but include description on how monitoring gets the data as well

6 Summary and outlook

References

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[4] P.S. Allison, X. Bertou, and C. Grunfeld, *Pulse-shape Agnostic Methods of Measuring the Dynode-Anode Ratio*, GAP-2004-033.