Lab Assignment #0

This lab is a tutorial lab. You don't have to design anything in this lab, just go through the tutorials and perform them on the lab computers individually. In this course, in almost all the labs we will be doing the following steps:

Step 1: Writing Verilog code of the circuit we want to implement
Step 2: Simulating the Verilog code using a simulator (ModelSim) to check if the intended functionality has been achieved
Step 3: Synthesizing the Verilog code using a tool from Xilinx called Vivado so that it can be programmed onto an FPGA
Step 4: Programming the FPGA (a Artix 7 series FPGA from Xilinx) on the lab board (called Basys3 board), also by using Vivado
Step 5: Applying inputs to and observing outputs from our circuit using the peripherals (like switches, buttons, LEDs, etc) on the Basys3 board

To be able to do all this, we need to learn how to use ModelSim and Vivado, and we also need to understand the capabilities of the Basys3 board and how can we program the Xilinx Artix 7 FPGA on it using Vivado. The following activities will help you go through all the steps so you can learn and use the concepts in the upcoming labs.

Activity 1: ModelSim tutorial

Mentor Graphic's Modelsim tool will be used to perform the functional simulation of our Verilog code for the course. This software is available on the lab computers in ECJ 1.222. Modelsim is also available as a free download with Xilinx's Webpack software so you can install it on your own computer.

Go through the "**Modelsim Tutorial**" posted on Canvas under the lab documentation page. This tutorial goes through the basic steps in compiling and simulating within the Modelsim environment using a simple D-flipflop as an example.

Activity 2: Vivado tutorial

The Vivado tool is used to synthesize circuits and place & route them for a particular FPGA. Then, a BIT file needs to be generated which can be programmed onto the FPGA so that the FPGA now contains the circuit you designed. Go through the "**Vivado Tutorial**" posted on Canvas under the lab documentation page. You may also visit www.xilinx.com and browse the Artix-7 manuals for help.

Activity 3: Basys3 board tutorial

Read through the **Basys3 Reference Manual** on Canvas under the lab documentation page to understand the features and capabilities of the board to be used in all the labs.

Questions

You should be able to answer (almost all of) the following questions after going through these tutorials:

1. What is ModelSim? What is the role of the transcript window which appears on the bottom of the main ModelSim window?
2. What is a delta cycle in a Verilog simulator like ModelSim?
3. How do you create a do-file of commands entered in the transcript window in ModelSim?
4. Describe the roles and functionality of the following tools in the Vivado suite: Flow Navigator, RTL schematic viewer.
5. Is it possible to display two digits using the 7SEG LEDs at the same time on the Basys3 boards? Note there are only 7 pins corresponding to a single 7-segment digit.
6. If we want to use the push buttons on the board reliably, what should we do first to the incoming signal into the FPGA? How do we implement this in Verilog?

Submission Details

Submit a text/doc/pdf file containing the answers to the questions given above on Canvas. Name the file "your_last_name.extension". No checkout is required for this lab.