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EE 460M

Lab 0 Questions

1. Modelsim is an environment in which Verilog or VHDL can be written and simulated. The transcript window is used to assign variables to values at specified times throughout a simulation.
2. A delta cycle in ModelSim is a cycle that doesn’t take simulated time. It’s how the simulator simulates parallelism.
3. A do-file of commands can be created in a file of simulator commands saved with a “.do” extension. They can be executed by clicking on Tools, Execute Macro, then selecting the file.
4. The Flow Navigator is a panel that displays commonly used commands such as run simulation, run synthesis, run implementation, and generate bitstream that are greyed out until the necessary tasks are completed. The RTL schematic viewer allows the user to see of a representation of the design in terms of modules such as adders, multipliers, and registers.
5. Yes, there are four 7 segment LEDs.
6. The signals from the code must be mapped to the corresponding IO ports. This is done by uncommenting the appropriate lines in the xdc file and setting them to match the right buttons.