Joel Guo jg55475

Ted Mao ttm455

EE 460M Lab 3 Synthesis Report

#-----------------------------------------------------------

# Vivado v2014.4 (64-bit)

# SW Build 1071353 on Tue Nov 18 18:29:27 MST 2014

# IP Build 1070531 on Tue Nov 18 01:10:18 MST 2014

# Start of session at: Mon Oct 10 16:11:05 2016

# Process ID: 13608

# Log file: C:/Users/jg55475/lab3/lab3.runs/synth\_1/top.vds

# Journal file: C:/Users/jg55475/lab3/lab3.runs/synth\_1\vivado.jou

#-----------------------------------------------------------

source top.tcl

# set\_param gui.test TreeTableDev

# set\_param xicom.use\_bs\_reader 1

# debug::add\_scope template.lib 1

# set\_msg\_config -id {HDL 9-1061} -limit 100000

# set\_msg\_config -id {HDL 9-1654} -limit 100000

# create\_project -in\_memory -part xc7a35tcpg236-1

# set\_param project.compositeFile.enableAutoGeneration 0

# set\_param synth.vivado.isSynthRun true

# set\_property webtalk.parent\_dir C:/Users/jg55475/lab3/lab3.cache/wt [current\_project]

# set\_property parent.project\_path C:/Users/jg55475/lab3/lab3.xpr [current\_project]

# set\_property default\_lib xil\_defaultlib [current\_project]

# set\_property target\_language Verilog [current\_project]

# read\_verilog -library xil\_defaultlib {

# {//austin.utexas.edu/disk/engrstu/ece/jg55475/Desktop/EE 460M/Lab3/TrafficController.v}

# {//austin.utexas.edu/disk/engrstu/ece/jg55475/Desktop/EE 460M/Lab3/Divider.v}

# {//austin.utexas.edu/disk/engrstu/ece/jg55475/Desktop/EE 460M/Lab3/Top.v}

# }

# read\_xdc {{//austin.utexas.edu/disk/engrstu/ece/jg55475/Desktop/EE 460M/Lab3/Basys3\_Master.xdc}}

# set\_property used\_in\_implementation false [get\_files {{//austin.utexas.edu/disk/engrstu/ece/jg55475/Desktop/EE 460M/Lab3/Basys3\_Master.xdc}}]

# catch { write\_hwdef -file top.hwdef }

INFO: [Vivado\_Tcl 4-279] hardware handoff file cannot be generated as there is no block diagram instance in the design

# synth\_design -top top -part xc7a35tcpg236-1

Command: synth\_design -top top -part xc7a35tcpg236-1

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a35t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'

INFO: [Common 17-1223] The version limit for your license is '2015.03' and will expire in -559 days. A version limit expiration means that, although you may be able to continue to use the current version of tools or IP with this license, you will not be eligible for any updates or new releases.

---------------------------------------------------------------------------------

Starting RTL Elaboration : Time (s): cpu = 00:00:07 ; elapsed = 00:00:11 . Memory (MB): peak = 239.750 ; gain = 81.074

---------------------------------------------------------------------------------

INFO: [Synth 8-638] synthesizing module 'top' [//austin.utexas.edu/disk/engrstu/ece/jg55475/Desktop/EE 460M/Lab3/Top.v:1]

INFO: [Synth 8-638] synthesizing module 'Divider' [//austin.utexas.edu/disk/engrstu/ece/jg55475/Desktop/EE 460M/Lab3/Divider.v:1]

INFO: [Synth 8-256] done synthesizing module 'Divider' (1#1) [//austin.utexas.edu/disk/engrstu/ece/jg55475/Desktop/EE 460M/Lab3/Divider.v:1]

INFO: [Synth 8-638] synthesizing module 'trafficlight' [//austin.utexas.edu/disk/engrstu/ece/jg55475/Desktop/EE 460M/Lab3/TrafficController.v:1]

INFO: [Synth 8-256] done synthesizing module 'trafficlight' (2#1) [//austin.utexas.edu/disk/engrstu/ece/jg55475/Desktop/EE 460M/Lab3/TrafficController.v:1]

INFO: [Synth 8-256] done synthesizing module 'top' (3#1) [//austin.utexas.edu/disk/engrstu/ece/jg55475/Desktop/EE 460M/Lab3/Top.v:1]

---------------------------------------------------------------------------------

Finished RTL Elaboration : Time (s): cpu = 00:00:09 ; elapsed = 00:00:12 . Memory (MB): peak = 272.977 ; gain = 114.301

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

---------------------------------------------------------------------------------

Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:09 ; elapsed = 00:00:13 . Memory (MB): peak = 272.977 ; gain = 114.301

---------------------------------------------------------------------------------

Loading clock regions from C:/Xilinx/Vivado/2014.4/data\parts/xilinx/artix7/artix7/xc7a35t/ClockRegion.xml

Loading clock buffers from C:/Xilinx/Vivado/2014.4/data\parts/xilinx/artix7/artix7/xc7a35t/ClockBuffers.xml

Loading clock placement rules from C:/Xilinx/Vivado/2014.4/data/parts/xilinx/artix7/ClockPlacerRules.xml

Loading package pin functions from C:/Xilinx/Vivado/2014.4/data\parts/xilinx/artix7/PinFunctions.xml...

Loading package from C:/Xilinx/Vivado/2014.4/data\parts/xilinx/artix7/artix7/xc7a35t/cpg236/Package.xml

Loading io standards from C:/Xilinx/Vivado/2014.4/data\./parts/xilinx/artix7/IOStandards.xml

Loading device configuration modes from C:/Xilinx/Vivado/2014.4/data\parts/xilinx/artix7/ConfigModes.xml

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [//austin.utexas.edu/disk/engrstu/ece/jg55475/Desktop/EE 460M/Lab3/Basys3\_Master.xdc]

Finished Parsing XDC File [//austin.utexas.edu/disk/engrstu/ece/jg55475/Desktop/EE 460M/Lab3/Basys3\_Master.xdc]

Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.006 . Memory (MB): peak = 562.414 ; gain = 0.000

---------------------------------------------------------------------------------

Finished Constraint Validation : Time (s): cpu = 00:00:20 ; elapsed = 00:00:25 . Memory (MB): peak = 562.414 ; gain = 403.738

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Loading Part and Timing Information

---------------------------------------------------------------------------------

Loading part: xc7a35tcpg236-1

---------------------------------------------------------------------------------

Finished Loading Part and Timing Information : Time (s): cpu = 00:00:20 ; elapsed = 00:00:25 . Memory (MB): peak = 562.414 ; gain = 403.738

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Applying 'set\_property' XDC Constraints

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:20 ; elapsed = 00:00:25 . Memory (MB): peak = 562.414 ; gain = 403.738

---------------------------------------------------------------------------------

ROM "slowClk" won't be mapped to RAM because address size (28) is larger than maximum supported(18)

ROM "State" won't be mapped to RAM because it is too sparse.

---------------------------------------------------------------------------------

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:20 ; elapsed = 00:00:25 . Memory (MB): peak = 562.414 ; gain = 403.738

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------------

Start RTL Component Statistics

---------------------------------------------------------------------------------

Detailed RTL Component Info :

+---Adders :

2 Input 28 Bit Adders := 1

2 Input 6 Bit Adders := 1

+---Registers :

28 Bit Registers := 1

6 Bit Registers := 1

1 Bit Registers := 1

+---Muxes :

2 Input 28 Bit Muxes := 1

10 Input 6 Bit Muxes := 1

2 Input 6 Bit Muxes := 2

2 Input 1 Bit Muxes := 1

10 Input 1 Bit Muxes := 8

---------------------------------------------------------------------------------

Finished RTL Component Statistics

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start RTL Hierarchical Component Statistics

---------------------------------------------------------------------------------

Hierarchical RTL Component report

Module top

Detailed RTL Component Info :

Module Divider

Detailed RTL Component Info :

+---Adders :

2 Input 28 Bit Adders := 1

+---Registers :

28 Bit Registers := 1

1 Bit Registers := 1

+---Muxes :

2 Input 28 Bit Muxes := 1

2 Input 1 Bit Muxes := 1

Module trafficlight

Detailed RTL Component Info :

+---Adders :

2 Input 6 Bit Adders := 1

+---Registers :

6 Bit Registers := 1

+---Muxes :

10 Input 6 Bit Muxes := 1

2 Input 6 Bit Muxes := 2

10 Input 1 Bit Muxes := 8

---------------------------------------------------------------------------------

Finished RTL Hierarchical Component Statistics

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Part Resource Summary

---------------------------------------------------------------------------------

Part Resources:

DSPs: 120 (col length:60)

BRAMs: 150 (col length: RAMB18 60 RAMB36 30)

---------------------------------------------------------------------------------

Finished Part Resource Summary

---------------------------------------------------------------------------------

Start Parallel Synthesis Optimization : Time (s): cpu = 00:00:21 ; elapsed = 00:00:26 . Memory (MB): peak = 562.414 ; gain = 403.738

---------------------------------------------------------------------------------

Start Cross Boundary Optimization

---------------------------------------------------------------------------------

ROM "slow/slowClk" won't be mapped to RAM because address size (28) is larger than maximum supported(18)

---------------------------------------------------------------------------------

Finished Cross Boundary Optimization : Time (s): cpu = 00:00:21 ; elapsed = 00:00:26 . Memory (MB): peak = 562.414 ; gain = 403.738

---------------------------------------------------------------------------------

Finished Parallel Reinference : Time (s): cpu = 00:00:21 ; elapsed = 00:00:26 . Memory (MB): peak = 562.414 ; gain = 403.738

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------------

Start RAM, DSP and Shift Register Reporting

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished RAM, DSP and Shift Register Reporting

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Area Optimization

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Area Optimization : Time (s): cpu = 00:00:21 ; elapsed = 00:00:26 . Memory (MB): peak = 562.414 ; gain = 403.738

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Area Optimization : Time (s): cpu = 00:00:21 ; elapsed = 00:00:26 . Memory (MB): peak = 562.414 ; gain = 403.738

---------------------------------------------------------------------------------

Finished Parallel Area Optimization : Time (s): cpu = 00:00:21 ; elapsed = 00:00:26 . Memory (MB): peak = 562.414 ; gain = 403.738

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

Finished Parallel Synthesis Optimization : Time (s): cpu = 00:00:21 ; elapsed = 00:00:26 . Memory (MB): peak = 562.414 ; gain = 403.738

---------------------------------------------------------------------------------

Start Timing Optimization

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Applying XDC Timing Constraints

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:39 ; elapsed = 00:00:44 . Memory (MB): peak = 562.414 ; gain = 403.738

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Timing Optimization : Time (s): cpu = 00:00:39 ; elapsed = 00:00:44 . Memory (MB): peak = 562.414 ; gain = 403.738

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------------

Start Technology Mapping

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Technology Mapping : Time (s): cpu = 00:00:39 ; elapsed = 00:00:44 . Memory (MB): peak = 562.414 ; gain = 403.738

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------------

Start IO Insertion

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Flattening Before IO Insertion

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Flattening Before IO Insertion

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Final Netlist Cleanup

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Final Netlist Cleanup

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished IO Insertion : Time (s): cpu = 00:00:40 ; elapsed = 00:00:45 . Memory (MB): peak = 562.414 ; gain = 403.738

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

---------------------------------------------------------------------------------

Start Renaming Generated Instances

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Renaming Generated Instances : Time (s): cpu = 00:00:40 ; elapsed = 00:00:45 . Memory (MB): peak = 562.414 ; gain = 403.738

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------------

Start Rebuilding User Hierarchy

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:40 ; elapsed = 00:00:45 . Memory (MB): peak = 562.414 ; gain = 403.738

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start RAM, DSP and Shift Register Reporting

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished RAM, DSP and Shift Register Reporting

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Writing Synthesis Report

---------------------------------------------------------------------------------

Report BlackBoxes:

+-+--------------+----------+

| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-------+------+

| |Cell |Count |

+------+-------+------+

|1 |BUFG | 1|

|2 |CARRY4 | 7|

|3 |LUT1 | 28|

|4 |LUT2 | 3|

|5 |LUT3 | 4|

|6 |LUT4 | 4|

|7 |LUT5 | 5|

|8 |LUT6 | 8|

|9 |FDRE | 35|

|10 |IBUF | 2|

|11 |OBUF | 8|

+------+-------+------+

Report Instance Areas:

+------+-------------+-------------+------+

| |Instance |Module |Cells |

+------+-------------+-------------+------+

|1 |top | | 105|

|2 | controller |trafficlight | 23|

|3 | slow |Divider | 71|

+------+-------------+-------------+------+

---------------------------------------------------------------------------------

Finished Writing Synthesis Report : Time (s): cpu = 00:00:40 ; elapsed = 00:00:45 . Memory (MB): peak = 562.414 ; gain = 403.738

---------------------------------------------------------------------------------

Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:32 . Memory (MB): peak = 562.414 ; gain = 84.184

Synthesis Optimization Complete : Time (s): cpu = 00:00:40 ; elapsed = 00:00:45 . Memory (MB): peak = 562.414 ; gain = 403.738

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 9 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-140] Inserted 0 IBUFs to IO ports without IO buffers.

INFO: [Opt 31-141] Inserted 0 OBUFs to IO ports without IO buffers.

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis

19 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:39 ; elapsed = 00:00:42 . Memory (MB): peak = 562.414 ; gain = 376.742

# write\_checkpoint -noxdef top.dcp

# catch { report\_utilization -file top\_utilization\_synth.rpt -pb top\_utilization\_synth.pb }

report\_utilization: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.158 . Memory (MB): peak = 562.414 ; gain = 0.000

INFO: [Common 17-206] Exiting Vivado at Mon Oct 10 16:11:53 2016...