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EE 460M Lab 3 Timing Summary Report

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| Tool Version : Vivado v.2014.4 (win64) Build 1071353 Tue Nov 18 18:29:27 MST 2014

| Date : Mon Oct 10 16:13:52 2016

| Host : ECJ1-222-19 running 64-bit Service Pack 1 (build 7601)

| Command : report\_timing\_summary -warn\_on\_violation -max\_paths 10 -file top\_timing\_summary\_routed.rpt -rpx top\_timing\_summary\_routed.rpx

| Design : top

| Device : 7a35t-cpg236

| Speed File : -1 PRODUCTION 1.14 2014-09-11

| Temperature Grade : C

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Timing Summary Report

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| Timer Settings

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Enable Multi Corner Analysis : Yes

Enable Pessimism Removal : Yes

Pessimism Removal Resolution : Nearest Common Node

Enable Input Delay Default Clock : No

Enable Preset / Clear Arcs : No

Disable Flight Delays : No

Corner Analyze Analyze

Name Max Paths Min Paths

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Slow Yes Yes

Fast Yes Yes

check\_timing report

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8. checking generated\_clocks

9. checking loops

10. checking partial\_input\_delay

11. checking partial\_output\_delay

12. checking unexpandable\_clocks

13. checking latch\_loops

1. checking no\_clock

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There are 6 register/latch pins with no clock driven by root clock pin: slow/slowClk\_reg/C (HIGH)

2. checking constant\_clock

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There are 0 register/latch pins with constant\_clock.

3. checking pulse\_width\_clock

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There are 0 register/latch pins which need pulse\_width check

4. checking unconstrained\_internal\_endpoints

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There are 12 pins that are not constrained for maximum delay. (HIGH)

There are 0 pins that are not constrained for maximum delay due to constant clock.

5. checking no\_input\_delay

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There is 1 input port with no input delay specified. (HIGH)

There are 0 input ports with no input delay but user has a false path constraint.

6. checking no\_output\_delay

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There are 8 ports with no output delay specified. (HIGH)

There are 0 ports with no output delay but user has a false path constraint

There are 0 ports with no output delay but with a timing clock defined on it or propagating through it

7. checking multiple\_clock

--------------------------

There are 0 register/latch pins with multiple clocks.

8. checking generated\_clocks

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There are 0 generated clocks that are not connected to a clock source.

9. checking loops

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There are 0 combinational loops in the design.

10. checking partial\_input\_delay

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There are 0 input ports with partial input delay specified.

11. checking partial\_output\_delay

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There are 0 ports with partial output delay specified.

12. checking unexpandable\_clocks

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There are 0 unexpandable clock pairs.

13. checking latch\_loops

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There are 0 combinational latch loops in the design through latch input

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| Design Timing Summary

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WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total Endpoints WHS(ns) THS(ns) THS Failing Endpoints THS Total Endpoints WPWS(ns) TPWS(ns) TPWS Failing Endpoints TPWS Total Endpoints

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5.960 0.000 0 56 0.265 0.000 0 56 4.500 0.000 0 30

All user specified timing constraints are met.

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| Clock Summary

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Clock Waveform(ns) Period(ns) Frequency(MHz)

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sys\_clk\_pin {0.000 5.000} 10.000 100.000

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| Intra Clock Table

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Clock WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total Endpoints WHS(ns) THS(ns) THS Failing Endpoints THS Total Endpoints WPWS(ns) TPWS(ns) TPWS Failing Endpoints TPWS Total Endpoints

----- ------- ------- --------------------- ------------------- ------- ------- --------------------- ------------------- -------- -------- ---------------------- --------------------

sys\_clk\_pin 5.960 0.000 0 56 0.265 0.000 0 56 4.500 0.000 0 30

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| Inter Clock Table

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From Clock To Clock WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total Endpoints WHS(ns) THS(ns) THS Failing Endpoints THS Total Endpoints

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| Other Path Groups Table

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Path Group From Clock To Clock WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total Endpoints WHS(ns) THS(ns) THS Failing Endpoints THS Total Endpoints

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| Timing Details

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From Clock: sys\_clk\_pin

To Clock: sys\_clk\_pin

Setup : 0 Failing Endpoints, Worst Slack 5.960ns, Total Violation 0.000ns

Hold : 0 Failing Endpoints, Worst Slack 0.265ns, Total Violation 0.000ns

PW : 0 Failing Endpoints, Worst Slack 4.500ns, Total Violation 0.000ns

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Max Delay Paths

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Slack (MET) : 5.960ns (required time - arrival time)

Source: slow/counter\_reg[16]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[25]/R

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 3.453ns (logic 0.766ns (22.181%) route 2.687ns (77.819%))

Logic Levels: 2 (LUT5=1 LUT6=1)

Clock Path Skew: -0.027ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 4.853ns = ( 14.853 - 10.000 )

Source Clock Delay (SCD): 5.154ns

Clock Pessimism Removal (CPR): 0.274ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.458 1.458 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.967 3.425 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.096 3.521 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.633 5.154 slow/clk\_IBUF\_BUFG

SLICE\_X2Y13 r slow/counter\_reg[16]/C

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SLICE\_X2Y13 FDRE (Prop\_fdre\_C\_Q) 0.518 5.672 f slow/counter\_reg[16]/Q

net (fo=2, routed) 1.075 6.747 slow/counter[16]

SLICE\_X3Y13 LUT6 (Prop\_lut6\_I4\_O) 0.124 6.871 f slow/counter[27]\_i\_3/O

net (fo=2, routed) 0.815 7.687 slow/n\_0\_counter[27]\_i\_3

SLICE\_X3Y12 LUT5 (Prop\_lut5\_I0\_O) 0.124 7.811 r slow/counter[27]\_i\_1/O

net (fo=27, routed) 0.797 8.608 slow/slowClk\_0

SLICE\_X2Y16 FDRE r slow/counter\_reg[25]/R

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

10.000 10.000 r

W5 0.000 10.000 r clk

net (fo=0) 0.000 10.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.388 11.388 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.862 13.250 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.091 13.341 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.512 14.853 slow/clk\_IBUF\_BUFG

SLICE\_X2Y16 r slow/counter\_reg[25]/C

clock pessimism 0.274 15.127

clock uncertainty -0.035 15.092

SLICE\_X2Y16 FDRE (Setup\_fdre\_C\_R) -0.524 14.568 slow/counter\_reg[25]

-------------------------------------------------------------------

required time 14.568

arrival time -8.608

-------------------------------------------------------------------

slack 5.960

Slack (MET) : 5.960ns (required time - arrival time)

Source: slow/counter\_reg[16]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[26]/R

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 3.453ns (logic 0.766ns (22.181%) route 2.687ns (77.819%))

Logic Levels: 2 (LUT5=1 LUT6=1)

Clock Path Skew: -0.027ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 4.853ns = ( 14.853 - 10.000 )

Source Clock Delay (SCD): 5.154ns

Clock Pessimism Removal (CPR): 0.274ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.458 1.458 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.967 3.425 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.096 3.521 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.633 5.154 slow/clk\_IBUF\_BUFG

SLICE\_X2Y13 r slow/counter\_reg[16]/C

------------------------------------------------------------------- -------------------

SLICE\_X2Y13 FDRE (Prop\_fdre\_C\_Q) 0.518 5.672 f slow/counter\_reg[16]/Q

net (fo=2, routed) 1.075 6.747 slow/counter[16]

SLICE\_X3Y13 LUT6 (Prop\_lut6\_I4\_O) 0.124 6.871 f slow/counter[27]\_i\_3/O

net (fo=2, routed) 0.815 7.687 slow/n\_0\_counter[27]\_i\_3

SLICE\_X3Y12 LUT5 (Prop\_lut5\_I0\_O) 0.124 7.811 r slow/counter[27]\_i\_1/O

net (fo=27, routed) 0.797 8.608 slow/slowClk\_0

SLICE\_X2Y16 FDRE r slow/counter\_reg[26]/R

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

10.000 10.000 r

W5 0.000 10.000 r clk

net (fo=0) 0.000 10.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.388 11.388 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.862 13.250 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.091 13.341 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.512 14.853 slow/clk\_IBUF\_BUFG

SLICE\_X2Y16 r slow/counter\_reg[26]/C

clock pessimism 0.274 15.127

clock uncertainty -0.035 15.092

SLICE\_X2Y16 FDRE (Setup\_fdre\_C\_R) -0.524 14.568 slow/counter\_reg[26]

-------------------------------------------------------------------

required time 14.568

arrival time -8.608

-------------------------------------------------------------------

slack 5.960

Slack (MET) : 5.960ns (required time - arrival time)

Source: slow/counter\_reg[16]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[27]/R

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 3.453ns (logic 0.766ns (22.181%) route 2.687ns (77.819%))

Logic Levels: 2 (LUT5=1 LUT6=1)

Clock Path Skew: -0.027ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 4.853ns = ( 14.853 - 10.000 )

Source Clock Delay (SCD): 5.154ns

Clock Pessimism Removal (CPR): 0.274ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.458 1.458 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.967 3.425 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.096 3.521 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.633 5.154 slow/clk\_IBUF\_BUFG

SLICE\_X2Y13 r slow/counter\_reg[16]/C

------------------------------------------------------------------- -------------------

SLICE\_X2Y13 FDRE (Prop\_fdre\_C\_Q) 0.518 5.672 f slow/counter\_reg[16]/Q

net (fo=2, routed) 1.075 6.747 slow/counter[16]

SLICE\_X3Y13 LUT6 (Prop\_lut6\_I4\_O) 0.124 6.871 f slow/counter[27]\_i\_3/O

net (fo=2, routed) 0.815 7.687 slow/n\_0\_counter[27]\_i\_3

SLICE\_X3Y12 LUT5 (Prop\_lut5\_I0\_O) 0.124 7.811 r slow/counter[27]\_i\_1/O

net (fo=27, routed) 0.797 8.608 slow/slowClk\_0

SLICE\_X2Y16 FDRE r slow/counter\_reg[27]/R

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

10.000 10.000 r

W5 0.000 10.000 r clk

net (fo=0) 0.000 10.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.388 11.388 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.862 13.250 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.091 13.341 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.512 14.853 slow/clk\_IBUF\_BUFG

SLICE\_X2Y16 r slow/counter\_reg[27]/C

clock pessimism 0.274 15.127

clock uncertainty -0.035 15.092

SLICE\_X2Y16 FDRE (Setup\_fdre\_C\_R) -0.524 14.568 slow/counter\_reg[27]

-------------------------------------------------------------------

required time 14.568

arrival time -8.608

-------------------------------------------------------------------

slack 5.960

Slack (MET) : 6.100ns (required time - arrival time)

Source: slow/counter\_reg[16]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[21]/R

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 3.315ns (logic 0.766ns (23.108%) route 2.549ns (76.892%))

Logic Levels: 2 (LUT5=1 LUT6=1)

Clock Path Skew: -0.026ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 4.854ns = ( 14.854 - 10.000 )

Source Clock Delay (SCD): 5.154ns

Clock Pessimism Removal (CPR): 0.274ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.458 1.458 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.967 3.425 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.096 3.521 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.633 5.154 slow/clk\_IBUF\_BUFG

SLICE\_X2Y13 r slow/counter\_reg[16]/C

------------------------------------------------------------------- -------------------

SLICE\_X2Y13 FDRE (Prop\_fdre\_C\_Q) 0.518 5.672 f slow/counter\_reg[16]/Q

net (fo=2, routed) 1.075 6.747 slow/counter[16]

SLICE\_X3Y13 LUT6 (Prop\_lut6\_I4\_O) 0.124 6.871 f slow/counter[27]\_i\_3/O

net (fo=2, routed) 0.815 7.687 slow/n\_0\_counter[27]\_i\_3

SLICE\_X3Y12 LUT5 (Prop\_lut5\_I0\_O) 0.124 7.811 r slow/counter[27]\_i\_1/O

net (fo=27, routed) 0.659 8.469 slow/slowClk\_0

SLICE\_X2Y15 FDRE r slow/counter\_reg[21]/R

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

10.000 10.000 r

W5 0.000 10.000 r clk

net (fo=0) 0.000 10.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.388 11.388 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.862 13.250 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.091 13.341 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.513 14.854 slow/clk\_IBUF\_BUFG

SLICE\_X2Y15 r slow/counter\_reg[21]/C

clock pessimism 0.274 15.128

clock uncertainty -0.035 15.093

SLICE\_X2Y15 FDRE (Setup\_fdre\_C\_R) -0.524 14.569 slow/counter\_reg[21]

-------------------------------------------------------------------

required time 14.569

arrival time -8.469

-------------------------------------------------------------------

slack 6.100

Slack (MET) : 6.100ns (required time - arrival time)

Source: slow/counter\_reg[16]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[22]/R

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 3.315ns (logic 0.766ns (23.108%) route 2.549ns (76.892%))

Logic Levels: 2 (LUT5=1 LUT6=1)

Clock Path Skew: -0.026ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 4.854ns = ( 14.854 - 10.000 )

Source Clock Delay (SCD): 5.154ns

Clock Pessimism Removal (CPR): 0.274ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.458 1.458 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.967 3.425 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.096 3.521 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.633 5.154 slow/clk\_IBUF\_BUFG

SLICE\_X2Y13 r slow/counter\_reg[16]/C

------------------------------------------------------------------- -------------------

SLICE\_X2Y13 FDRE (Prop\_fdre\_C\_Q) 0.518 5.672 f slow/counter\_reg[16]/Q

net (fo=2, routed) 1.075 6.747 slow/counter[16]

SLICE\_X3Y13 LUT6 (Prop\_lut6\_I4\_O) 0.124 6.871 f slow/counter[27]\_i\_3/O

net (fo=2, routed) 0.815 7.687 slow/n\_0\_counter[27]\_i\_3

SLICE\_X3Y12 LUT5 (Prop\_lut5\_I0\_O) 0.124 7.811 r slow/counter[27]\_i\_1/O

net (fo=27, routed) 0.659 8.469 slow/slowClk\_0

SLICE\_X2Y15 FDRE r slow/counter\_reg[22]/R

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

10.000 10.000 r

W5 0.000 10.000 r clk

net (fo=0) 0.000 10.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.388 11.388 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.862 13.250 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.091 13.341 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.513 14.854 slow/clk\_IBUF\_BUFG

SLICE\_X2Y15 r slow/counter\_reg[22]/C

clock pessimism 0.274 15.128

clock uncertainty -0.035 15.093

SLICE\_X2Y15 FDRE (Setup\_fdre\_C\_R) -0.524 14.569 slow/counter\_reg[22]

-------------------------------------------------------------------

required time 14.569

arrival time -8.469

-------------------------------------------------------------------

slack 6.100

Slack (MET) : 6.100ns (required time - arrival time)

Source: slow/counter\_reg[16]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[23]/R

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 3.315ns (logic 0.766ns (23.108%) route 2.549ns (76.892%))

Logic Levels: 2 (LUT5=1 LUT6=1)

Clock Path Skew: -0.026ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 4.854ns = ( 14.854 - 10.000 )

Source Clock Delay (SCD): 5.154ns

Clock Pessimism Removal (CPR): 0.274ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.458 1.458 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.967 3.425 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.096 3.521 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.633 5.154 slow/clk\_IBUF\_BUFG

SLICE\_X2Y13 r slow/counter\_reg[16]/C

------------------------------------------------------------------- -------------------

SLICE\_X2Y13 FDRE (Prop\_fdre\_C\_Q) 0.518 5.672 f slow/counter\_reg[16]/Q

net (fo=2, routed) 1.075 6.747 slow/counter[16]

SLICE\_X3Y13 LUT6 (Prop\_lut6\_I4\_O) 0.124 6.871 f slow/counter[27]\_i\_3/O

net (fo=2, routed) 0.815 7.687 slow/n\_0\_counter[27]\_i\_3

SLICE\_X3Y12 LUT5 (Prop\_lut5\_I0\_O) 0.124 7.811 r slow/counter[27]\_i\_1/O

net (fo=27, routed) 0.659 8.469 slow/slowClk\_0

SLICE\_X2Y15 FDRE r slow/counter\_reg[23]/R

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

10.000 10.000 r

W5 0.000 10.000 r clk

net (fo=0) 0.000 10.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.388 11.388 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.862 13.250 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.091 13.341 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.513 14.854 slow/clk\_IBUF\_BUFG

SLICE\_X2Y15 r slow/counter\_reg[23]/C

clock pessimism 0.274 15.128

clock uncertainty -0.035 15.093

SLICE\_X2Y15 FDRE (Setup\_fdre\_C\_R) -0.524 14.569 slow/counter\_reg[23]

-------------------------------------------------------------------

required time 14.569

arrival time -8.469

-------------------------------------------------------------------

slack 6.100

Slack (MET) : 6.100ns (required time - arrival time)

Source: slow/counter\_reg[16]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[24]/R

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 3.315ns (logic 0.766ns (23.108%) route 2.549ns (76.892%))

Logic Levels: 2 (LUT5=1 LUT6=1)

Clock Path Skew: -0.026ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 4.854ns = ( 14.854 - 10.000 )

Source Clock Delay (SCD): 5.154ns

Clock Pessimism Removal (CPR): 0.274ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.458 1.458 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.967 3.425 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.096 3.521 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.633 5.154 slow/clk\_IBUF\_BUFG

SLICE\_X2Y13 r slow/counter\_reg[16]/C

------------------------------------------------------------------- -------------------

SLICE\_X2Y13 FDRE (Prop\_fdre\_C\_Q) 0.518 5.672 f slow/counter\_reg[16]/Q

net (fo=2, routed) 1.075 6.747 slow/counter[16]

SLICE\_X3Y13 LUT6 (Prop\_lut6\_I4\_O) 0.124 6.871 f slow/counter[27]\_i\_3/O

net (fo=2, routed) 0.815 7.687 slow/n\_0\_counter[27]\_i\_3

SLICE\_X3Y12 LUT5 (Prop\_lut5\_I0\_O) 0.124 7.811 r slow/counter[27]\_i\_1/O

net (fo=27, routed) 0.659 8.469 slow/slowClk\_0

SLICE\_X2Y15 FDRE r slow/counter\_reg[24]/R

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

10.000 10.000 r

W5 0.000 10.000 r clk

net (fo=0) 0.000 10.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.388 11.388 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.862 13.250 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.091 13.341 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.513 14.854 slow/clk\_IBUF\_BUFG

SLICE\_X2Y15 r slow/counter\_reg[24]/C

clock pessimism 0.274 15.128

clock uncertainty -0.035 15.093

SLICE\_X2Y15 FDRE (Setup\_fdre\_C\_R) -0.524 14.569 slow/counter\_reg[24]

-------------------------------------------------------------------

required time 14.569

arrival time -8.469

-------------------------------------------------------------------

slack 6.100

Slack (MET) : 6.110ns (required time - arrival time)

Source: slow/counter\_reg[16]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[10]/R

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 3.307ns (logic 0.766ns (23.164%) route 2.541ns (76.836%))

Logic Levels: 2 (LUT5=1 LUT6=1)

Clock Path Skew: -0.024ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 4.856ns = ( 14.856 - 10.000 )

Source Clock Delay (SCD): 5.154ns

Clock Pessimism Removal (CPR): 0.274ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.458 1.458 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.967 3.425 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.096 3.521 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.633 5.154 slow/clk\_IBUF\_BUFG

SLICE\_X2Y13 r slow/counter\_reg[16]/C

------------------------------------------------------------------- -------------------

SLICE\_X2Y13 FDRE (Prop\_fdre\_C\_Q) 0.518 5.672 f slow/counter\_reg[16]/Q

net (fo=2, routed) 1.075 6.747 slow/counter[16]

SLICE\_X3Y13 LUT6 (Prop\_lut6\_I4\_O) 0.124 6.871 f slow/counter[27]\_i\_3/O

net (fo=2, routed) 0.815 7.687 slow/n\_0\_counter[27]\_i\_3

SLICE\_X3Y12 LUT5 (Prop\_lut5\_I0\_O) 0.124 7.811 r slow/counter[27]\_i\_1/O

net (fo=27, routed) 0.651 8.461 slow/slowClk\_0

SLICE\_X2Y12 FDRE r slow/counter\_reg[10]/R

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

10.000 10.000 r

W5 0.000 10.000 r clk

net (fo=0) 0.000 10.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.388 11.388 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.862 13.250 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.091 13.341 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.515 14.856 slow/clk\_IBUF\_BUFG

SLICE\_X2Y12 r slow/counter\_reg[10]/C

clock pessimism 0.274 15.130

clock uncertainty -0.035 15.095

SLICE\_X2Y12 FDRE (Setup\_fdre\_C\_R) -0.524 14.571 slow/counter\_reg[10]

-------------------------------------------------------------------

required time 14.571

arrival time -8.461

-------------------------------------------------------------------

slack 6.110

Slack (MET) : 6.110ns (required time - arrival time)

Source: slow/counter\_reg[16]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[11]/R

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 3.307ns (logic 0.766ns (23.164%) route 2.541ns (76.836%))

Logic Levels: 2 (LUT5=1 LUT6=1)

Clock Path Skew: -0.024ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 4.856ns = ( 14.856 - 10.000 )

Source Clock Delay (SCD): 5.154ns

Clock Pessimism Removal (CPR): 0.274ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.458 1.458 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.967 3.425 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.096 3.521 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.633 5.154 slow/clk\_IBUF\_BUFG

SLICE\_X2Y13 r slow/counter\_reg[16]/C

------------------------------------------------------------------- -------------------

SLICE\_X2Y13 FDRE (Prop\_fdre\_C\_Q) 0.518 5.672 f slow/counter\_reg[16]/Q

net (fo=2, routed) 1.075 6.747 slow/counter[16]

SLICE\_X3Y13 LUT6 (Prop\_lut6\_I4\_O) 0.124 6.871 f slow/counter[27]\_i\_3/O

net (fo=2, routed) 0.815 7.687 slow/n\_0\_counter[27]\_i\_3

SLICE\_X3Y12 LUT5 (Prop\_lut5\_I0\_O) 0.124 7.811 r slow/counter[27]\_i\_1/O

net (fo=27, routed) 0.651 8.461 slow/slowClk\_0

SLICE\_X2Y12 FDRE r slow/counter\_reg[11]/R

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

10.000 10.000 r

W5 0.000 10.000 r clk

net (fo=0) 0.000 10.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.388 11.388 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.862 13.250 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.091 13.341 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.515 14.856 slow/clk\_IBUF\_BUFG

SLICE\_X2Y12 r slow/counter\_reg[11]/C

clock pessimism 0.274 15.130

clock uncertainty -0.035 15.095

SLICE\_X2Y12 FDRE (Setup\_fdre\_C\_R) -0.524 14.571 slow/counter\_reg[11]

-------------------------------------------------------------------

required time 14.571

arrival time -8.461

-------------------------------------------------------------------

slack 6.110

Slack (MET) : 6.110ns (required time - arrival time)

Source: slow/counter\_reg[16]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[12]/R

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 3.307ns (logic 0.766ns (23.164%) route 2.541ns (76.836%))

Logic Levels: 2 (LUT5=1 LUT6=1)

Clock Path Skew: -0.024ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 4.856ns = ( 14.856 - 10.000 )

Source Clock Delay (SCD): 5.154ns

Clock Pessimism Removal (CPR): 0.274ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.458 1.458 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.967 3.425 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.096 3.521 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.633 5.154 slow/clk\_IBUF\_BUFG

SLICE\_X2Y13 r slow/counter\_reg[16]/C

------------------------------------------------------------------- -------------------

SLICE\_X2Y13 FDRE (Prop\_fdre\_C\_Q) 0.518 5.672 f slow/counter\_reg[16]/Q

net (fo=2, routed) 1.075 6.747 slow/counter[16]

SLICE\_X3Y13 LUT6 (Prop\_lut6\_I4\_O) 0.124 6.871 f slow/counter[27]\_i\_3/O

net (fo=2, routed) 0.815 7.687 slow/n\_0\_counter[27]\_i\_3

SLICE\_X3Y12 LUT5 (Prop\_lut5\_I0\_O) 0.124 7.811 r slow/counter[27]\_i\_1/O

net (fo=27, routed) 0.651 8.461 slow/slowClk\_0

SLICE\_X2Y12 FDRE r slow/counter\_reg[12]/R

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

10.000 10.000 r

W5 0.000 10.000 r clk

net (fo=0) 0.000 10.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 1.388 11.388 r clk\_IBUF\_inst/O

net (fo=1, routed) 1.862 13.250 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.091 13.341 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 1.515 14.856 slow/clk\_IBUF\_BUFG

SLICE\_X2Y12 r slow/counter\_reg[12]/C

clock pessimism 0.274 15.130

clock uncertainty -0.035 15.095

SLICE\_X2Y12 FDRE (Setup\_fdre\_C\_R) -0.524 14.571 slow/counter\_reg[12]

-------------------------------------------------------------------

required time 14.571

arrival time -8.461

-------------------------------------------------------------------

slack 6.110

Min Delay Paths

--------------------------------------------------------------------------------------

Slack (MET) : 0.265ns (arrival time - required time)

Source: slow/counter\_reg[11]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[11]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.399ns (logic 0.274ns (68.589%) route 0.125ns (31.411%))

Logic Levels: 1 (CARRY4=1)

Clock Path Skew: 0.000ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 1.989ns

Source Clock Delay (SCD): 1.475ns

Clock Pessimism Removal (CPR): 0.514ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.226 0.226 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.631 0.858 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.026 0.884 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.592 1.475 slow/clk\_IBUF\_BUFG

SLICE\_X2Y12 r slow/counter\_reg[11]/C

------------------------------------------------------------------- -------------------

SLICE\_X2Y12 FDRE (Prop\_fdre\_C\_Q) 0.164 1.639 r slow/counter\_reg[11]/Q

net (fo=2, routed) 0.125 1.765 slow/counter[11]

SLICE\_X2Y12 CARRY4 (Prop\_carry4\_S[2]\_O[2])

0.110 1.875 r slow/counter\_reg[12]\_i\_1/O[2]

net (fo=1, routed) 0.000 1.875 slow/n\_5\_counter\_reg[12]\_i\_1

SLICE\_X2Y12 FDRE r slow/counter\_reg[11]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.414 0.414 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.685 1.099 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.029 1.128 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.862 1.989 slow/clk\_IBUF\_BUFG

SLICE\_X2Y12 r slow/counter\_reg[11]/C

clock pessimism -0.514 1.475

SLICE\_X2Y12 FDRE (Hold\_fdre\_C\_D) 0.134 1.609 slow/counter\_reg[11]

-------------------------------------------------------------------

required time -1.609

arrival time 1.875

-------------------------------------------------------------------

slack 0.265

Slack (MET) : 0.265ns (arrival time - required time)

Source: slow/counter\_reg[23]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[23]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.399ns (logic 0.274ns (68.589%) route 0.125ns (31.411%))

Logic Levels: 1 (CARRY4=1)

Clock Path Skew: 0.000ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 1.987ns

Source Clock Delay (SCD): 1.474ns

Clock Pessimism Removal (CPR): 0.513ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.226 0.226 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.631 0.858 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.026 0.884 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.591 1.474 slow/clk\_IBUF\_BUFG

SLICE\_X2Y15 r slow/counter\_reg[23]/C

------------------------------------------------------------------- -------------------

SLICE\_X2Y15 FDRE (Prop\_fdre\_C\_Q) 0.164 1.638 r slow/counter\_reg[23]/Q

net (fo=2, routed) 0.125 1.764 slow/counter[23]

SLICE\_X2Y15 CARRY4 (Prop\_carry4\_S[2]\_O[2])

0.110 1.874 r slow/counter\_reg[24]\_i\_1/O[2]

net (fo=1, routed) 0.000 1.874 slow/n\_5\_counter\_reg[24]\_i\_1

SLICE\_X2Y15 FDRE r slow/counter\_reg[23]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.414 0.414 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.685 1.099 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.029 1.128 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.860 1.987 slow/clk\_IBUF\_BUFG

SLICE\_X2Y15 r slow/counter\_reg[23]/C

clock pessimism -0.513 1.474

SLICE\_X2Y15 FDRE (Hold\_fdre\_C\_D) 0.134 1.608 slow/counter\_reg[23]

-------------------------------------------------------------------

required time -1.608

arrival time 1.874

-------------------------------------------------------------------

slack 0.265

Slack (MET) : 0.265ns (arrival time - required time)

Source: slow/counter\_reg[7]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[7]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.399ns (logic 0.274ns (68.589%) route 0.125ns (31.411%))

Logic Levels: 1 (CARRY4=1)

Clock Path Skew: 0.000ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 1.991ns

Source Clock Delay (SCD): 1.476ns

Clock Pessimism Removal (CPR): 0.515ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.226 0.226 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.631 0.858 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.026 0.884 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.593 1.476 slow/clk\_IBUF\_BUFG

SLICE\_X2Y11 r slow/counter\_reg[7]/C

------------------------------------------------------------------- -------------------

SLICE\_X2Y11 FDRE (Prop\_fdre\_C\_Q) 0.164 1.640 r slow/counter\_reg[7]/Q

net (fo=2, routed) 0.125 1.766 slow/counter[7]

SLICE\_X2Y11 CARRY4 (Prop\_carry4\_S[2]\_O[2])

0.110 1.876 r slow/counter\_reg[8]\_i\_1/O[2]

net (fo=1, routed) 0.000 1.876 slow/n\_5\_counter\_reg[8]\_i\_1

SLICE\_X2Y11 FDRE r slow/counter\_reg[7]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.414 0.414 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.685 1.099 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.029 1.128 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.864 1.991 slow/clk\_IBUF\_BUFG

SLICE\_X2Y11 r slow/counter\_reg[7]/C

clock pessimism -0.515 1.476

SLICE\_X2Y11 FDRE (Hold\_fdre\_C\_D) 0.134 1.610 slow/counter\_reg[7]

-------------------------------------------------------------------

required time -1.610

arrival time 1.876

-------------------------------------------------------------------

slack 0.265

Slack (MET) : 0.266ns (arrival time - required time)

Source: slow/counter\_reg[15]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[15]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.400ns (logic 0.274ns (68.524%) route 0.126ns (31.476%))

Logic Levels: 1 (CARRY4=1)

Clock Path Skew: 0.000ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 1.988ns

Source Clock Delay (SCD): 1.474ns

Clock Pessimism Removal (CPR): 0.514ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.226 0.226 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.631 0.858 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.026 0.884 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.591 1.474 slow/clk\_IBUF\_BUFG

SLICE\_X2Y13 r slow/counter\_reg[15]/C

------------------------------------------------------------------- -------------------

SLICE\_X2Y13 FDRE (Prop\_fdre\_C\_Q) 0.164 1.638 r slow/counter\_reg[15]/Q

net (fo=2, routed) 0.126 1.764 slow/counter[15]

SLICE\_X2Y13 CARRY4 (Prop\_carry4\_S[2]\_O[2])

0.110 1.874 r slow/counter\_reg[16]\_i\_1/O[2]

net (fo=1, routed) 0.000 1.874 slow/n\_5\_counter\_reg[16]\_i\_1

SLICE\_X2Y13 FDRE r slow/counter\_reg[15]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.414 0.414 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.685 1.099 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.029 1.128 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.861 1.988 slow/clk\_IBUF\_BUFG

SLICE\_X2Y13 r slow/counter\_reg[15]/C

clock pessimism -0.514 1.474

SLICE\_X2Y13 FDRE (Hold\_fdre\_C\_D) 0.134 1.608 slow/counter\_reg[15]

-------------------------------------------------------------------

required time -1.608

arrival time 1.874

-------------------------------------------------------------------

slack 0.266

Slack (MET) : 0.267ns (arrival time - required time)

Source: slow/counter\_reg[3]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[3]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.401ns (logic 0.274ns (68.412%) route 0.127ns (31.588%))

Logic Levels: 1 (CARRY4=1)

Clock Path Skew: 0.000ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 1.991ns

Source Clock Delay (SCD): 1.476ns

Clock Pessimism Removal (CPR): 0.515ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.226 0.226 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.631 0.858 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.026 0.884 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.593 1.476 slow/clk\_IBUF\_BUFG

SLICE\_X2Y10 r slow/counter\_reg[3]/C

------------------------------------------------------------------- -------------------

SLICE\_X2Y10 FDRE (Prop\_fdre\_C\_Q) 0.164 1.640 r slow/counter\_reg[3]/Q

net (fo=2, routed) 0.127 1.767 slow/counter[3]

SLICE\_X2Y10 CARRY4 (Prop\_carry4\_S[2]\_O[2])

0.110 1.877 r slow/counter\_reg[4]\_i\_1/O[2]

net (fo=1, routed) 0.000 1.877 slow/n\_5\_counter\_reg[4]\_i\_1

SLICE\_X2Y10 FDRE r slow/counter\_reg[3]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.414 0.414 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.685 1.099 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.029 1.128 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.864 1.991 slow/clk\_IBUF\_BUFG

SLICE\_X2Y10 r slow/counter\_reg[3]/C

clock pessimism -0.515 1.476

SLICE\_X2Y10 FDRE (Hold\_fdre\_C\_D) 0.134 1.610 slow/counter\_reg[3]

-------------------------------------------------------------------

required time -1.610

arrival time 1.877

-------------------------------------------------------------------

slack 0.267

Slack (MET) : 0.267ns (arrival time - required time)

Source: slow/counter\_reg[19]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[19]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.401ns (logic 0.274ns (68.412%) route 0.127ns (31.588%))

Logic Levels: 1 (CARRY4=1)

Clock Path Skew: 0.000ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 1.988ns

Source Clock Delay (SCD): 1.474ns

Clock Pessimism Removal (CPR): 0.514ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.226 0.226 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.631 0.858 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.026 0.884 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.591 1.474 slow/clk\_IBUF\_BUFG

SLICE\_X2Y14 r slow/counter\_reg[19]/C

------------------------------------------------------------------- -------------------

SLICE\_X2Y14 FDRE (Prop\_fdre\_C\_Q) 0.164 1.638 r slow/counter\_reg[19]/Q

net (fo=2, routed) 0.127 1.765 slow/counter[19]

SLICE\_X2Y14 CARRY4 (Prop\_carry4\_S[2]\_O[2])

0.110 1.875 r slow/counter\_reg[20]\_i\_1/O[2]

net (fo=1, routed) 0.000 1.875 slow/n\_5\_counter\_reg[20]\_i\_1

SLICE\_X2Y14 FDRE r slow/counter\_reg[19]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.414 0.414 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.685 1.099 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.029 1.128 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.861 1.988 slow/clk\_IBUF\_BUFG

SLICE\_X2Y14 r slow/counter\_reg[19]/C

clock pessimism -0.514 1.474

SLICE\_X2Y14 FDRE (Hold\_fdre\_C\_D) 0.134 1.608 slow/counter\_reg[19]

-------------------------------------------------------------------

required time -1.608

arrival time 1.875

-------------------------------------------------------------------

slack 0.267

Slack (MET) : 0.267ns (arrival time - required time)

Source: slow/counter\_reg[27]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[27]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.401ns (logic 0.274ns (68.401%) route 0.127ns (31.599%))

Logic Levels: 1 (CARRY4=1)

Clock Path Skew: 0.000ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 1.986ns

Source Clock Delay (SCD): 1.473ns

Clock Pessimism Removal (CPR): 0.513ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.226 0.226 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.631 0.858 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.026 0.884 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.590 1.473 slow/clk\_IBUF\_BUFG

SLICE\_X2Y16 r slow/counter\_reg[27]/C

------------------------------------------------------------------- -------------------

SLICE\_X2Y16 FDRE (Prop\_fdre\_C\_Q) 0.164 1.637 r slow/counter\_reg[27]/Q

net (fo=2, routed) 0.127 1.764 slow/counter[27]

SLICE\_X2Y16 CARRY4 (Prop\_carry4\_S[2]\_O[2])

0.110 1.874 r slow/counter\_reg[27]\_i\_2/O[2]

net (fo=1, routed) 0.000 1.874 slow/n\_5\_counter\_reg[27]\_i\_2

SLICE\_X2Y16 FDRE r slow/counter\_reg[27]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.414 0.414 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.685 1.099 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.029 1.128 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.859 1.986 slow/clk\_IBUF\_BUFG

SLICE\_X2Y16 r slow/counter\_reg[27]/C

clock pessimism -0.513 1.473

SLICE\_X2Y16 FDRE (Hold\_fdre\_C\_D) 0.134 1.607 slow/counter\_reg[27]

-------------------------------------------------------------------

required time -1.607

arrival time 1.874

-------------------------------------------------------------------

slack 0.267

Slack (MET) : 0.274ns (arrival time - required time)

Source: slow/counter\_reg[0]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[0]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.365ns (logic 0.186ns (50.911%) route 0.179ns (49.089%))

Logic Levels: 1 (LUT1=1)

Clock Path Skew: 0.000ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 1.991ns

Source Clock Delay (SCD): 1.476ns

Clock Pessimism Removal (CPR): 0.515ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.226 0.226 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.631 0.858 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.026 0.884 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.593 1.476 slow/clk\_IBUF\_BUFG

SLICE\_X3Y11 r slow/counter\_reg[0]/C

------------------------------------------------------------------- -------------------

SLICE\_X3Y11 FDRE (Prop\_fdre\_C\_Q) 0.141 1.617 f slow/counter\_reg[0]/Q

net (fo=3, routed) 0.179 1.796 slow/counter[0]

SLICE\_X3Y11 LUT1 (Prop\_lut1\_I0\_O) 0.045 1.841 r slow/counter[0]\_i\_1/O

net (fo=1, routed) 0.000 1.841 slow/counter\_1[0]

SLICE\_X3Y11 FDRE r slow/counter\_reg[0]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.414 0.414 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.685 1.099 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.029 1.128 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.864 1.991 slow/clk\_IBUF\_BUFG

SLICE\_X3Y11 r slow/counter\_reg[0]/C

clock pessimism -0.515 1.476

SLICE\_X3Y11 FDRE (Hold\_fdre\_C\_D) 0.091 1.567 slow/counter\_reg[0]

-------------------------------------------------------------------

required time -1.567

arrival time 1.841

-------------------------------------------------------------------

slack 0.274

Slack (MET) : 0.281ns (arrival time - required time)

Source: slow/counter\_reg[0]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[1]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.431ns (logic 0.299ns (69.339%) route 0.132ns (30.661%))

Logic Levels: 1 (CARRY4=1)

Clock Path Skew: 0.016ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 1.991ns

Source Clock Delay (SCD): 1.476ns

Clock Pessimism Removal (CPR): 0.499ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.226 0.226 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.631 0.858 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.026 0.884 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.593 1.476 slow/clk\_IBUF\_BUFG

SLICE\_X3Y11 r slow/counter\_reg[0]/C

------------------------------------------------------------------- -------------------

SLICE\_X3Y11 FDRE (Prop\_fdre\_C\_Q) 0.141 1.617 r slow/counter\_reg[0]/Q

net (fo=3, routed) 0.132 1.749 slow/counter[0]

SLICE\_X2Y10 CARRY4 (Prop\_carry4\_CYINIT\_O[0])

0.158 1.907 r slow/counter\_reg[4]\_i\_1/O[0]

net (fo=1, routed) 0.000 1.907 slow/n\_7\_counter\_reg[4]\_i\_1

SLICE\_X2Y10 FDRE r slow/counter\_reg[1]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.414 0.414 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.685 1.099 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.029 1.128 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.864 1.991 slow/clk\_IBUF\_BUFG

SLICE\_X2Y10 r slow/counter\_reg[1]/C

clock pessimism -0.499 1.492

SLICE\_X2Y10 FDRE (Hold\_fdre\_C\_D) 0.134 1.626 slow/counter\_reg[1]

-------------------------------------------------------------------

required time -1.626

arrival time 1.907

-------------------------------------------------------------------

slack 0.281

Slack (MET) : 0.301ns (arrival time - required time)

Source: slow/counter\_reg[11]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: slow/counter\_reg[12]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.435ns (logic 0.310ns (71.185%) route 0.125ns (28.815%))

Logic Levels: 1 (CARRY4=1)

Clock Path Skew: 0.000ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 1.989ns

Source Clock Delay (SCD): 1.475ns

Clock Pessimism Removal (CPR): 0.514ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.226 0.226 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.631 0.858 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.026 0.884 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.592 1.475 slow/clk\_IBUF\_BUFG

SLICE\_X2Y12 r slow/counter\_reg[11]/C

------------------------------------------------------------------- -------------------

SLICE\_X2Y12 FDRE (Prop\_fdre\_C\_Q) 0.164 1.639 r slow/counter\_reg[11]/Q

net (fo=2, routed) 0.125 1.765 slow/counter[11]

SLICE\_X2Y12 CARRY4 (Prop\_carry4\_S[2]\_O[3])

0.146 1.911 r slow/counter\_reg[12]\_i\_1/O[3]

net (fo=1, routed) 0.000 1.911 slow/n\_4\_counter\_reg[12]\_i\_1

SLICE\_X2Y12 FDRE r slow/counter\_reg[12]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

W5 0.000 0.000 r clk

net (fo=0) 0.000 0.000 clk

W5 IBUF (Prop\_ibuf\_I\_O) 0.414 0.414 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.685 1.099 clk\_IBUF

BUFGCTRL\_X0Y0 BUFG (Prop\_bufg\_I\_O) 0.029 1.128 r clk\_IBUF\_BUFG\_inst/O

net (fo=29, routed) 0.862 1.989 slow/clk\_IBUF\_BUFG

SLICE\_X2Y12 r slow/counter\_reg[12]/C

clock pessimism -0.514 1.475

SLICE\_X2Y12 FDRE (Hold\_fdre\_C\_D) 0.134 1.609 slow/counter\_reg[12]

-------------------------------------------------------------------

required time -1.609

arrival time 1.911

-------------------------------------------------------------------

slack 0.301

Pulse Width Checks

--------------------------------------------------------------------------------------

Clock Name: sys\_clk\_pin

Waveform: { 0 5 }

Period: 10.000

Sources: { clk }

Check Type Corner Lib Pin Reference Pin Required Actual Slack Location Pin

Min Period n/a BUFG/I n/a 2.155 10.000 7.845 BUFGCTRL\_X0Y0 clk\_IBUF\_BUFG\_inst/I

Min Period n/a FDRE/C n/a 1.000 10.000 9.000 SLICE\_X3Y11 slow/counter\_reg[0]/C

Min Period n/a FDRE/C n/a 1.000 10.000 9.000 SLICE\_X2Y12 slow/counter\_reg[10]/C

Min Period n/a FDRE/C n/a 1.000 10.000 9.000 SLICE\_X2Y12 slow/counter\_reg[11]/C

Min Period n/a FDRE/C n/a 1.000 10.000 9.000 SLICE\_X2Y12 slow/counter\_reg[12]/C

Min Period n/a FDRE/C n/a 1.000 10.000 9.000 SLICE\_X2Y13 slow/counter\_reg[13]/C

Min Period n/a FDRE/C n/a 1.000 10.000 9.000 SLICE\_X2Y13 slow/counter\_reg[14]/C

Min Period n/a FDRE/C n/a 1.000 10.000 9.000 SLICE\_X2Y13 slow/counter\_reg[15]/C

Min Period n/a FDRE/C n/a 1.000 10.000 9.000 SLICE\_X2Y13 slow/counter\_reg[16]/C

Min Period n/a FDRE/C n/a 1.000 10.000 9.000 SLICE\_X2Y14 slow/counter\_reg[17]/C

Low Pulse Width Slow FDRE/C n/a 0.500 5.000 4.500 SLICE\_X3Y11 slow/counter\_reg[0]/C

Low Pulse Width Slow FDRE/C n/a 0.500 5.000 4.500 SLICE\_X2Y12 slow/counter\_reg[10]/C

Low Pulse Width Fast FDRE/C n/a 0.500 5.000 4.500 SLICE\_X2Y12 slow/counter\_reg[10]/C

Low Pulse Width Slow FDRE/C n/a 0.500 5.000 4.500 SLICE\_X2Y12 slow/counter\_reg[11]/C

Low Pulse Width Fast FDRE/C n/a 0.500 5.000 4.500 SLICE\_X2Y12 slow/counter\_reg[11]/C

Low Pulse Width Slow FDRE/C n/a 0.500 5.000 4.500 SLICE\_X2Y12 slow/counter\_reg[12]/C

Low Pulse Width Fast FDRE/C n/a 0.500 5.000 4.500 SLICE\_X2Y12 slow/counter\_reg[12]/C

Low Pulse Width Slow FDRE/C n/a 0.500 5.000 4.500 SLICE\_X2Y13 slow/counter\_reg[13]/C

Low Pulse Width Fast FDRE/C n/a 0.500 5.000 4.500 SLICE\_X2Y13 slow/counter\_reg[13]/C

Low Pulse Width Slow FDRE/C n/a 0.500 5.000 4.500 SLICE\_X2Y13 slow/counter\_reg[14]/C

High Pulse Width Slow FDRE/C n/a 0.500 5.000 4.500 SLICE\_X2Y10 slow/counter\_reg[1]/C

High Pulse Width Slow FDRE/C n/a 0.500 5.000 4.500 SLICE\_X2Y10 slow/counter\_reg[2]/C

High Pulse Width Slow FDRE/C n/a 0.500 5.000 4.500 SLICE\_X2Y10 slow/counter\_reg[3]/C

High Pulse Width Slow FDRE/C n/a 0.500 5.000 4.500 SLICE\_X2Y10 slow/counter\_reg[4]/C

High Pulse Width Slow FDRE/C n/a 0.500 5.000 4.500 SLICE\_X3Y11 slow/counter\_reg[0]/C

High Pulse Width Slow FDRE/C n/a 0.500 5.000 4.500 SLICE\_X2Y12 slow/counter\_reg[10]/C

High Pulse Width Slow FDRE/C n/a 0.500 5.000 4.500 SLICE\_X2Y12 slow/counter\_reg[11]/C

High Pulse Width Slow FDRE/C n/a 0.500 5.000 4.500 SLICE\_X2Y12 slow/counter\_reg[12]/C

High Pulse Width Slow FDRE/C n/a 0.500 5.000 4.500 SLICE\_X2Y13 slow/counter\_reg[13]/C

High Pulse Width Slow FDRE/C n/a 0.500 5.000 4.500 SLICE\_X2Y13 slow/counter\_reg[14]/C

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