Joel Guo jg55475

Ted Mao ttm455

Touba – EE460M

Lab 3 Questions

* 1. Requirements: what is required to solve the problem
  2. Design specifications: what specifications are needed to solve that problem
  3. Design formulation: formulate a plan with a block diagram or algorithm
  4. Design Entry: design modules using Verilog to fit those blocks/algorithms
  5. Simulation: test the modules at high level to confirm that they function correctly
  6. Logic Synthesis: convert high level description to low level gates and flip flops
  7. Post synthesis simulation: test at low level looking at specific implementations/timing
  8. Mapping, placement, routing: putting the hardware description on actual hardware
  9. ASIC Masks: custom routed design used to generate a photo mask for fab process
  10. FPGA Programming Unit: what is used to program an FPGA
  11. Configured FPGAs: format design to write 0s and 1s to programmable cells

1. Tools are not required for requirements and design specifications. ModelSim is used for design entry to write the code and also for simulation. Vivado is used for logic synthesis, post synthesis simulation, and mapping, placement and routing onto the Basys Board. We do not generate ASIC masks in EE 460M lab. We use PCs as the FPGA Programming Unit to program FPGAs.
2. A problem is needed for requirements and design specifications, and a block diagram or algorithm is formulated. That block diagram or algorithm is realized using Verilog code. The Verilog code is debugged and fixed in simulation then synthesized, outputting a netlist, which specifies a list of gates and how to interconnect them. Post synthesis simulation takes this and debugs it on a lower level. A bitstream is then generated and the FPGA takes it to place the hardware design on an FPGA.