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# Vivado v2015.4 (64-bit)

# SW Build 1412921 on Wed Nov 18 09:43:45 MST 2015

# IP Build 1412160 on Tue Nov 17 13:47:24 MST 2015

# Start of session at: Thu Nov 10 22:31:03 2016

# Process ID: 7436

# Current directory: C:/Users/joelguo/Digital Systems/lab6/lab6.runs/synth\_1

# Command line: vivado.exe -log top.vds -mode batch -messageDb vivado.pb -notrace -source top.tcl

# Log file: C:/Users/joelguo/Digital Systems/lab6/lab6.runs/synth\_1/top.vds

# Journal file: C:/Users/joelguo/Digital Systems/lab6/lab6.runs/synth\_1\vivado.jou

#-----------------------------------------------------------

source top.tcl -notrace

Command: synth\_design -top top -part xc7a35tcpg236-1

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a35t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'

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Starting RTL Elaboration : Time (s): cpu = 00:00:07 ; elapsed = 00:00:10 . Memory (MB): peak = 263.609 ; gain = 91.891

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INFO: [Synth 8-638] synthesizing module 'top' [//Mac/Dropbox/Digital Systems/Labs/Lab6/lab6.v:1]

INFO: [Synth 8-638] synthesizing module 'controller' [//Mac/Dropbox/Digital Systems/Labs/Lab6/lab6.v:44]

INFO: [Synth 8-638] synthesizing module 'sevenSegClock' [//Mac/Dropbox/Digital Systems/Labs/Lab6/sevenSeg.v:71]

INFO: [Synth 8-256] done synthesizing module 'sevenSegClock' (1#1) [//Mac/Dropbox/Digital Systems/Labs/Lab6/sevenSeg.v:71]

INFO: [Synth 8-638] synthesizing module 'twoHexSeven' [//Mac/Dropbox/Digital Systems/Labs/Lab6/sevenSeg.v:32]

INFO: [Synth 8-638] synthesizing module 'hexSeven' [//Mac/Dropbox/Digital Systems/Labs/Lab6/sevenSeg.v:44]

INFO: [Synth 8-226] default block is never used [//Mac/Dropbox/Digital Systems/Labs/Lab6/sevenSeg.v:49]

INFO: [Synth 8-256] done synthesizing module 'hexSeven' (2#1) [//Mac/Dropbox/Digital Systems/Labs/Lab6/sevenSeg.v:44]

INFO: [Synth 8-256] done synthesizing module 'twoHexSeven' (3#1) [//Mac/Dropbox/Digital Systems/Labs/Lab6/sevenSeg.v:32]

INFO: [Synth 8-638] synthesizing module 'sevenSeg2' [//Mac/Dropbox/Digital Systems/Labs/Lab6/sevenSeg.v:1]

INFO: [Synth 8-256] done synthesizing module 'sevenSeg2' (4#1) [//Mac/Dropbox/Digital Systems/Labs/Lab6/sevenSeg.v:1]

INFO: [Synth 8-638] synthesizing module 'synchSP' [//Mac/Dropbox/Digital Systems/Labs/Lab6/input.v:1]

INFO: [Synth 8-638] synthesizing module 'debounce\_divider' [//Mac/Dropbox/Digital Systems/Labs/Lab6/input.v:36]

INFO: [Synth 8-256] done synthesizing module 'debounce\_divider' (5#1) [//Mac/Dropbox/Digital Systems/Labs/Lab6/input.v:36]

INFO: [Synth 8-638] synthesizing module 'debouncer' [//Mac/Dropbox/Digital Systems/Labs/Lab6/input.v:12]

INFO: [Synth 8-256] done synthesizing module 'debouncer' (6#1) [//Mac/Dropbox/Digital Systems/Labs/Lab6/input.v:12]

INFO: [Synth 8-638] synthesizing module 'singlePulse' [//Mac/Dropbox/Digital Systems/Labs/Lab6/input.v:24]

INFO: [Synth 8-256] done synthesizing module 'singlePulse' (7#1) [//Mac/Dropbox/Digital Systems/Labs/Lab6/input.v:24]

INFO: [Synth 8-256] done synthesizing module 'synchSP' (8#1) [//Mac/Dropbox/Digital Systems/Labs/Lab6/input.v:1]

INFO: [Synth 8-256] done synthesizing module 'controller' (9#1) [//Mac/Dropbox/Digital Systems/Labs/Lab6/lab6.v:44]

INFO: [Synth 8-638] synthesizing module 'memory' [//Mac/Dropbox/Digital Systems/Labs/Lab6/lab6.v:226]

INFO: [Synth 8-256] done synthesizing module 'memory' (10#1) [//Mac/Dropbox/Digital Systems/Labs/Lab6/lab6.v:226]

INFO: [Synth 8-256] done synthesizing module 'top' (11#1) [//Mac/Dropbox/Digital Systems/Labs/Lab6/lab6.v:1]

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Finished RTL Elaboration : Time (s): cpu = 00:00:08 ; elapsed = 00:00:11 . Memory (MB): peak = 299.785 ; gain = 128.066

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:08 ; elapsed = 00:00:11 . Memory (MB): peak = 299.785 ; gain = 128.066

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INFO: [Device 21-403] Loading part xc7a35tcpg236-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [//Mac/Dropbox/Digital Systems/Labs/Lab6/Basys3\_Master.xdc]

Finished Parsing XDC File [//Mac/Dropbox/Digital Systems/Labs/Lab6/Basys3\_Master.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [//Mac/Dropbox/Digital Systems/Labs/Lab6/Basys3\_Master.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/top\_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/top\_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used\_in\_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.016 . Memory (MB): peak = 583.965 ; gain = 0.000

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Finished Constraint Validation : Time (s): cpu = 00:00:18 ; elapsed = 00:00:21 . Memory (MB): peak = 583.965 ; gain = 412.246

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Start Loading Part and Timing Information

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Loading part: xc7a35tcpg236-1

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:18 ; elapsed = 00:00:21 . Memory (MB): peak = 583.965 ; gain = 412.246

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Start Applying 'set\_property' XDC Constraints

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Applied set\_property RAM\_STYLE = BLOCK for ctrl. (constraint file {//Mac/Dropbox/Digital Systems/Labs/Lab6/Basys3\_Master.xdc}, line 6).

Applied set\_property RAM\_STYLE = BLOCK for mem. (constraint file {//Mac/Dropbox/Digital Systems/Labs/Lab6/Basys3\_Master.xdc}, line 6).

Applied set\_property RAM\_STYLE = BLOCK for data\_bus1\_i. (constraint file {//Mac/Dropbox/Digital Systems/Labs/Lab6/Basys3\_Master.xdc}, line 6).

Applied set\_property RAM\_STYLE = BLOCK for data\_bus0. (constraint file {//Mac/Dropbox/Digital Systems/Labs/Lab6/Basys3\_Master.xdc}, line 6).

Applied set\_property RAM\_STYLE = BLOCK for data\_bus0\_\_0. (constraint file {//Mac/Dropbox/Digital Systems/Labs/Lab6/Basys3\_Master.xdc}, line 6).

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Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:18 ; elapsed = 00:00:22 . Memory (MB): peak = 583.965 ; gain = 412.246

---------------------------------------------------------------------------------

INFO: [Synth 8-5547] Trying to map ROM "clk1KHz" into Block RAM due to explicit "ram\_style" or "rom\_style" specification

INFO: [Synth 8-5586] ROM size for "clk1KHz" is below threshold of ROM address width. However it will be mapped to Block Ram due to explicit rom\_style/ram\_style attribute

INFO: [Synth 8-5547] Trying to map ROM "clk20Hz" into Block RAM due to explicit "ram\_style" or "rom\_style" specification

INFO: [Synth 8-5586] ROM size for "clk20Hz" is below threshold of ROM address width. However it will be mapped to Block Ram due to explicit rom\_style/ram\_style attribute

INFO: [Synth 8-3537] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the inputs of the operator [//Mac/Dropbox/Digital Systems/Labs/Lab6/lab6.v:86]

INFO: [Synth 8-5546] ROM "empty" won't be mapped to RAM because it is too sparse

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:32 ; elapsed = 00:00:35 . Memory (MB): peak = 593.703 ; gain = 421.984

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Report RTL Partitions:

+------+----------------------+------------+----------+

| |RTL Partition |Replication |Instances |

+------+----------------------+------------+----------+

|1 |rom\_\_1 | 1| 131071|

|2 |debounce\_divider\_\_GB1 | 1| 624|

|3 |synchSP\_\_GC0 | 1| 5|

|4 |controller\_\_GC0 | 1| 2968|

|5 |top\_\_GC0 | 1| 27|

+------+----------------------+------------+----------+

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Start RTL Component Statistics

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Detailed RTL Component Info :

+---Adders :

2 Input 22 Bit Adders := 2

2 Input 16 Bit Adders := 1

3 Input 8 Bit Adders := 1

2 Input 7 Bit Adders := 5

+---Registers :

22 Bit Registers := 4

16 Bit Registers := 2

8 Bit Registers := 5

7 Bit Registers := 3

5 Bit Registers := 1

1 Bit Registers := 11

+---RAMs :

1024 Bit RAMs := 1

+---Muxes :

2 Input 16 Bit Muxes := 1

18 Input 8 Bit Muxes := 1

2 Input 8 Bit Muxes := 1

16 Input 7 Bit Muxes := 2

2 Input 7 Bit Muxes := 9

6 Input 7 Bit Muxes := 1

14 Input 5 Bit Muxes := 1

2 Input 4 Bit Muxes := 3

18 Input 4 Bit Muxes := 1

18 Input 3 Bit Muxes := 2

18 Input 2 Bit Muxes := 1

2 Input 2 Bit Muxes := 1

2 Input 1 Bit Muxes := 4

18 Input 1 Bit Muxes := 3

4 Input 1 Bit Muxes := 1

5 Input 1 Bit Muxes := 1

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Finished RTL Component Statistics

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---------------------------------------------------------------------------------

Start RTL Hierarchical Component Statistics

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Hierarchical RTL Component report

Module debounce\_divider

Detailed RTL Component Info :

+---Adders :

2 Input 22 Bit Adders := 1

+---Registers :

22 Bit Registers := 2

1 Bit Registers := 1

Module debouncer

Detailed RTL Component Info :

+---Registers :

1 Bit Registers := 2

Module singlePulse

Detailed RTL Component Info :

+---Registers :

1 Bit Registers := 1

Module sevenSegClock

Detailed RTL Component Info :

+---Adders :

2 Input 16 Bit Adders := 1

+---Registers :

16 Bit Registers := 2

1 Bit Registers := 1

+---Muxes :

2 Input 16 Bit Muxes := 1

Module hexSeven\_\_1

Detailed RTL Component Info :

+---Muxes :

16 Input 7 Bit Muxes := 1

Module hexSeven

Detailed RTL Component Info :

+---Muxes :

16 Input 7 Bit Muxes := 1

Module sevenSeg2

Detailed RTL Component Info :

+---Registers :

1 Bit Registers := 1

+---Muxes :

2 Input 7 Bit Muxes := 1

2 Input 4 Bit Muxes := 1

2 Input 1 Bit Muxes := 1

Module controller

Detailed RTL Component Info :

+---Adders :

3 Input 8 Bit Adders := 1

2 Input 7 Bit Adders := 5

+---Registers :

8 Bit Registers := 4

7 Bit Registers := 3

5 Bit Registers := 1

1 Bit Registers := 1

+---Muxes :

18 Input 8 Bit Muxes := 1

2 Input 8 Bit Muxes := 1

2 Input 7 Bit Muxes := 8

6 Input 7 Bit Muxes := 1

14 Input 5 Bit Muxes := 1

2 Input 4 Bit Muxes := 2

18 Input 4 Bit Muxes := 1

18 Input 3 Bit Muxes := 2

18 Input 2 Bit Muxes := 1

2 Input 2 Bit Muxes := 1

18 Input 1 Bit Muxes := 3

2 Input 1 Bit Muxes := 3

4 Input 1 Bit Muxes := 1

5 Input 1 Bit Muxes := 1

Module memory

Detailed RTL Component Info :

+---Registers :

8 Bit Registers := 1

+---RAMs :

1024 Bit RAMs := 1

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Finished RTL Hierarchical Component Statistics

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Start Part Resource Summary

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Part Resources:

DSPs: 90 (col length:60)

BRAMs: 100 (col length: RAMB18 60 RAMB36 30)

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Finished Part Resource Summary

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Start Parallel Synthesis Optimization : Time (s): cpu = 00:00:33 ; elapsed = 00:00:37 . Memory (MB): peak = 593.703 ; gain = 421.984

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Start Cross Boundary Optimization

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INFO: [Synth 8-5547] Trying to map ROM "clk1KHz" into Block RAM due to explicit "ram\_style" or "rom\_style" specification

INFO: [Synth 8-5586] ROM size for "clk1KHz" is below threshold of ROM address width. However it will be mapped to Block Ram due to explicit rom\_style/ram\_style attribute

INFO: [Synth 8-5546] ROM "empty" won't be mapped to RAM because it is too sparse

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Finished Cross Boundary Optimization : Time (s): cpu = 00:00:34 ; elapsed = 00:00:38 . Memory (MB): peak = 593.703 ; gain = 421.984

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Finished Parallel Reinference : Time (s): cpu = 00:00:34 ; elapsed = 00:00:38 . Memory (MB): peak = 593.703 ; gain = 421.984

Report RTL Partitions:

+------+----------------------+------------+----------+

| |RTL Partition |Replication |Instances |

+------+----------------------+------------+----------+

|1 |rom\_\_1 | 1| 131071|

|2 |debounce\_divider\_\_GB1 | 1| 581|

|3 |synchSP\_\_GC0 | 1| 5|

|4 |controller\_\_GC0 | 1| 935|

|5 |top\_\_GC0 | 1| 27|

+------+----------------------+------------+----------+

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Start ROM, RAM, DSP and Shift Register Reporting

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ROM:

+-----------------+------------+---------------+----------------+

|Module Name | RTL Object | Depth x Width | Implemented As |

+-----------------+------------+---------------+----------------+

|sevenSegClock | rom | 65536x1 | LUT |

|debounce\_divider | rom\_\_1 | 4194304x1 | LUT |

|controller | rom\_\_2 | 32x1 | LUT |

|controller | rom\_\_3 | 32x1 | LUT |

|controller | rom\_\_4 | 32x1 | LUT |

|controller | rom\_\_5 | 32x1 | LUT |

|controller | rom\_\_6 | 32x1 | LUT |

|top | rom\_\_7 | 2x8 | LUT |

|sevenSegClock | rom | 65536x1 | LUT |

|controller\_\_GC0 | rom\_\_8 | 32x1 | LUT |

|controller\_\_GC0 | rom\_\_9 | 32x1 | LUT |

|controller\_\_GC0 | rom\_\_10 | 32x1 | LUT |

|controller\_\_GC0 | rom\_\_11 | 32x1 | LUT |

|controller\_\_GC0 | rom\_\_12 | 32x1 | LUT |

|top\_\_GC0 | rom\_\_13 | 2x8 | LUT |

+-----------------+------------+---------------+----------------+

Block RAM:

+------------+------------+------------------------+---+---+------------------------+---+---+---------+--------+--------+-------------------+

|Module Name | RTL Object | PORT A (Depth x Width) | W | R | PORT B (Depth x Width) | W | R | OUT\_REG | RAMB18 | RAMB36 | Hierarchical Name |

+------------+------------+------------------------+---+---+------------------------+---+---+---------+--------+--------+-------------------+

|top\_\_GC0 | RAM\_reg | 128 x 8(READ\_FIRST) | W | R | | | | Port A | 1 | 0 | memory/extram\_\_2 |

+------------+------------+------------------------+---+---+------------------------+---+---+---------+--------+--------+-------------------+

Note: The table above shows the Block RAMs at the current stage of the synthesis flow. Some Block RAMs may be reimplemented as non Block RAM primitives later in the synthesis flow. Multiple instantiated Block RAMs are reported only once. "Hierarchical Name" reflects the Block RAM name as it appears in the hierarchical module and only part of it is displayed.

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Finished ROM, RAM, DSP and Shift Register Reporting

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Start Area Optimization

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Finished Area Optimization : Time (s): cpu = 00:00:36 ; elapsed = 00:00:40 . Memory (MB): peak = 593.703 ; gain = 421.984

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Finished Parallel Area Optimization : Time (s): cpu = 00:00:36 ; elapsed = 00:00:40 . Memory (MB): peak = 593.703 ; gain = 421.984

Report RTL Partitions:

+------+----------------------+------------+----------+

| |RTL Partition |Replication |Instances |

+------+----------------------+------------+----------+

|1 |rom\_\_1 | 2| 17|

|2 |debounce\_divider\_\_GB1 | 2| 106|

|3 |synchSP\_\_GC0 | 2| 5|

|4 |controller\_\_GC0 | 1| 614|

|5 |top\_\_GC0 | 1| 19|

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Start Timing Optimization

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Start Applying XDC Timing Constraints

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Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:52 ; elapsed = 00:00:57 . Memory (MB): peak = 593.703 ; gain = 421.984

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Finished Timing Optimization : Time (s): cpu = 00:00:52 ; elapsed = 00:00:57 . Memory (MB): peak = 593.703 ; gain = 421.984

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Report RTL Partitions:

+------+----------------------+------------+----------+

| |RTL Partition |Replication |Instances |

+------+----------------------+------------+----------+

|1 |rom\_\_1 | 2| 17|

|2 |debounce\_divider\_\_GB1 | 2| 106|

|3 |synchSP\_\_GC0 | 2| 5|

|4 |controller\_\_GC0 | 1| 614|

|5 |top\_\_GC0 | 1| 19|

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Start Technology Mapping

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INFO: [Synth 8-4480] The timing for the instance RAM\_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing.

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Finished Technology Mapping : Time (s): cpu = 00:00:53 ; elapsed = 00:00:57 . Memory (MB): peak = 593.703 ; gain = 421.984

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Finished Parallel Technology Mapping Optimization : Time (s): cpu = 00:00:53 ; elapsed = 00:00:57 . Memory (MB): peak = 593.703 ; gain = 421.984

Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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Finished Parallel Synthesis Optimization : Time (s): cpu = 00:00:53 ; elapsed = 00:00:57 . Memory (MB): peak = 593.703 ; gain = 421.984

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Start IO Insertion

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Start Flattening Before IO Insertion

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Finished Flattening Before IO Insertion

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Start Final Netlist Cleanup

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Finished Final Netlist Cleanup

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Finished IO Insertion : Time (s): cpu = 00:00:53 ; elapsed = 00:00:58 . Memory (MB): peak = 593.703 ; gain = 421.984

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:53 ; elapsed = 00:00:58 . Memory (MB): peak = 593.703 ; gain = 421.984

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:53 ; elapsed = 00:00:58 . Memory (MB): peak = 593.703 ; gain = 421.984

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Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:53 ; elapsed = 00:00:58 . Memory (MB): peak = 593.703 ; gain = 421.984

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:54 ; elapsed = 00:00:58 . Memory (MB): peak = 593.703 ; gain = 421.984

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---------------------------------------------------------------------------------

Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:54 ; elapsed = 00:00:58 . Memory (MB): peak = 593.703 ; gain = 421.984

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Start Writing Synthesis Report

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Report BlackBoxes:

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| |BlackBox name |Instances |

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Report Cell Usage:

+------+---------+------+

| |Cell |Count |

+------+---------+------+

|1 |BUFG | 1|

|2 |CARRY4 | 18|

|3 |LUT1 | 64|

|4 |LUT2 | 25|

|5 |LUT3 | 67|

|6 |LUT4 | 50|

|7 |LUT5 | 24|

|8 |LUT6 | 74|

|9 |MUXF7 | 7|

|10 |RAMB18E1 | 1|

|11 |FDRE | 145|

|12 |IBUF | 13|

|13 |OBUF | 19|

+------+---------+------+

Report Instance Areas:

+------+-------------+-------------------+------+

| |Instance |Module |Cells |

+------+-------------+-------------------+------+

|1 |top | | 508|

|2 | mem |memory | 1|

|3 | ctrl |controller | 473|

|4 | buttonL |synchSP | 142|

|5 | db |debouncer\_1 | 64|

|6 | dbdiv |debounce\_divider\_2 | 77|

|7 | sp |singlePulse\_3 | 1|

|8 | buttonR |synchSP\_0 | 103|

|9 | db |debouncer | 25|

|10 | dbdiv |debounce\_divider | 77|

|11 | sp |singlePulse | 1|

|12 | display |sevenSeg2 | 9|

|13 | sevenClk |sevenSegClock | 62|

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:54 ; elapsed = 00:00:58 . Memory (MB): peak = 593.703 ; gain = 421.984

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Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:41 ; elapsed = 00:00:47 . Memory (MB): peak = 593.703 ; gain = 119.965

Synthesis Optimization Complete : Time (s): cpu = 00:00:54 ; elapsed = 00:00:59 . Memory (MB): peak = 593.703 ; gain = 421.984

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 32 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 1 inverter(s) to 1 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis

45 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:52 ; elapsed = 00:00:55 . Memory (MB): peak = 593.703 ; gain = 406.059

report\_utilization: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.031 . Memory (MB): peak = 593.703 ; gain = 0.000

INFO: [Common 17-206] Exiting Vivado at Thu Nov 10 22:32:04 2016...