ANKARA UNIVERSITY

DEPARTMENT
OF
COMPUTER ENGINEERING

COM/BLM 275
DIGITAL LOGIC
DESIGN

LABORATORY
MANUAL

Experiment #4

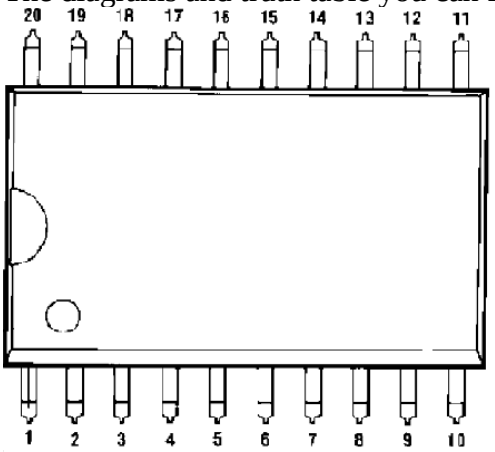
D-LATCHES AND SEQUENTIAL CIRCUIT DESIGN

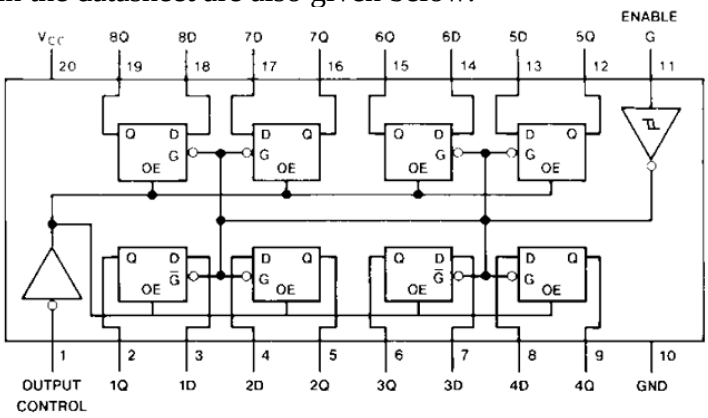
Objective:

To experiment with a D-latch integrated circuit and use it in a simple sequential circuit

Experiments :

You were given a datasheet for the integrated circuit (IC) type DM74S373N. Your first task was to read the datasheet and understand as much as you can. This IC contains eight D-latches. While the enable (G) is HIGH the Q outputs will follow the data (D) inputs. When the enable is LOW the output will be keeping the last value. The diagrams and truth table you can find in the datasheet are also given below.





DM74S373N

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = HIGH Level (Steady State)
L = LOW Level (Steady State)
X = Don't Care
Z = High Impedance State
Q_0 = The level of the output before steady-state input conditions were established.

You should first test that the IC given to you works as described in the truth table above. Make connections for using one of the latches inside the IC and test the output for varying inputs. Complete the timing diagram below for your circuit.