



数字系统课程设计

**信息科学与工程学院
毫米波国家重点实验室**

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课程时间安排

■ 理论课:

➤ 短学期第1周

周二(1-4)、周五(6-9)

➤ 地点: 教二101

■ 实验课:

➤ 短学期2-4周

周二上午9:00-12:00/周五下午1:30-4:30

➤ 地点: 信息学院中心机房 (图书馆东侧)





课程内容

一、CPLD&FPGA

二、数字系统设计基础

三、硬件描述语言VHDL基础

四、XILINX FPGA开发环境

五、课程设计题目与考核要求





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可编程逻辑器件（PLD）的发展

- 可编程只读存储器PROM、紫外线可擦除只读存储器 EPROM、电可擦除只读存储器 EEPROM。
- 可编程阵列逻辑PAL、通用阵列逻辑GAL。
（“与” & “或”）
- 20世纪80年代，ALTERA和XILINX分别推出了复杂可编程逻辑器件 CPLD — Complex Programmable Logic Device和现场可编程门阵列FPGA—Field Programmable Gate Array。





CPLD简介

- CPLD多基于乘积项Product-Term或Look-Up-Table结构。采用EEPROM或FLASH工艺，断电后信息不丢失。多用于1万门以下的小规模设计，适合做复杂的组合逻辑。
- 采用CPLD结构的PLD芯片有：

- ALTERA MAX CPLD系列简介

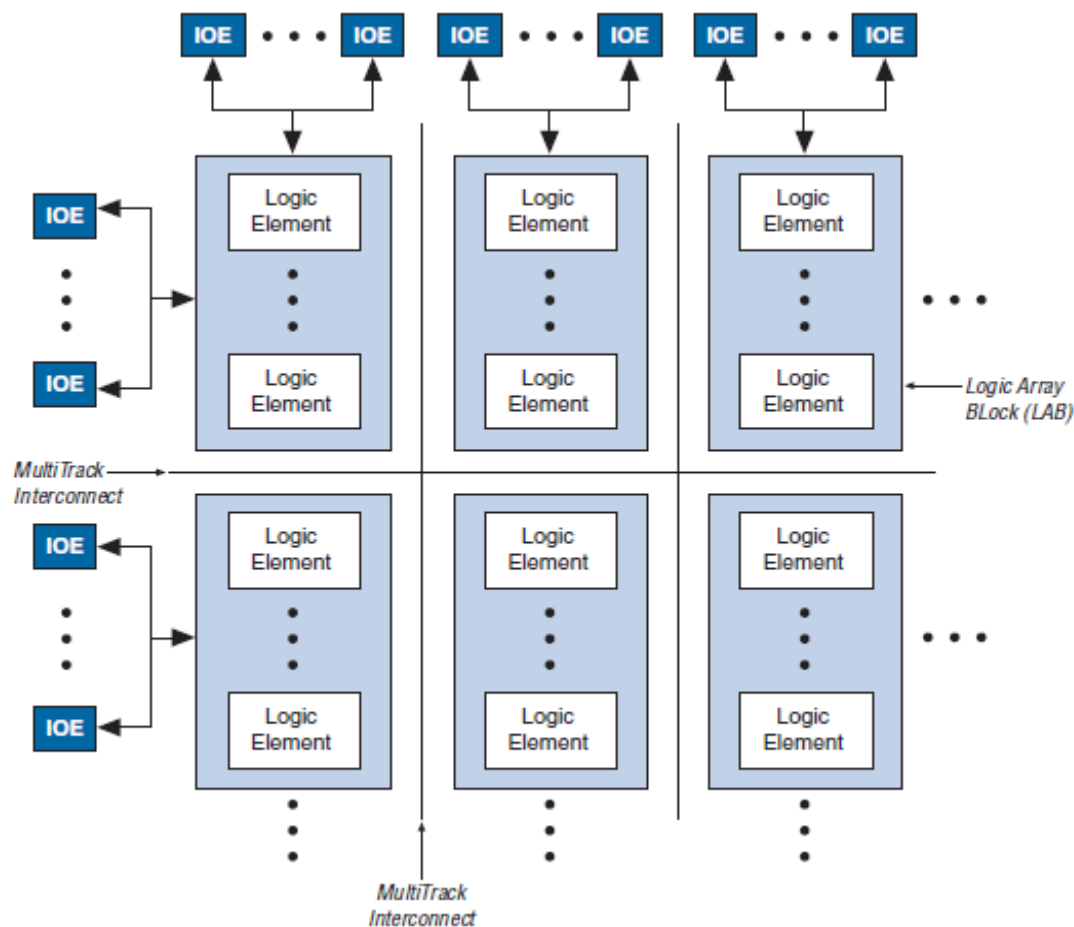
	MAX 7000S	MAX 3000A	MAX II	MAX IIZ	MAX V
推出年份	1995	2002	2004	2007	2010
工艺技术	0.5 μm	0.30 μm	0.18 μm	0.18 μm	0.18 μm
关键特性	5.0-V I/O	低成本	I/O数量	零功耗	低成本，低功耗

- XILINX公司的XC9500系列（FLASH工艺）



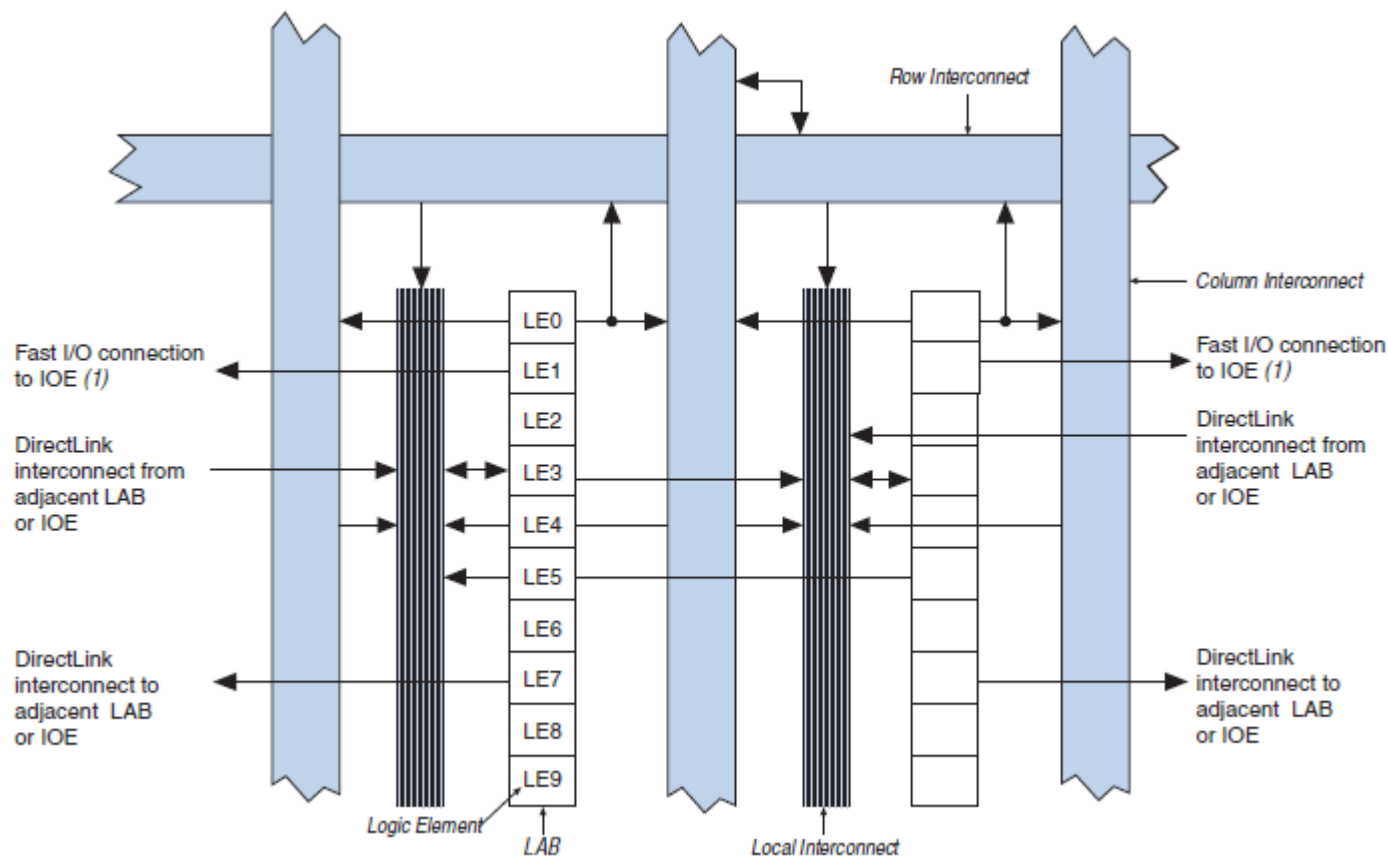


CPLD简介—MAX II 系列CPLD内部结构



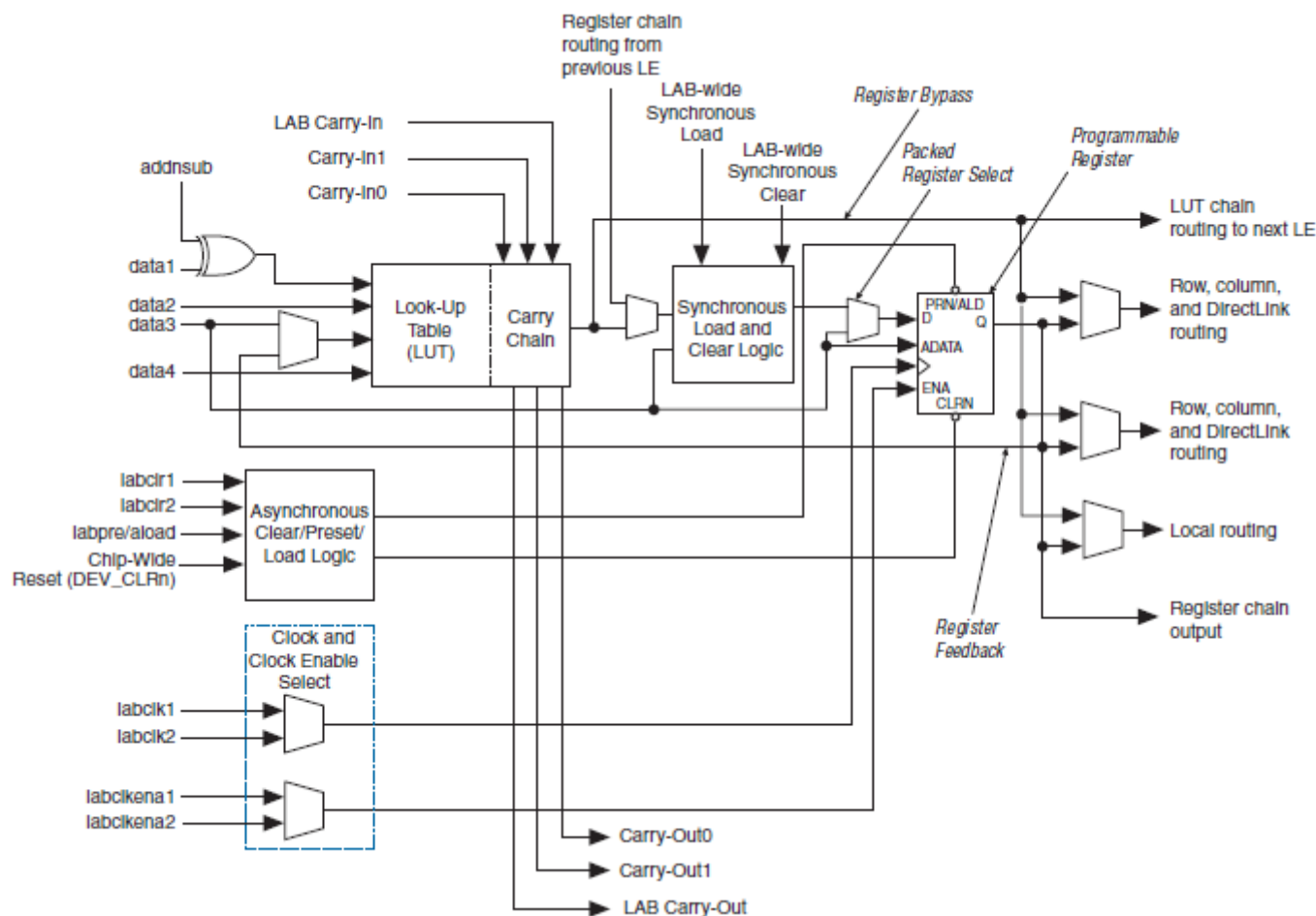


CPLD简介—MAX II 系列LAB结构





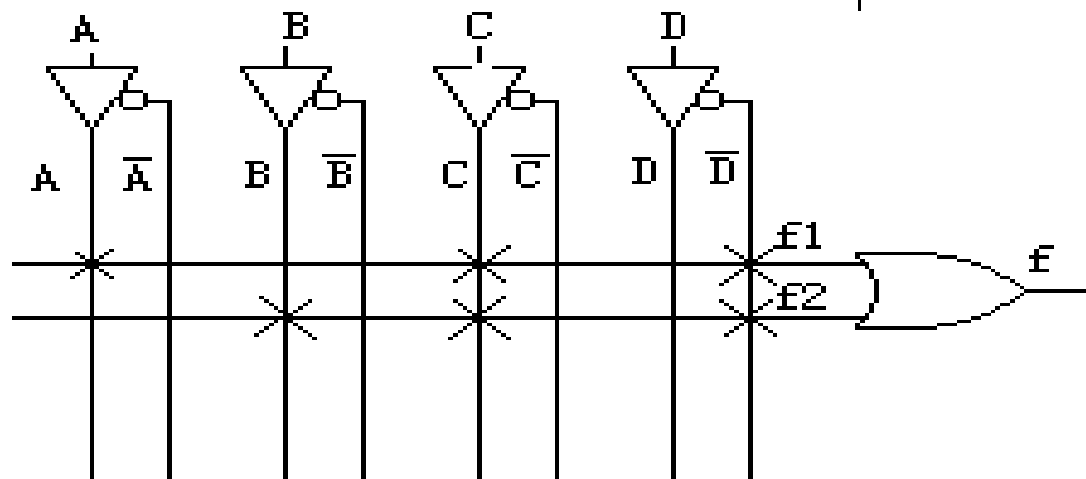
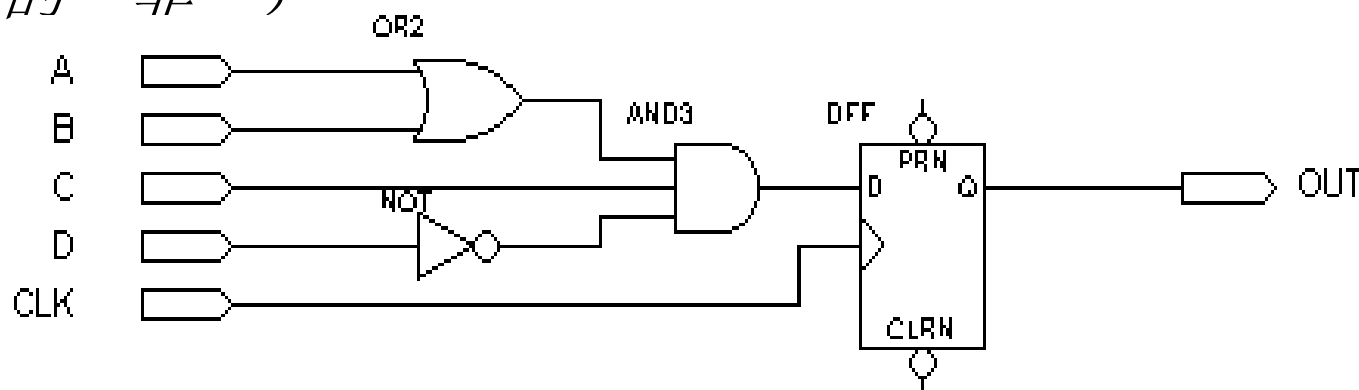
CPLD简介—MAX II 系列LE结构





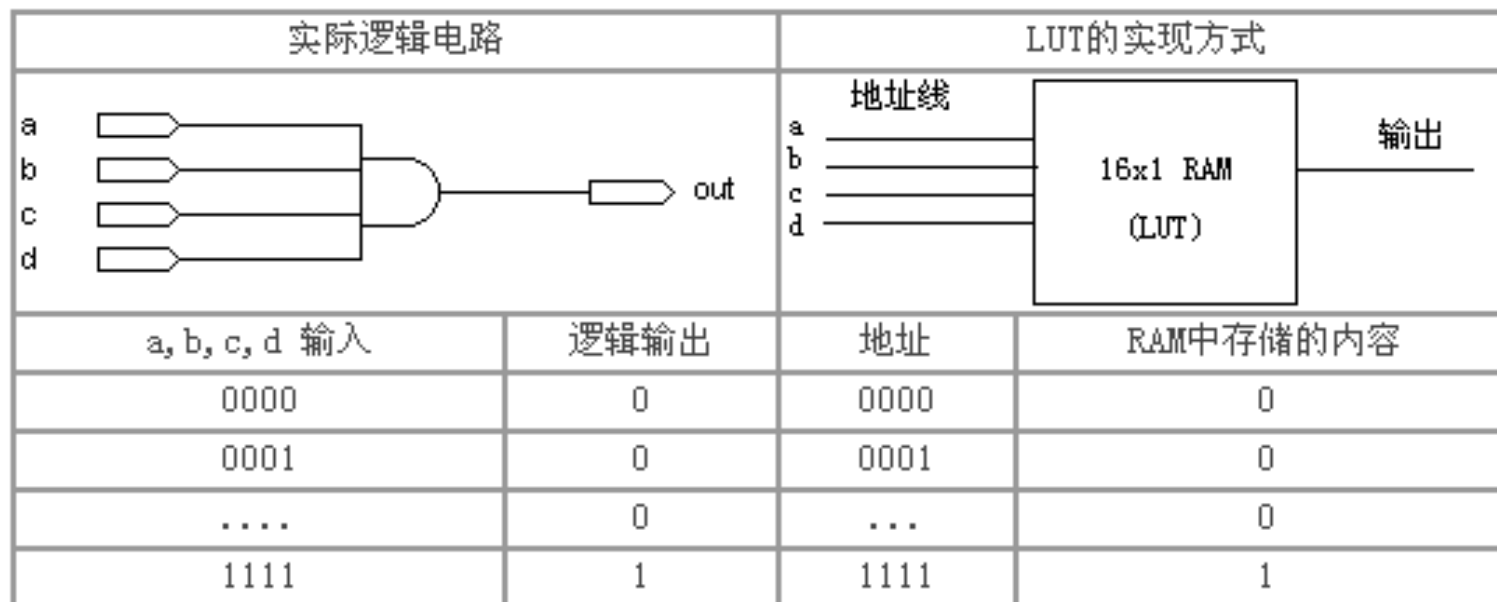
CPLD逻辑实现-乘积项

- 假设组合逻辑的输出 (AND3 的输出) 为 f , 则 $f=(A+B)*C*(!D)=A*C*!D + B*C*!D$ (我们以 $!D$ 表示 D 的“非”)





CPLD逻辑实现-查找表（LUT）



- 查找表（Look-Up-Table）简称为LUT，LUT本质上是一个RAM。目前多使用4输入的LUT，所以每一个LUT可以看成为一个具有4位地址线的16x1的RAM。
- 当用户通过原理图或HDL语言描述了一个逻辑电路以后，开发软件会自动计算逻辑电路的所有可能的结果，并把结果事先写入RAM。
- 每输入一个信号进行逻辑运算就等于输入一个地址进行查表，找出地址对应的内容，然后输出即可。





FPGA简介

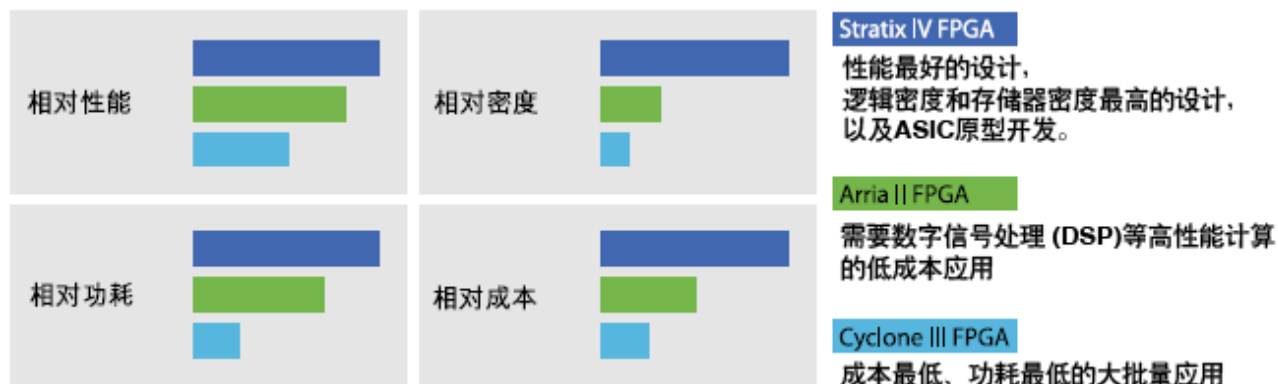
- FPGA多基于查找表(Look-Up Table)结构，采用SRAM工艺，密度高，触发器多，多用于10,000门以上的大规模设计，适合做复杂的时序逻辑，如数字信号处理和各种算法。FPGA能完成任何数字器件的功能,上至高性能CPU，下至简单的74电路，都可以用FPGA来实现。FPGA已经成为高性能数字系统的首选方案，是电子设计领域最具活力和发展前途的技术，其影响不亚于70年代单片机的发明和使用。



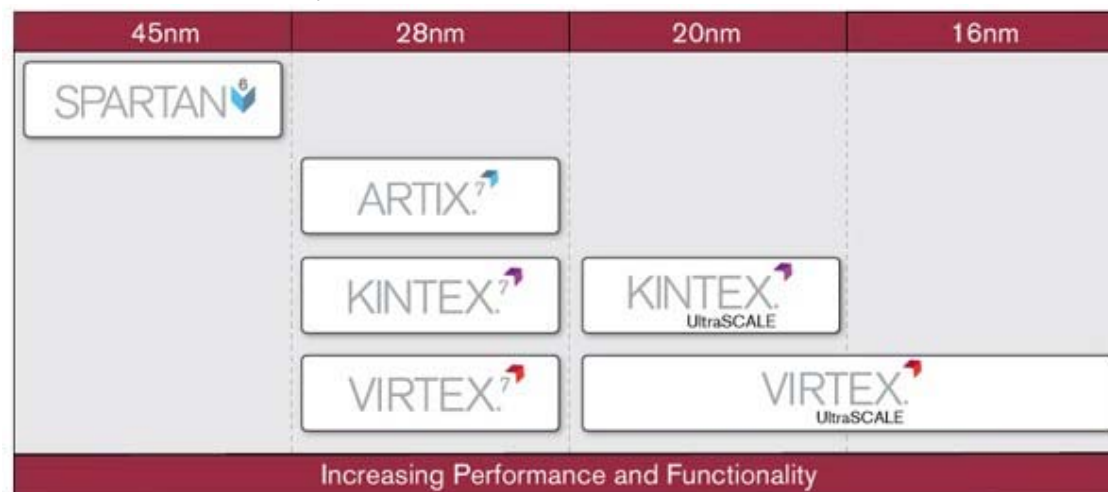


常用FPGA产品

■ ALTERA公司



■ XILINX公司

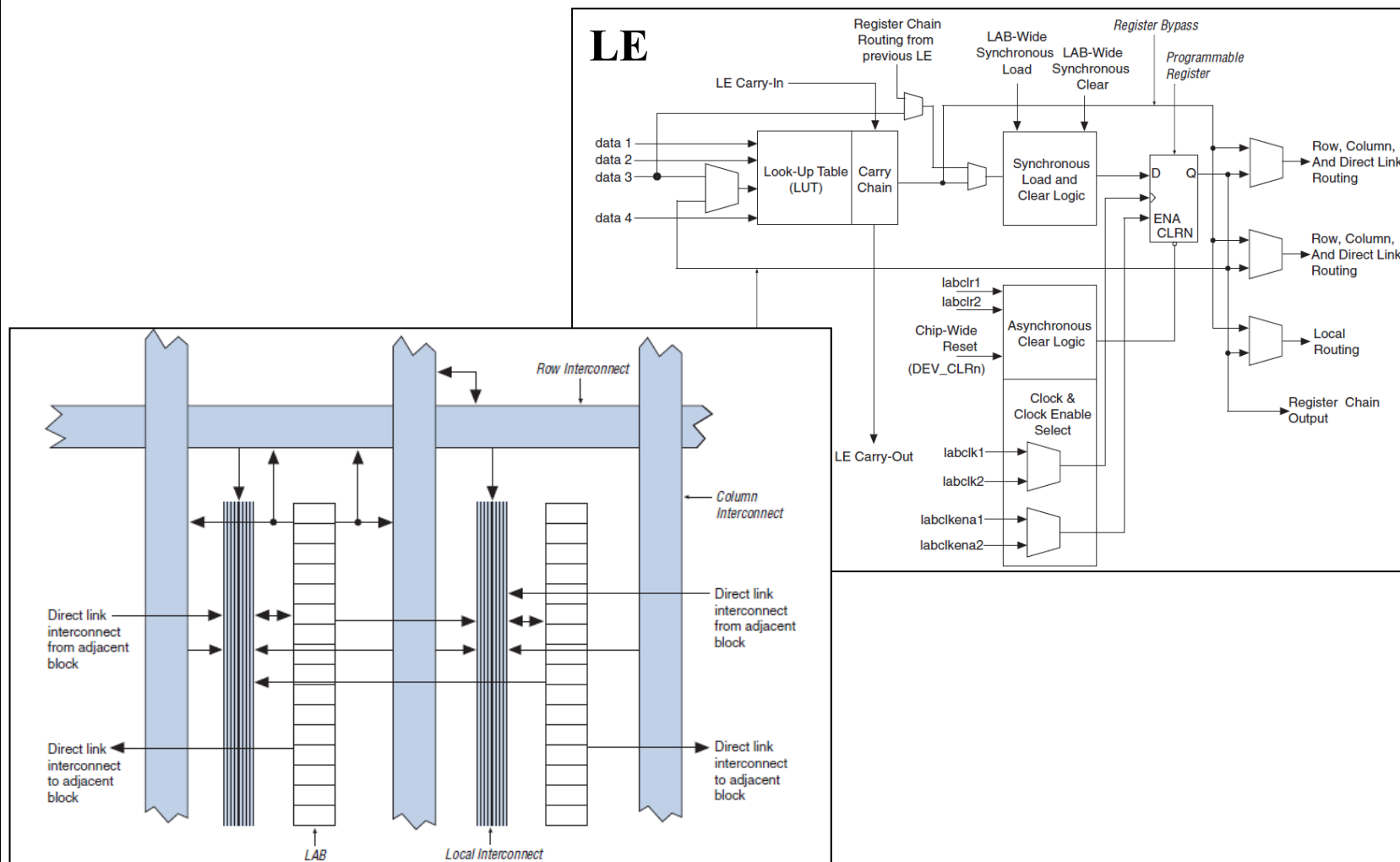


■ LATTICE公司



FPGA简介—CycloneII系列内部结构

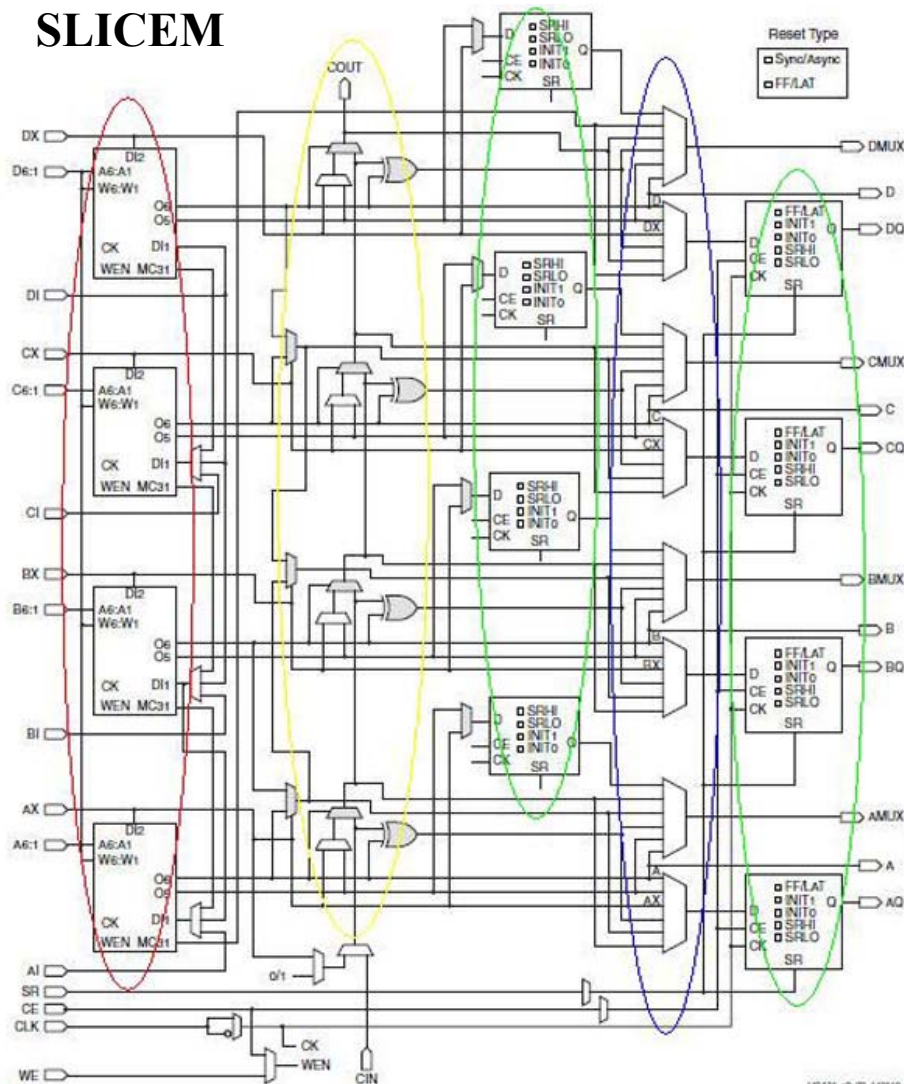
数字系统课程设计





FPGA简介—Kintex-7系列内部结构

SLICEM



- CLB构成了Kintex7主要逻辑单元，其中包含2个Slice，并且 Slice 分为 2 种：SLICEL和SLICEM。
- SLICEL为普通的Slice逻辑单元，而SLICEM在基本逻辑功能的基础上可以扩展为分布式RAM或者移位寄存器。
- 在所有Slice资源中，有2/3是SLICEL，因此一个CLB可以有2个SLICEL或者1个SLICEL、1个SLICEM组成。





FPGA与CPLD的区别

- 简单地说，FPGA就是将CPLD的电路规模，功能，性能等方面强化之后的产物。

- ◆ **PLD : Programmable Logic Device**（可编程逻辑器件）

- 可反复编程的逻辑器件
- 用户可自行设计与实现
- 可即时进行设计与产品规格上的变更
- 可以以标准零件的形式购买





FPGA与CPLD的区别

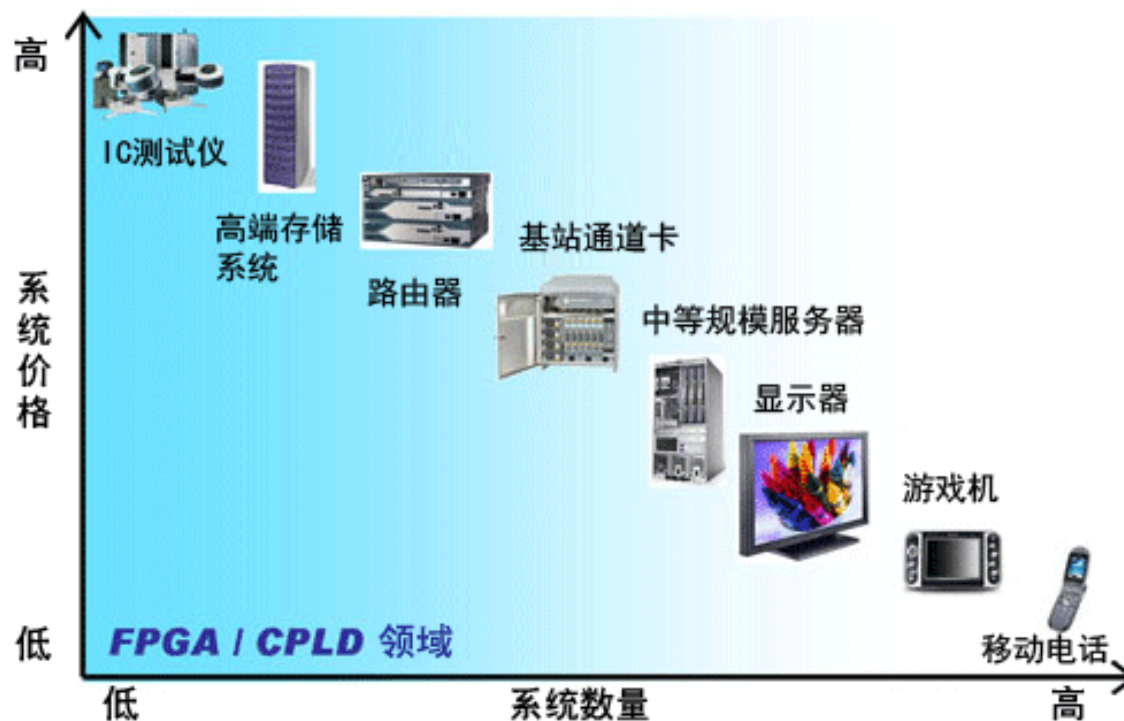
	CPLD	FPGA
组合逻辑的实现方法	乘积项 (product-term), 查找表 (LUT, Look up table)	查找表 (LUT, look up table)
编程元素	非易失性 (Flash, EEPROM)	易失性 (SRAM)
特点	<ul style="list-style-type: none">•非易失性: 即使切断电源, 电路上的数据也不会丢失•立即上电: 上电后立即开始运作•可在单芯片上运作	<ul style="list-style-type: none">•内建高性能硬宏功能<ul style="list-style-type: none">○ PLL○ 存储器模块○ DSP 模块•用最先进的技术实现高集成度, 高性能•需要外部配置ROM
应用范围	偏向于简单的控制通道应用以及胶合逻辑	偏向于较复杂且高速的控制通道应用以及数据处理
集成度	小~中规模	中~大规模





FPGA的应用

- 如下图所示，FPGA被广泛地使用在通讯基站、大型路由器等高端网络设备，以及显示器(电视)、投影仪等日常家用电器里。





FPGA的优势

- **FPGA**最大的优势特点就是能够缩短开发所需时间。换句话说，通过使用**FPGA**，设计人员可以有效地利用每一分钟进行开发。例如，在开发过程中使用**FPGA**与否，可以导致开发时间上 $1/2 \sim 1/3$ 的差别。这使得**FPGA**成为实现“少量多品种”以及“产品周期短”市场不可缺少的器件之一。





FPGA的优势

工程师



- 迅速应用最新的协议与规格
- 可以在产品开发的任何阶段修改设计
- 开发人员可以调用丰富的IP，集中精力在开发创新技术上
- 应用众多可靠的功能，从而缩短设计时间
- 降低功耗以及空间占用量
- 通过使用各种自动化工具，使时序分析等复杂的设计验证更准确，更容易

开发部门负责人



- 缩短开发周期
- 消除了器件停产所带来的风险
- 通过丰富的IP与自动化工具，可以将开发资源集中在不同的产品线上
- 迅速应用最新的协议与规格
- 更有效率的工程师培训
- 可以重新使用设计资源，降低开发成本并且提高设计质量

管理层



- 降低开发成本
 - ✓ 不需要NRE（Non-recurring Expense：非经常性费用，开发初期所需费用）
 - ✓ 避免因重新制作所造成的NRE负担
 - ✓ 开发周期的短缩，从而降低劳动力成本
- 降低风险
 - ✓ 不存在产品停产所带来的风险
 - ✓ 众多可靠的功能
- 迅速使产品投入市场
- 针对竞争产品实施差异化战略





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数字系统设计基础知识

- 组合逻辑 & 时序逻辑
- 建立时间 & 保持时间
- 触发器 & 锁存器
- 资源共享
- 流水线设计





组合逻辑(Combinational Logic)

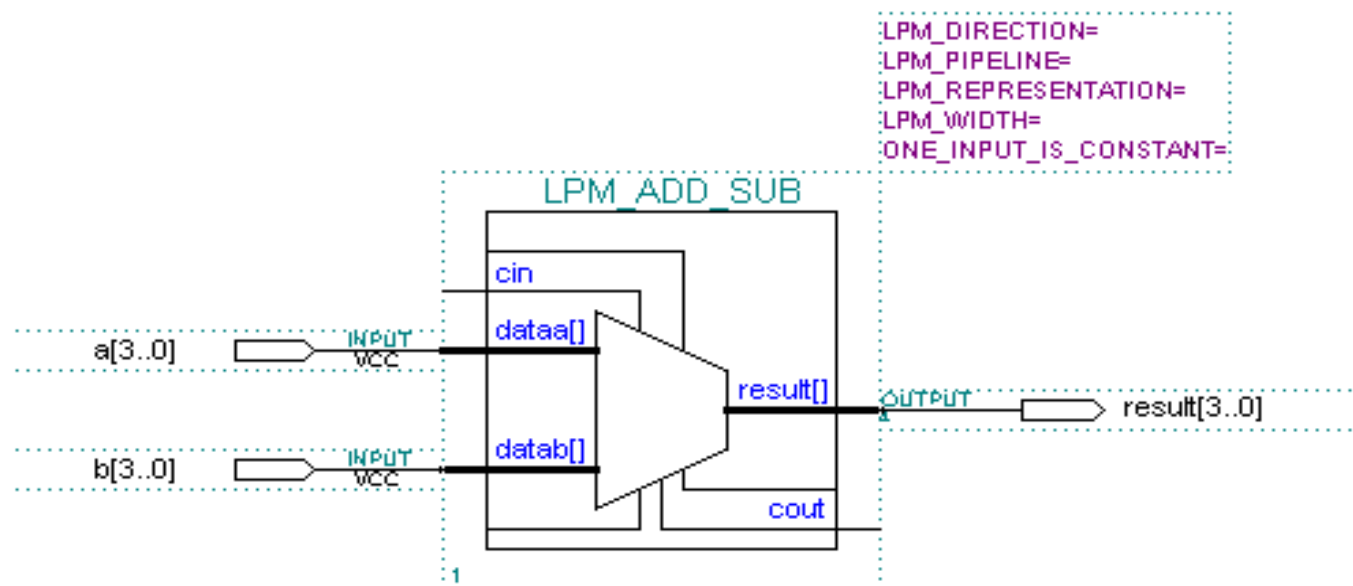
- 某一时刻的输出只和**此刻**的输入有关系
比如：译码器、加法器、数据选择器等等





组合逻辑(Combinational Logic)

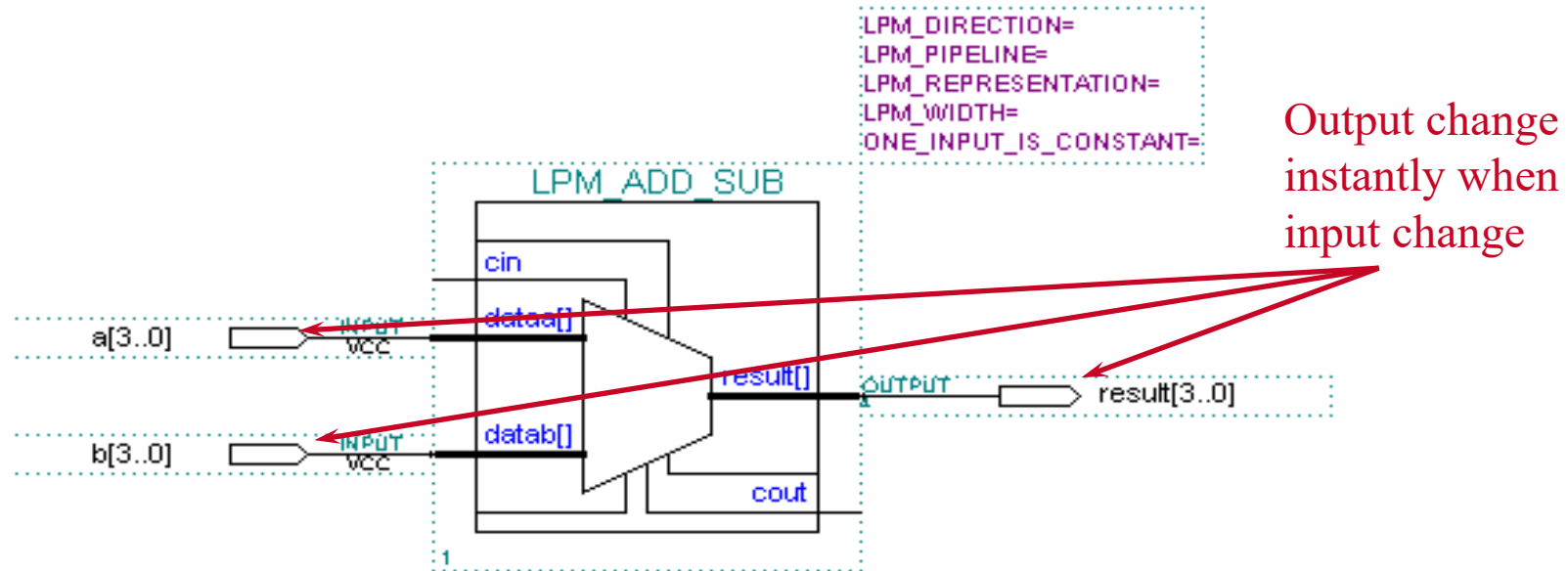
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时序逻辑(Sequential Logic)

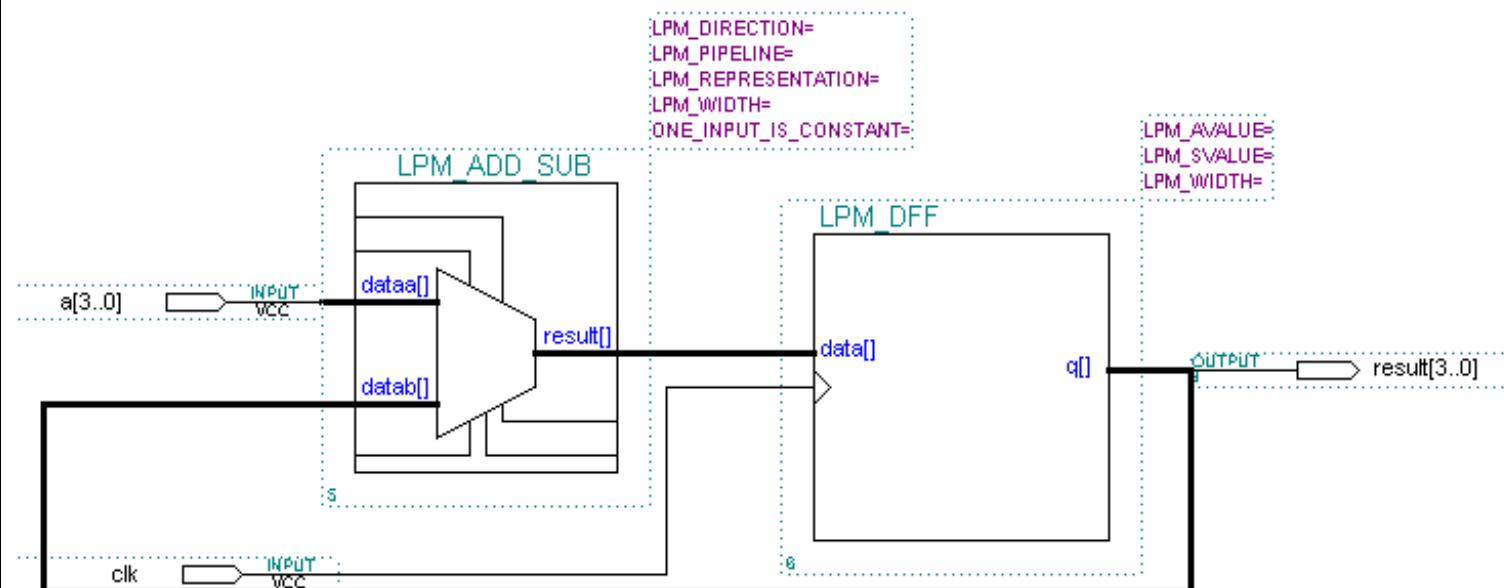
- 某一时刻的输出和当时以及以前的时刻都有关系
- 所有的时序电路都必须包含一个或多个寄存器
比如：状态机、计数器、移位寄存器、控制器





时序逻辑(Sequential Logic)

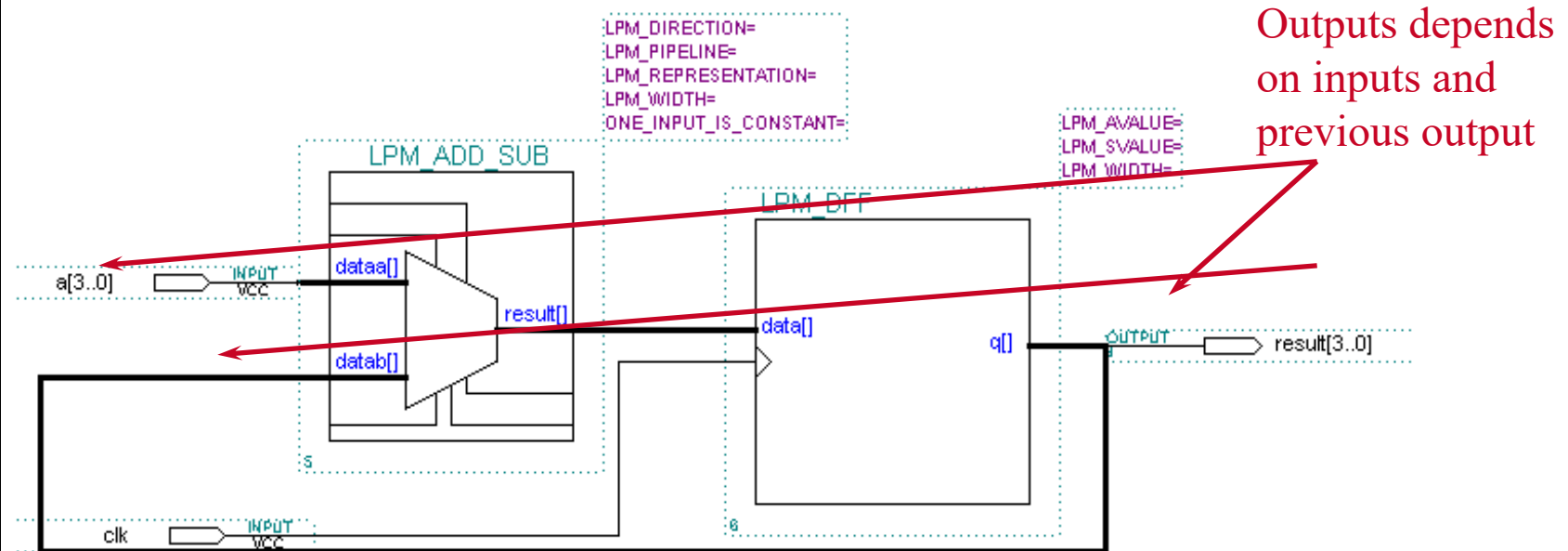
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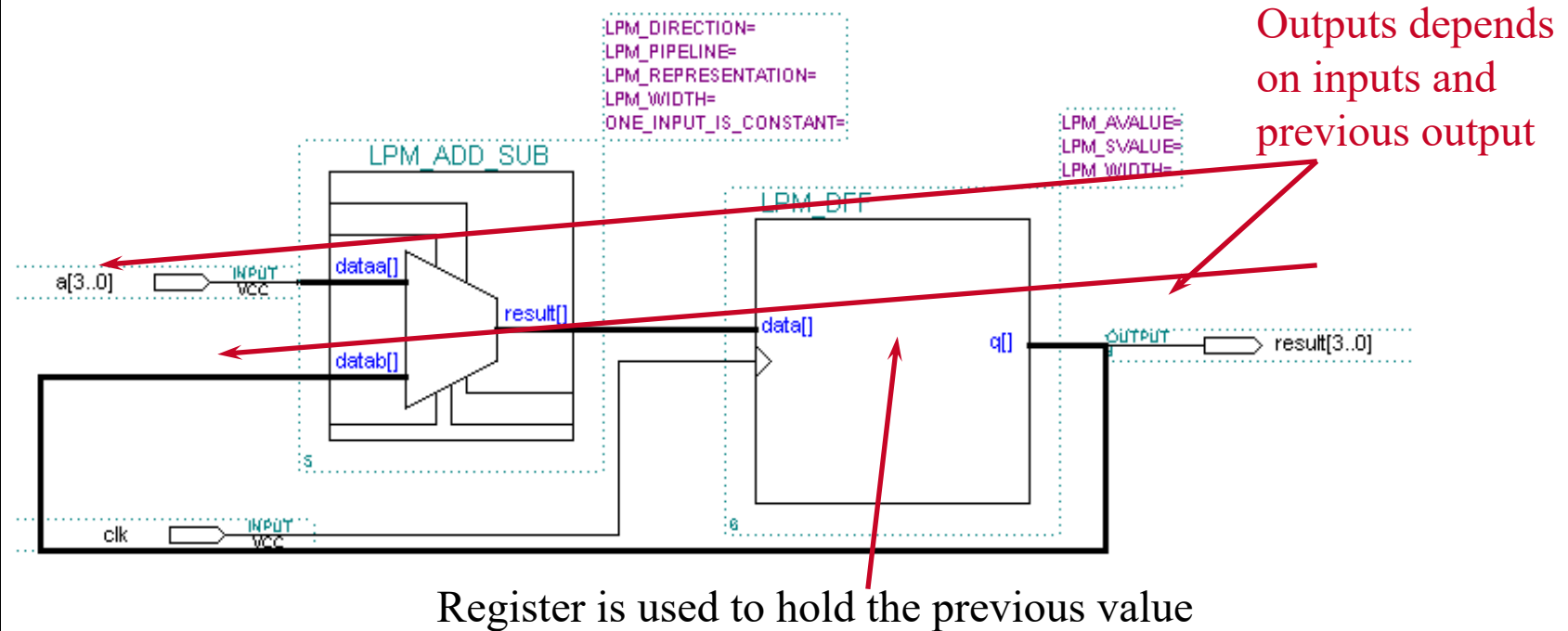
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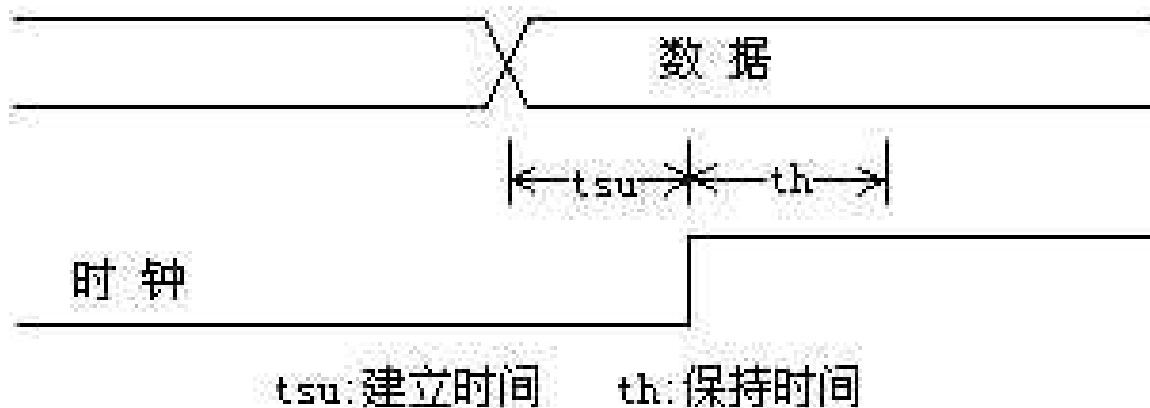
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建立时间 & 保持时间

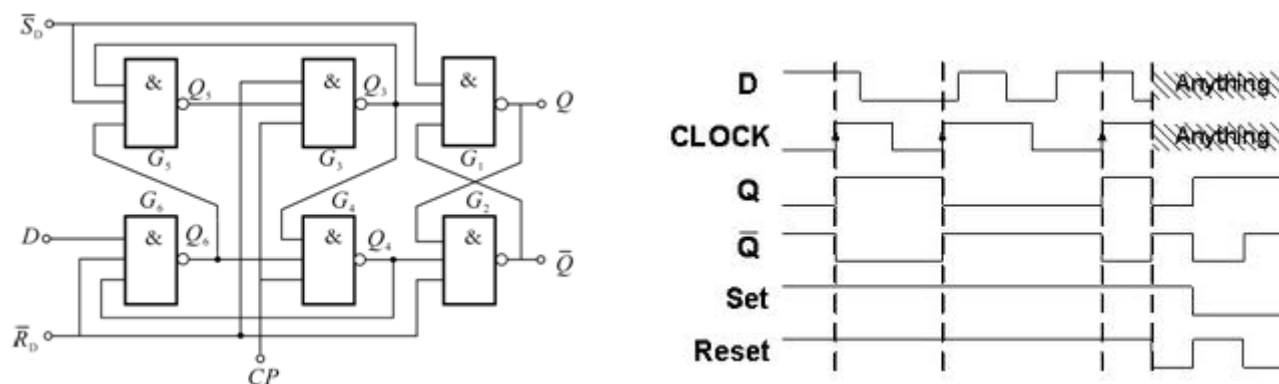
- 建立时间 (setup time) 是指在触发器的时钟信号上升沿到来以前, 数据稳定不变的时间, 如果建立时间不够, 数据将不能在这个时钟上升沿被打入触发器。
- 保持时间 (hold time) 是指在触发器的时钟信号上升沿到来以后, 数据稳定不变的时间, 如果保持时间不够, 数据同样不能被打入触发器。
- 数据稳定传输必须满足建立和保持时间的要求。



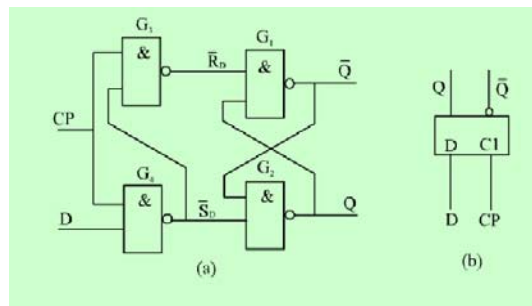


触发器 & 锁存器

- 触发器是在时钟边沿进行数据的锁存的，而触发器的Q输出端在每一个时钟边沿被更新。



- 锁存器是用电平使能来锁存数据的，锁存器在使能电平有效期间才会被更新。





资源共享

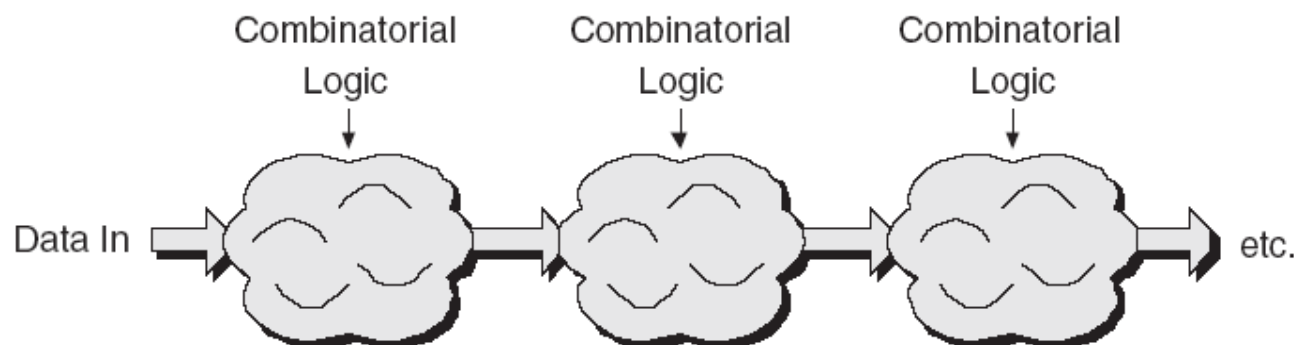
- 资源共享是一种优化技术，该技术使得可以使用单个功能模块（比如说一个加法器或一个比较器）来实现一系列操作。比如说，一个乘法器可能先处理两个值A和B，然后同样是这个乘法器，再来处理C和D。资源共享的典型应用是时分复用（Time-Division Multiplexing—TDM）。





流水线设计 (Pipeline)

- 假设我们要设计的电路或电路的一部分可以由一些组合逻辑块串联实现，如图表示。
- 假设每个组合逻辑块需要使用N纳秒来实现其功能，而我们假设现在有3个这样的组合逻辑块，那么从数据进入第一个块到最后输出，共花费 $3 \times N$ 纳秒的时间。





流水线设计 (Pipeline)

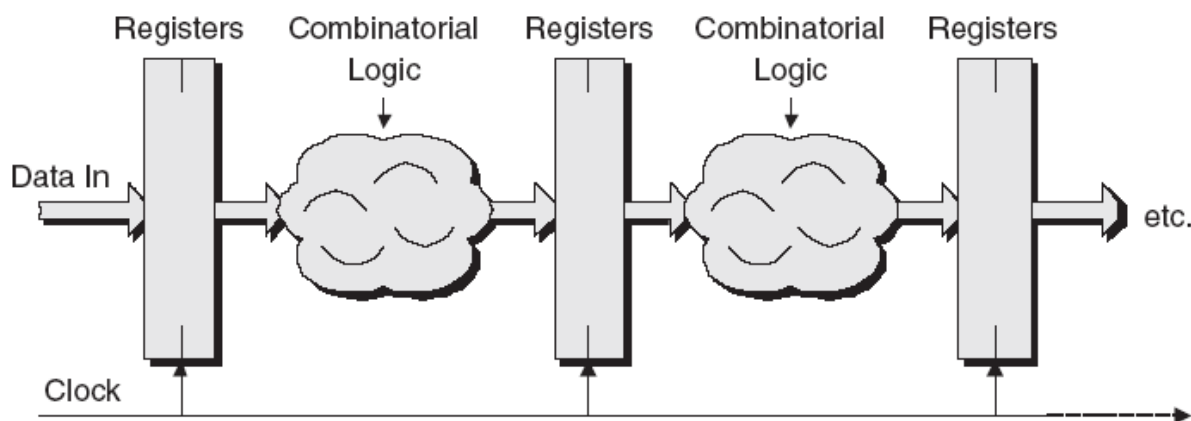
- 通常情况下，组合电路中，在我们得到有效的输出数据之前，无法输入新的数据。这样带来的结果是每个组合逻辑块在一次数据处理过程中（ $3 \times N$ 纳秒）只有 N 纳秒在有效工作。那么如何每个块都充分的利用起来呢？答案就是使用流水线操作技术，将逻辑块与块之间用寄存器进行隔离，以提高效率和速度。





流水线设计 (Pipeline)

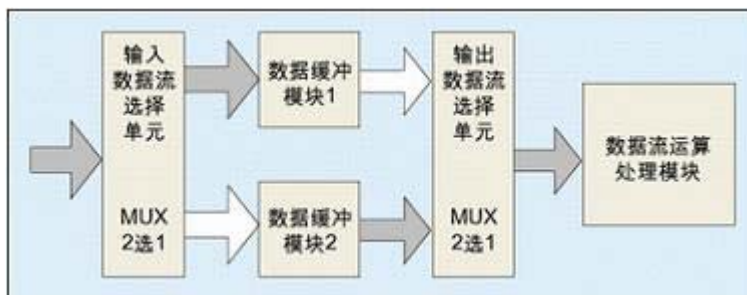
- 所有寄存器使用共同的时钟信号，在每一个有效的时钟边沿时刻，寄存器的值都要更新一次，更新的值是该寄存器前一级的组合电路的输出。于是这些值被逐级传输直到输出。在这种情况下，一旦“水泵中的水被抽满”，流水线饱和运作，处理一个数据的时间将变为 N 纳秒。





乒乓操作

- 在第一个缓冲周期，将输入的数据流缓存到“数据缓冲模块1”；在第2个缓冲周期，通过“输入数据选择单元”的切换，将输入的数据流缓存到“数据缓冲模块2”，同时将“数据缓冲模块1”缓存的第1个周期数据通过“输出数据选择单元”的选择，送到“数据流运算处理模块”进行运算处理；在第3个缓冲周期通过“输入数据选择单元”的再次切换，将输入的数据流缓存到“数据缓冲模块1”，同时将“数据缓冲模块2”缓存的第2个周期的数据通过“输出数据选择单元”切换，送到“数据流运算处理模块”进行运算处理。如此循环。





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硬件描述语言（HDL）

■ HDL（Hardware Description Language）

■ Verilog

- Verilog是由Gateway设计自动化公司的工程师于1983年末创立的。
- Verilog成为了IEEE 1364-1995标准，即通常所说的Verilog-95。
- Verilog-2001是对Verilog-95的一个重大改进版本，目前是Verilog的最主流版本，被大多数商业电子设计自动化软件包支持。
- Verilog与C语言在语法上有相似之处，因此具有C语言基础的设计人员更容易掌握它

■ Verilog与VHDL比较

- VHDL的设计之初就更加针对标准化进行设计，Verilog则具有简明、高效的代码风格
- Verilog的逻辑门级、开关级电路描述能力更强，VHDL的系统级抽象描述能力则比Verilog强。





VHDL简介

■ Very high speed integrated circuit Hardware

Description Language

- 1987底,VHDL被IEEE和美国国防部确认为标准硬件描述语言。此后VHDL在电子设计领域得到了广泛的接受,并逐步取代了原有的非标准的硬件描述语言。现在,VHDL和Verilog作为IEEE的工业标准硬件描述语言,又得到众多EDA公司的支持,在电子工程领域,已成为事实上的通用硬件描述语言。





VHDL简介

- VHDL主要用于描述数字系统的结构、行为、功能和接口。
- VHDL具有强大的行为描述能力，是系统设计领域最佳的硬件描述语言。强大的行为描述能力是避开具体的器件结构,从逻辑行为上描述和设计大规模电子系统的重要保证。
- VHDL对设计的描述具有相对独立性，工程师可以不懂硬件的结构，也不必管最终设计实现的目标器件是什么，而进行独立的设计。





HDL的可综合性问题

- HDL有两种用途:系统仿真和硬件实现。如果程序只用于仿真,那么几乎所有的语法都可以使用。但如果程序是用于硬件实现(例如:用于FPGA实现),必须保证程序是可综合的,即程序的功能可以用硬件电路实现。不可综合的HDL语句在软件综合时将被忽略或者报错。
- 所有的HDL描述都可以用于仿真,但不是所有的HDL描述都能用硬件实现。





用硬件电路设计思想来编写HDL

- 学好HDL的关键是充分理解HDL语句和硬件电路的关系。编写HDL，就是在描述一个电路，写完一段程序以后，应当对生成的电路有一些大体上的了解，而不能用纯软件的设计思路来编写硬件描述语言。





VHDL基本结构

- 库 (LIBRARY)
用来存储可编译的设计单元
- 实体 (ENTITY)
描述设计模块的输入输出端口类型
- 结构体 (ARCHITECTURE)
描述电路的具体功能





VHDL基本结构一库

- 库调用语句放在程序的最前面，最常用的库调用语句为：

```
LIBRARY IEEE;
```

```
USE IEEE.STD_LOGIC_1164.ALL;
```

```
USE IEEE.STD_LOGIC_UNSIGNED.ALL;
```





VHDL基本结构—实体

- 实体定义设计的全部输入输出信号.
格式如下:

ENTITY 实体名 IS

PORT

(输入输出信号列表);

END 实体名;





VHDL基本结构—实体

■ 一个计数器的实体部分

```
ENTITY count_m16 IS
PORT(
reset : IN    std_logic;
clk   : IN    std_logic;
co    : OUT   std_logic;
count : BUFFER std_logic_vector(3 DOWNT0 0));
END count_m16;
```





VHDL基本结构—实体

■ 端口模式

1. IN 输入信号，不能给输入端口赋值
2. OUT 输出信号，不能在内部反馈使用
3. INOUT 双向信号
4. BUFFER 输出信号，可在内部反馈

■ 数据类型

`std_logic` : 0(0), 1(1), Z(高阻态), X(不定态).

`std_logic_vector` : `std_logic` 的矢量形式





VHDL基本结构—结构体

- 结构体描述实体的结构或行为，格式为：

ARCHITECTURE 结构体名 OF 实体名 IS

定义语句 { 内部信号、常数、数据类型、函数 }

BEGIN

并行处理语句;

进程语句(PROCESS);

END 结构体名;





VHDL基本结构—结构体

■ 上述计数器的结构体部分

```
ARCHITECTURE behave OF count_m16 IS
BEGIN
    PROCESS (clk)
    BEGIN
        IF (clk'event and clk='1')THEN
            IF (reset='1')THEN count<="0000";co<='0';
                ELSIF (count="1111")THEN
                    count<="0000";co<='1';
                ELSE count<=count+1; co<='0';
            END IF;
        END IF;
    END PROCESS;
END behave;
```





VHDL基本结构—结构体

■ 一个加法器结构体的例子

```
ARCHITECTURE behave OF adder8 IS  
BEGIN  
    SUM1<=ADD_A+ADD_B;  
    SUM2<=ADD_C+ADD_D;  
    SUM3<=ADD_E+ADD_F;  
END behave;
```



VHDL基本结构—结构体—数据对象

- 常量—在设计描述中保持特定值不变。
CONSTANT 常数名:数据类型:=表达式;
CONSTANT width : integer:=8;
- 信号—声明内部信号，在元件间起互连作用。
SIGNAL 信号名:数据类型;
SIGNAL a:std_logic_vector(3 downto 0);
- 变量—用于声明进程或子程序中的局部值;
VARIABLE 变量名:数据类型;
VARIABLE a : std_logic;





VHDL基本结构—结构体-信号vs变量

- 信号是全局量,常在结构体中声明:

```
ARCHITECTURE behave OF Entity_Name IS  
SIGNAL sig_temp: std_logic;
```

- 变量是局部量, 常在进程中声明:

```
ARCHITECTURE behave OF Entity_Name IS  
BEGIN  
PROCESS (...)  
VARIABLE var_temp: std_logic;
```





VHDL基本结构—结构体-信号vs变量

- 信号赋值的符号为 “<=

如： SIG_temp <= '1' ;

- 变量赋值的符号为 “:=

如： VAR_temp := '1' ;





VHDL基本结构—结构体-信号vs变量

- 在进程中，信号赋值在进程结束时更新。如果一个进程中多次对同一个信号赋值，最后一个赋值有效。

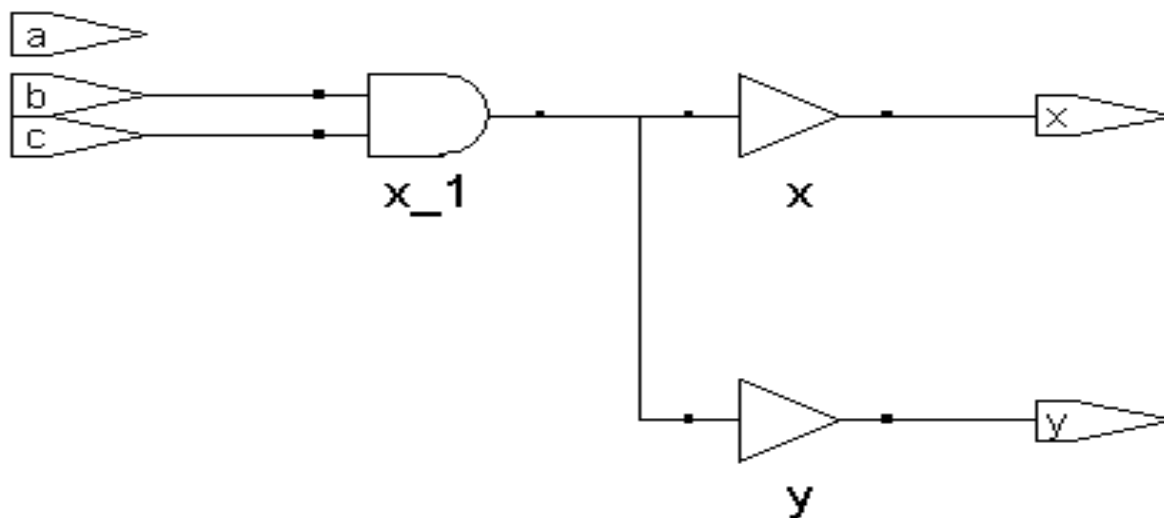
```
SIGNAL d: std_logic;  
PROCESS (a, b, c)  
BEGIN  
  d<=a;      ——此赋值被忽略  
  x<=c and d;  
  d<=b;      ——此赋值有效  
  y<=c and d;  
END PROCESS;
```





VHDL基本结构—结构体-信号vs变量

- 执行结果 $x \leq c \text{ and } b$; $y \leq c \text{ and } b$ 。
- 以下是综合器的综合结果。





VHDL基本结构—结构体-信号vs变量

- 在进程中，变量赋值立即生效，没有延时。

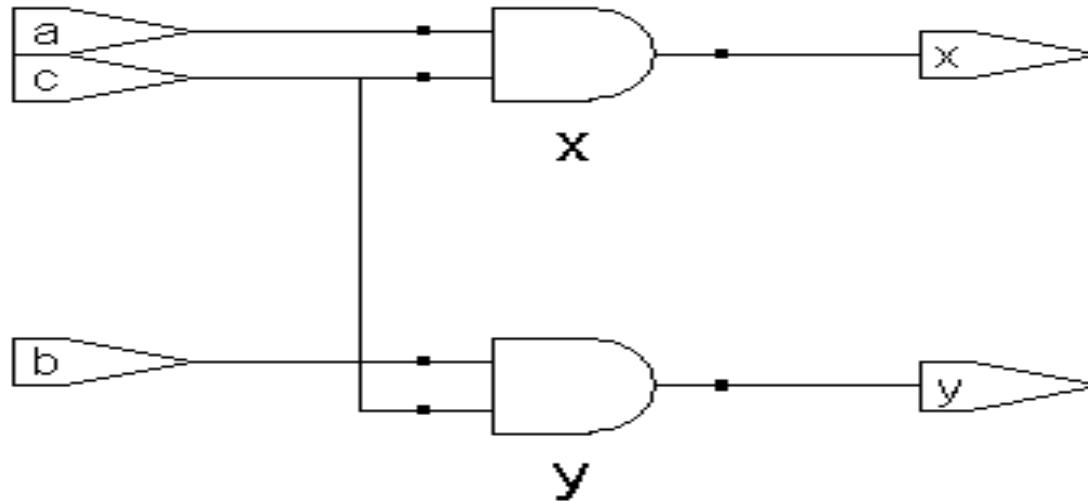
```
PROCESS (a, b, c )  
VARIABLE d: std_logic;  
BEGIN  
  d:=a;  
  x<=c and d;  
  d:=b;  
  y<=c and d;  
END PROCESS;
```





VHDL基本结构—结构体-信号vs变量

- 执行结果 $x \leq c \text{ and } a$; $y \leq c \text{ and } b$ 。
- 以下是综合器的综合结果





VHDL描述方法

- 并发语句(Concurrent Statement)
 - 简单赋值语句
 - 条件赋值语句
 - 选择信号赋值语句

- 顺序语句(Sequential Statement)
 - IF 语句
 - CASE 语句

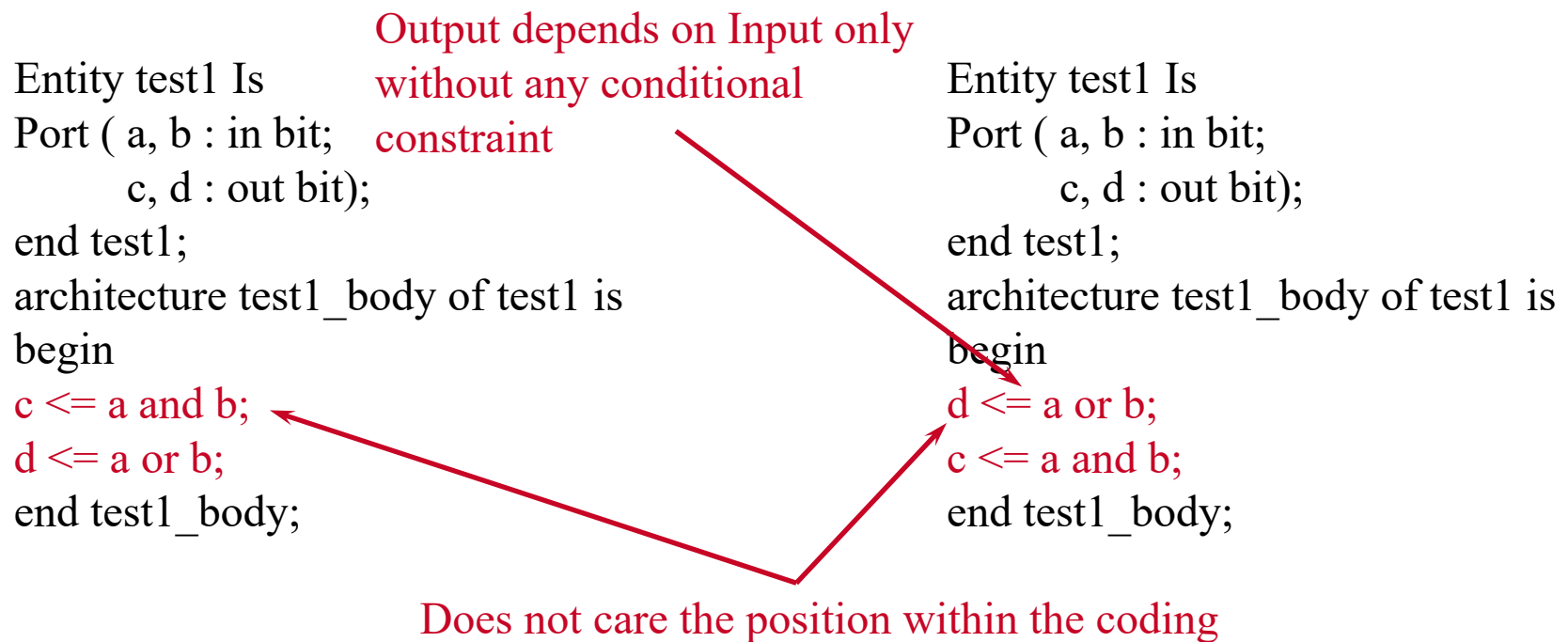
- 进程语句(Process Statement)





并发语句

- 所有的并发语句都是并行执行
- 并发语句不关心在程序中的位置
- 并发语句的输出依赖于输入





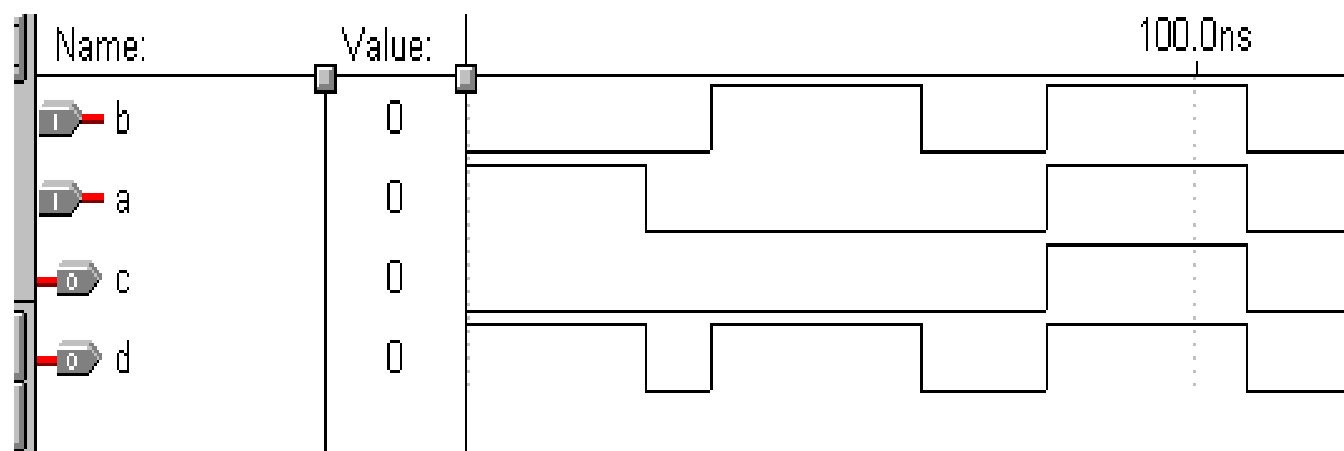
并发语句

$c \leq a \text{ and } b;$
 $d \leq a \text{ or } b;$

$d \leq a \text{ or } b;$
 $c \leq a \text{ and } b;$

$C = A \text{ and } B$

$D = A \text{ OR } B$





并发语句

■ 简单赋值语句

赋值目标 \leq 表达式;

.....

赋值目标 \leq 表达式;

如 $c \leq a + b$;

$c \leq a$ and b ;

$c \leq a$;





并发语句

■ 条件赋值语句

目标 <= 表达式 WHEN 赋值条件 ELSE
表达式 WHEN 赋值条件 ELSE
.....
表达式;

如: y <= a0 WHEN s="00" ELSE
a1 WHEN s="01" ELSE
a2 WHEN s="10" ELSE
a3;





并发语句

■ 选择信号赋值语句

WITH 选择表达式 SELECT
赋值目标信号 <= 表达式 WHEN 选择值,
.....
表达式 WHEN 选择值;

如: WITH s SELECT
y<= a0 WHEN “00”,
a1 WHEN “01”,
a2 WHEN “10”,
a3 WHEN OTHERS;





顺序语句

■ IF语句

```
PROCESS (s, a0, a1, a2, a3 )  
BEGIN  
    IF s="00" THEN y<=a0;  
    ELSIF s="01" THEN y<=a1;  
    ELSIF s="10" THEN y<=a2;  
    ELSE y<=a3;  
    END IF;  
END PROCESS;
```




顺序语句

■ CASE语句

```
PROCESS (s, a0, a1, a2, a3 )  
BEGIN  
    CASE s IS  
        WHEN "00"  => y<=a0;  
        WHEN "01"  => y<=a1;  
        WHEN "10"  => y<=a2;  
        WHEN others=> y<=a3;  
    END CASE;  
END PROCESS;
```





进程语句

- 进程语句由一段程序构成，各个进程之间是并行执行的，进程内部是顺序执行的。一个结构体可以包含多个进程语句。
- PROCESS 必须要有敏感信号表（SENTIVITY LIST），敏感表中的信号变化导致进程触发。

PROCESS (敏感信号表)

[声明区];--此处声明局部变量等.

BEGIN --进程开始

[顺序语句];

END PROCESS;--进程结束





进程语句 (EXAMPLE 1)

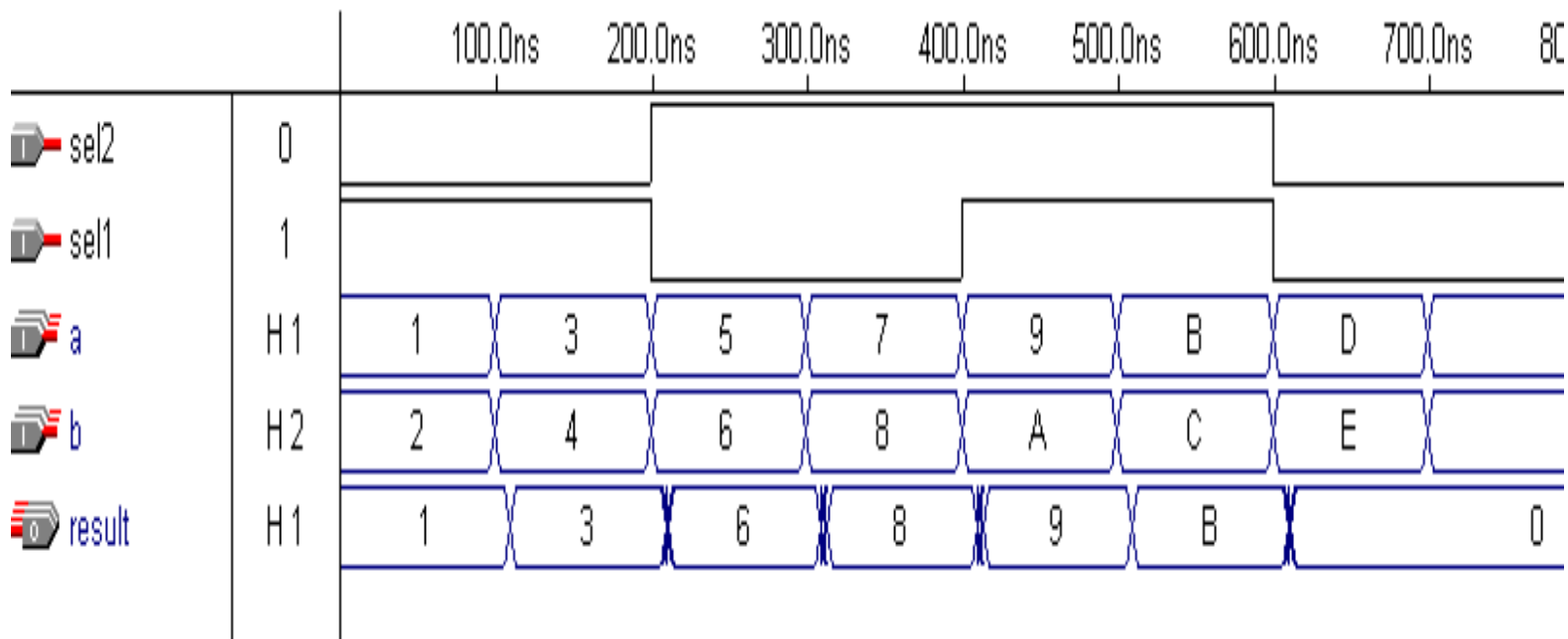
```
entity test is
  port(a,b      : in std_logic_vector(3 downto 0);
        sel1,sel2: in std_logic;
        result: out std_logic_vector(3 downto 0));
end test;
```

```
architecture behave of test is
begin
  process(sel1,sel2,a,b)
  begin
    if(sel1='1') then result<=a;
    elsif(sel2='1') then result<=b;
    else result<="0000";
    end if;
  end process;
end behave;
```





进程语句 (EXAMPLE 1)





进程语句 (EXAMPLE 2)

```
■ Entity test1 IS
  PORT ( clk, d1, d2 : in std_logic;
        q1, q2 : out std_logic);
END test1;
```

```
ARCHITECTURE test1_body OF test1 IS
BEGIN
```

```
  PROCESS (clk, d1)
  BEGIN
    IF (clk'event and clk = '1') THEN q1 <= d1; END IF;
  END PROCESS;
```

```
  PROCESS (clk, d2)
  BEGIN
    IF (clk'event and clk = '1') THEN q2 <= d2; END IF;
  END PROCESS;
```

```
END test1_body;
```





进程语句 (EXAMPLE 2)

- Entity test2 IS

```
PORT ( clk, d1, d2 : in std_logic;  
       q1, q2 : out std_logic);  
END test1;
```

```
ARCHITECTURE test1_body OF test1 IS  
BEGIN
```

```
    PROCESS (clk, d2)  
    BEGIN  
        IF (clk'event and clk = '1') THEN q2 <= d2; END IF;  
    END PROCESS;
```

```
    PROCESS (clk, d1)  
    BEGIN  
        IF (clk'event and clk = '1') THEN q1 <= d1; END IF;  
    END PROCESS;
```

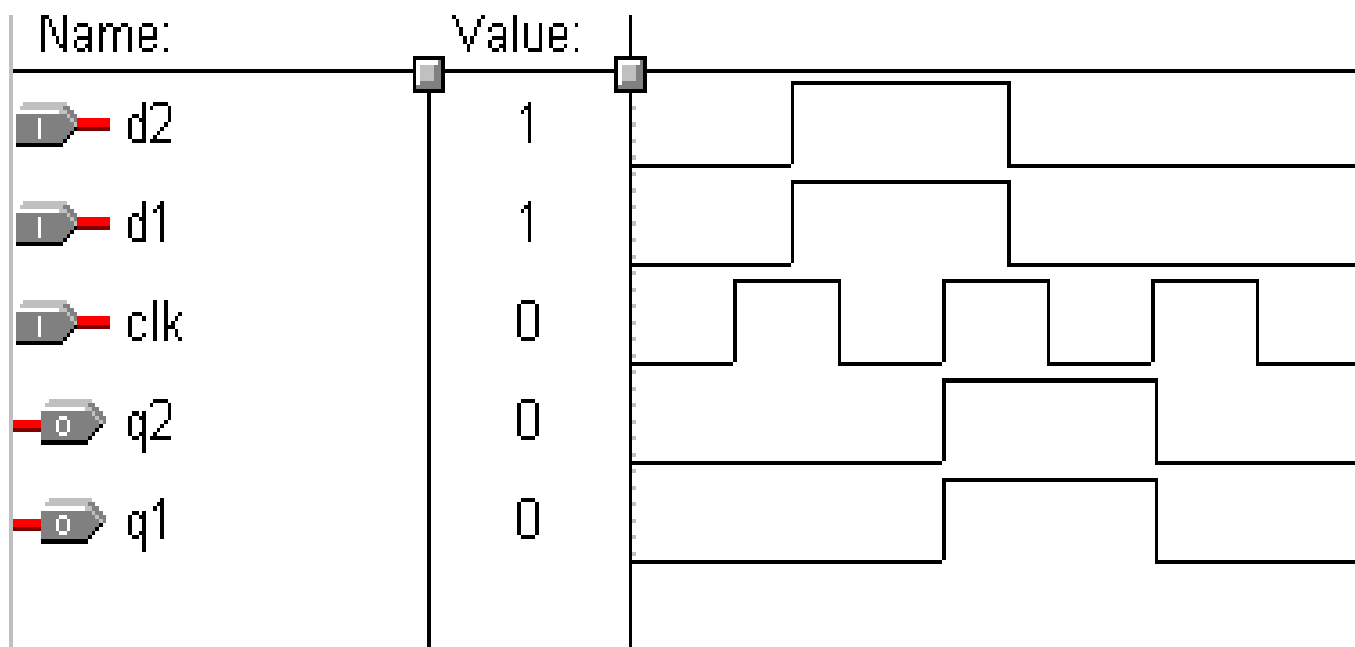
```
END test1_body;
```





进程语句 (EXAMPLE 2)

- 上述两个程序的仿真波形是相同的，如下所示：





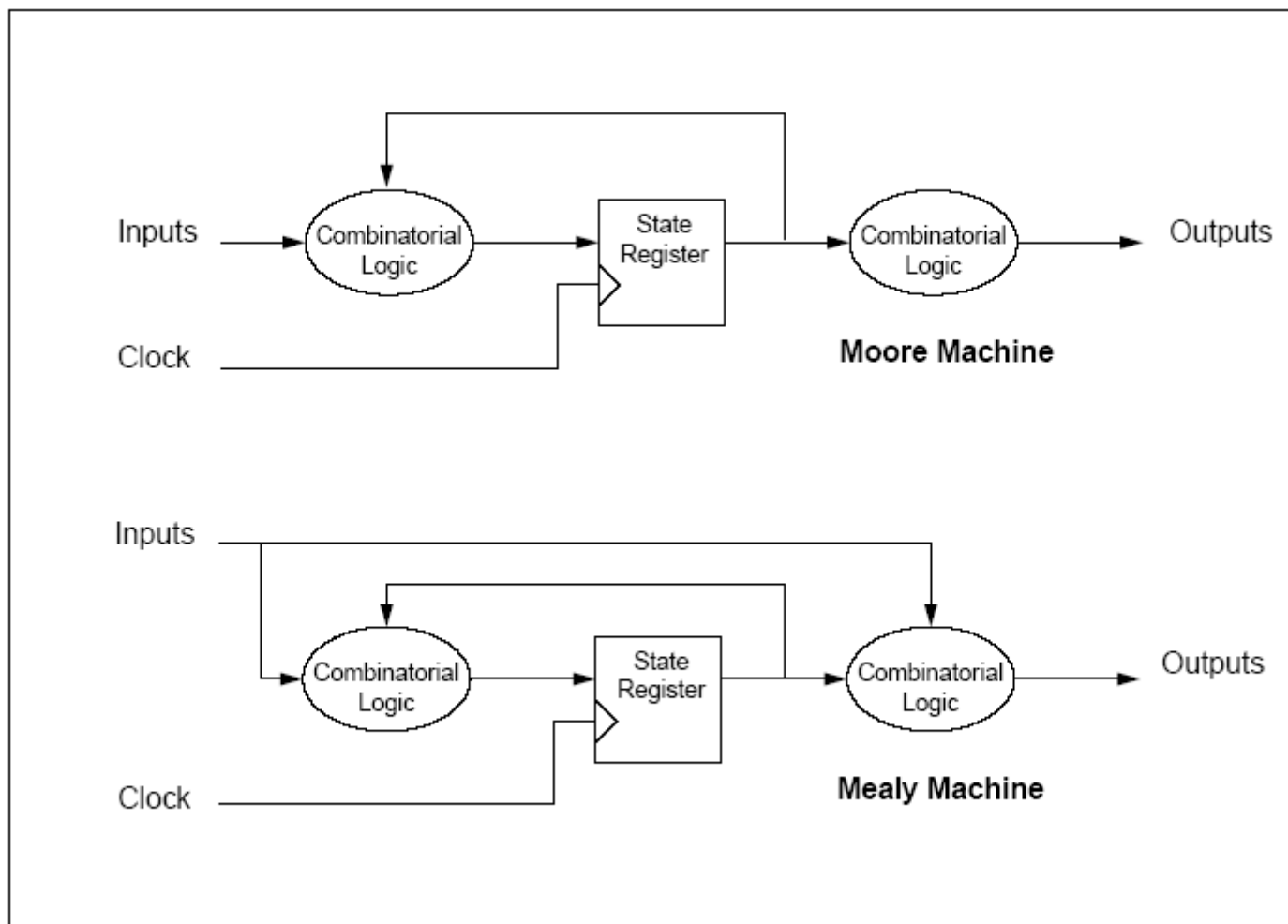
状态机设计

- 状态机是大型电子设计的基础，通常用状态机来实现数字系统的控制器。
- 最基本的两种状态机方式：
 - Moore型
较简单的一种状态机，输出仅是当前状态的函数。
 - Mealy型
输出是当前状态和输入状态的函数。



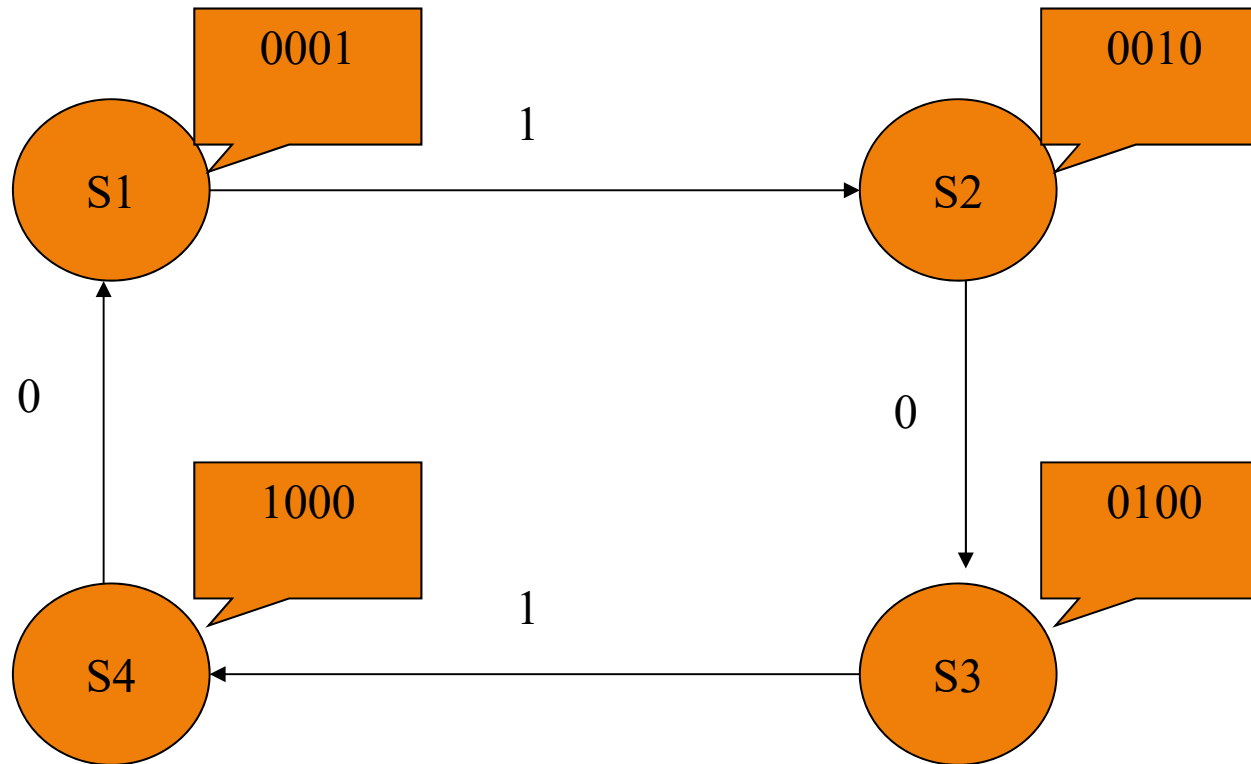


Moore *VS* Mealy





Moore Machine





Moore Machine

```
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE IEEE.std_logic_unsigned.ALL;

ENTITY moore_example IS
PORT
    (clk, datain, reset : IN std_logic;
     dataout: OUT std_logic_vector(3 downto 0));
END moore_example;

ARCHITECTURE behave OF moore_example IS
TYPE state_type IS ( s1,s2,s3,s4);
SIGNAL state: state_type;
BEGIN
```



Moore Machine

```
PROCESS (clk, reset )
```

```
  IF reset='1' THEN state<=s1;
```

```
  ELSIF ( clk'event and clk='1') THEN
```

```
    CASE state IS
```

```
      WHEN s1 => IF datain='1' THEN state<=s2; END IF;
```

```
      WHEN s2 => IF datain='0' THEN state<=s3; END IF;
```

```
      WHEN s3 => IF datain='1' THEN state<=s4; END IF;
```

```
      WHEN s4 => IF datain='0' THEN state<=s1; END IF;
```

```
    END CASE;
```

```
  END IF;
```

```
END PROCESS;
```



Moore Machine

```
PROCESS (state)
```

```
BEGIN
```

```
    CASE state IS
```

```
        WHEN s1 => dataout<="0001";
```

```
        WHEN s2 => dataout<="0010";
```

```
        WHEN s3 => dataout<="0100";
```

```
        WHEN s4 => dataout<="1000";
```

```
    END CASE;
```

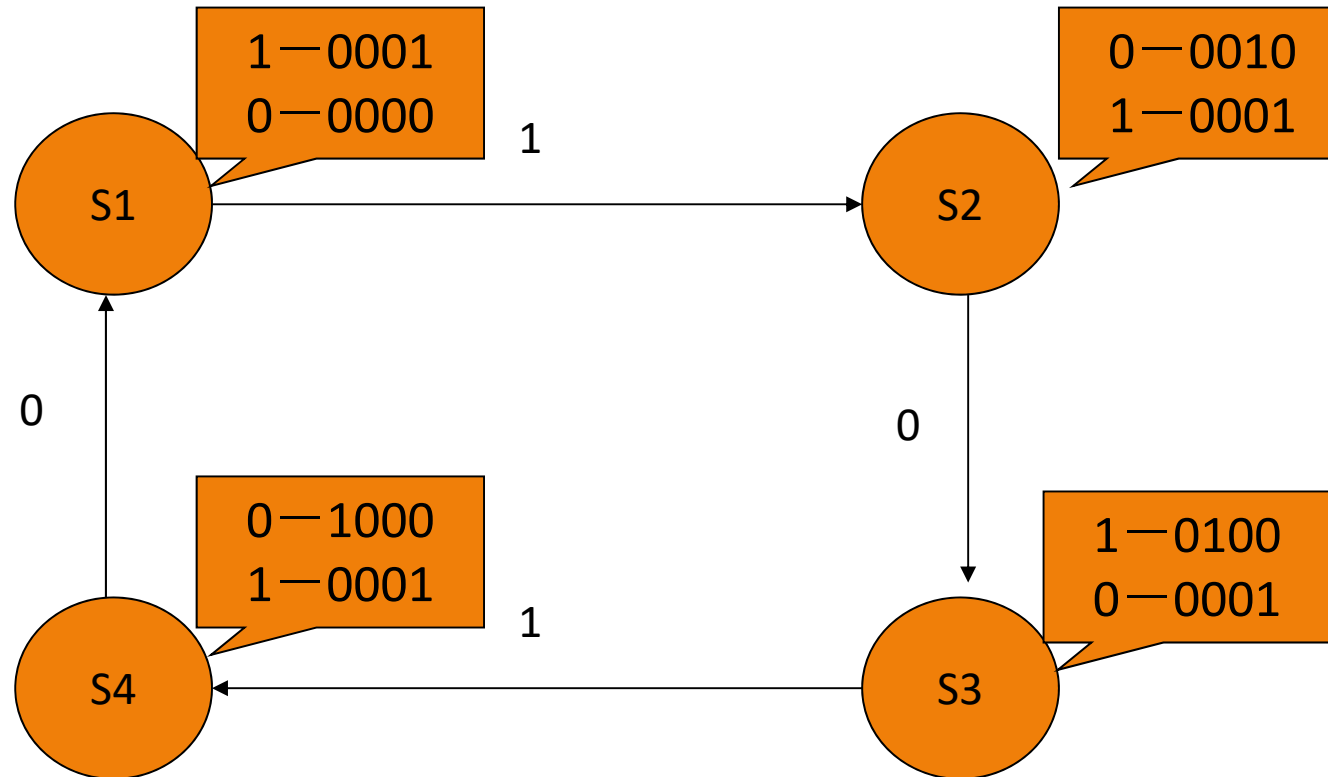
```
END PROCESS;
```

```
END behave;
```





Mealy Machine





Mealy Machine

```
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE IEEE.std_logic_unsigned.ALL;

ENTITY mealy_example IS
PORT
    (clk, datain, reset : IN std_logic;
     dataout: OUT std_logic_vector(3 downto 0));
END mealy_example;

ARCHITECTURE behave OF mealy_example IS
TYPE state_type IS ( s1,s2,s3,s4);
SIGNAL state: state_type;
BEGIN
```



Mealy Machine

```
PROCESS (clk, reset )
IF reset='1' THEN state<=s1;
ELSIF ( clk'event and clk='1') THEN
    CASE state IS
        WHEN s1=>IF datain='1' THEN state<=s2;END IF;
        WHEN s2=>IF datain='0' THEN state<=s3;END IF;
        WHEN s3=>IF datain='1' THEN state<=s4;END IF;
        WHEN s4=>IF datain='0' THEN state<=s1;END IF;
    END CASE;
END IF;
END PROCESS;
```





Mealy Machine

PROCESS (state)

BEGIN

CASE state IS

WHEN s1 => IF datain='1' THEN dataout<="0001";
ELSE dataout<="0000" END IF;

WHEN s2 => IF datain='0' THEN dataout<="0010";
ELSE dataout<="0001"; END IF;

WHEN s3 => IF datain='1' THEN dataout<="0100";
ELSE dataout<="0001"; END IF;

WHEN s4 => IF datain='0' THEN dataout<="1000";
ELSE dataout<="0001"; END IF;

END CASE;

END PROCESS;

END behave;



课程内容

一、CPLD&FPGA

二、数字系统设计基础

三、硬件描述语言VHDL基础

四、XILINX FPGA开发环境

五、课程设计题目与考核要求





Vivado设计套件简介

- ◆ Vivado是Xilinx公司支持7系列，UltraScale及UltraScale+ 系列等更高性能FPGA而设计的开发工具
- ◆ Vivado的算法考虑到不断增长的FPGA容量的情况下，采用新的确定性布局布线和路由算法，对全局数据结构具有相同的视图
- ◆ Vivado中除SDK和Vivado HLS之外的所有工具被集成在用户图形化接口中

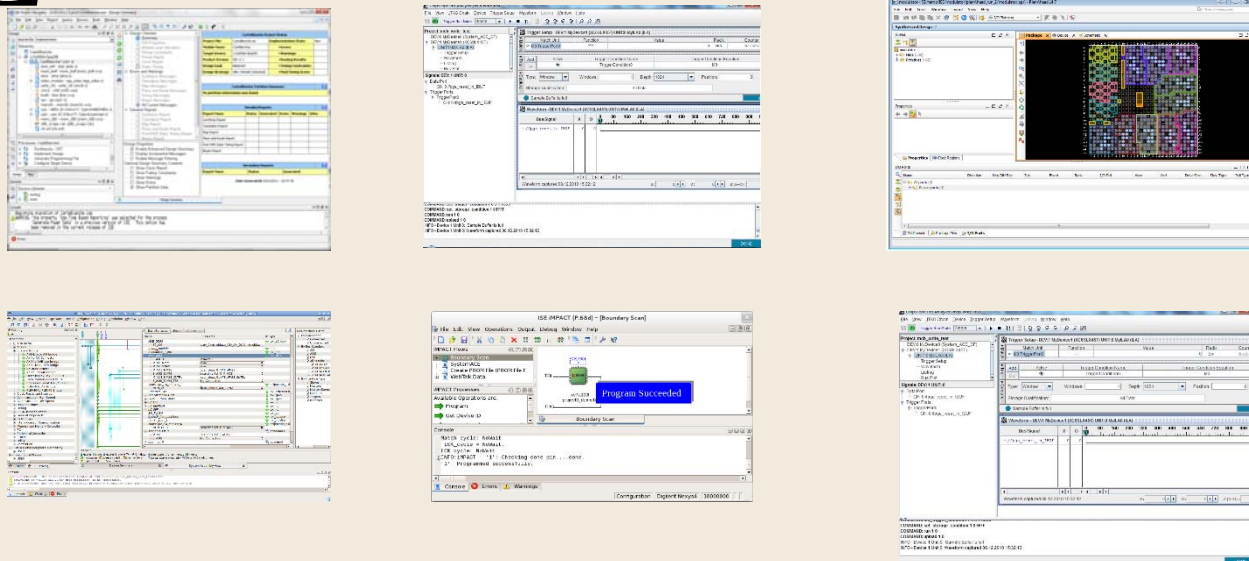




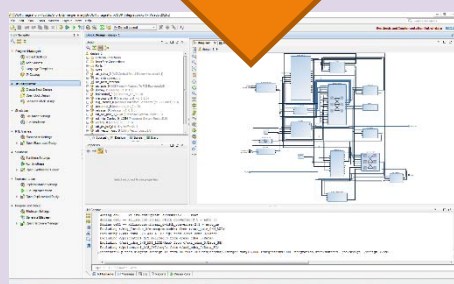
用户集成化的开发环境

数字系统课程设计

ISE



Vivado



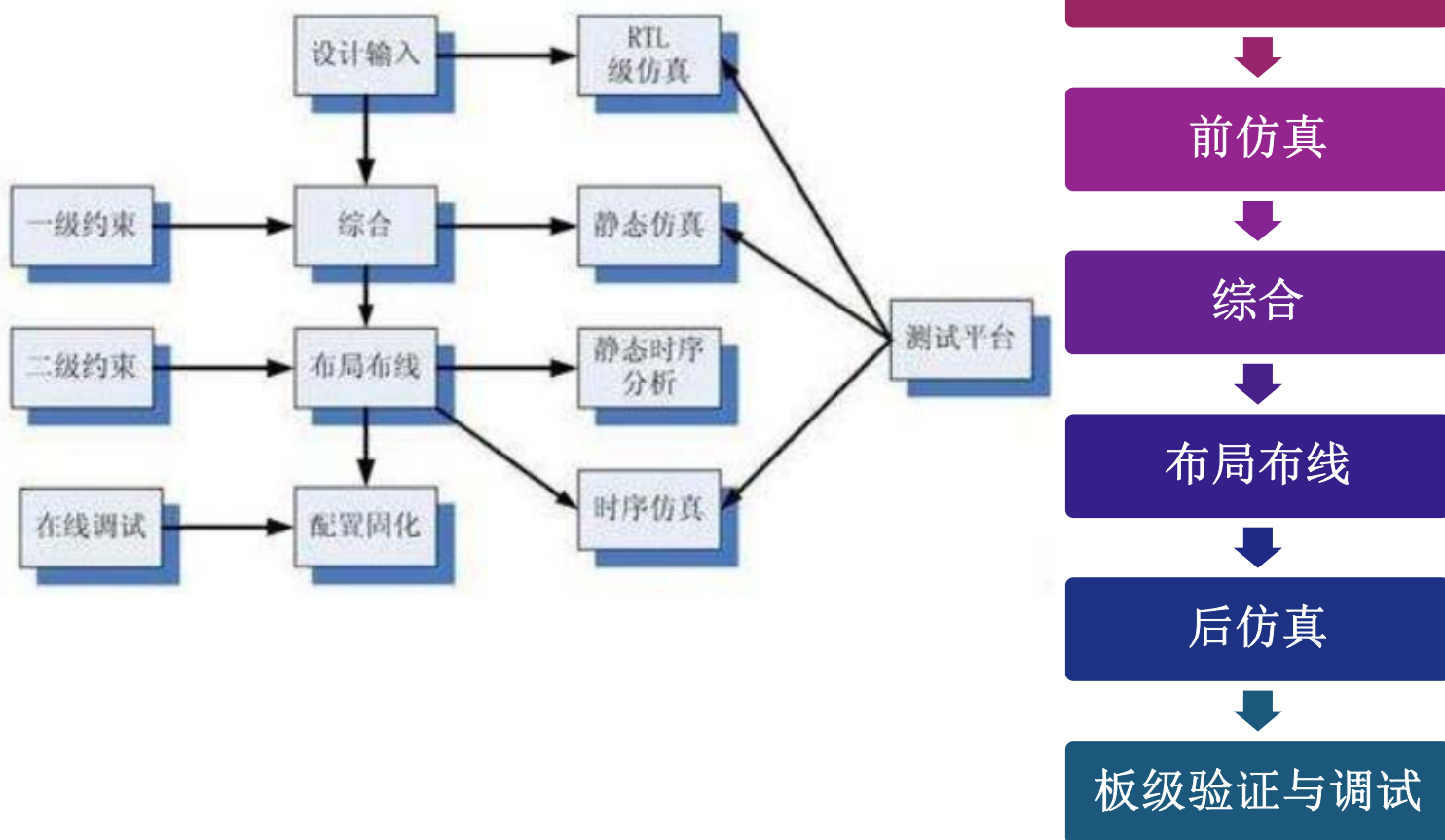
除SDK和HLS以外，所有早期ISE的工具都被集成在Vivado的GUI中



State Key Laboratory of Millimeter Waves



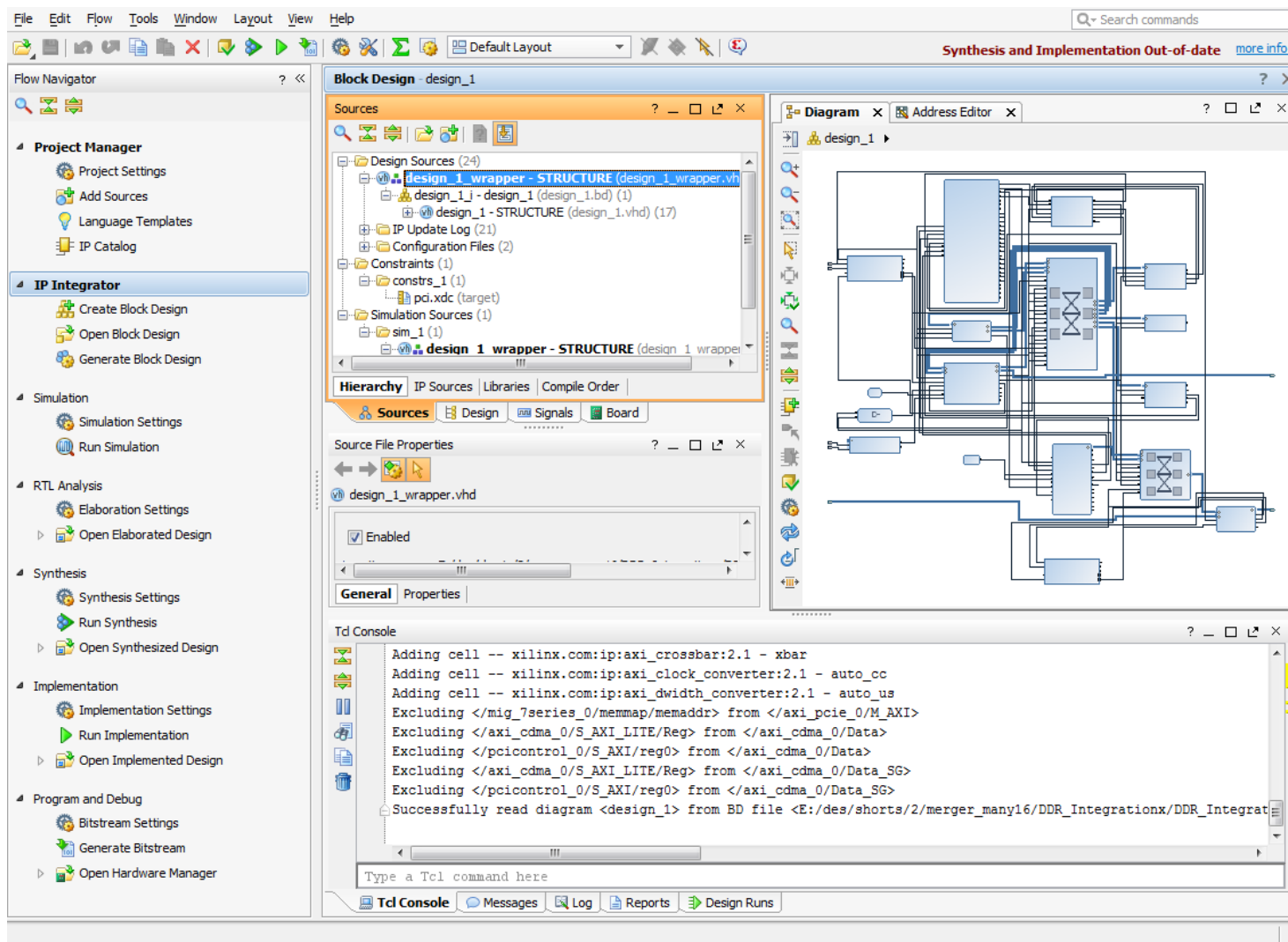
FPGA开发流程





Vivado GUI

数字系统课程设计





数字系统课程设计

创建新的工程

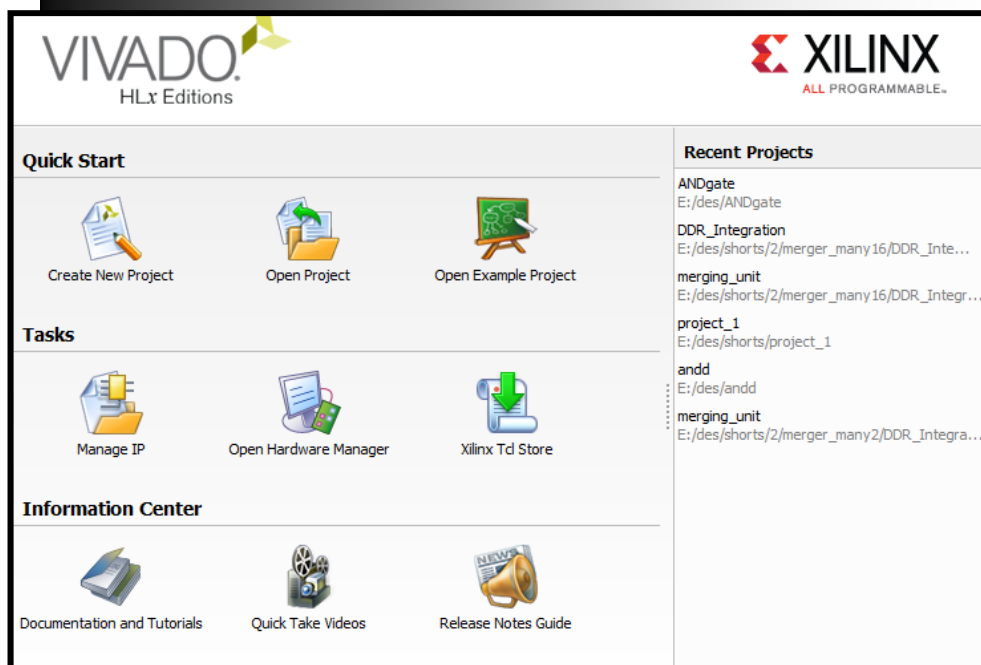


State Key Laboratory of Millimeter Waves



创建新的工程

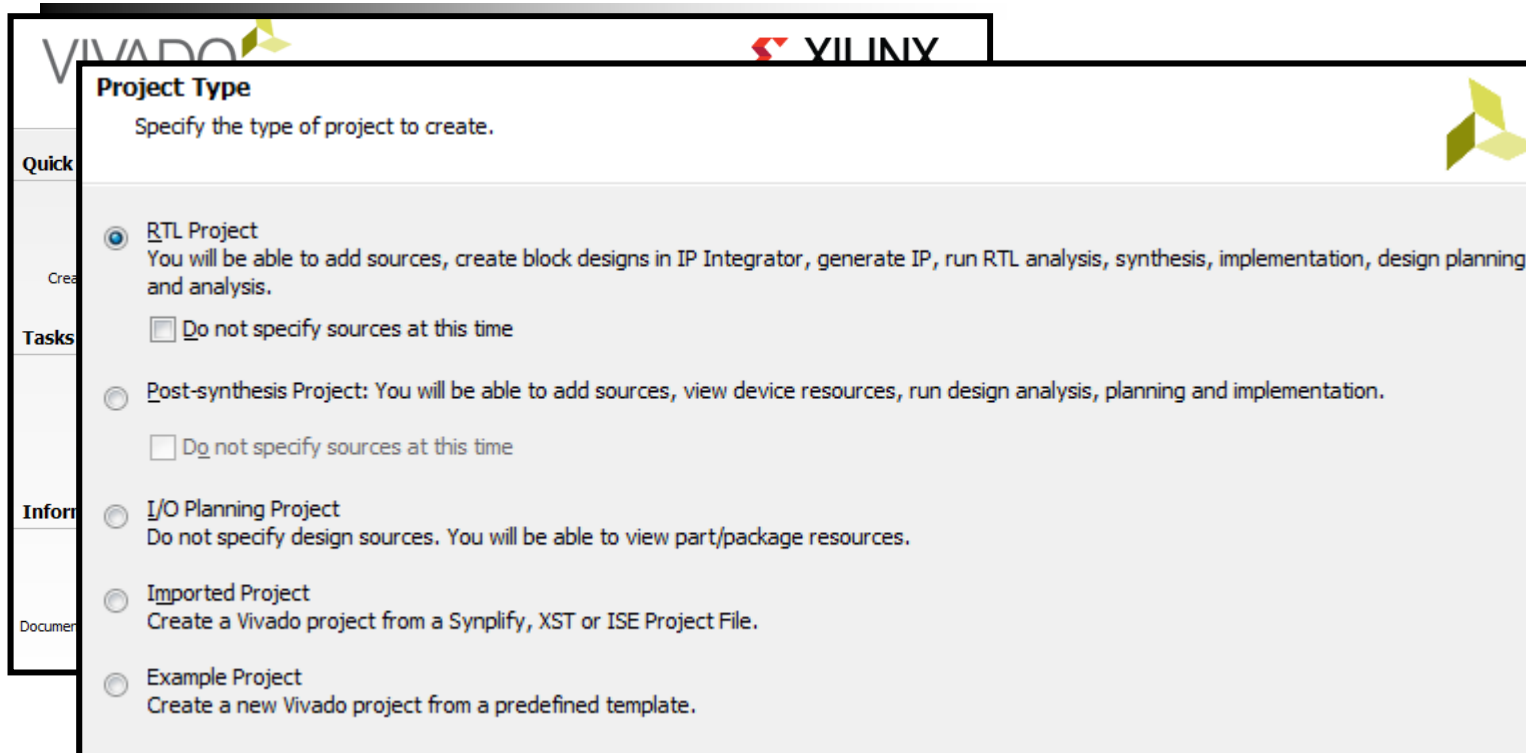
数字系统课程设计





创建新的工程

数字系统课程设计



The image shows the 'Project Type' dialog box in the Vivado IDE. The dialog has a title bar with 'VIVADO' and 'XILINX' logos. Below the title bar, it says 'Project Type' and 'Specify the type of project to create.' There are five radio button options: 'RTL Project' (selected), 'Post-synthesis Project', 'I/O Planning Project', 'Imported Project', and 'Example Project'. Each option has a description. There are also checkboxes for 'Do not specify sources at this time' for the first two options. On the left side of the dialog, there is a sidebar with labels: 'Quick', 'Create', 'Tasks', 'Inform', and 'Document'.

Project Type
Specify the type of project to create.

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
☐ Do not specify sources at this time

☐ **Post-synthesis Project:** You will be able to add sources, view device resources, run design analysis, planning and implementation.
☐ Do not specify sources at this time

☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**
Create a new Vivado project from a predefined template.



创建新的工程

数字系统课程设计

VIVADO YILINIX

Project Type
Specify the type of project to create.

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

☐ Example Project
Create a new Vivado project from a predefined template.

☐ Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.

☒ Create project subdirectory
Project will be created at: E:/Designs

Project name:

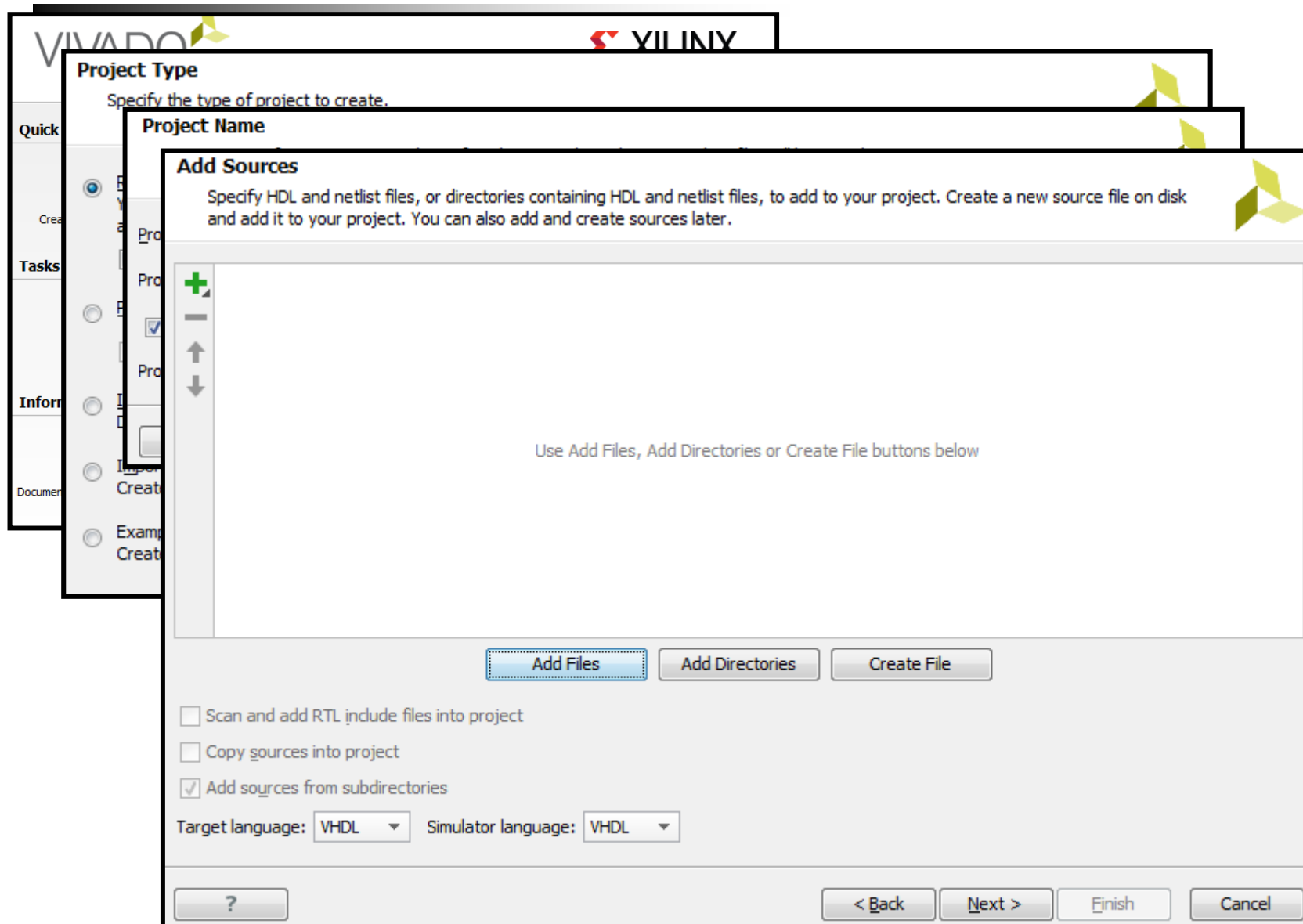
Project location: E:/Designs





创建新的工程

数字系统课程设计



The image shows the Vivado Project Creation Wizard dialog box, which is a multi-step process for creating a new project. The dialog is titled "VIVADO" and "YILINX". It has a sidebar on the left with options: "Quick", "Create", "Tasks", "Inform", and "Document". The main area is divided into three sections: "Project Type", "Project Name", and "Add Sources". The "Add Sources" section is currently active, showing a list of sources with a green plus icon and a minus icon. Below the list are three buttons: "Add Files", "Add Directories", and "Create File". At the bottom, there are checkboxes for "Scan and add RTL include files into project", "Copy sources into project", and "Add sources from subdirectories". The "Target language" is set to "VHDL" and the "Simulator language" is also set to "VHDL". Navigation buttons at the bottom include "< Back", "Next >", "Finish", and "Cancel".

Project Type
Specify the type of project to create.

Project Name

Add Sources
Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Use Add Files, Add Directories or Create File buttons below

☐ Scan and add RTL include files into project
☐ Copy sources into project
☒ Add sources from subdirectories

Target language: VHDL Simulator language: VHDL

< Back Next > Finish Cancel



创建新的工程

数字系统课程设计

VIVADO

Project Type

Specify the type of project to create.

Project Name

Add Sources

Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to the project.

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select: ☒ Parts ☐ Boards

Filter / Preview

Vendor:

Display Name:

Board Rev:

Search:

Display Name	Vendor	Board Rev	Part	I/O Pin Count	File Version	Blod RAM
ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	d	xc7z020dg484-1	484	1.3	140
Artix-7 AC701 Evaluation Platform	xilinx.com	1.1	xc7a200tfg676-2	676	1.3	365
Kintex-7 KC705 Evaluation Platform	xilinx.com	1.1	xc7k325tffg900-2	900	1.3	445
Kintex-UltraScale KCU105 Evaluation Platform	xilinx.com	1.0	xcku040-ffva1156-2-e	1,156	1.1	600
Virtex-7 VC707 Evaluation Platform	xilinx.com	1.1	xc7vx485tffg1761-2	1,761	1.3	1030
Virtex-7 VC709 Evaluation Platform	xilinx.com	1.0	xc7vx690tffg1761-2	1,761	1.8	1470
Virtex-UltraScale VCU108 Evaluation Platform	xilinx.com	1.0	xcvu095-ffva2104-2-e	2,104	1.1	1728

Target language: Simulator language:



创建新的工程

数字系统课程设计

VIVADO

Project Type

Specify the type of project to create.

Project Name

Add Sources

Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to the project.

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Entity name: ANG_gate

Architecture name: Behavioral

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
A	in	<input type="checkbox"/>	0	0
B	in	<input type="checkbox"/>	0	0
O	out	<input type="checkbox"/>	0	0

OK Cancel

Target language: VHDL Simulator language: VHDL

< Back Next > Finish Cancel





工程管理器

数字系统课程设计

File Edit Flow Tools Window Layout View Help

Flow Navigator

- Project Manager
 - Project Settings
 - Add Sources
 - Language Templates
 - IP Catalog
 - Package IP
- IP Integrator
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- Simulation
 - Simulation Settings
 - Run Simulation
- RTL Analysis
 - Elaboration Settings
 - Open Elaborated Design
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Open Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation
 - Open Implemented Design
- Program and Debug
 - Bitstream Settings

Project Manager - ANDgate

Sources

- Design Sources (3)
 - design_1_wrapper - STRUCTURE (design_1_wrapper.vhd) (1)
 - AND_Gate - Behavioral (AND_Gate.vhd)
 - IP-XACT (1)
- Constraints (1)
- Simulation Sources (2)

Hierarchy IP Sources Libraries Compile Order

Source File Properties

design_1_wrapper.vhd

☒ Enabled

Location: E:/des/ANDgate/ANDgate.srcs/sources_1/bd/design_1/

Type: VHDL

Library: xil_defaultlib

General Properties

Project Summary

Project Settings

Project name: ANDgate

Project location: E:/des/ANDgate

Product family: Zynq-7000

Project part: ZedBoard Zynq Evaluation and Development Kit (xc7z020clq484-1)

Top module name: design_1_wrapper

Target language: VHDL

Simulator language: VHDL

Board Part

Display name: ZedBoard Zynq Evaluation and Development Kit

Board part name: em.avnet.com:zed:part0:1.3

Repository path: C:/Xilinx/Vivado/2016.2/data/boards/board_files

URL: <http://www.zedboard.org>

Board overview: ZedBoard Zynq Evaluation and Development Kit

Synthesis

Status: ☒ Complete

Messages: 2 warnings

Implementation

Status:

Messages:

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM
synth_1	constrs_1	synth_design Complete!								1	0
impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA		0	1	0

Tcl Console Messages Log Reports Design Runs





工程管理器

数字系统课程设计

Flow Navigator

- Project Manager
- IP Integrator
- Simulation
- RTL Analysis
- Synthesis
- Implementation
- Program and Debug

Project Manager - ANDgate

Sources

- Design Sources (3)
 - design_1_wrapper - STRUCTURE (design_1_wrapper.vhd) (1)
 - AND_Gate - Behavioral (AND_Gate.vhd)
 - IP-XACT (1)
- Constraints (1)
- Simulation Sources (2)

Hierarchy | IP Sources | Libraries | Compile Order

Source File Properties

design_1_wrapper.vhd

☒ Enabled

Location: E:/des/ANDgate/ANDgate.srcs/sources_1/bd/design_1/

Type: VHDL

Library: xil_defaultlib

General | Properties

Project Summary

Project Settings

Project name: ANDgate

Project location: E:/des/ANDgate

Product family: Zynq-7000

Project part: ZedBoard Zynq Evaluation and Development Kit (xc7z020clq484-1)

Top module name: design_1_wrapper

Target language: VHDL

Simulator language: VHDL

Board Part

Display name: ZedBoard Zynq Evaluation and Development Kit

Board part name: em.avnet.com:zed:part0:1.3

Repository path: C:/Xilinx/Vivado/2016.2/data/boards/board_files

URL: <http://www.zedboard.org>

Board overview: ZedBoard Zynq Evaluation and Development Kit

Synthesis

Status: ☒ Complete

Messages: 2 warnings

Implementation

Status:

Messages:

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM
synth_1	constrs_1	synth_design Complete!								1	0
impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA		0	1	0

Tcl Console | Messages | Log | Reports | Design Runs





工程管理器

数字系统课程设计

File Edit Flow Tools Window Layout View Help

Flow Navigator

- Project Manager
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 - Generate Block Design
- Simulation
 - Simulation Settings
 - Run Simulation
- RTL Analysis
 - Elaboration Settings
 - Open Elaborated Design
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Open Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation
 - Open Implemented Design
- Program and Debug
 - Bitstream Settings

Project Manager - ANDgate

Sources

- Design Sources (3)
 - design_1_wrapper - STRUCTURE (design_1_wrapper.vhd) (1)
 - AND_Gate - Behavioral (AND_Gate.vhd)
 - IP-XACT (1)
- Constraints (1)
- Simulation Sources (2)

Hierarchy IP Sources Libraries Compile Order

Source File Properties

design_1_wrapper.vhd

☒ Enabled

Location: E:/des/ANDgate/ANDgate.srcs/sources_1/bd/design_1/

Type: VHDL

Library: xil_defaultlib

General Properties

Project Summary

Project Settings

Project name: ANDgate

Project location: E:/des/ANDgate

Product family: Zynq-7000

Project part: ZedBoard Zynq Evaluation and Development Kit (xc7z020clq484-1)

Top module name: design_1_wrapper

Target language: VHDL

Simulator language: VHDL

Board Part

Display name: ZedBoard Zynq Evaluation and Development Kit

Board part name: em.avnet.com:zed:part0:1.3

Repository path: C:/Xilinx/Vivado/2016.2/data/boards/board_files

URL: <http://www.zedboard.org>

Board overview: ZedBoard Zynq Evaluation and Development Kit

Synthesis

Status: ☒ Complete

Messages: 2 warnings

Implementation

Status:

Messages:

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM
synth_1	constrs_1	synth_design Complete!								1	0
impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA		0	1	0

Tcl Console Messages Log Reports Design Runs





工程管理器

数字系统课程设计

Flow Navigator

- Project Manager
 - Project Settings
 - Add Sources
 - Language Templates
 - IP Catalog
 - Package IP
- IP Integrator
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- Simulation
 - Simulation Settings
 - Run Simulation
- RTL Analysis
 - Elaboration Settings
 - Open Elaborated Design
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Open Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation
 - Open Implemented Design
- Program and Debug
 - Bitstream Settings

Project Manager - ANDgate

Sources

- Design Sources (3)
 - design_1_wrapper - STRUCTURE (design_1_wrapper.vhd) (1)
 - AND_Gate - Behavioral (AND_Gate.vhd)
 - IP-XACT (1)
- Constraints (1)
- Simulation Sources (2)

Hierarchy | IP Sources | Libraries | Compile Order

Source File Properties

design_1_wrapper.vhd

☒ Enabled

Location: E:/des/ANDgate/ANDgate.srcs/sources_1/bd/design_1/

Type: VHDL

Library: xil_defaultlib

General | Properties

Project Summary

Project Settings

Project name: ANDgate

Project location: E:/des/ANDgate

Product family: Zynq-7000

Project part: ZedBoard Zynq Evaluation and Development Kit (xc7z020clq484-1)

Top module name: design_1_wrapper

Target language: VHDL

Simulator language: VHDL

Board Part

Display name: ZedBoard Zynq Evaluation and Development Kit

Board part name: em.avnet.com:zed:part0:1.3

Repository path: C:/Xilinx/Vivado/2016.2/data/boards/board_files

URL: <http://www.zedboard.org>

Board overview: ZedBoard Zynq Evaluation and Development Kit

Synthesis

Status: ☒ Complete

Messages: 2 warnings

Implementation

Status:

Messages:

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM
synth_1	constrs_1	synth_design Complete!								1	0
impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA		0	1	0

Tcl Console | Messages | Log | Reports | Design Runs





工程管理器

数字系统课程设计

File Edit Flow Tools Window Layout View Help

Flow Navigator

- Project Manager
 - Project Settings
 - Add Sources
 - Language Templates
 - IP Catalog
 - Package IP
- IP Integrator
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- Simulation
 - Simulation Settings
 - Run Simulation
- RTL Analysis
 - Elaboration Settings
 - Open Elaborated Design
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Open Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation
 - Open Implemented Design
- Program and Debug
 - Bitstream Settings

Project Manager - ANDgate

Sources

- Design Sources (3)
 - design_1_wrapper - STRUCTURE (design_1_wrapper.vhd) (1)
 - AND_Gate - Behavioral (AND_Gate.vhd)
 - IP-XACT (1)
- Constraints (1)
- Simulation Sources (2)

Hierarchy IP Sources Libraries Compile Order

Source File Properties

design_1_wrapper.vhd

☒ Enabled

Location: E:/des/ANDgate/ANDgate.srcs/sources_1/bd/design_1/

Type: VHDL

Library: xil_defaultlib

General Properties

Project Summary

Project Settings

Project name: ANDgate

Project location: E:/des/ANDgate

Product family: Zynq-7000

Project part: ZedBoard Zynq Evaluation and Development Kit (xc7z020clq484-1)

Top module name: design_1_wrapper

Target language: VHDL

Simulator language: VHDL

Board Part

Display name: ZedBoard Zynq Evaluation and Development Kit

Board part name: em.avnet.com:zed:part0:1.3

Repository path: C:/Xilinx/Vivado/2016.2/data/boards/board_files

URL: <http://www.zedboard.org>

Board overview: ZedBoard Zynq Evaluation and Development Kit

Synthesis

Status: ☒ Complete

Messages: 2 warnings

Implementation

Status:

Messages:

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM
synth_1	constrs_1	synth_design Complete!								1	0
impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA		0	1	0

Tcl Console Messages Log Reports Design Runs





工程管理器

数字系统课程设计

Flow Navigator

- Project Manager
 - Project Settings
 - Add Sources
 - Language Templates
 - IP Catalog
 - Package IP
- IP Integrator
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- Simulation
 - Simulation Settings
 - Run Simulation
- RTL Analysis
 - Elaboration Settings
 - Open Elaborated Design
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Open Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation
 - Open Implemented Design
- Program and Debug
 - Bitstream Settings

Project Manager - ANDgate

Sources

- Design Sources (3)
 - design_1_wrapper - STRUCTURE (design_1_wrapper.vhd) (1)
 - AND_Gate - Behavioral (AND_Gate.vhd)
 - IP-XACT (1)
- Constraints (1)
- Simulation Sources (2)

Hierarchy | IP Sources | Libraries | Compile Order

Source File Properties

design_1_wrapper.vhd

☒ Enabled

Location: E:/des/ANDgate/ANDgate.srcs/sources_1/bd/design_1/

Type: VHDL

Library: xil_defaultlib

General | Properties

Project Summary

Project Settings

Project name: ANDgate

Project location: E:/des/ANDgate

Product family: Zynq-7000

Project part: ZedBoard Zynq Evaluation and Development Kit (xc7z020clq484-1)

Top module name: design_1_wrapper

Target language: VHDL

Simulator language: VHDL

Board Part

Display name: ZedBoard Zynq Evaluation and Development Kit

Board part name: em.avnet.com:zed:part0:1.3

Repository path: C:/Xilinx/Vivado/2016.2/data/boards/board_files

URL: <http://www.zedboard.org>

Board overview: ZedBoard Zynq Evaluation and Development Kit

Synthesis

Status: ☒ Complete

Messages: 2 warnings

Implementation

Status:

Messages:

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM
synth_1	constrs_1	synth_design Complete!								1	0
impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA		0	1	0

Tcl Console | Messages | Log | Reports | Design Runs



State Key Laboratory of Millimeter Waves



IP核

数字系统课程设计

The screenshot displays the Xilinx Vivado IDE interface for a project named "design_1". The left sidebar contains the "Project Manager" and "IP Integrator" sections. The "IP Integrator" section is active, showing options like "Create Block Design", "Open Block Design", and "Generate Block Design". The "Block Design" window shows a hierarchy of sources, including "design_1_wrapper - STRUCTURE", "design_1 - design_1 (design_1.bd)", "design_1 - STRUCTURE (design_1.vhd)", "AND_Gate_0 - design_1_AND_Gate_0_0 (design_1_AND_Gate_0_Behavioral (AND_Gate.vhd))", "IP-XACT (1)", "Constraints (1)", and "Simulation Sources (2)". The "Diagram" window shows a block diagram of the AND gate, with inputs A and B, and output O. The "Tcl Console" window at the bottom shows the following log:

```
INFO: [IP_Flow 19-1700] Loaded user IP repository 'e:/des/ANDgate'.  
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2016.2/data/ip'.  
open_project: Time (s): cpu = 00:00:10 ; elapsed = 00:00:05 . Memory (MB): peak = 1465.188 ; gain = 0.000  
update_compile_order -fileset sources_1  
current_project DDR_Integration  
current_project ANDgate  
open_bd_design {E:/des/ANDgate/ANDgate.srcs/sources_1/bd/design_1/design_1.bd}  
Adding cell -- xilinx.com:user:AND_Gate:1.0 - AND_Gate_0  
Successfully read diagram <design_1> from BD file <E:/des/ANDgate/ANDgate.srcs/sources_1/bd/design_1/design_1.bd>
```





IP核

数字系统课程设计

The screenshot displays the Xilinx Vivado IDE interface during the IP Integrator process. The left sidebar shows the 'Project Manager' and 'IP Integrator' sections. An orange arrow points to the 'IP Integrator' section. The main workspace is divided into several panes:

- Block Design - design_1**: Shows the 'Sources' pane with a tree view of the design hierarchy, including 'design_1_wrapper - STRUCTURE', 'design_1 - design_1 (design_1.bd)', 'design_1 - STRUCTURE (design_1.vhd)', 'AND_Gate_0 - design_1_AND_Gate_0_0 (design_1_AND_Gate_0_Behavioral (AND_Gate.vhd))', 'IP-XACT (1)', 'Constraints (1)', and 'Simulation Sources (2)'. The 'Hierarchy' pane shows the 'Sources' tab selected.
- Diagram**: Shows a block diagram of the design, featuring an 'AND_Gate_0' block connected to inputs 'A' and 'B' and output 'O'.
- Tcl Console**: Displays the following log messages:

```
INFO: [IP_Flow 19-1700] Loaded user IP repository 'e:/des/ANDgate'.  
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2016.2/data/ip'.  
open_project: Time (s): cpu = 00:00:10 ; elapsed = 00:00:05 . Memory (MB): peak = 1465.188 ; gain = 0.000  
update_compile_order -fileset sources_1  
current_project DDR_Integration  
current_project ANDgate  
open_bd_design {E:/des/ANDgate/ANDgate.srcs/sources_1/bd/design_1/design_1.bd}  
Adding cell -- xilinx.com:user:AND_Gate:1.0 - AND_Gate_0  
Successfully read diagram <design_1> from BD file <E:/des/ANDgate/ANDgate.srcs/sources_1/bd/design_1/design_1.bd>
```





IP核

数字系统课程设计

The screenshot displays the Xilinx Vivado IDE interface for a project named "design_1". The left sidebar contains the "Project Manager" and "IP Integrator" sections. The "IP Integrator" section is active, showing the "Create Block Design" workflow. The main workspace is divided into several panes:

- Sources:** Shows the project hierarchy, including "design_1_wrapper - STRUCTURE", "design_1 - design_1 (design_1.bd)", "design_1 - STRUCTURE (design_1.vhd)", "AND_Gate_0 - design_1_AND_Gate_0_0 (design_1.vhd)", "IP-XACT (1)", "Constraints (1)", and "Simulation Sources (2)".
- Hierarchy:** Shows the block design hierarchy, including "AND_Gate_0" and "AND_Gate_0_0".
- Diagram:** Shows the block design diagram, which is a simple AND gate circuit. The inputs are labeled "A" and "B", and the output is labeled "O". The gate is labeled "AND_Gate_0" and "AND_Gate_0_0".
- Tcl Console:** Displays the command history and output, including:
 - INFO: [IP_Flow 19-1700] Loaded user IP repository 'e:/des/ANDgate'.
 - INFO: [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2016.2/data/ip'.
 - open_project: Time (s): cpu = 00:00:10 ; elapsed = 00:00:05 . Memory (MB): peak = 1465.188 ; gain = 0.000
 - update_compile_order -fileset sources_1
 - current_project DDR_Integration
 - current_project ANDgate
 - open_bd_design {E:/des/ANDgate/ANDgate.srcs/sources_1/bd/design_1/design_1.bd}
 - Adding cell -- xilinx.com:user:AND_Gate:1.0 - AND_Gate_0
 - Successfully read diagram <design_1> from BD file <E:/des/ANDgate/ANDgate.srcs/sources_1/bd/design_1/design_1.bd>





IP核

数字系统课程设计

The screenshot displays the Xilinx Vivado IDE interface during the IP Integrator workflow. The left sidebar shows the 'IP Integrator' section with options like 'Create Block Design', 'Open Block Design', and 'Generate Block Design'. The main workspace is divided into several panes:

- Block Design - design_1**: The top pane shows the 'Sources' tab with a tree view of the design files, including 'design_1_wrapper - STRUCTURE', 'design_1 - design_1 (design_1.bd)', 'design_1 - STRUCTURE (design_1.vhd)', 'AND_Gate_0 - design_1_AND_Gate_0_0 (design_1.vhd)', 'IP-XACT (1)', 'Constraints (1)', and 'Simulation Sources (2)'. The 'Hierarchy' tab is also visible.
- Diagram**: The right pane shows a block diagram of the AND gate. It features two input ports labeled 'A' and 'B', connected to an AND gate block labeled 'AND_Gate_0' and 'AND_Gate_0_0', which then connects to an output port.
- Source File Properties**: The bottom-left pane shows the properties for the 'design_1.bd' file, with the 'General' tab selected. It indicates the file is 'Enabled' and provides the location path: 'E:/des/ANDgate/ANDgate.srcs/sources_1/bd/design_1.bd'.
- Tcl Console**: The bottom-right pane shows the command history and output. It includes messages such as 'INFO: [IP_Flow 19-1700] Loaded user IP repository 'e:/des/ANDgate'', 'INFO: [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2016.2/data/ip'', and 'Successfully read diagram <design_1> from BD file <E:/des/ANDgate/ANDgate.srcs/sources_1/bd/design_1/design_1.bd'.

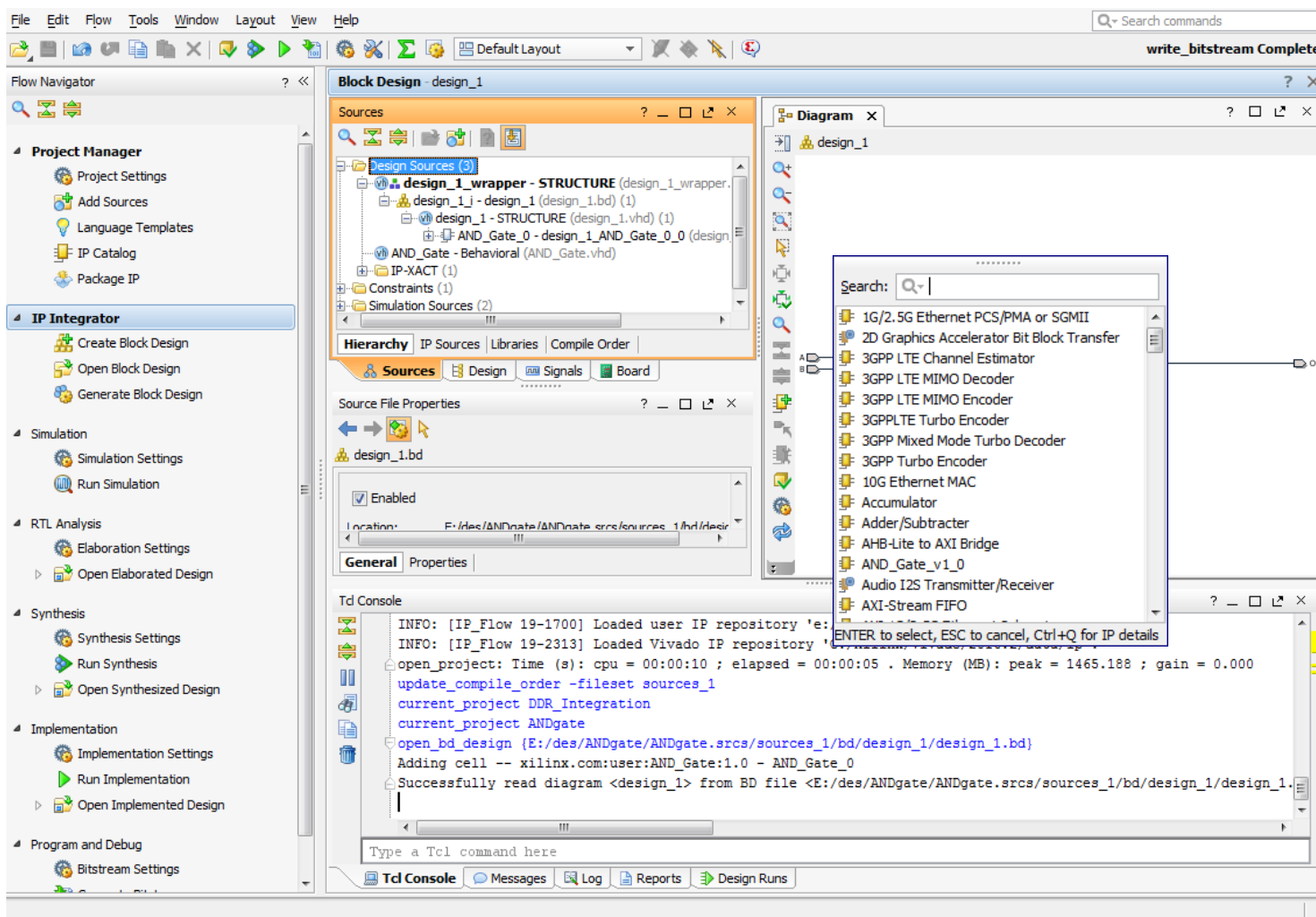
An orange arrow points from the 'Sources' pane to the 'Diagram' pane, indicating the flow of the design process.





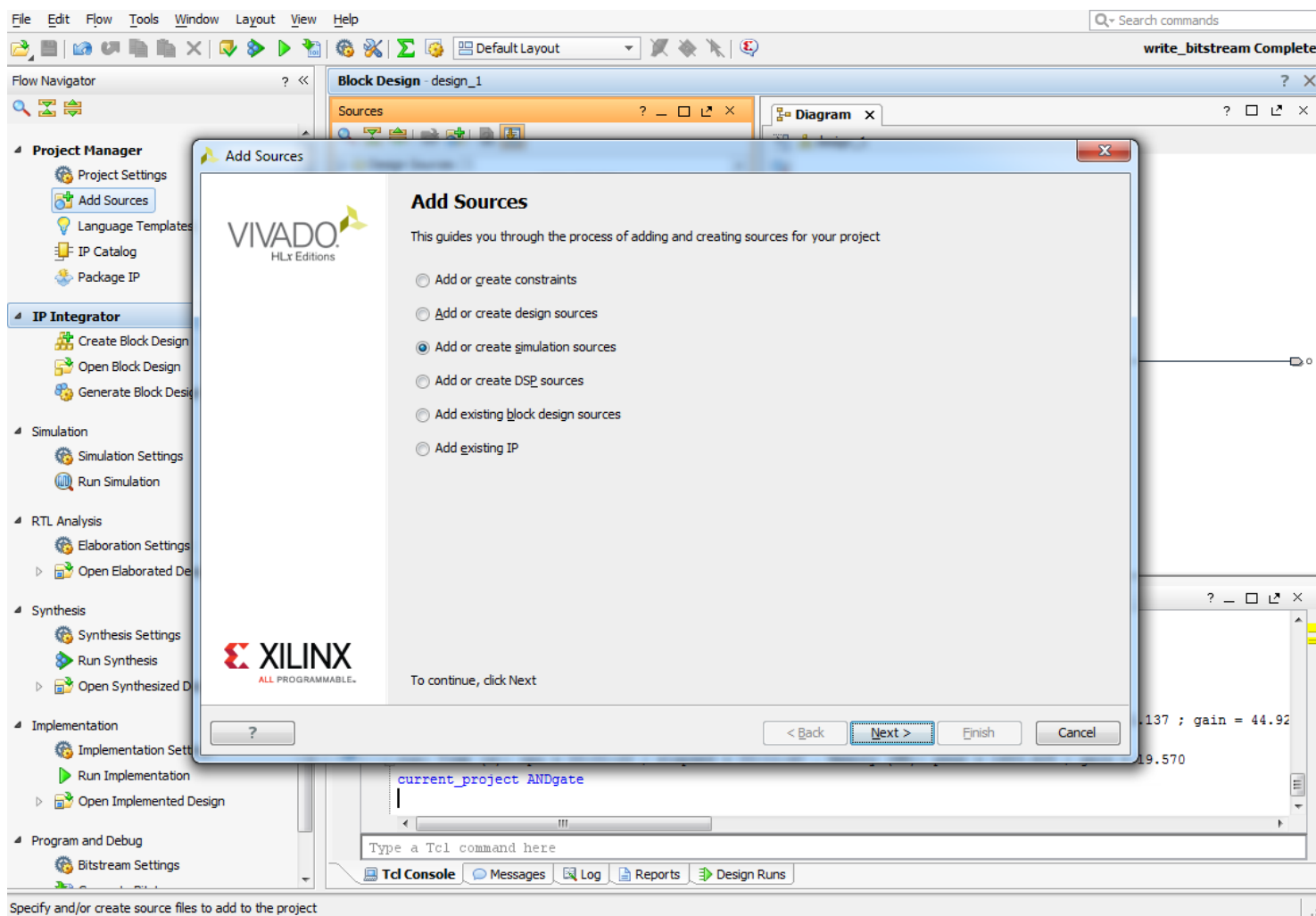
IP核

数字系统课程设计





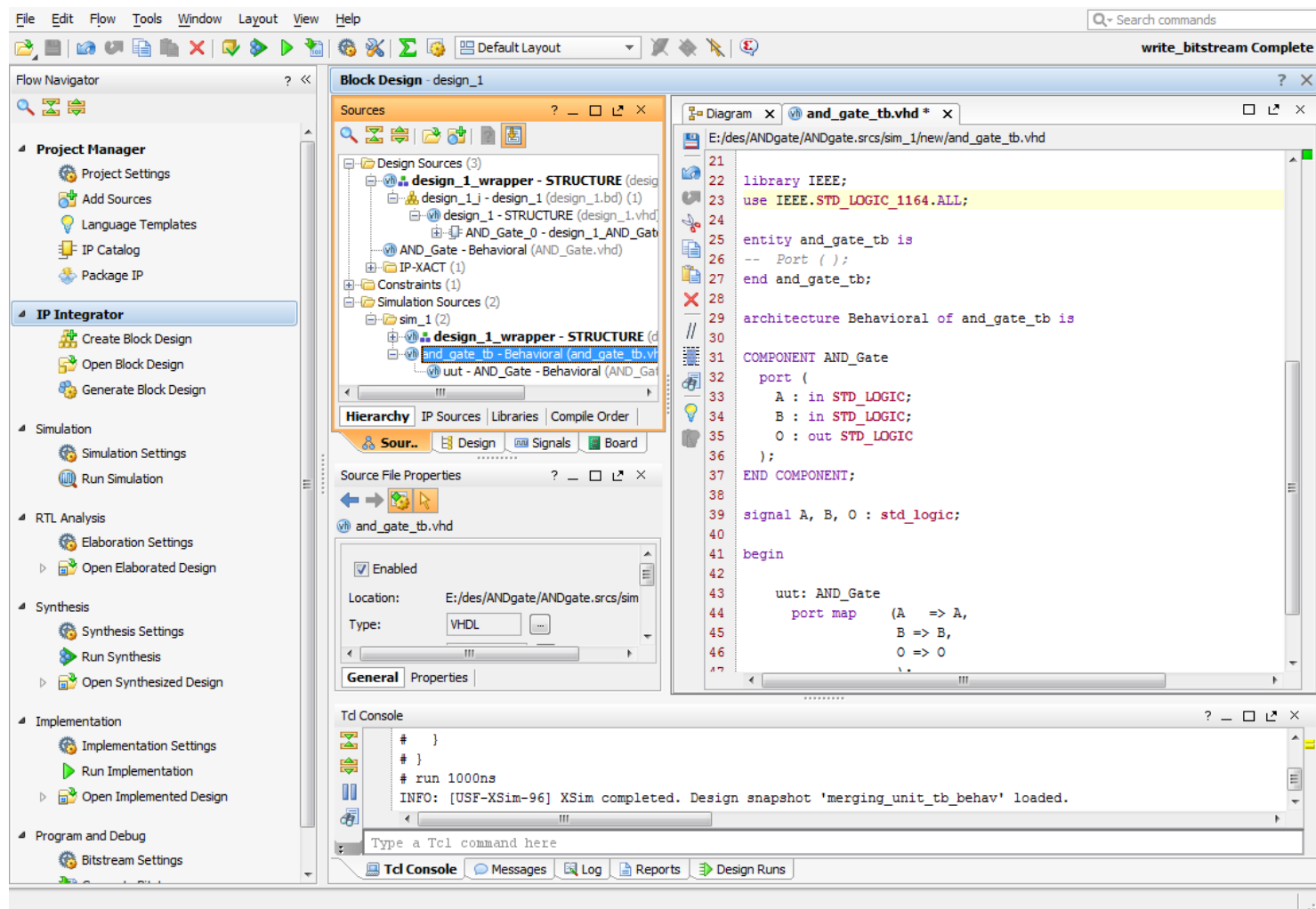
仿真：创建测试平台/testbench





仿真：编辑测试文件/testbench

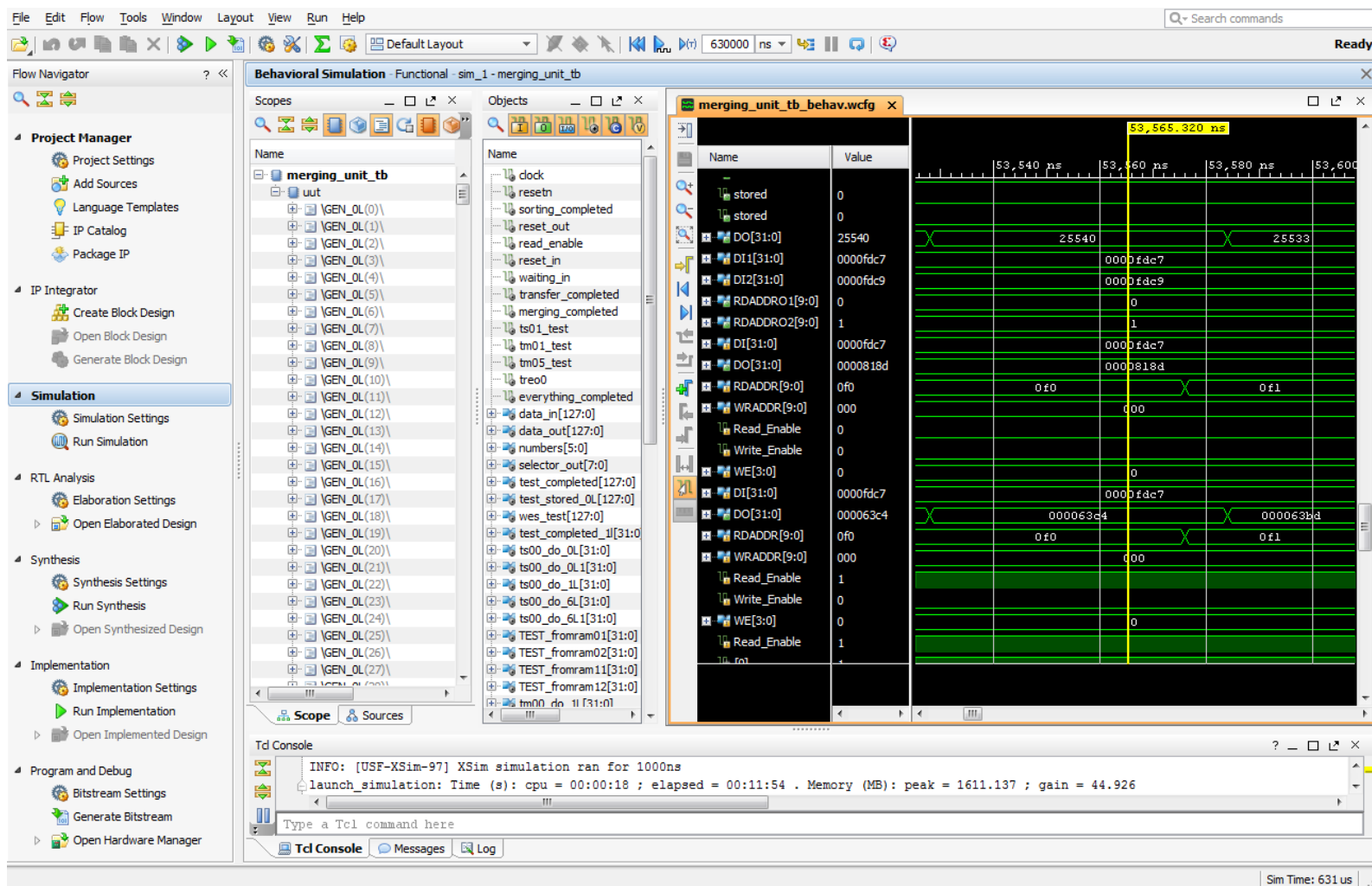
数字系统课程设计





仿真：运行仿真环境

数字系统课程设计





仿真：运行仿真环境

数字系统课程设计

Behavioral Simulation - Functional - sim_1 - merging_unit_tb

Scopes

Objects

merging_unit_tb_behav.wcfg

Name	Value
clock	
resetn	
sorting_completed	
reset_out	
read_enable	
reset_in	
waiting_in	
transfer_completed	
merging_completed	
ts01_test	
tm01_test	
tm05_test	
tree0	
everything_completed	
data_in[127:0]	
data_out[127:0]	
numbers[5:0]	
selector_out[7:0]	
test_completed[127:0]	
test_stored_0L[127:0]	
wes_test[127:0]	
test_completed_1L[31:0]	
ts00_do_0L[31:0]	
ts00_do_0L1[31:0]	
ts00_do_1L[31:0]	
ts00_do_6L[31:0]	
ts00_do_6L1[31:0]	
TEST_fromram01[31:0]	
TEST_fromram02[31:0]	
TEST_fromram11[31:0]	
TEST_fromram12[31:0]	
tm00_do_1L[31:0]	

Simulation Settings

Run Simulation

Simulation Console

INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:18 ; elapsed = 00:11:54 . Memory (MB): peak = 1611.137 ; gain = 44.926

Sim Time: 631 us





仿真：运行仿真环境

数字系统课程设计

The screenshot displays the Xilinx Vivado Behavioral Simulation environment. The top toolbar shows the simulation controls, with the 'Run' button (a green play icon) highlighted. The simulation time is set to 630000 ns. The main window is divided into several panes:

- Project Manager:** Located on the left, it shows the project hierarchy, including the 'merging_unit_tb' testbench and its associated sources.
- Behavioral Simulation:** The central pane shows the simulation results. It includes a table of signals and their values, and a waveform viewer displaying the timing of these signals. The signals listed include DO[31:0], DI[31:0], RDADDR[9:0], WRADDR[9:0], Read_Enable, Write_Enable, WE[3:0], and Read_Enable. The waveform shows the signals' behavior over time, with a vertical cursor at 53,565.320 ns.
- Tcl Console:** At the bottom, it shows the simulation log, including the message 'INFO: [USF-XSim-97] XSim simulation ran for 1000ns' and 'launch_simulation: Time (s): cpu = 00:00:18 ; elapsed = 00:11:54 . Memory (MB): peak = 1611.137 ; gain = 44.926'.

The simulation is running for 631 us, as indicated in the bottom right corner.





仿真：运行仿真环境

数字系统课程设计

The screenshot displays the Xilinx Vivado simulation environment. The main window shows the testbench `merging_unit_tb_behav.wcfg` with a list of signals and their values. The simulation is running for 630000 ns. The Tcl Console at the bottom shows the simulation results, including the time taken for the simulation to complete (00:00:18) and the memory usage (peak = 1611.137 MB).

Name	Value
clock	
resetn	
sorting_completed	
reset_out	
read_enable	
reset_in	
waiting_in	
transfer_completed	
merging_completed	
ts01_test	
tm01_test	
tm05_test	
tree0	
everything_completed	
data_in[127:0]	
data_out[127:0]	
numbers[5:0]	
selector_out[7:0]	
test_completed[127:0]	
test_stored_0L[127:0]	
wes_test[127:0]	
test_completed_1L[31:0]	
ts00_do_0L[31:0]	
ts00_do_0L1[31:0]	
ts00_do_1L[31:0]	
ts00_do_6L[31:0]	
ts00_do_6L1[31:0]	
TEST_fromram01[31:0]	
TEST_fromram02[31:0]	
TEST_fromram11[31:0]	
TEST_fromram12[31:0]	
tm00_dp_1L[31:0]	

Tcl Console:

```
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:18 ; elapsed = 00:11:54 . Memory (MB): peak = 1611.137 ; gain = 44.926
```





仿真：运行仿真环境

数字系统课程设计

Behavioral Simulation - Functional - sim_1 - merging_unit_tb

Flow Navigator

- Project Manager
 - Project Settings
 - Add Sources
 - Language Templates
 - IP Catalog
 - Package IP
- IP Integrator
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- Simulation
 - Simulation Settings
 - Run Simulation
- RTL Analysis
 - Elaboration Settings
 - Open Elaborated Design
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Open Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation
 - Open Implemented Design
- Program and Debug
 - Bitstream Settings
 - Generate Bitstream
 - Open Hardware Manager

Scopes

Objects

merging_unit_tb_behav.wcfg

Name	Value
stored	0
DI1[31:0]	0000fdc7
DI2[31:0]	0000fdc9
RDADDR01[9:0]	0
RDADDR02[9:0]	1
DI[31:0]	0000fdc7
DO[31:0]	0000818d
RDADDR[9:0]	0f0
WRADDR[9:0]	000
Read_Enable	0
Write_Enable	0
WE[3:0]	0
DI[31:0]	0000fdc7
DO[31:0]	000063c4
RDADDR[9:0]	0f0
WRADDR[9:0]	000
Read_Enable	1
Write_Enable	0
WE[3:0]	0
Read_Enable	1

Tcl Console

INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:18 ; elapsed = 00:11:54 . Memory (MB): peak = 1611.137 ; gain = 44.926

Sim Time: 631 us





设计约束/Specifying constraints

- ◆ XDC约束文件替代UCF约束
- ◆ XDC约束包含：
 - 工业标准Synopsys设计约束 (SDC)
 - Xilinx专有物理性约束
- ◆ XDC约束特性：
 - 不是简单的字符串，而是遵循Tcl语法的命令
 - 像Vivado Tcl解释器的任何其他Tcl命令一样解释
 - 与其他Tcl命令相同的方式读入与解析





约束文件：UCF向XDC的迁移

UCF	SDC
TIMESPEC PERIOD	create_clock create_generated_clock
OFFSET = IN <x> BEFORE <clk>	set_input_delay
OFFSET = OUT <x> BEFORE <clk>	set_output_delay
FROM:TO "TS_"*2	set_multicycle_path
FROM:TO	set_max_delay
TIG	set_false_path
NET "clk_p" LOC = AD12	set_property LOC AD12 [get_ports clk_p]
NET "clk_p" IOSTANDARD = LVDS	set_property IOSTANDARD LVDS [get_ports clk_p]

Source: Vivado Design Suite Migration Methodology Guide (UG911) p 23



约束文件：UCF向XDC的迁移

UCF	SDC
TIMESPEC PERIOD	create_clock create_generated_clock
OFFSET = IN <x> BEFORE <clk>	set_input_delay
OFFSET = OUT <x> BEFORE <clk>	set_output_delay
FROM:TO "TS_"*2	set_multicycle_path
FROM:TO	set_max_delay
TIG	set_false_path
NET "clk_p" LOC = AD12	set_property LOC AD12 [get_ports clk_p]
NET "clk_p" IOSTANDARD = LVDS	set_property IOSTANDARD LVDS [get_ports clk_p]

Source: Vivado Design Suite Migration Methodology Guide (UG911) p 23



约束文件：UCF向XDC的迁移

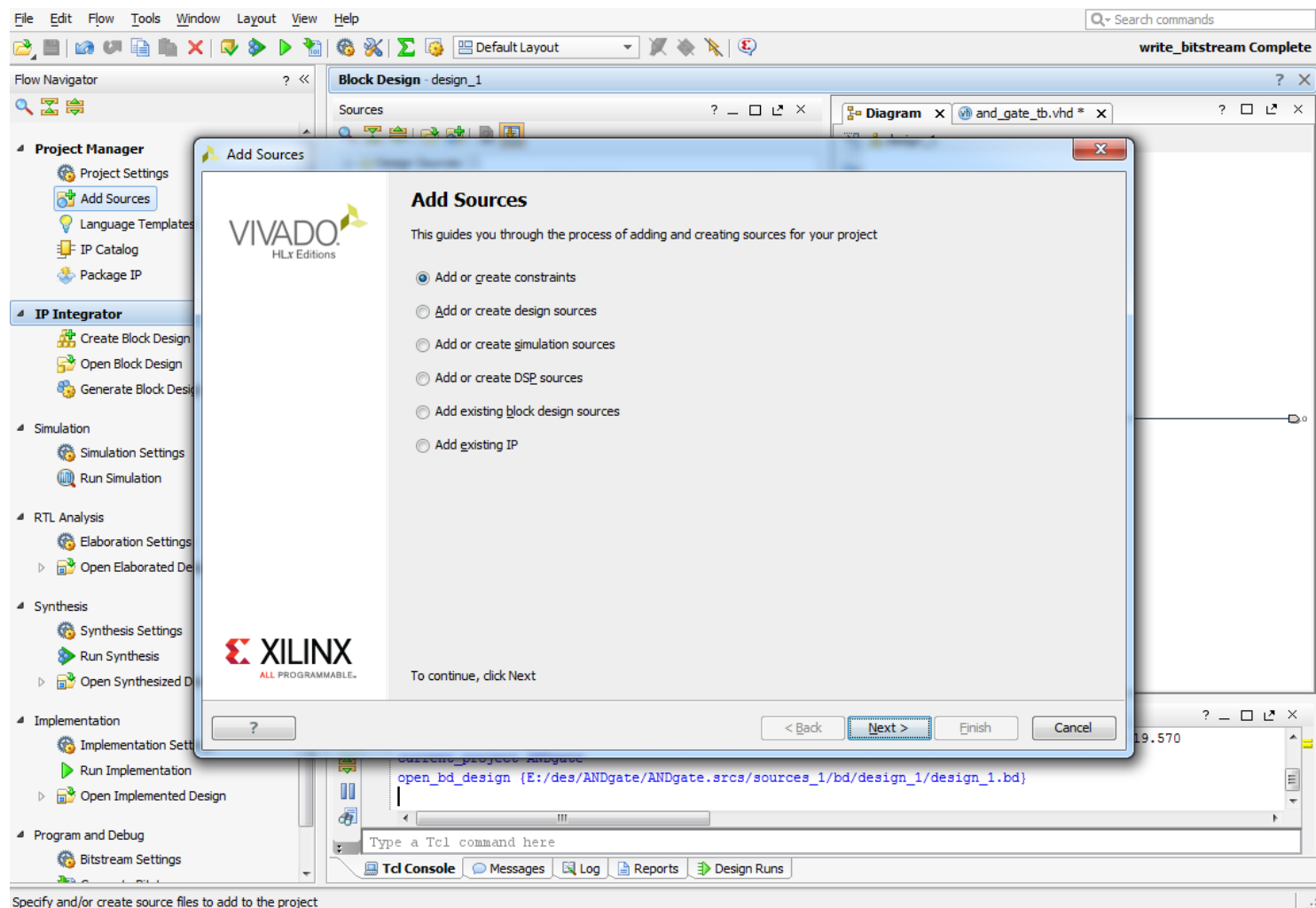
UCF	SDC
TIMESPEC PERIOD	create_clock create_generated_clock
OFFSET = IN <x> BEFORE <clk>	set_input_delay
OFFSET = OUT <x> BEFORE <clk>	set_output_delay
FROM:TO "TS_"*2	set_multicycle_path
FROM:TO	set_max_delay
TIG	set_false_path
NET "clk_p" LOC = AD12	set_property LOC AD12 [get_ports clk_p]
NET "clk_p" IOSTANDARD = LVDS	set_property IOSTANDARD LVDS [get_ports clk_p]

Source: Vivado Design Suite Migration Methodology Guide (UG911) p 23





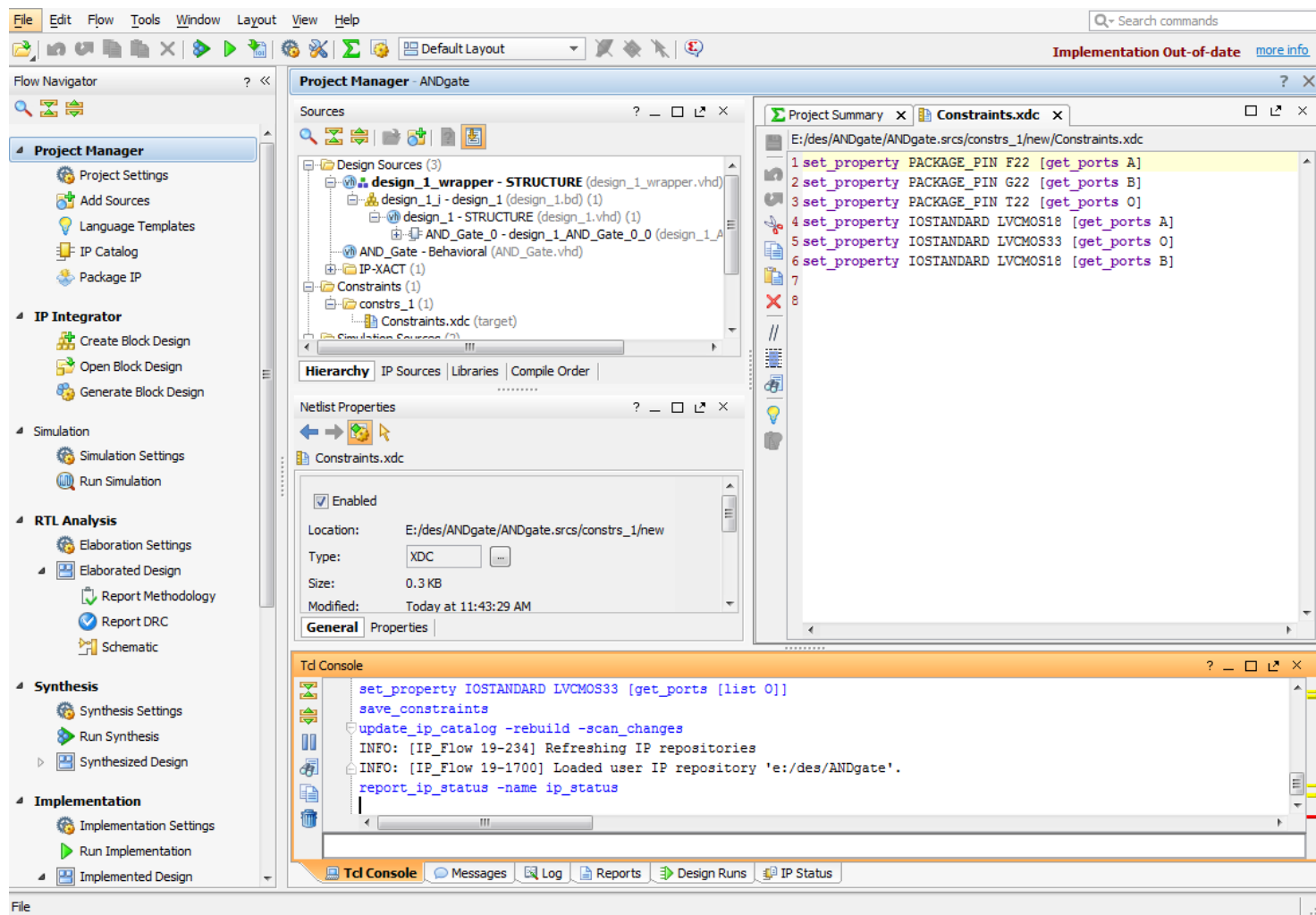
约束文件：创建/添加XDC约束文件





约束文件：编辑XDC约束文件

数字系统课程设计





约束文件：举例

◆ 结合开发板的XDC文件进行解释

- ISE约束文件：ucf
- Vivado约束文件：xdc





设计演示：输入输出规划 I/O Planning

数字系统课程设计

File Edit Flow Tools Window Layout View Help

Search commands

Implementation Out-of-date [more info](#)

Flow Navigator

- Project Manager
 - Project Settings
 - Add Sources
 - Language Templates
 - IP Catalog
 - Package IP
- IP Integrator
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- Simulation
 - Simulation Settings
 - Run Simulation
- RTL Analysis
 - Elaboration Settings
 - Elaborated Design
 - Report Methodology
 - Report DRC
 - Report Noise
 - Schematic
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation

Elaborated Design - xc7z020dkg484-1 (active)

Device Constraints

- Internal VREF
 - 0.6V
 - 0.675V
 - 0.75V
 - 0.9V
- NONE (-4)
 - I/O Bank 13
 - I/O Bank 33
 - I/O Bank 34
 - I/O Bank 35

Source File Properties

Name: O
Direction: OUT

General Properties Configure

Properties Clock Regions

I/O Ports

Name	Direction	Board Part Pin	Board Part Inte...	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std
All ports (3)								
Scalar ports (3)								
A	IN				F22	✓	35	LVC MOS18
B	IN				G22	✓	35	LVC MOS18
O	OUT				T22	✓	33	LVC MOS33*

Tcl Console Messages Log Reports Design Runs Package Pins I/O Ports

Package x Device x Constraints.xdc x Schematic

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22

A B C D E F G H J K L M N P R T U V W Y AA AB





设计演示：输入输出规划 I/O Planning

数字系统课程设计

File Edit Flow Tools Window Layout View Help

Search commands

Implementation Out-of-date [more info](#)

Flow Navigator

- Project Manager
 - Project Settings
 - Add Sources
 - Language Templates
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 - Open Block Design
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 - Elaborated Design
 - Report Methodology
 - Report DRC
 - Report Noise
 - Schematic
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation

Elaborated Design - xc7z020dkg484-1 (active)

Device Constraints

- Internal VREF
 - 0.6V
 - 0.675V
 - 0.75V
 - 0.9V
- NONE (-)
- I/O Bank 13
- I/O Bank 33
- I/O Bank 34
- I/O Bank 35

Source File Properties

Direction: OUT

General Properties Configure

Properties Clock Regions

I/O Ports

Name	Direction	Board Part Pin	Board Part Inte...	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std
All ports (3)								
Scalar ports (3)								
A	IN				F22	✓	35	LVC MOS18
B	IN				G22	✓	35	LVC MOS18
O	OUT				T22	✓	33	LVC MOS33*

Tcl Console Messages Log Reports Design Runs Package Pins I/O Ports

Package x Device x Constraints.xdc x Schematic

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22

A B C D E F G H J K L M N P R T U V W Y AA AB





设计演示：输入输出规划 I/O Planning

数字系统课程设计

File Edit Flow Tools Window Layout View Help

Search commands

Implementation Out-of-date [more info](#)

Flow Navigator

- Project Manager
 - Project Settings
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 - Package IP
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 - Create Block Design
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 - Elaborated Design
 - Report Methodology
 - Report DRC
 - Report Noise
 - Schematic
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation

Elaborated Design - xc7z020dkg484-1 (active)

Device Constraints

- Internal VREF
 - 0.6V
 - 0.675V
 - 0.75V
 - 0.9V
- NONE (-)
- I/O Bank 13
- I/O Bank 33
- I/O Bank 34
- I/O Bank 35

Source File Properties

Name: O
Direction: OUT

General Properties Configure

Properties Clock Regions

I/O Ports

Name	Direction	Board Part Pin	Board Part Inte...	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std
All ports (3)								
Scalar ports (3)								
A	IN				F22	✓	35	LVC MOS18
B	IN				G22	✓	35	LVC MOS18
O	OUT				T22	✓	33	LVC MOS33

Package x Device x Constraints.xdc x Schematic

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22

A B C D E F G H J K L M N P R T U V W Y AA AB





设计演示：输入输出规划 I/O Planning

数字系统课程设计

File Edit Flow Tools Window Layout View Help

Search commands

Implementation Out-of-date [more info](#)

Flow Navigator

- Project Manager
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- Implementation
 - Implementation Settings
 - Run Implementation

Elaborated Design - xc7z020dkg484-1 (active)

Device Constraints

- Internal VREF
 - 0.6V
 - 0.675V
 - 0.75V
 - 0.9V
- NONE (-)
- I/O Bank 13
- I/O Bank 33
- I/O Bank 34
- I/O Bank 35

Source File Properties

Name: O
Direction: OUT

General Properties Constraints Regions

I/O Ports

Name	Direction	Board Part Pin	Board Part Inte...	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std
All ports (3)								
Scalar ports (3)								
A	IN				F22	✓	35	LVC MOS18
B	IN				G22	✓	35	LVC MOS18
O	OUT				T22	✓	33	LVC MOS33

Package x Device x Constraints.xdc x Schematic

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22

A B C D E F G H J K L M N P R T U V W Y AA AB





设计演示：输入输出规划 I/O Planning

数字系统课程设计

File Edit Flow Tools Window Layout View Help

Search commands

Implementation Out-of-date [more info](#)

Flow Navigator

- Project Manager
 - Project Settings
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- Implementation
 - Implementation Settings
 - Run Implementation

Elaborated Design - xc7z020dkg484-1 (active)

Device Constraints

- Internal VREF
 - 0.6V
 - 0.675V
 - 0.75V
 - 0.9V
 - NONE (-)
 - I/O Bank 13
 - I/O Bank 33
 - I/O Bank 34
 - I/O Bank 35

Source File Properties

Name: O
Direction: OUT

General Properties Regions

I/O Ports

Name	Direction	Board Part Pin	Board Part Inte...	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std
All ports (3)								
Scalar ports (3)								
A	IN				F22	✓	35	LVC MOS18
B	IN				G22	✓	35	LVC MOS18
O	OUT				T22	✓	33	LVC MOS33*

Package x Device x Constraints.xdc x Schematic

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22

A B C D E F G H J K L M N P R T U V W Y AA AB





设计演示：输入输出规划 I/O Planning

数字系统课程设计

Elaborated Design - xc7z020dkg484-1 (active)

Device Constraints

- Internal VREF
 - 0.6V
 - 0.675V
 - 0.75V
 - 0.9V
- NONE (-)
- I/O Bank 13
- I/O Bank 33
- I/O Bank 34
- I/O Bank 35

Source File Properties

Name: O
Direction: OUT

I/O Ports

Name	Direction	Board Part Pin	Board Part Inte...	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std
All ports (3)								
Scalar ports (3)								
A	IN				F22	✓	35	LVC MOS18
B	IN				G22	✓	35	LVC MOS18
O	OUT				T22	✓	33	LVC MOS33





设计演示

数字系统课程设计

File Edit Flow Tools Window Layout View Help

write_bitstream Complete

Flow Navigator

- Project Settings
- Add Sources
- Language Templates
- IP Catalog
- Package IP
- IP Integrator**
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- Simulation
 - Simulation Settings
 - Run Simulation
- RTL Analysis**
 - Elaboration Settings
 - Elaborated Design**
 - Report Methodology
 - Report DRC
 - Report Noise
 - Schematic
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Open Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation
 - Open Implemented Design

Elaborated Design - xc7z020dg484-1 (active)

Device Constraints

- Internal VREF
 - 0.6V
 - 0.675V
 - 0.75V
 - 0.9V
 - NONE (4)
 - I/O Bank 13
 - I/O Bank 33
 - I/O Bank 34
 - I/O Bank 35

Sources RTL Netlist Device Constraints

Source File Properties

Constraints.xdc

☒ Enabled

General Properties

Properties Clock Regions

I/O Ports

Port	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std
All ports (3)								
Scalar ports (3)								
A	IN				F22	✓		35 LVCMOS33*
B	IN				G22	✓		35 LVCMOS33*
O	OUT				T22	✓		33 LVCMOS33*

Schematic (2)

1 Cell 3 I/O Ports 3 Nets

design_1_i

design_1

A B O





设计演示

数字系统课程设计

File Edit Flow Tools Window Layout View Help

write_bitstream Complete

Flow Navigator

- Project Settings
- Add Sources
- Language Templates
- IP Catalog
- Package IP
- IP Integrator**
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- Simulation
 - Simulation Settings
 - Run Simulation
- RTL Analysis**
 - Elaboration Settings
 - Elaborated Design**
 - Report Methodology
 - Report DRC
 - Report Noise
 - Schematic
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Open Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation
 - Open Implemented Design

Elaborated Design - xc7z020dgg484 1 (active)

Device Constraints

- Internal VREF
 - 0.6V
 - 0.675V
 - 0.75V
 - 0.9V
 - NONE (4)
 - I/O Bank 13
 - I/O Bank 33
 - I/O Bank 34
 - I/O Bank 35

Sources RTL Netlist Device Constraints

Source File Properties

Constraints.xdc

Enabled

General Properties

Properties Clock Regions

Schematic (2)

1 Cell 3 I/O Ports 3 Nets

design_1_i

A B

O

design_1

I/O Ports

Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std
All ports (3)							
Scalar ports (3)							
IN				F22	✓		35 LVCMOS33*
IN				G22	✓		35 LVCMOS33*
OUT				T22	✓		33 LVCMOS33*

Tcl Console Messages Log Reports Design Runs Package Pins I/O Ports





设计演示

数字系统课程设计

File Edit Flow Tools Window Layout View Help

write_bitstream Complete

Flow Navigator

- Project Settings
- Add Sources
- Language Templates
- IP Catalog
- Package IP
- IP Integrator**
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- Simulation
 - Simulation Settings
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 - Elaboration Settings
 - Elaborated Design**
 - Report Methodology
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 - Report Noise
 - Schematic
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Open Synthesized Design
- Implementation
 - Implementation Settings
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 - Open Implemented Design

Elaborated Design - xc7z020dg484 1 (active)

Device Constraints

- Internal VREF
 - 0.6V
 - 0.675V
 - 0.75V
 - 0.9V
 - NONE (4)
 - I/O Bank 13
 - I/O Bank 33
 - I/O Bank 34
 - I/O Bank 35

Sources RTL Netlist Device Constraints

Source File Properties

Constraints.xdc

Enabled

General Properties

Properties Clock Regions

I/O Ports

Port	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std
All ports (3)								
Scalar ports (3)								
A	IN				F22	✓		35 LVCMOS33*
B	IN				G22	✓		35 LVCMOS33*
O	OUT				T22	✓		33 LVCMOS33*

Schematic (2)

1 Cell 3 I/O Ports 3 Nets

design_1_i

design_1

A B O





设计演示：综合设计/Synthesis

数字系统课程设计

Flow Navigator

- Project Manager
 - Project Settings
 - Add Sources
 - Language Templates
 - IP Catalog
 - Package IP
- IP Integrator
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- Simulation
 - Simulation Settings
 - Run Simulation
- RTL Analysis
 - Elaboration Settings
 - Elaborated Design
 - Report Methodology
 - Report DRC
 - Report Noise
 - Schematic
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation

Synthesized Design - xc7z020dgg484 1 (active)

Device Constraints

- Internal VREF
 - 0.6V
 - 0.675V
 - 0.75V
 - 0.9V
 - NONE (4)
 - I/O Bank 13
 - I/O Bank 33
 - I/O Bank 34
 - I/O Bank 35

Properties

Select an object to see properties

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM	UF
synth_1	constrs_1	synth_design Complete!							1	0	0	0
impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA		0	1	0	0

Schematic

7 Cells 31 I/O Ports 15 Nets

write_bitstream Complete





设计演示：综合设计/Synthesis

数字系统课程设计

The screenshot displays the Xilinx ISE software interface during the synthesis process. The 'Synthesized Design' window is active, showing a schematic diagram of an AND gate. The 'Design Runs' table at the bottom provides a summary of the design process.

	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM	UF
synth_1	constrs_1	synth_design Complete!							1	0	0	0
impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA		0	1	0	0



设计演示：综合设计/Synthesis

数字系统课程设计

The screenshot shows the Xilinx ISE software interface during the synthesis process. The 'Synthesized Design' window is active, displaying a schematic of an AND gate implementation. The 'Design Runs' table at the bottom shows the synthesis and implementation steps completed successfully.

	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM	UF
synth_1	constrs_1	synth_design Complete!							1	0	0	0
impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA		0	1	0	0



设计演示：应用设计/Implement

数字系统课程设计

The screenshot displays the Xilinx Vivado IDE interface during the implementation phase. The 'Flow Navigator' on the left shows the project flow, with 'Implementation' selected. The 'Netlist' window shows the design hierarchy, including 'design_1_wrapper', 'Nets (6)', 'Leaf Cells (3)', and 'design_1_i (design_1)'. The 'Timing Summary' window shows a table of timing metrics for 'impl_1'.

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): NA	Worst Hold Slack (WHS): NA	Worst Pulse Width Slack (WPWS): NA
Total Negative Slack (TNS): NA	Total Hold Slack (THS): NA	Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: NA	Number of Failing Endpoints: NA	Number of Failing Endpoints: NA
Total Number of Endpoints: NA	Total Number of Endpoints: NA	Total Number of Endpoints: NA

There are no user specified timing constraints.





设计演示：应用设计/Implement

数字系统课程设计

The screenshot displays the Xilinx Vivado IDE interface during the implementation phase. The Flow Navigator on the left shows the project flow, with the 'Implementation' section highlighted. The main window is divided into several panes:

- Netlist:** Shows the hierarchical structure of the design, including the wrapper, nets, leaf cells, and the AND_Gate_0 component.
- Netlist Properties:** Provides details about the selected netlist, including primitive statistics and I/O nets.
- Timing Summary - impl_1:** Displays the design timing summary, including setup, hold, and pulse width constraints.

The Timing Summary report indicates that there are no user-specified timing constraints. The report includes the following data:

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): NA	Worst Hold Slack (WHS): NA	Worst Pulse Width Slack (WPWS): NA
Total Negative Slack (TNS): NA	Total Hold Slack (THS): NA	Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: NA	Number of Failing Endpoints: NA	Number of Failing Endpoints: NA
Total Number of Endpoints: NA	Total Number of Endpoints: NA	Total Number of Endpoints: NA

The bottom status bar shows the netlist name: design_1_wrapper.





设计演示：应用设计/Implement

数字系统课程设计

Flow Navigator

- Elaboration Settings
- Elaborated Design
 - Report Methodology
 - Report DRC
 - Report Noise
 - Schematic
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Synthesized Design
- Implementation**
 - Implementation Settings
 - Run Implementation
 - Implemented Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Noise
 - Report Utilization
 - Report Power
 - Program and Debug
 - Bitstream Settings
 - Generate Bitstream
 - Open Hardware Manager

Netlist: design_1_wrapper

Implemented Design - xc7z020dg484-1 (active)

Netlist

- design_1_wrapper
 - Nets (6)
 - Leaf Cells (3)
 - design_1_i (design_1)
 - Nets (3)
 - AND_Gate_0 (design_1_AND_Gate_0_0)
 - Nets (3)
 - U0 (AND_Gate)
 - Nets (3)
 - Leaf Cells (1)

Netlist Properties

Primitive Statistics

Primitive type Count

Statistics Properties I/O Nets

Timing - Timing Summary - impl_1

Design Timing Summary

This is a [saved report](#)

General Information

Timer Settings

Design Timing Summary

Check Timing (0)

User Ignored Paths

Unconstrained Paths

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	NA	Worst Hold Slack (WHS):	NA	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	NA	Total Hold Slack (THS):	NA	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	NA	Number of Failing Endpoints:	NA	Number of Failing Endpoints:	NA
Total Number of Endpoints:	NA	Total Number of Endpoints:	NA	Total Number of Endpoints:	NA

There are no user specified timing constraints.

Timing Summary - impl_1

Td Console Messages Log Reports Package Pins Design Runs Power Timing





设计演示：应用设计/Implement

数字系统课程设计

Flow Navigator

- Elaboration Settings
- Elaborated Design
 - Report Methodology
 - Report DRC
 - Report Noise
 - Schematic
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation
 - Implemented Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Noise
 - Report Utilization
 - Report Power
 - Program and Debug
 - Bitstream Settings
 - Generate Bitstream
 - Open Hardware Manager

Netlist: design_1_wrapper

Netlist Properties

Primitive Statistics

Primitive type Count

Statistics Properties I/O Nets

Timing - Timing Summary - impl_1

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): NA	Worst Hold Slack (WHS): NA	Worst Pulse Width Slack (WPWS): NA
Total Negative Slack (TNS): NA	Total Hold Slack (THS): NA	Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: NA	Number of Failing Endpoints: NA	Number of Failing Endpoints: NA
Total Number of Endpoints: NA	Total Number of Endpoints: NA	Total Number of Endpoints: NA

There are no user specified timing constraints.

Timing Summary - impl_1

Td Console Messages Log Reports Package Pins Design Runs Power Timing





设计演示：应用设计/Implement

数字系统课程设计

Netlist

- design_1_wrapper
 - Nets (6)
 - Leaf Cells (3)
 - design_1_i (design_1)
 - Nets (3)
 - AND_Gate_0 (design_1_AND_Gate_0_0)
 - Nets (3)
 - U0 (AND_Gate)
 - Nets (3)
 - Leaf Cells (1)

Timing Summary - impl_1

This is a [saved report](#)

General Information

Timer Settings

Design Timing Summary

Check Timing (0)

User Ignored Paths

Unconstrained Paths

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	NA	Worst Hold Slack (WHS):	NA	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	NA	Total Hold Slack (THS):	NA	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	NA	Number of Failing Endpoints:	NA	Number of Failing Endpoints:	NA
Total Number of Endpoints:	NA	Total Number of Endpoints:	NA	Total Number of Endpoints:	NA

There are no user specified timing constraints.

Timing Summary - impl_1

Td Console Messages Log Reports Package Pins Design Runs Power Timing



设计演示：产生设计报告

The screenshot displays the Vivado IDE interface with the following components:

- Properties Panel (Left):** Shows details for the selected component 'get/s_shiftReg[6]_i_1', including its parent 'get', reference name 'LUT3', type 'LUT', and various configuration options like 'B6LUT', 'Fixed', 'SLICE_X8Y75', 'CLBLM_R_X55Y75', and 'X1Y1'.
- Synthesis Panel (Top Middle):** Indicates a successful synthesis with 'Status: Complete' and 'Messages: No errors or warnings'. It also shows the part number 'xc7a100tcsq324-1' and the strategy 'Vivado Synthesis Defaults'.
- Implementation Panel (Top Right):** Shows a successful implementation with 'Status: Complete' and 'Messages: 1 warning'. It includes the part number 'xc7a100tcsq324-1' and the strategy 'Vivado Implementation Defaults'.
- DRC Violations Panel (Middle Left):** Reports 'Summary: 0 errors, 0 critical warnings, 1 warning, 0 advisories'.
- Utilization - Post-Implementation Panel (Middle Left):** A bar chart showing resource utilization: FF (1%), LUT (1%), I/O (11%), and BUFG (3%).
- Timing - Post-Implementation Panel (Middle Right):** Displays timing metrics: Worst Negative Slack (WNS): 8.219 ns, Total Negative Slack (TNS): 0 ns, Number of Failing Endpoints: 0, and Total Number of Endpoints: 25.
- Power Panel (Bottom Right):** Shows power consumption: Total On-Chip Power: 0.098 W, Junction Temperature: 25.4 °C, Thermal Margin: 59.6 °C (12.9 W), Effective θ_{JA} : 4.6 °C/W, and Power supplied to off-chip devices: 0 W.
- Timing Summary - impl_1 Panel (Bottom):** A detailed table of timing constraints and their status.

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 8.219 ns	Worst Hold Slack (WHS): 0.258 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 25	Total Number of Endpoints: 25	Total Number of Endpoints: 22

All user specified timing constraints are met.



设计演示：生成Bit流文件 Generating Bitstream

Flow Navigator

- Elaboration Settings
- Elaborated Design
 - Report Methodology
 - Report DRC
 - Report Noise
 - Schematic
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation
 - Implemented Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Utilization
 - Report Power
 - Program and Debug
 - Bitstream Settings
 - Generate Bitstream
 - Open Hardware Manager

Implemented Design - xc7z020dgg484-1 (active)

Netlist

- design_1_wrapper
 - Nets (6)
 - Leaf Cells (3)
 - design_1_i (design_1)
 - Nets (3)
 - AND_Gate_0 (design_1_AND_Gate_0_0)
 - Nets (3)
 - U0 (AND_Gate)
 - Nets (3)
 - Leaf Cells (1)

Netlist Properties

design_1_wrapper

Primitive Statistics

Primitive type	Count

Statistics Properties I/O Nets

Timing - Timing Summary - impl_1

Design Timing Summary

This is a saved report

General Information

Timer Settings

Design Timing Summary

Check Timing (0)

User Ignored Paths

Unconstrained Paths

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): NA	Worst Hold Slack (WHS): NA	Worst Pulse Width Slack (WPWS): NA
Total Negative Slack (TNS): NA	Total Hold Slack (THS): NA	Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: NA	Number of Failing Endpoints: NA	Number of Failing Endpoints: NA
Total Number of Endpoints: NA	Total Number of Endpoints: NA	Total Number of Endpoints: NA

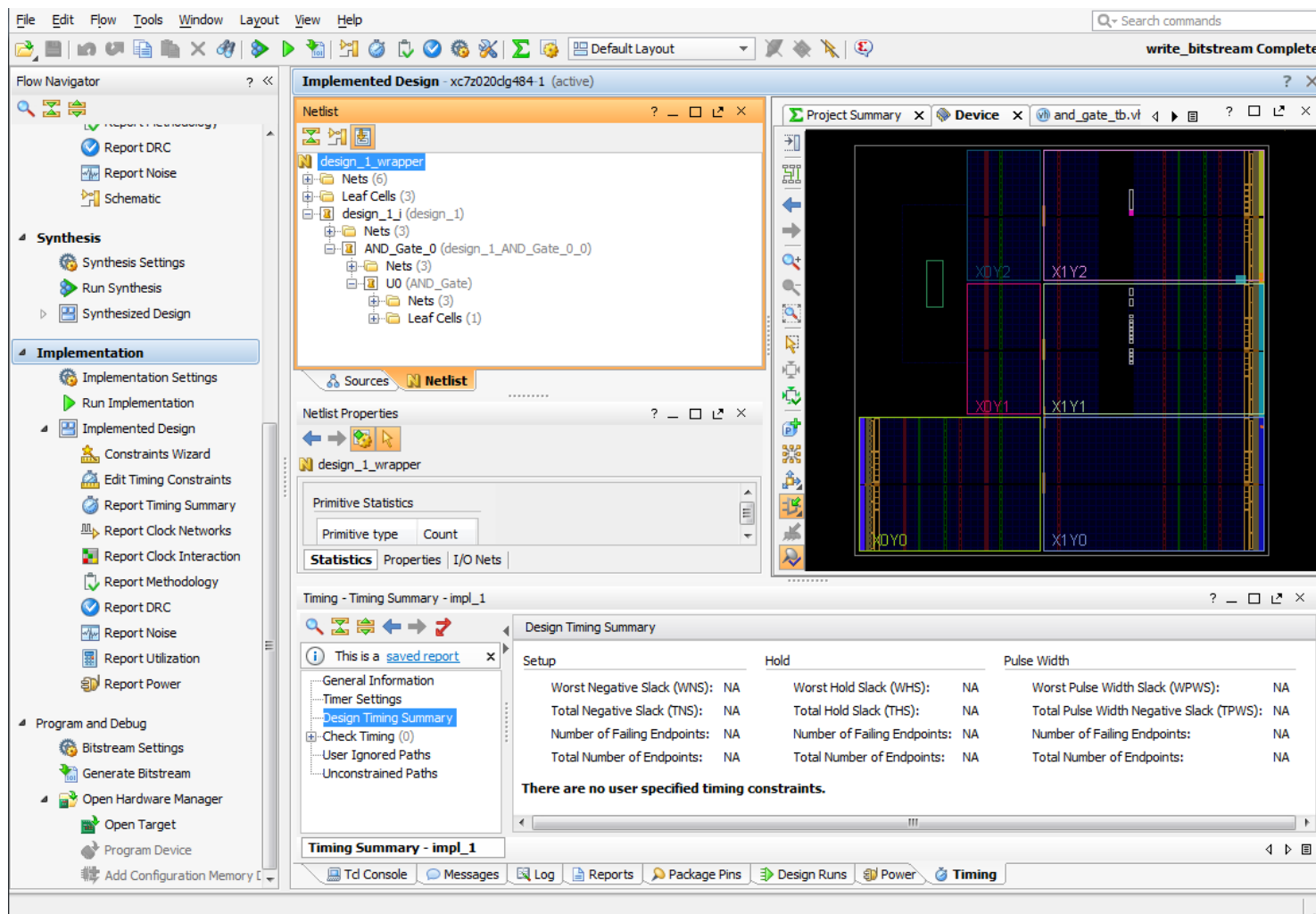
There are no user specified timing constraints.

Netlist: design_1_wrapper





硬件管理器：打开目标设备





硬件管理器：打开目标设备

数字系统课程设计

The screenshot displays the Xilinx Vivado IDE interface. On the left, the 'Flow Navigator' pane is open, showing the 'Implementation' section. Under 'Implementation', the 'Open Hardware Manager' option is highlighted with a red arrow. The main workspace shows the 'Implemented Design' for 'xc7z020dgg484 1'. The 'Netlist' window displays the design hierarchy, including 'design_1_wrapper', 'Nets (6)', 'Leaf Cells (3)', and 'design_1_i (design_1)'. The 'Netlist Properties' window shows the 'Primitive Statistics' for 'design_1_wrapper'. The 'Timing - Timing Summary - impl_1' window is open, displaying the 'Design Timing Summary' table.

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	NA	Worst Hold Slack (WHS):	NA	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	NA	Total Hold Slack (THS):	NA	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	NA	Number of Failing Endpoints:	NA	Number of Failing Endpoints:	NA
Total Number of Endpoints:	NA	Total Number of Endpoints:	NA	Total Number of Endpoints:	NA

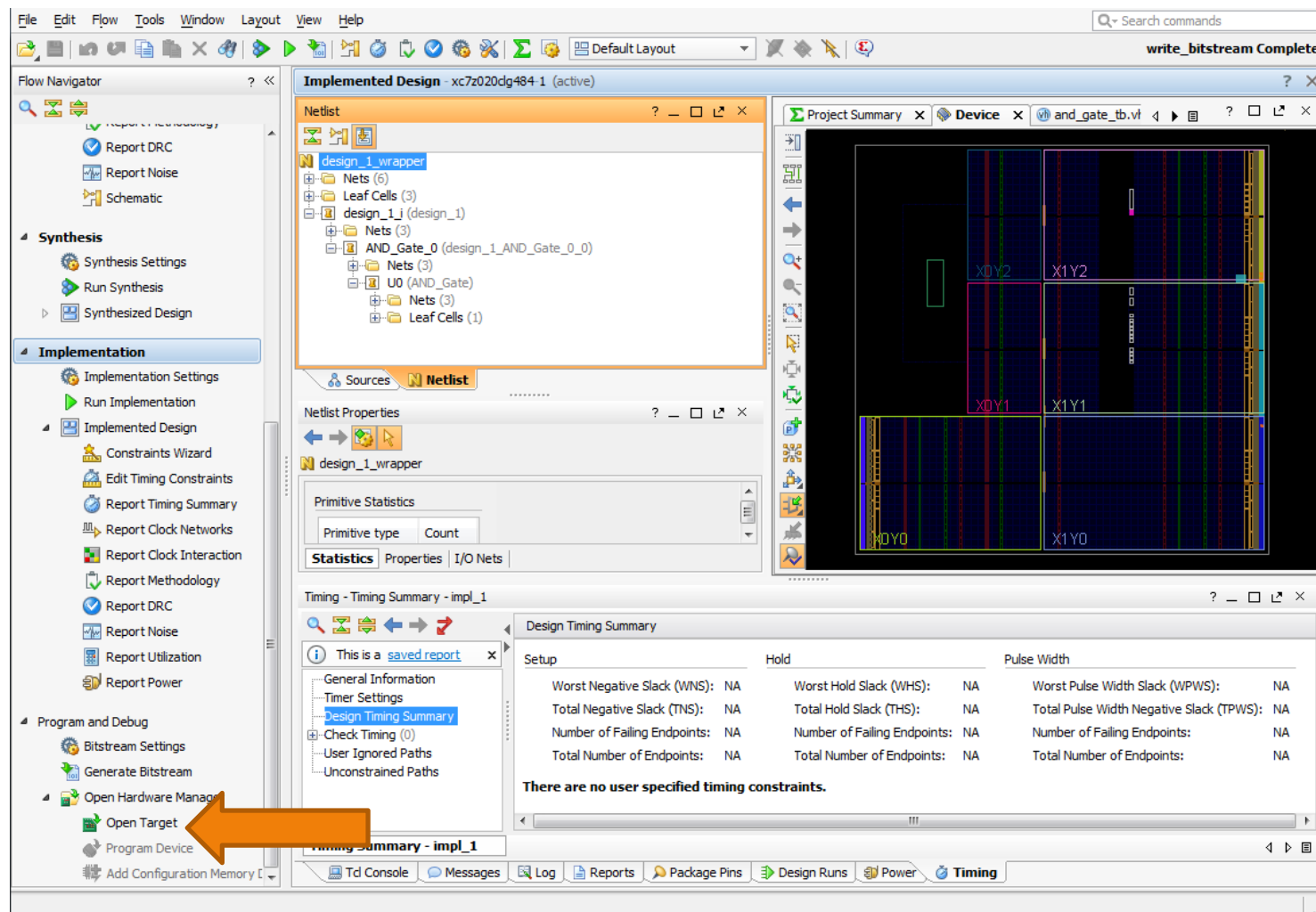
There are no user specified timing constraints.





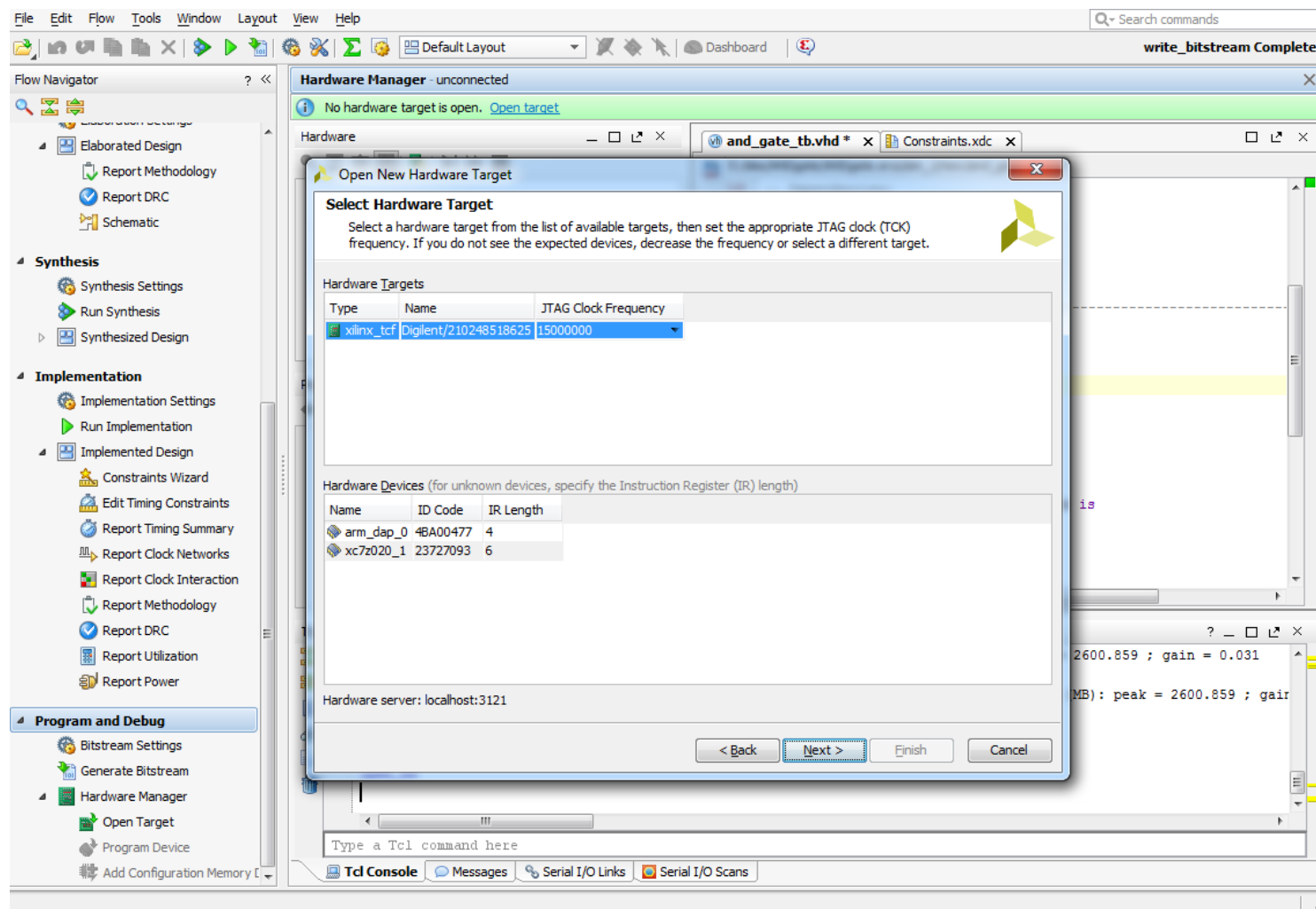
硬件管理器：打开目标设备

数字系统课程设计





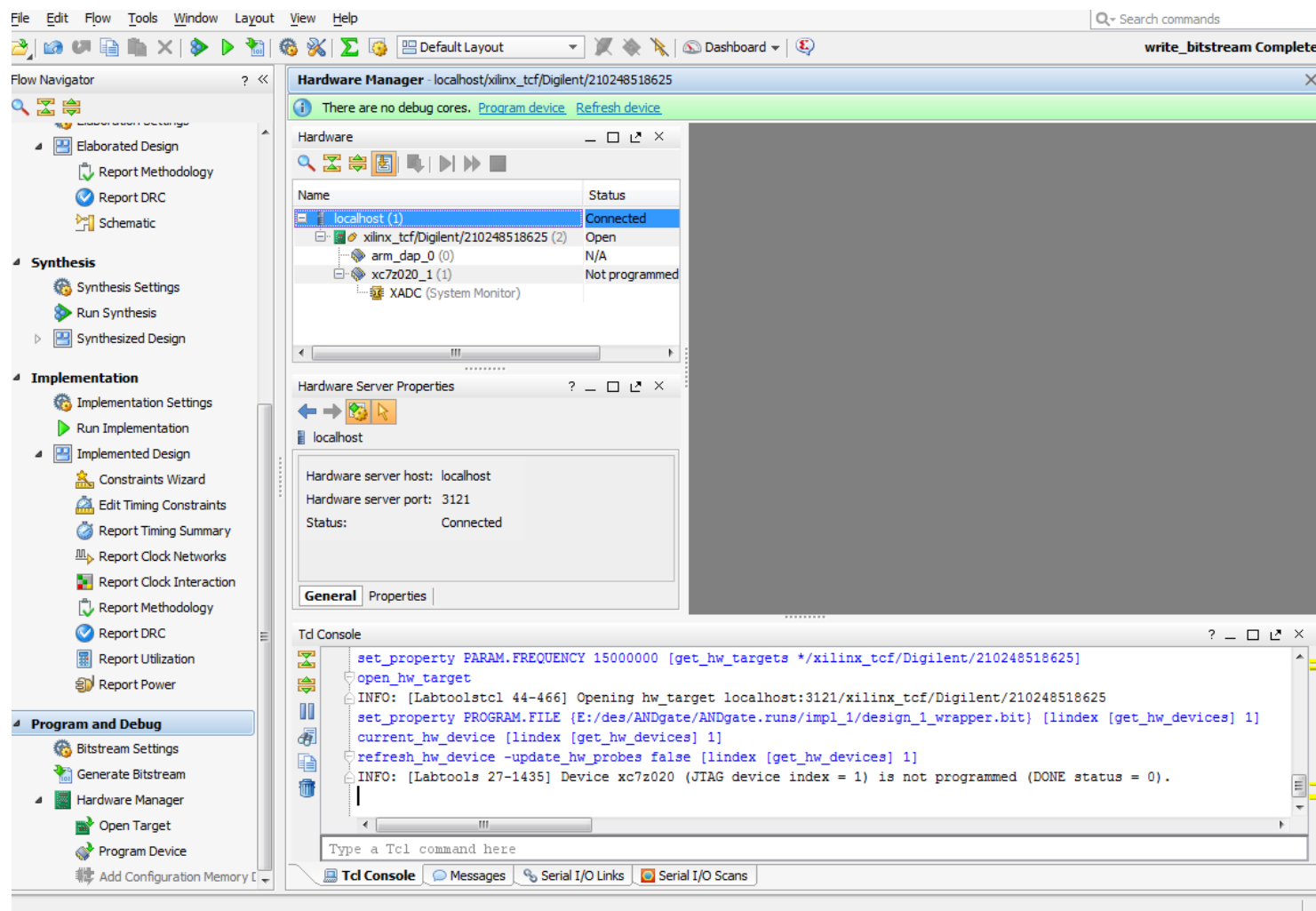
硬件管理器：打开目标设备





硬件管理器：对设备进行编程

数字系统课程设计





硬件管理器：对设备进行编程

数字系统课程设计

The screenshot displays the Xilinx Hardware Manager interface. The left sidebar shows the 'Program and Debug' section with 'Hardware Manager' selected. The main window shows a table of hardware devices:

Name	Status
localhost (1)	Connected
xilinx_tcf/Digilent/210248518625 (2)	Open
arm_dap_0 (0)	N/A
xc7z020_1 (1)	Not programmed
XADC (System Monitor)	

An orange arrow points to the 'xc7z020_1 (1)' device. Below the table, the 'Hardware Server Properties' for 'localhost' are shown:

Hardware server host: localhost
Hardware server port: 3121
Status: Connected

The 'Tcl Console' at the bottom shows the following commands and output:

```
set_property PARAM.FREQUENCY 15000000 [get_hw_targets */xilinx_tcf/Digilent/210248518625]
open_hw_target
INFO: [Labtoolstcl 44-466] Opening hw_target localhost:3121/xilinx_tcf/Digilent/210248518625
set_property PROGRAM.FILE {E:/des/ANDgate/ANDgate.runs/impl_1/design_1_wrapper.bit} [lindex [get_hw_devices] 1]
current_hw_device [lindex [get_hw_devices] 1]
refresh_hw_device -update_hw_probes false [lindex [get_hw_devices] 1]
INFO: [Labtools 27-1435] Device xc7z020 (JTAG device index = 1) is not programmed (DONE status = 0).
```



硬件管理器：对设备进行编程

数字系统课程设计

The screenshot displays the Xilinx Hardware Manager interface. The Hardware Manager window shows a table of devices connected to the system:

Name	Status
localhost (1)	Connected
xilinx_tcf/Digilent/210248518625 (2)	Open
arm_dap_0 (0)	N/A
xc7z020_1 (1)	Not programmed
XADC (System Monitor)	

An orange arrow points to the 'xc7z020_1 (1)' device, which is currently 'Not programmed'. Below the table, the Hardware Server Properties for 'localhost' are shown:

- Hardware server host: localhost
- Hardware server port: 3121
- Status: Connected

The Tcl Console window at the bottom shows the following commands and output:

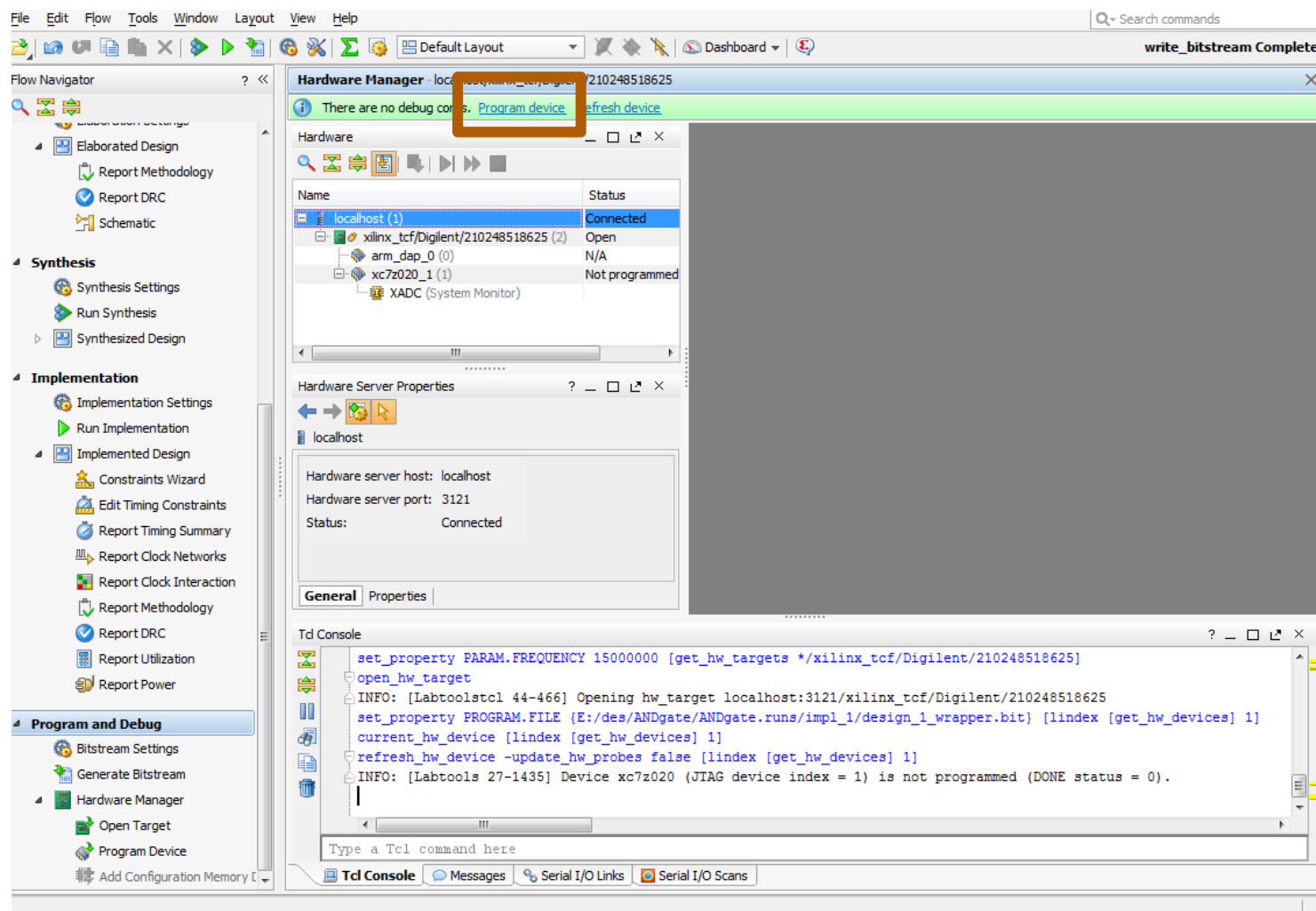
```
set_property PARAM.FREQUENCY 15000000 [get_hw_targets */xilinx_tcf/Digilent/210248518625]
open_hw_target
INFO: [Labtoolstcl 44-466] Opening hw_target localhost:3121/xilinx_tcf/Digilent/210248518625
set_property PROGRAM.FILE {E:/des/ANDgate/ANDgate.runs/impl_1/design_1_wrapper.bit} [lindex [get_hw_devices] 1]
current_hw_device [lindex [get_hw_devices] 1]
refresh_hw_device -update_hw_probes false [lindex [get_hw_devices] 1]
INFO: [Labtools 27-1435] Device xc7z020 (JTAG device index = 1) is not programmed (DONE status = 0).
```





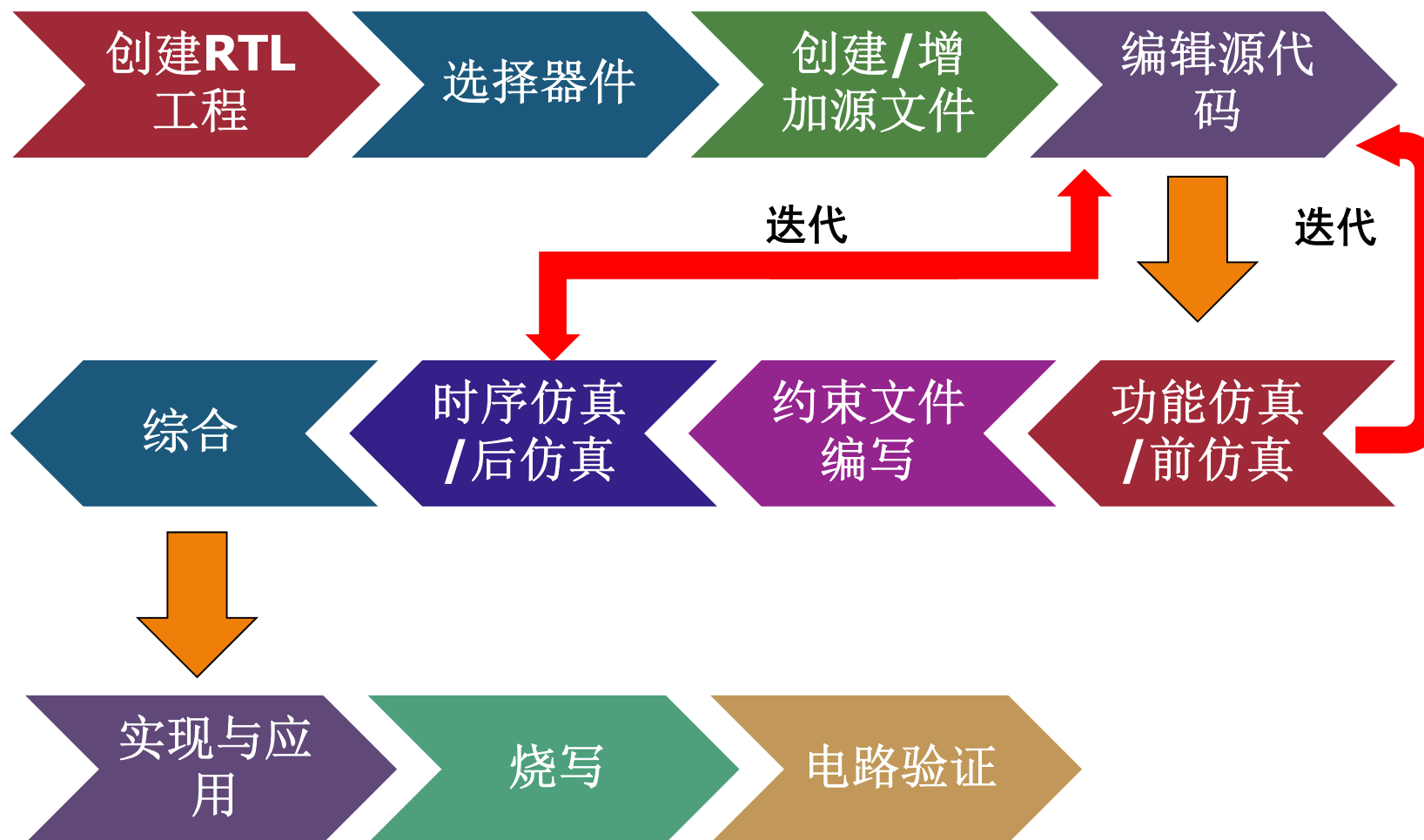
硬件管理器：对设备进行编程

数字系统课程设计





Vivado数字逻辑开发流程小结





课程设计的参考资源

◆ 开发板型号: Nexys 4 DDR

- ❑ FPGA型号: Artix-7 / XC7A100T-1CSG324C
- ❑ 用户使用手册和原理图
- ❑ 开发板的Vivado配置文件
- ❑ 约束文件XDC和UCF

◆ 资源链接



<https://reference.digilentinc.com/reference/programmable-logic/nexys-4-ddr/>





使用开发板在Vivado中设计流程



◆ Vivado中配置开发板

<https://reference.digilentinc.com/reference/software/vivado/board-files?redirect=1>

◆ 编程步骤/LED&Switch

<https://reference.digilentinc.com/learn/programmable-logic/tutorials/nexys-4-ddr-programming-guide/start>

◆ 示例程序/GPIO

<https://reference.digilentinc.com/learn/programmable-logic/tutorials/nexys-4-ddr-gpio-demo/start>





课程内容

一、CPLD&FPGA

二、数字系统设计基础

三、硬件描述语言VHDL基础

四、XILINX FPGA开发环境

五、课程设计题目与考核要求





设计题目：（一）密码锁控制器

◆ 功能描述：

用于模仿密码锁的工作过程，完成密码锁的核心控制功能。

◆ 功能要求及验收要点：

设计一个密码锁，平时处于等待状态。

- ① 管理员可以通过设置（专用按键）更改密码。
- ② 如果没有预置密码，密码缺省为“0000”。





设计题目：（一）密码锁控制器

- ③ 用户如果需要开锁，拨动相应的开关进入输入密码状态，输入4位密码，按下确定键后，若密码正确，锁打开，若密码错误，将提示密码错误，要求重新输入，三次输入都错误，将发出报警信号。
- ④ 报警后，只有管理员作相应的处理（专用按键）才能停止报警。
- ⑤ 用户输入密码时，在按下确定键之前，可以通过按退格键修正，每按一次退格键消除一位密码。





设计题目：（一）密码锁控制器

- ⑥ 正确开锁后，用户处理完毕后，按下确定键，系统回到等待状态。
- ⑦ 系统操作过程中，只要密码锁没有打开，如果10秒没有对系统操作，系统回到等待状态。
- ⑧ 系统操作过程中，如果密码锁已经打开，如果20秒没有对系统操作，系统自动上锁，回到等待状态。





设计题目：（一）密码锁控制器

◆ 提示：

- ① 密码正确，锁打开时，可以使用开关上方的LED灯配合显示效果，比如LED全亮等。密码错误，提示信号也可以使用LED进行显示。报警信号也可以使用LED进行显示，比如不停的闪烁等。
- ② 数码管要充分使用，用以显示用户输入的数字等。





设计题目：（二）多功能电子表

◆ 功能描述：

设计FPGA模块模拟多功能电子表的工作过程，具备多种功能

◆ 功能要求及验收要点：

- ① 时间显示界面，要求从00:00点计到23:59。
- ② 日期显示界面，要求显示当前日期，包含年、月、日。



设计题目：（二）多功能电子表

- ③ 调整时间界面，即可以设置或更改当前的时间（小时、分）。
- ④ 日期设置界面。可以设置当前的日期，比如2017年09月22日。要求支持闰年与大小月的识别。
- ⑤ 闹钟设置界面，可以设置3个闹钟，闹钟时间到了后会用LED闪烁提醒，提醒时间持续5秒，如果提醒时按解除键，则该闹钟解除提醒，如果闹钟响时没有按键或按其他按键，则响完5秒之后暂停，然后10秒钟后重新提醒一次后解除。





设计题目：（二）多功能电子表

- ⑥ 倒计时功能。可以设定倒计时的起始时间，比如1分钟，然后开始倒计时，从01:00倒计时到00:00，然后LED灯闪烁5秒钟。倒计时中间可以暂停或重新开始。
- ⑦ 电子表只有六个按键。请只使用六个按键来完成所有功能。





设计题目：（三）自动售货机

◆ 功能描述：

设计FPGA 模块模拟自动售货机的工作过程

◆ 功能要求及验收要点：

- ① 售货机有两个进币孔，一个是输入硬币，一个是输入纸币，硬币的识别范围是1元的硬币，纸币的识别范围是5元，10元，20元，50元。乘客可以连续多次投入钱币。





设计题目：（三）自动售货机

- ② 顾客可以选择的商品种类有16种，分别为A11-A44；价格如下表所示

A11: 3	A12: 4	A13: 6	A14: 3
A21:10	A22: 8	A23: 9	A24: 7
A31: 4	A32: 6	A33:15	A34: 8
A41: 9	A42: 4	A43: 5	A44: 5

顾客可以通过输入商品的编号来实现商品的选择

- ③ 顾客选择完商品后，可以选择需要的数量，数量为1-3件



设计题目：（三）自动售货机

- ④ 顾客可以继续选择商品及其数量，最多可选择两种商品。
- ⑤ 选择完货品，按确认键确认。
- ⑥ 系统计算并显示出所需金额。
- ⑦ 顾客此时可以投币，并且显示已经投币的总币值。当投币值达到或超过所需币值后，售货机出货，并扣除所需金额，并找出多余金额。





设计题目：（三）自动售货机

- ⑧ 找零时需要手动找零，每次一元。比如需找零3元，则需要按三次手动找零键。
- ⑨ 在投币期间，顾客可以按取消键取消本次操作，可以按手动找零键退出硬币。如果没有退出，可以重新选择货品进行交易。





设计题目：（四）地铁售票模拟系统

◆ 功能描述：

用于模仿地铁售票的自动售票，完成地铁售票的核心控制功能。

◆ 功能要求及验收要点：

- ① 地铁售票机有两个进币孔，可以输入硬币和纸币，售货机有两个进币孔，一个是输入硬币，一个是输入纸币，硬币的识别范围是1 元的硬币，纸币的识别范围是5 元，10 元，20元。乘客可以连续多次投入钱币。





设计题目：（四）地铁售票模拟系统

- ② 以南京市轨道交通1/2/3/4号线为基准进行设计考虑。站点数较多，需自行编码。
- ③ 系统可以通过按键设定当前站点为4条线路中任意一站。





设计题目：（四）地铁售票模拟系统

- ④ 乘客买票时可以有两种选择，第一种，乘客已经知道所需费用，直接选择票价，如2元、3元或4元或更多。第二种，不知道票价，选择出站口，系统以目的地与当前站的站数来进行计算价格，计算方式参考南京市轨道交通计价标准。请注意，由于换乘站的存在导致两地之间有可能有多种价格的，以最低价格为准。





设计题目：（四）地铁售票模拟系统

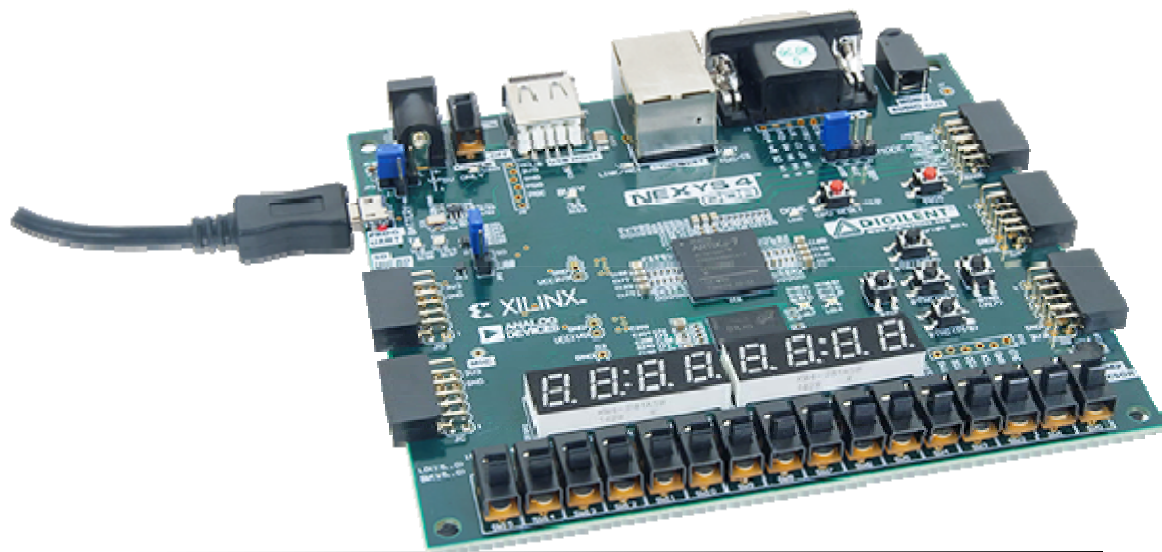
- ⑤ 得到票价单价后，选择所需购买的票数，然后进行投币，投入的钱币达到所需金额时，售票机自动出票，并一次性找出余额，本次交易结束，等待下一次的交易。在投币期间，乘客可以按取消键取消本次操作，钱币自动一次性退出。





课程设计题目的总体要求

- ◆ 善于利用按键、开关、LED灯、数码管的输入、输出与显示功能。
- ◆ 所设计的功能展示能够充分直观体现。
- ◆ 锁定管脚参考Nexys4 DDR的参考手册。





课程考核方式 - 总体要求

- 考核方式为考查方式，无笔试。每组同学都需要完成指定的设计并通过验收，撰写完整的设计报告。
- 总分**100**分，其中平时成绩**10**分，课题验收占**70**分，设计报告**20**分。
 - ◆ 平时：根据学生出勤与课堂表现等打分。
 - ◆ 验收：考核对课题理解与完成情况，根据选题、设计思路与方法，设计流程与结果，代码质量等进行评分。
 - ◆ 报告：论文报告的书写格式、报告内容的结构和条理性等方面





课程考核方式 - 分组

- 各班同学按照两人一组自行分组。
- 课上给出课程设计题目，由各组同学根据兴趣自行选择。





课程考核方式 - 分组

- 高效的**Teamwork**是本课程鼓励和考查的重点。协调组内的关系和协力高效完成课题需要各位组员的通力合作。报告中需要专门列出一个环节讲述**Teamwork**的内容，包括如何领导（如果有小组负责人）、如何分工、如何协调进展以及成效与总结。





课程考核方式 - 分组

- 组内分工时每位同学都需要参与程序设计、仿真与下载调试的相应部分，并且熟练掌握全部程序设计、仿真与下载调试。
- 做相同题目的各组可以互相讨论，但不得以任何理由抄袭全部或部分程序。否则抄袭与被抄袭各组均要受到同样处理，先验收的同学请自行保管好程序，否则责任自负。





课程考核方式 - 验收

- 每个小组在完成设计后必须验收。验收时请带上一卡通证件。
- 必须在完成给定题目的要求后方可要求验收，每组只验收一次，按当时的验收情况给分，如果之后有任何改进，请在报告中明示。





课程考核方式 - 验收

- 验收时由教师逐个指定组员陈述和回答相关问题，所有组员不论分工如何，都必须熟练掌握全部的设计内容。**教师根据各个组员验收情况给予分别评分。**
- 验收和报告时如发现有不同组之间部分雷同现象，涉及的小组所有组员一律减**20**分处理，如发现程序主体和结构多处雷同，涉及的相关小组所有组员一律减**30-40**分处理直至不及格。





课程考核方式 - 验收

- 验收截止于第四周最后一次实验课上，逾期不予验收。





课程考核方式 - 报告

- 课程设计报告每个小组交一份，以**Email**方式发送至教师信箱,格式为**PDF**文件或**DOC**文件及打包的程序附件，文件名为“数字系统课程设计报告_组员**1**学号姓名_组员**2**学号姓名”。信中请留下至少一名组员的通讯方式。
- 邮件地址 **course_nzzhang@163.com**

